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REVISION HISTORY

9/13—Revision D: Initial Version

FUNCTIONAL BLOCK DIAGRAM

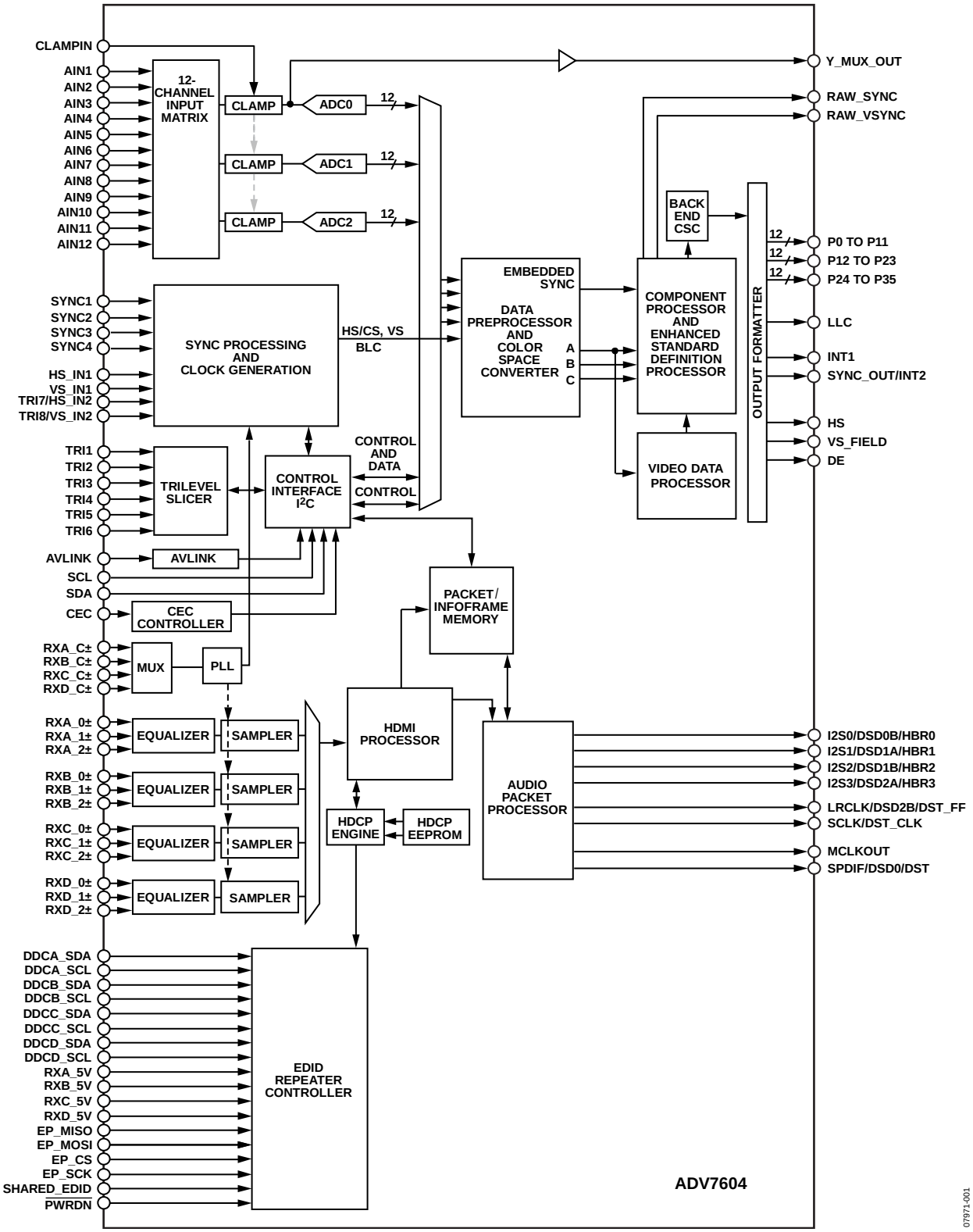


Figure 1.

SPECIFICATIONS

AVDD = 1.8 V ± 5%, DVDD = 1.8 V ± 5%, DVDDIO = 3.3 V ± 5%, PVDD = 1.8 V ± 5%, TVDD = 3.3 V ± 5%, CVDD = 1.8 V ± 5%, T_{MIN} to T_{MAX} = −40°C to +70°C.

ANALOG, DIGITAL, HDMI, AND AC SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG					
Clamp Circuitry					
External Clamp Capacitor			100		nF
Input Impedance	Clamps switched off		10		MΩ
ADC Midscale (CML)			0.89		V
ADC Full-Scale Level			CML + 0.550		V
ADC Zero-Scale Level			CML − 0.550		V
ADC Dynamic Range			1.1		V
Clamp Level (When Locked)	Component input (Y signal)		CML − 0.130		V
	Component input (Pr signal)		CML		V
	Component input (Pb signal)		CML		V
	PC RGB input (R, G, B)		CML − 0.130		V
DIGITAL INPUTS					
Input High Voltage (V_{IH})		2			V
Input Low Voltage (V_{IL})				0.8	V
Input Current (I_{IN})	$\overline{\text{RESET}}$ pin	−60		+60	µA
	Other digital inputs	−10		+10	µA
Input Capacitance (C_{IN})				10	pF
DIGITAL INPUTS (5 V TOLERANT)[1]					
Input High Voltage (V_{IH})		2.6			V
Input Low Voltage (V_{IL})				0.8	V
Input Current (I_{IN})	SHARED_EDID pin	−150		+60	µA
	Other 5 V digital inputs	−82		+82	µA
DIGITAL OUTPUTS					
Output High Voltage (V_{OH})		2.4			V
Output Low Voltage (V_{OL})				0.4	V
High Impedance Leakage Current (I_{LEAK})			10		µA
Output Capacitance (C_{OUT})				20	pF
HDMI					
TMDS Differential Pin Capacitance			0.3		pF
AC SPECIFICATIONS					
Intrapair (+ to −) Differential Input Skew for TMDS Clock Rates up to 222.75 MHz		0.4 T_{BIT}			ps
Intrapair (+ to −) Differential Input Skew for TMDS Clock Rates Above 222.75 MHz		0.15 T_{BIT} + 112			ps
Channel-to-Channel Differential Input Skew				0.2 t_{PIXEL} + 1.78	ns
TMDS Input Clock Range		25		225	MHz
Input Clock Jitter Tolerance			0.5	0.25 T_{BIT}	T_{BIT}

[1] The following pins are 5 V tolerant: HS_IN1, HS_IN2, $\overline{\text{VS\_IN1}}$, VS_IN2, DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, DDCD_SDA, RXA_5V, RXB_5V, RXC_5V, RXD_5V, SHARED_EDID, $\overline{\text{PWRDN}}$, EP_MISO.

VIDEO SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE SPECIFICATIONS		Measure at 27 MHz LLC				
SNR Unweighted		Luma ramp		60		dB
		Luma flat field		60		dB
Analog Front-End Crosstalk				60		dB
VIDEO STATIC PERFORMANCE						
Resolution (Each ADC)	N			12		
Integral Nonlinearity	INL	27 MHz (at a 12-bit level)		−3.0 to +8.0		LSB
		54 MHz (at a 12-bit level)		−3.0 to +8.0		LSB
		74.25 MHz (at a 12-bit level)		−4.0 to +7.0		LSB
		108 MHz (at an 11-bit level)		−3.5 to +8.0		LSB
		170 MHz (at a 9-bit level)		−0.7 to +1.5		LSB
Differential Nonlinearity	DNL	27 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		54 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		75 MHz (at a 12-bit level)		−0.7 to +0.8		LSB
		108 MHz (at an 11-bit level)		−0.7 to +0.8		LSB
		170 MHz (at a 9-bit level)		−0.6 to +0.5		LSB

DATA AND I²C TIMING CHARACTERISTICS

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VIDEO SYSTEM CLOCK AND XTAL						
Crystal Nominal Frequency				24.576/28.6363		MHz
Crystal Frequency Stability					±100	ppm
Horizontal Sync Input Frequency			10		110	kHz
LLC Frequency Range			12.825		170	MHz
External Clock Source[1]		External crystal must operate at 1.8 V				
Input High Voltage	V_{IH}	Ball H15 (XTALP) driven with external clock source	1.2			V
Input Low Voltage	V_{IL}	Ball H15 (XTALP) driven with external clock source			0.4	V
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
I²C PORTS (FAST MODE)						
xCL Frequency[2]					400	kHz
xCL Minimum Pulse Width High[2]	t_1		600			ns
xCL Minimum Pulse Width Low[2]	t_2		1.3			µs
Hold Time (Start Condition)	t_3		600			ns
Setup Time (Start Condition)	t_4		600			ns
xDA Setup Time[2]	t_5		100			ns
xCL and xDA Rise Time[2]	t_6				300	ns
xCL and xDA Fall Time[2]	t_7				300	ns
Setup Time (Stop Condition)	t_8		0.6			µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
I²C PORTS						
Normal Mode						
xCL Frequency[2]					100	kHz
xCL Minimum Pulse Width High[2]	t_1		4.0			µs
xCL Minimum Pulse Width Low[2]	t_2		4.7			µs
Hold Time (Start Condition)[2]	t_3		4.0			µs
Setup Time (Start Condition)[2]	t_4		4.7			µs
xDA Setup Time[2]	t_5		250			ns
xCL and xDA Rise Time[2]	t_6				1000	ns
xCL and xDA Fall Time[2]	t_7				300	ns
Setup Time (Stop Condition)	t_8		4.0			µs
DATA AND CONTROL OUTPUTS[3]						
Data Output Transition Time SDR (CP)	t_{11}	End of valid data to negative clock edge		0.55		ns
Data Output Transition Time SDR (CP)	t_{12}	Negative clock edge to start of valid data		1.0		ns
VIDEO I²S PORT						
Master Mode						
SCLK Mark Space Ratio	t_{13}:t_{14}		45:55		55:45	% duty cycle
LRCLK Data Transition Time	t_{15}	End of valid data to negative SCLK edge			10	ns
LRCLK Data Transition Time	t_{16}	Negative SCLK edge to start of valid data			10	ns
I2Sx Data Transition Time[4]	t_{17}	End of valid data to negative SCLK edge			5	ns
I2Sx Data Transition Time[4]	t_{18}	Negative SCLK edge to start of valid data			5	ns

[1] The XTAL_CTRL bit in AFE Map 0x4C[7:6] = 10b. This configures the XTAL pins for external oscillator operation. A 1.8 V oscillator must be used.
[2] The prefix x refers to S, DDCA_S, DDCB_S, DDCC_S, and DDCD_S.
[3] LLC DLL disabled.
[4] The suffix x refers to 0, 1, 2, and 3.

TIMING DIAGRAMS

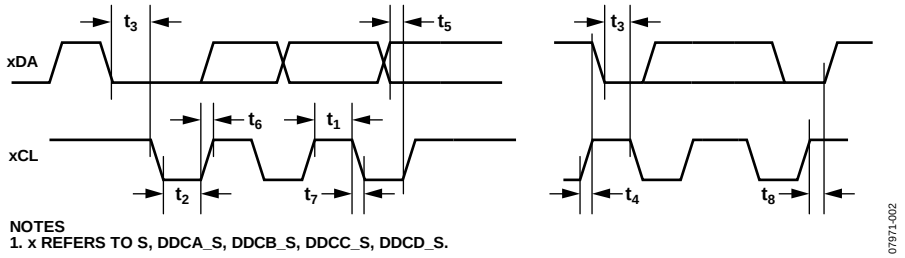


Figure 2. I²C Timing

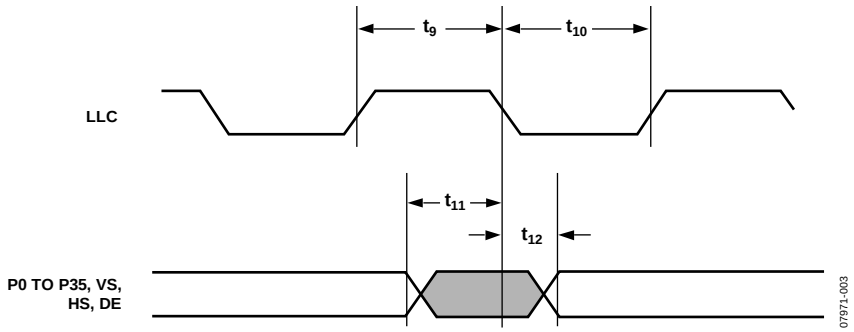


Figure 3. Pixel Port and Control SDR Output Timing

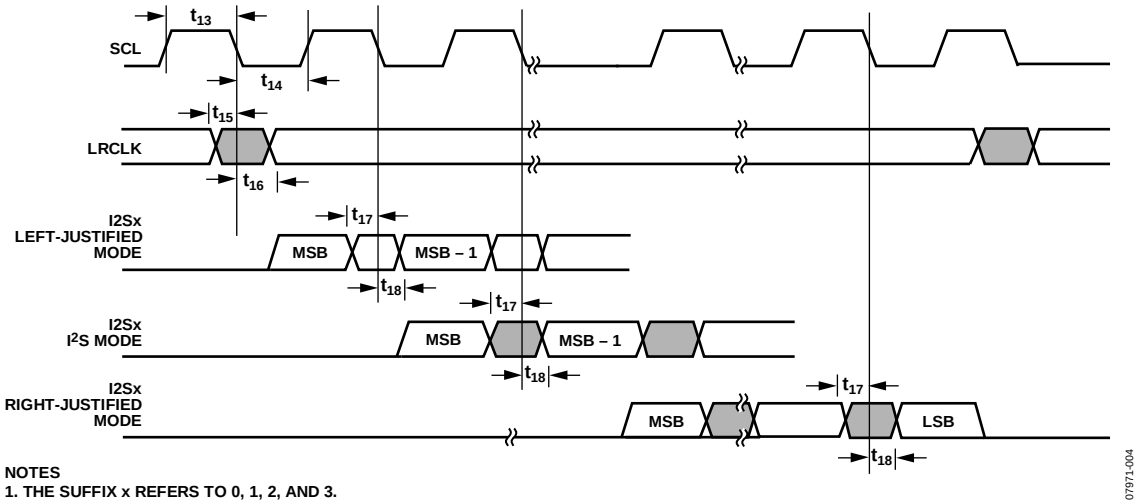


Figure 4. I²S Timing

POWER SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLIES					
Analog Supply (AVDD)	1.71	1.8	1.89	V	
Digital Core Power Supply (DVDD)	1.71	1.8	1.89	V	
Digital I/O Power Supply (DVDDIO)	3.14	3.3	3.46	V	
PLL Power Supply (PVDD)	1.71	1.8	1.89	V	
Terminator Power Supply (TVDD)	3.14	3.3	3.46	V	
Comparator Power Supply (CVDD)	1.71	1.8	1.89	V	
CURRENT CONSUMPTION[1, 2, 3, 4]					
Analog Power Supply (I_{AVDD})		200.0	258.3	mA	Analog only: RGB sampling at 162 MHz (UXGA)
		0.1	0.1	mA	HDMI only: 1080p 12-bit Deep Color with 4-channel PCM
		199.9	255.4	mA	Simultaneous mode: 1080p 12-bit Deep Color with 4-channel PCM and RGB sampling at 1080p
		0.0	0.0	mA	Power-Down Mode 0
Comparator Power Supply (I_{CVDD})		3.6	5.6	mA	Analog only: RGB sampling at 162 MHz (UXGA)
		102.9	121.9	mA	HDMI only: 1080p 12-bit Deep Color with 4-channel PCM
		102.8	120.2	mA	Simultaneous mode: 1080p 12-bit Deep Color with 4-channel PCM and RGB sampling at 1080p
		3.7	4.0	mA	Power-Down Mode 0
Digital Core Power Supply (I_{DVDD})		143.7	204.2	mA	Analog only: RGB sampling at 162 MHz (UXGA)
		212.4	290.2	mA	HDMI only: 1080p 12-bit Deep Color with 4-channel PCM
		239.7	303.7	mA	Simultaneous mode: 1080p 12-bit Deep Color with 4-channel PCM and RGB sampling at 1080p
		2.3	2.5	mA	Power-Down Mode 0
Digital I/O Power Supply (I_{DVDDIO})		54.2	131.2	mA	Analog only: RGB sampling at 162 MHz (UXGA)
		29.7	167.0	mA	HDMI only: 1080p 12-bit Deep Color with 4-channel PCM
		101.8	165.8	mA	Simultaneous mode: 1080p 12-bit Deep Color with 4-channel PCM and RGB sampling at 1080p
		1.3	1.4	mA	Power-Down Mode 0
PLL Power Supply (I_{PVDD})		64.1	75.6	mA	Analog only: RGB sampling at 162 MHz (UXGA)
		74.7	87.5	mA	HDMI only: 1080p 12-bit Deep Color with 4-channel PCM
		75.1	88.2	mA	Simultaneous mode: 1080p 12-bit Deep Color with 4-channel PCM and RGB sampling at 1080p
		0.2	0.22	mA	Power-Down Mode 0
Termination Power Supply (I_{TVDD})		2.5	4.8	mA	Analog only: RGB sampling at 162 MHz (UXGA)
		185.3	204.5	mA	HDMI only: 1080p 12-bit Deep Color with 4-channel PCM
		185.3	204.5	mA	Simultaneous mode: 1080p 12-bit Deep Color with 4-channel PCM and RGB sampling at 1080p
		1.1	1.2	mA	Power-Down Mode 0

[1] All maximum current values are guaranteed by characterization to assist in power supply design.
[2] Typical current consumption values are recorded with nominal voltage supply levels and a SMPTEBAR pattern.
[3] Maximum current consumption values are recorded with maximum rated voltage supply levels and a MOIRE X pattern.
[4] Termination power supply includes TVDD current consumed off chip.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to GND	2.2 V
DVDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4.0 V
CVDD to GND	2.2 V
TVDD to GND	4.0 V
Digital Inputs Voltage to GND	GND – 0.3 V to DVDDIO + 0.3 V
5 V Tolerant Digital Inputs to GND[1]	5.3 V
Digital Output Voltage to GND	GND – 0.3 V to DVDDIO + 0.3 V
Analog Inputs to GND	GND – 0.3 V to AVDD + 0.3 V
XTAL Pins	–0.3 V to PVDD to 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature	150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] The following inputs are 3.3 V inputs but are 5 V tolerant: HS_IN1, HS_IN2, VS_IN1, VS_IN2, DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, DDCD_SDA, RXA_5V, RXB_5V, RXC_5V, RXD_5V, SHARED_EDID, PWRDN, EP_MISO.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7604, the user is advised to turn off unused sections of the part.

Due to printed circuit board metal variation and, thus, variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the θ_{JA} value.

The maximum junction temperature ($T_{J\ MAX}$) of 125°C must not be exceeded. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on DUT:

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
T_S = the package surface temperature (°C).
Ψ_{JT} = 0.3°C/W for a 260-ball CSP_BGA.
$W_{TOTAL} = ((PVDD \times I_{PVDD}) + (0.05 \times TVDD \times I_{TVDD}) + (CVDD \times I_{CVDD}) + (AVDD \times I_{AVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}))$.

Note that for W_{TOTAL}, 5% of TVDD power is dissipated on the part itself.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

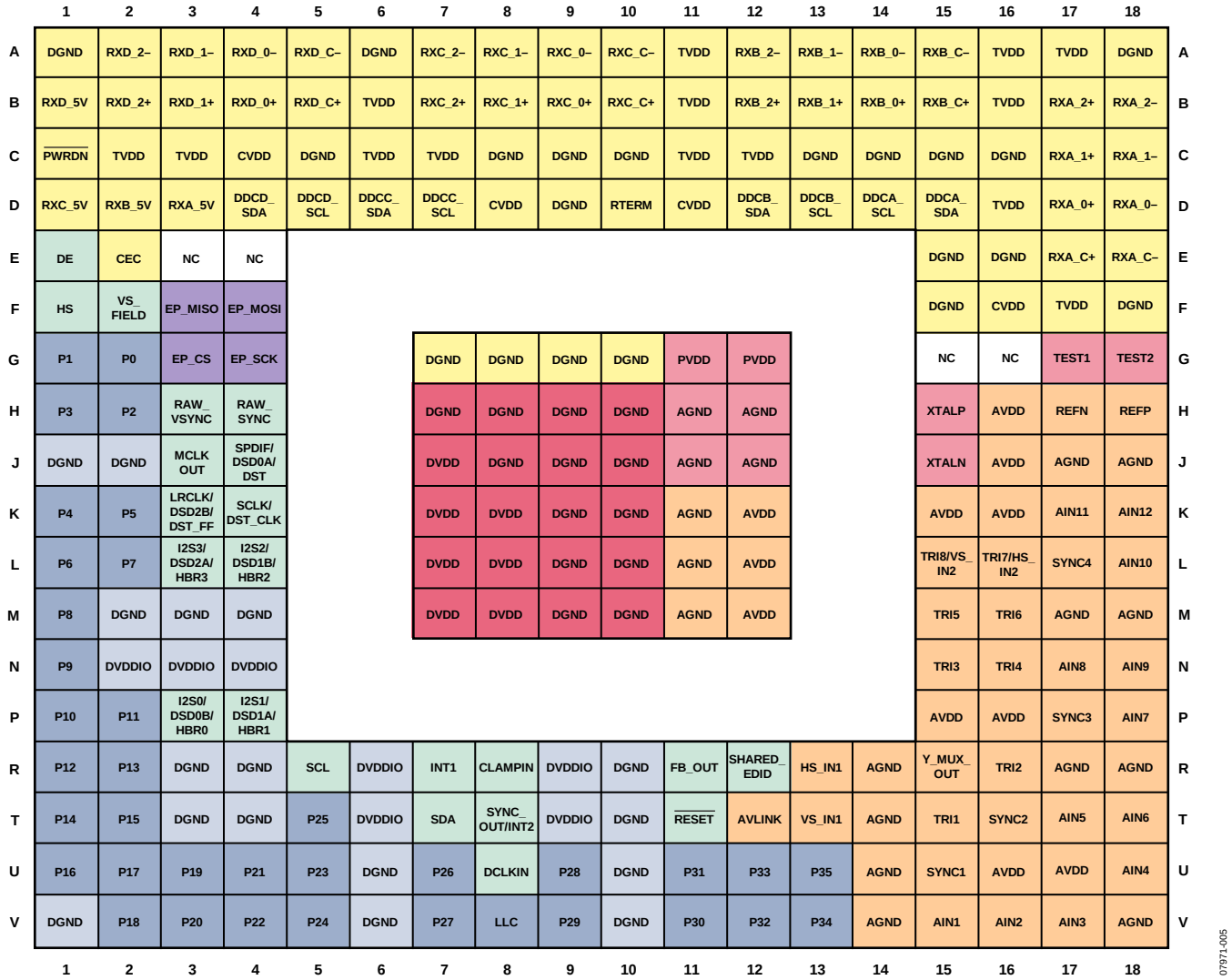


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	DGND	Ground	Ground.
A2	RXD_2–	HDMI input	Digital Input Channel 2 Complement of Port D in the HDMI Interface.
A3	RXD_1–	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
A4	RXD_0–	HDMI input	Digital Input Channel 0 Complement of Port D in the HDMI Interface.
A5	RXD_C–	HDMI input	Digital Input Clock Complement of Port D in the HDMI Interface.
A6	DGND	Ground	Ground.
A7	RXC_2–	HDMI input	Digital Input Channel 2 Complement of Port C in the HDMI Interface.
A8	RXC_1–	HDMI input	Digital Input Channel 1 Complement of Port C in the HDMI Interface.
A9	RXC_0–	HDMI input	Digital Input Channel 0 Complement of Port C in the HDMI Interface.
A10	RXC_C–	HDMI input	Digital Input Clock Complement of Port C in the HDMI Interface.
A11	TVDD	Power	Terminator Supply Voltage (3.3 V).
A12	RXB_2–	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
A13	RXB_1–	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
A14	RXB_0–	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
A15	RXB_C–	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.

Pin No.	Mnemonic	Type	Description
A16	TVDD	Power	Terminator Supply Voltage (3.3 V).
A17	TVDD	Power	Terminator Supply Voltage (3.3 V).
A18	DGND	Ground	Ground.
B1	RXD_5V	HDMI input	5 V Detect Pin for Port D in the HDMI Interface.
B2	RXD_2+	HDMI input	Digital Input Channel 2 True of Port D in the HDMI Interface.
B3	RXD_1+	HDMI input	Digital Input Channel 1 True of Port D in the HDMI Interface.
B4	RXD_0+	HDMI input	Digital Input Channel 0 True of Port D in the HDMI Interface.
B5	RXD_C+	HDMI input	Digital Input Clock True of Port D in the HDMI Interface.
B6	TVDD	Power	Terminator Supply Voltage (3.3 V).
B7	RXC_2+	HDMI input	Digital Input Channel 2 True of Port C in the HDMI Interface.
B8	RXC_1+	HDMI input	Digital Input Channel 1 True of Port C in the HDMI Interface.
B9	RXC_0+	HDMI input	Digital Input Channel 0 True of Port C in the HDMI Interface.
B10	RXC_C+	HDMI input	Digital Input Clock True of Port C in the HDMI Interface.
B11	TVDD	Power	Terminator Supply Voltage (3.3 V).
B12	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
B13	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
B14	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
B15	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
B16	TVDD	Power	Terminator Supply Voltage (3.3 V).
B17	RXA_2+	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
B18	RXA_2−	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
C1	$\overline{\text{PWRDN}}$	Input	Active Low System Power Detect. If low, EDID can be powered from 5 V signal of HDMI port when connected to active equipment.
C2	TVDD	Power	Terminator Supply Voltage (3.3 V).
C3	TVDD	Power	Terminator Supply Voltage (3.3 V).
C4	CVDD	Power	Comparator Supply Voltage (1.8 V).
C5	DGND	Ground	Ground.
C6	TVDD	Power	Terminator Supply Voltage (3.3 V).
C7	TVDD	Power	Terminator Supply Voltage (3.3 V).
C8	DGND	Ground	Ground.
C9	DGND	Ground	Ground.
C10	DGND	Ground	Ground.
C11	TVDD	Power	Terminator Supply Voltage (3.3 V).
C12	TVDD	Power	Terminator Supply Voltage (3.3 V).
C13	DGND	Ground	Ground.
C14	DGND	Ground	Ground.
C15	DGND	Ground	Ground.
C16	DGND	Ground	Ground.
C17	RXA_1+	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI interface.
C18	RXA_1−	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI interface.
D1	RXC_5V	HDMI input	5 V Detect Pin for Port C in the HDMI Interface.
D2	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface.
D3	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface.
D4	DDCD_SDA	HDMI input	HDCP Slave Serial Data Port D. DDCD_SDA is a 3.3 V input that is 5 V tolerant.
D5	DDCD_SCL	HDMI input	HDCP Slave Serial Clock Port D. DDCD_SCL is a 3.3 V input that is 5 V tolerant.
D6	DDCC_SDA	HDMI input	HDCP Slave Serial Data Port C. DDCC_SDA is a 3.3 V input that is 5 V tolerant.
D7	DDCC_SCL	HDMI input	HDCP Slave Serial Clock Port C. DDCC_SCL is a 3.3 V input that is 5 V tolerant.
D8	CVDD	Power	Comparator Supply Voltage (1.8 V).
D9	DGND	Ground	Ground.
D10	RTERM	Miscellaneous analog	Terminal Resistance. This pin sets internal termination resistance. Use a 500 Ω resistor between this pin and GND.

Pin No.	Mnemonic	Type	Description
D11	CVDD	Power	Comparator Supply Voltage (1.8 V).
D12	DDCB_SDA	HDMI input	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input that is 5 V tolerant.
D13	DDCB_SCL	HDMI input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
D14	DDCA_SCL	HDMI input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
D15	DDCA_SDA	HDMI input	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input that is 5 V tolerant.
D16	TVDD	Power	Terminator Supply Voltage (3.3 V).
D17	RXA_0+	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
D18	RXA_0–	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
E1	DE	Digital video output	Data Enable. DE is a signal that indicates active pixel data.
E2	CEC	Digital I/O	Consumer Electronic Control Channel.
E3	NC	No connect	Do Not Connect.
E4	NC	No connect	Do Not Connect.
E15	DGND	Ground	Ground.
E16	DGND	Ground	Ground.
E17	RXA_C+	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
E18	RXA_C–	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
F1	HS	Digital video output	Horizontal Synchronization Output Signal in the CP and HDMI Processor.
F2	VS_FIELD	Digital video output	Vertical Synchronization Output Signal in the CP and HDMI Processor. FIELD is a field synchronization output signal in all interlaced video modes. VS or FIELD can be configured for this pin.
F3	EP_MISO	Digital input	SPI Master In/Slave Out for External EDID Interface.
F4	EP_MOSI	Digital output	SPI Master Out/Slave In for External EDID Interface.
F15	DGND	Ground	Ground.
F16	CVDD	Power	Comparator Supply Voltage (1.8 V).
F17	TVDD	Power	Terminator Supply Voltage (3.3 V).
F18	DGND	Ground	Ground.
G1	P1	Digital video output	Video Pixel Output Port.
G2	P0	Digital video output	Video Pixel Output Port.
G3	EP_CS	Digital output	SPI Chip Select for External EDID Interface.
G4	EP_SCK	Digital output	SPI Clock for External EDID Interface.
G7	DGND	Ground	Ground.
G8	DGND	Ground	Ground.
G9	DGND	Ground	Ground.
G10	DGND	Ground	Ground.
G11	PVDD	Power	PLL Supply Voltage (1.8 V).
G12	PVDD	Power	PLL Supply Voltage (1.8 V).
G15	NC	No connect	Do Not Connect.
G16	NC	No connect	Do Not Connect.
G17	TEST1	Test	Do Not Connect.
G18	TEST2	Test	Do Not Connect.
H1	P3	Digital video output	Video Pixel Output Port.
H2	P2	Digital video output	Video Pixel Output Port.
H3	RAW_VSYNC	Analog output	This pin outputs the raw-sliced, embedded CSYNC or raw digital HS/CS.
H4	RAW_SYNC	Analog output	This pin outputs the raw-sliced, embedded CSYNC or raw digital HS/CS.
H7	DGND	Ground	Ground.
H8	DGND	Ground	Ground.
H9	DGND	Ground	Ground.
H10	DGND	Ground	Ground.
H11	AGND	Ground	Ground.
H12	AGND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
H15	XTALP	Miscellaneous analog	Input pin for the 28.63636 MHz crystal or can be overdriven by an external 1.8 V 28.63636 MHz clock oscillator source to clock the ADV7604. The following crystal frequencies are also supported: 24.576 MHz and 27.00 MHz.
H16	AVDD	Power	Analog Supply Voltage (1.8 V).
H17	REFN	Misc analog	Internal Voltage Reference Output.
H18	REFP	Misc analog	Internal Voltage Reference Output.
J1	DGND	Ground	Ground.
J2	DGND	Ground	Ground.
J3	MCLKOUT	Digital output	Audio Master Clock Output.
J4	SPDIF/DSD0A/DST	Digital output	Multipurpose Pin. S/PDIF Digital Audio Output. First DSD Data Channel. DST Stream.
J7	DVDD	Power	Digital Supply Voltage (1.8 V).
J8	DGND	Ground	Ground.
J9	DGND	Ground	Ground.
J10	DGND	Ground	Ground.
J11	AGND	Ground	Ground.
J12	AGND	Ground	Ground.
J15	XTALN	Miscellaneous analog	This pin should be connected to the 28.63636 MHz crystal or left as a no connect if an external 1.8 V 28.63636 MHz clock oscillator source is used to clock the ADV7604. In crystal mode, the crystal must be a fundamental crystal. The following crystal frequencies are also supported: 24.576 MHz and 27.00 MHz.
J16	AVDD	Power	Analog Supply Voltage (1.8 V).
J17	AGND	Ground	Ground.
J18	AGND	Ground	Ground.
K1	P4	Digital video output	Video Pixel Output Port.
K2	P5	Digital video output	Video Pixel Output Port.
K3	LRCLK/DSD2B/DST_FF	Digital output	Dual Purpose Pin. Data Output Clock. Left and right audio channels. Sixth DSD Data Channel. DST Frame.
K4	SCLK/DST_CLK	Digital output	Dual Purpose Pin. Audio Serial Clock Output. DST Clock.
K7	DVDD	Power	Digital Supply Voltage (1.8 V).
K8	DVDD	Power	Digital Supply Voltage (1.8 V).
K9	DGND	Ground	Ground.
K10	DGND	Ground	Ground.
K11	AGND	Ground	Ground.
K12	AVDD	Power	Analog Supply Voltage (1.8 V).
K15	AVDD	Power	Analog Supply Voltage (1.8 V).
K16	AVDD	Power	Analog Supply Voltage (1.8 V).
K17	AIN11	Analog video input	Analog Video Input Channel.
K18	AIN12	Analog video input	Analog Video Input Channel.
L1	P6	Digital video output	Video Pixel Output Port.
L2	P7	Digital video output	Video Pixel Output Port.
L3	I2S3/DSD2A/HBR3	Digital output	Multipurpose Pin. I^2S Audio (Channel 7 and Channel 8). Fifth DSD Data Channel. Fourth Block of HBR Stream.
L4	I2S2/DSD1B/HBR2	Digital output	Multipurpose Pin. I^2S Audio (Channel 5 and Channel 6). Fourth DSD Data Channel. Third Block of HBR Stream.
L7	DVDD	Power	Digital Supply Voltage (1.8 V).
L8	DVDD	Power	Digital Supply Voltage (1.8 V).
L9	DGND	Ground	Ground.
L10	DGND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
L11	AGND	Ground	Ground.
L12	AVDD	Power	Analog Supply Voltage (1.8 V).
L15	TRI8/VS_IN2	Analog input	Dual Purpose Pin. Trilevel/bilevel input on the SCART or D-terminal connector. Results are available via I²C. This signal can be buffered and output to the FB_OUT pin. VS on Graphics Port 2. The VS input signal is used in CP mode for 5-wire timing mode. VS_IN2 is a 3.3 V input that is 5 V tolerant.
L16	TRI7/HS_IN2	Analog input	Dual Purpose Pin. Trilevel/bilevel input on the SCART or D-terminal connector. Results are available via I²C. This signal can be buffered and output to the FB_OUT pin. HS on Graphics Port 2. The HS input signal is used in CP mode for 5-wire timing mode. HS_IN2 is a 3.3 V input that is 5 V tolerant.
L17	SYNC4	Analog input	Synchronization on green or luma input (SOG/SOY). Used in embedded synchronization mode. User configurable.
L18	AIN10	Analog video input	Analog Video Input Channel.
M1	P8	Digital video output	Video Pixel Output Port.
M2	DGND	Ground	Ground.
M3	DGND	Ground	Ground.
M4	DGND	Ground	Ground.
M7	DVDD	Power	Digital Supply Voltage (1.8 V).
M8	DVDD	Power	Digital Supply Voltage (1.8 V).
M9	DGND	Ground	Ground.
M10	DGND	Ground	Ground.
M11	AGND	Ground	Ground.
M12	AVDD	Power	Analog Supply Voltage (1.8 V).
M15	TRI5	Analog input	Trilevel/bilevel input on the SCART or D-terminal connector. Results are available via I²C. This signal can be buffered and output to the FB_OUT pin.
M16	TRI6	Analog input	Trilevel/bilevel input on the SCART or D-terminal connector. Results are available via I²C. This signal can be buffered and output to the FB_OUT pin.
M17	AGND	Ground	Ground.
M18	AGND	Ground	Ground.
N1	P9	Digital video output	Video Pixel Output Port.
N2	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
N3	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
N4	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
N15	TRI3	Analog input	Trilevel/bilevel input on the SCART or D-terminal connector. Results are available via I²C. This signal can be buffered and output to the FB_OUT pin.
N16	TRI4	Analog input	Trilevel/bilevel input on the SCART or D-terminal connector. Results are available via I²C. This signal can be buffered and output to the FB_OUT pin.
N17	AIN8	Analog video input	Analog Video Input Channel.
N18	AIN9	Analog video input	Analog Video Input Channel.
P1	P10	Digital video output	Video Pixel Output Port.
P2	P11	Digital video output	Video Pixel Output Port.
P3	I2S0/DSD0B/HBR0	Digital output	I²S Audio (Channel 1 and Channel 2). Second DSD Data Channel. First Block of HBR Stream.
P4	I2S1/DSD1A/HBR1	Digital output	I²S Audio (Channel 3 and Channel 4). Third DSD Data Channel. Second Block of HBR Stream.
P15	AVDD	Power	Analog Supply Voltage (1.8 V).
P16	AVDD	Power	Analog Supply Voltage (1.8 V).
P17	SYNC3	Analog input	Synchronization on green or luma input (SOG/SOY). Used in embedded synchronization mode. User configurable.
P18	AIN7	Analog video input	Analog Video Input Channel.

Pin No.	Mnemonic	Type	Description
R1	P12	Digital video output	Video Pixel Output Port.
R2	P13	Digital video output	Video Pixel Output Port.
R3	DGND	Ground	Ground.
R4	DGND	Ground	Ground.
R5	SCL	Digital I/O	I²C Port Serial Clock Input. Maximum clock rate of 400 kHz. SCL is the clock line for the control port.
R6	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
R7	INT1	Digital output	Interrupt Pin 1. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
R8	CLAMPIN	External clamp	External Clamp Signal. This is an optional mode of operation for the ADV7604.
R9	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
R10	DGND	Ground	Ground.
R11	FB_OUT	Misc digital	FB Output. This is the muxed fast blank output from TRI1 to TRI8 (programmable).
R12	SHARED_EDID	Digital input	EDID Flag. When high, all four HDMI ports share common EDID. When low, Port D does not share common EDID; Port D operates with a separate EDID.
R13	HS_IN1	Analog input	HS on Graphics Port 1. HS input signal is used in CP mode for 5-wire timing mode. HS_IN1 is a 3.3 V input that is 5 V tolerant.
R14	AGND	Ground	Ground.
R15	Y_MUX_OUT	Analog output	Buffered Output of the Y Channel.
R16	TRI2	Analog input	Trilevel/bilevel input on the SCART or D-terminal connector. Results are available via I²C. This signal can be buffered and output to the FB_OUT pin.
R17	AGND	Ground	Ground.
R18	AGND	Ground	Ground.
T1	P14	Digital video output	Video Pixel Output Port.
T2	P15	Digital video output	Video Pixel Output Port.
T3	DGND	Ground	Ground.
T4	DGND	Ground	Ground.
T5	P25	Digital video output	Video Pixel Output Port.
T6	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
T7	SDA	Digital I/O	I²C Port Serial Data Input/Output Pin. SDA is the data line for the control port.
T8	SYNC_OUT/INT2	Digital output	Dual Purpose Pin. Sliced Synchronization Output For the CP Core. Interrupt Pin 2. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
T9	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
T10	DGND	Ground	Ground.
T11	$\overline{\text{RESET}}$	Digital input	Chip Reset. Active low. Minimum low time for a reset to take place is 5 ms.
T12	AVLINK	Digital I/O	Digital SCART Control Channel.
T13	VS_IN1	Analog input	VS on Graphics Port 1. The VS input signal is used in CP mode for 5-wire timing mode. VS_IN1 is a 3.3 V input that is 5 V tolerant.
T14	AGND	Ground	Ground.
T15	TRI1	Analog input	Trilevel/bilevel input on the SCART or D-terminal connector. Results are available via I²C. This signal can be buffered and output to the FB_OUT pin.
T16	SYNC2	Analog input	Synchronization on green or luma input (SOG/SOY). Used in embedded synchronization mode. User configurable.
T17	AIN5	Analog video input	Analog Video Input Channel.
T18	AIN6	Analog video input	Analog Video Input Channel.
U1	P16	Digital video output	Video Pixel Output Port.
U2	P17	Digital video output	Video Pixel Output Port.
U3	P19	Digital video output	Video Pixel Output Port.
U4	P21	Digital video output	Video Pixel Output Port.
U5	P23	Digital video output	Video Pixel Output Port.
U6	DGND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
U7	P26	Digital video output	Video Pixel Output Port.
U8	DCLKIN	External clock and clamp	External Clock for ADC Sampling. This is an optional mode of operation for the ADV7604.
U9	P28	Digital video output	Video Pixel Output Port.
U10	DGND	Ground	Ground.
U11	P31	Digital video output	Video Pixel Output Port.
U12	P33	Digital video output	Video Pixel Output Port.
U13	P35	Digital video output	Video Pixel Output Port.
U14	AGND	Ground	Ground.
U15	SYNC1	Analog input	Synchronization on green or luma input (SOG/SOY). Used in embedded synchronization mode. User configurable.
U16	AVDD	Power	Analog Supply Voltage (1.8 V).
U17	AVDD	Power	Analog Supply Voltage (1.8 V).
U18	AIN4	Analog video input	Analog Video Input Channel.
V1	DGND	Ground	Ground.
V2	P18	Digital video output	Video Pixel Output Port.
V3	P20	Digital video output	Video Pixel Output Port.
V4	P22	Digital video output	Video Pixel Output Port.
V5	P24	Digital video output	Video Pixel Output Port.
V6	DGND	Ground	Ground.
V7	P27	Digital video output	Video Pixel Output Port.
V8	LLC	Digital video output	Line Locked Output Clock for the Pixel data. Range is 13.5 MHz to 170 MHz.
V9	P29	Digital video output	Video Pixel Output Port.
V10	DGND	Ground	Ground.
V11	P30	Digital video output	Video Pixel Output Port.
V12	P32	Digital video output	Video Pixel Output Port.
V13	P34	Digital video output	Video Pixel Output Port.
V14	AGND	Ground	Ground.
V15	AIN1	Analog video input	Analog Video Input Channel.
V16	AIN2	Analog video input	Analog Video Input Channel.
V17	AIN3	Analog video input	Analog Video Input Channel.
V18	AGND	Ground	Ground.

THEORY OF OPERATION

ANALOG FRONT END

The ADV7604 analog front end comprises three 170 MHz, 12-bit ADCs that digitize the analog video signal before applying it to the CP, enabling true 12-bit video decoding. The analog front end uses differential channels to each ADC to ensure high performance in a mixed-signal application.

The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7604 without the requirement of an external mux.

Three voltage clamp control loops ensure that any dc offsets are removed from the video signal. The voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping in the CP.

For component 525i, 625i, 525p, and 625p sources, 2× oversampling is performed. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external antialiasing filters with the benefit of an increased signal-to-noise ratio (SNR).

HDMI RECEIVER

The HDMI receiver on the ADV7604 incorporates active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. The equalization is programmable. It is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance at even the highest HDMI data rates. The HDMI receiver supports all HDTV formats up to 1080p and all display resolutions up to UXGA (1600 × 1200 at 60 Hz). The receiver contains a programmable data island packet interrupt generator.

With the inclusion of HDCP, displays can receive encrypted video content. The HDMI interface of the ADV7604 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP 1.3 protocol.

The HDMI receiver offers advanced audio functionality. It supports multichannel I²S audio for up to eight channels. It also supports a 6-DSD channel interface with each channel carrying an oversampled 1-bit representation of the audio signal as delivered on a super audio CD (SACD). It incorporates a DST interface that outputs audio data decoded from DST audio packets. The ADV7604 can also receive HBR audio packet streams and outputs them through the HBR interface in an SPDIF format conforming to the IEC60958 standard. It supports multichannel I²S audio for up to eight channels. The receiver also contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, the audio data can be ramped to prevent audio clicks or pops.

COMPONENT PROCESSOR (CP)

The CP section is capable of decoding/digitizing a wide range of component video formats in any color space. Component video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, 1250i, VGA up to UXGA at 60 Hz, and many other standards.

The CP section of the ADV7604 contains an AGC block. In cases where no embedded synchronization is present, the video gain can be set manually. The AGC section is followed by a digital clamp circuit that ensures that the video signal is clamped to the correct blanking level. Automatic adjustments within the CP include gain (contrast) and offset (brightness); manual adjustment controls are also supported.

A fully programmable any-to-any 3 × 3 color space conversion (CSC) matrix is placed between the analog front end and the CP section. This enables YPrPb-to-RGB and RGB-to-YCrCb conversions. Many other standards of color space can be implemented using the color space converter.

The CP section contains circuitry to enable the detection of Macrovision® encoded YPrPb signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust when decoding these types of signals.

VBI extraction of CGMS data is performed by the CP section of the ADV7604 for interlaced, progressive, and high definition scanning rates. The data extracted can be read back over the I²C interface.

CP PIXEL DATA OUTPUT MODES

The output section of the CP is highly flexible. It can be configured in an SDR mode with one data packet per clock cycle or in a DDR mode where data is presented on the rising and falling edge of the clock. In SDR mode, a 16-/20-/24-bit 4:2:2 or 24-/30-/36-bit 4:4:4 output is possible. In these modes, the HS, VS/FIELD, and DE/FIELD (where applicable) timing reference signals are provided. In DDR mode, the ADV7604 can be configured in an 8-/10-/12-bit 4:2:2 YCrCb or 12-bit 4:4:4 RGB/YCrCb pixel output interface with corresponding timing signals.

RGB GRAPHICS PROCESSING

The ADV7604 provides automatic detection of synchronization source and polarity by the SSPD block, standard identification that is enabled by the STDI blocks, optimum pixel sample through a 32-phase DLL, and arbitrary pixel sampling for nonstandard video sources. A data enable (DE) output signal is supplied for direct connection to the HDMI/DVI transmitter IC.

The following additional graphics functions are provided:

- Automatic or manual clamp and gain controls for graphics modes
- Contrast and brightness controls
- A 170 MSPS conversion rate that supports RGB input resolutions up to 1600 × 1200 at 60 Hz (UXGA)
- Color space conversion of RGB to YCrCb and decimation to a 4:2:2 format for video-centric back end IC interfacing

ENHANCED STANDARD DEFINITION PROCESSOR

The ESDP is designed to provide robust synchronization separation capability for component video input modes that are likely to have an unstable time base. These are component signals that have originated from CVBS signals such as noisy/weak RF signals or VCR signals with head switches. The ESDP is available for SD (480i, 576i) and ED (480p, 576p) component video input modes with embedded synchronization because these are most likely to suffer from timing impairments.

The ESDP contains circuitry for identifying characteristics of the input signal, and these are then used within the device to automatically configure it optimally for different inputs. It uses digitally controlled analog clamping to maximize the range of the video signal within the ADC. This effectively compensates for the poor signal quality that may be present on the input.

I²C INTERFACE

The ADV7604 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. The ADV7604 is controlled by an external I²C master device, such as a microcontroller.

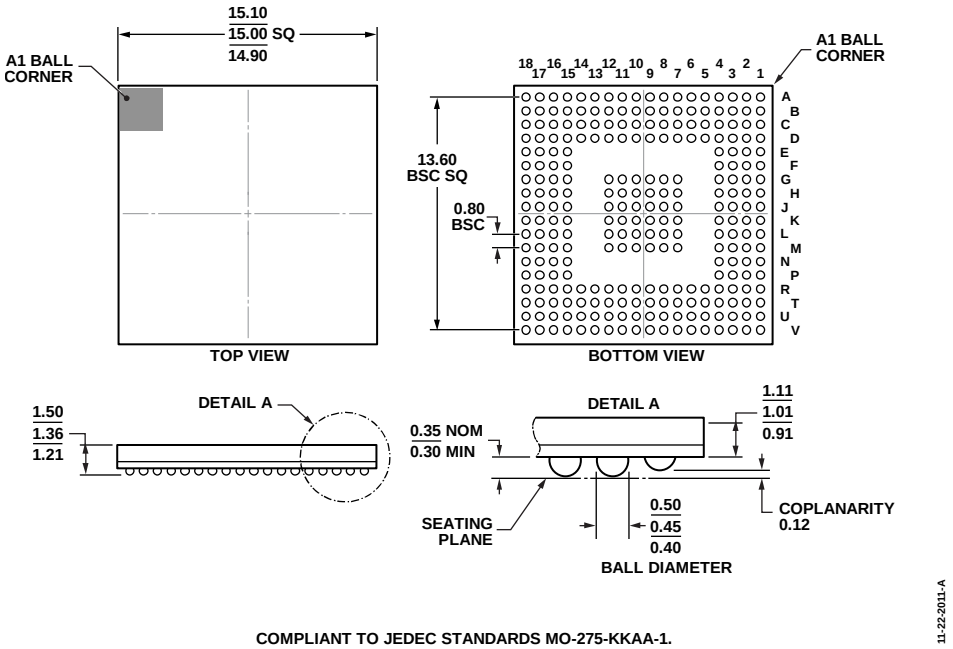
OTHER FEATURES

In addition to HS, VS, and FIELD output signals with programmable position, polarity, and width, the ADV7604 provides the following:

- Programmable interrupt request output pins: INT1 and INT2
- Low power consumption: 1.8 V digital core, 1.8 V analog and 3.3 V digital input/output, low power power-down mode, and green PC mode
- Temperature range: −40°C to +70°C
- 15 mm × 15 mm, RoHS-compliant BGA package

For more detailed product information about the ADV7604, contact a local Analog Devices, Inc., sales office.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-KKAA-1.

Figure 6. 260-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-260-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADV7604BBCZ-5	–40°C to +70°C	260-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-260-1
ADV7604BBCZ-5P	–40°C to +70°C	260-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-260-1
EVAL-ADV7604EB1Z		ADV7604BBCZ-5 Front End Evaluation Board	
EVAL-ADV7604EB2Z		ADV7604BBCZ-5P Front End Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The ADV7604BBCZ-5 is programmed with internal HDCP keys. Customers must have HDCP adopter status (consult Digital Content Protection LLC for licensing requirements) to purchase any components with internal HDCP keys.
[3] The ADV7604BBCZ-5P is not programmed with internal HDCP keys for professional applications. Customers are not required to have HDCP adopter status.

NOTES

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).

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