ADV7127* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

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- AN-213: Low Cost, Two-Chip, Voltage -Controlled Amplifier and Video Switch

Data Sheet

- ADV7127: CMOS, 240 MHz, 10-Bit, High Speed Video DAC Data Sheet

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- ADV7127 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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1/2017—Rev. 0 to Rev. A

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4/1998—Revision 0: Initial Version

SPECIFICATIONS

5 V ELECTRICAL CHARACTERISTICS

V_{AA} = 5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[1] unless otherwise noted. $T_{J\,MAX}$ = 110°C.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE						
Resolution (Each DAC)		10			Bits	
Integral Nonlinearity (INL)		−1	+0.4	+1	LSB	
Differential Nonlinearity		−1	+0.25	+1	LSB	Guaranteed monotonic
DIGITAL AND CONTROL INPUTS						
Input Voltage						
High	V_{IH}	2			V	
Low	V_{IL}			0.8	V	
$\overline{\text{PDOWN}}$ Input Voltage						
High			3		V	
Low			1		V	
Input Current	I_{IN}	−1		+1	μA	V_{IN} = 0.0 V or V_{AA}
Pull-Up Current						
$\overline{\text{PSAVE}}$			20		μA	
$\overline{\text{PDOWN}}$			20		μA	
Input Capacitance	C_{IN}		10		pF	
ANALOG OUTPUTS						
Output Current		2.0		18.5	mA	
Output Compliance Range	V_{OC}	0		1.4	V	
Output Impedance	R_{OUT}		100		kΩ	
Output Capacitance	C_{OUT}		10		pF	I_{OUT} = 0 mA
Offset Error		−0.025		+0.025	% FSR	Tested with DAC output = 0 V
Gain Error[2]		−5.0		+5.0	% FSR	FSR = 17.62 mA
VOLTAGE REFERENCE (EXTERNAL AND INTERNAL)[3]						
Reference Range	V_{REF}	1.12	1.235	1.35	V	
POWER DISSIPATION						
Supply Current						
Digital			1.5	3	mA	f_{CLK} = 50 MHz
			4	6	mA	f_{CLK} = 140 MHz
			6.5	10	mA	f_{CLK} = 240 MHz
Analog			23	27	mA	R_{SET} = 560 Ω
			5		mA	R_{SET} = 4933 Ω
Standby[4]			3.8	6	mA	$\overline{\text{PSAVE}}$ = low, digital and control inputs at V_{AA}
$\overline{\text{PDOWN}}$			1		mA	
Power Supply Rejection Ratio	PSRR		0.1	0.5	%/%	

[1] Temperature range T_{MIN} to T_{MAX}: −40°C to +85°C at 50 MHz and 140 MHz, and 0°C to 70°C at 240 MHz.
[2] Gain error = ((Measured (FSC)/Ideal (FSC) − 1) × 100), where Ideal = V_{REF}/R_{SET} × K × (0x3FF) and K = 7.9896.
[3] The digital supply is measured with a continuous clock, with data input corresponding to a ramp pattern, and with an input level at 0 V and V_{DD}.
[4] These typical/maximum specifications are guaranteed by characterization to be over the 4.75 V to 5.25 V range.

3.3 V ELECTRICAL CHARACTERISTICS

V_{AA} = 3.0 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[1] unless otherwise noted. $T_{J\,MAX}$ = 110°C.

Table 2.

Parameter[2]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE						R_{SET} = 680 Ω
Resolution (Each DAC)				10	Bits	
Integral Nonlinearity (INL)		−1	+0.5	+1	LSB	
Differential Nonlinearity		−1	+0.25	+1	LSB	
DIGITAL AND CONTROL INPUTS						
Input Voltage						
High	V_{IH}	2.0			V	
Low	V_{IL}		0.8		V	
$\overline{\text{PDOWN}}$ Input Voltage						
High			2.1		V	
Low			0.6		V	
Input Current	I_{IN}	−1		+1	μA	V_{IN} = 0.0 V or V_{DD}
$\overline{\text{PSAVE}}$ Pull-Up Current			20		μA	
Input Capacitance	C_{IN}		10		pF	
ANALOG OUTPUTS						
Output Current		2.0		18.5	mA	
Output Compliance Range	V_{OC}	0		1.4	V	
Output Impedance	R_{OUT}		70		kΩ	
Output Capacitance	C_{OUT}		10		pF	
Offset Error			0	0	% FSR	Tested with DAC output = 0 V
Gain Error[3]			0		% FSR	FSR = 17.62 mA
VOLTAGE REFERENCE (EXTERNAL)						
Reference Range	V_{REF}	1.12	1.235	1.35	V	
VOLTAGE REFERENCE (INTERNAL)						
Reference Range	V_{REF}		1.235		V	
POWER DISSIPATION						
Supply Current						
Digital[4]			1	2	mA	f_{CLK} = 50 MHz
			2.5	4.5	mA	f_{CLK} = 140 MHz
			4	6	mA	f_{CLK} = 240 MHz
Analog			22	25	mA	R_{SET} = 560 Ω
			5		mA	R_{SET} = 4933 Ω
Standby			2.6	3	mA	$\overline{\text{PSAVE}}$ = low, digital and control inputs at V_{DD}
$\overline{\text{PDOWN}}$			20		μA	
Power Supply Rejection Ratio	PSRR		0.1	0.5	%/%	

[1] Temperature range T_{MIN} to T_{MAX}: −40°C to +85°C at 50 MHz and 140 MHz and 0°C to 70°C at 240 MHz.
[2] These maximum/minimum specifications are guaranteed by characterization to be over 3.0 V to 3.6 V range.
[3] Gain error = ((Measured (FSC)/Ideal (FSC) − 1) × 100), where Ideal = $V_{REF}/R_{SET} \times K \times$ (0x3FF) and K = 7.9896.
[4] The digital supply is measured with a continuous clock, with data input corresponding to a ramp pattern, and with an input level at 0 V and V_{DD}.

5 V TIMING SPECIFICATIONS

V_{AA} = 5 V ± 5%,[1] V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[2] unless otherwise noted. $T_{J\,MAX}$ = 110°C.

Table 3.

Parameter[3]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG OUTPUTS						
Delay	t_6		5.5		ns	
Rise/Fall Time[4]	t_7		1.0		ns	
Transition Time[5]	t_8		15		ns	
Skew[6]	t_9		1	2	ns	Not shown in Figure 2
CLOCK CONTROL[7]						
	f_{CLK}	0.5		50	MHz	50 MHz grade
		0.5		140	MHz	140 MHz grade
		0.5		240	MHz	240 MHz grade
Data and Control						
Setup	t_1	1.5			ns	
Hold	t_2	2.5			ns	
Clock Pulse Width						
High	t_4	1.875	1.1		ns	f_{MAX} = 240 MHz
		2.85			ns	f_{MAX} = 140 MHz
		8.0			ns	f_{MAX} = 50 MHz
Low	t_5	1.875	1.25		ns	f_{MAX} = 240 MHz
		2.85			ns	f_{MAX} = 140 MHz
		8.0			ns	f_{MAX} = 50 MHz
Pipeline Delay[6]	t_{PD}	1.0	1.0	1.0	Clock cycles	Not shown in Figure 2
Up Time						
$\overline{\text{PSAVE}}$[6]	t_{10}		2	10	ns	Not shown in Figure 2
$\overline{\text{PDOWN}}$	t_{11}		320		ns	Not shown in Figure 2

[1] Maximum and minimum specifications are guaranteed over this range in Table 3.
[2] Temperature range: T_{MIN} to T_{MAX}: −40°C to +85°C at 50 MHz and 140 MHz, and 0°C to 70°C at 240 MHz.
[3] Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}) for both 5 V and 3.3 V supplies.
[4] Rise time was measured from the 10% to 90% point of zero to full-scale transition, and fall time from the 90% to 10% point of a full-scale transition.
[5] Measured from 50% point of full-scale transition to 2% of final value.
[6] Guaranteed by characterization.
[7] f_{CLK} maximum specification production tested at 125 MHz and 5 V. Limits specified in Table 3 are guaranteed by characterization.

3.3 V TIMING SPECIFICATIONS

V_{AA} = 3.0 V to 3.6 V,[1] V_{REF} = 1.235 V, R_{SET} = 560 Ω. All specifications T_{MIN} to T_{MAX},[2] unless otherwise noted. $T_{J\,MAX}$ = 110°C.

Table 4.

Parameter[3]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG OUTPUTS						
Delay	t_6		7.5		ns	
Rise/Fall Time[4]	t_7		1.0		ns	
Transition Time[5]	t_8		15		ns	
Skew[6]	t_9		1	2	ns	Not shown in Figure 2
CLOCK CONTROL[7]						
	f_{CLK}			50	MHz	50 MHz grade
				140	MHz	140 MHz grade
				240	MHz	240 MHz grade
Data and Control						
Setup[6]	t_1	1.5			ns	
Hold[6]	t_2	2.5			ns	
Clock Period[6]	t_3		2.5		ns	f_{MAX} = 240 MHz
Clock Pulse Width						
High	t_4		1.1		ns	f_{MAX} = 240 MHz
	t_4[6]	2.85			ns	f_{MAX} = 140 MHz
	t_4[6]	8.0			ns	f_{MAX} = 50 MHz
Low[6]	t_5		1.4		ns	f_{MAX} = 240 MHz
	t_5	2.85			ns	f_{MAX} = 140 MHz
	t_5	8.0			ns	f_{MAX} = 50 MHz
Pipeline Delay[6]	t_{PD}	1.0	1.0	1.0	Clock cycles	Not shown in Figure 2
Up Time						
$\overline{\text{PSAVE}}$[6]	t_{10}		4	10	ns	Not shown in Figure 2
$\overline{\text{PDOWN}}$	t_{11}		320		ns	Not shown in Figure 2

[1] The values stated in Table 4 were obtained using V_{AA} in the range of 3.0 V to 3.6 V.
[2] Temperature range: T_{MIN} to T_{MAX}: −40°C to +85°C at 50 MHz and 140 MHz, and 0°C to 70°C at 240 MHz.
[3] Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}) for both 5 V and 3.3 V supplies.
[4] Rise time was measured from the 10% to 90% point of zero to full-scale transition, and fall time from the 90% to 10% point of a full-scale transition.
[5] Measured from 50% point of full-scale transition to 2% of final value.
[6] Guaranteed by characterization.
[7] f_{CLK} maximum specification production tested at 125 MHz and 3.3 V. Limits specified in Table 4 are guaranteed by characterization.

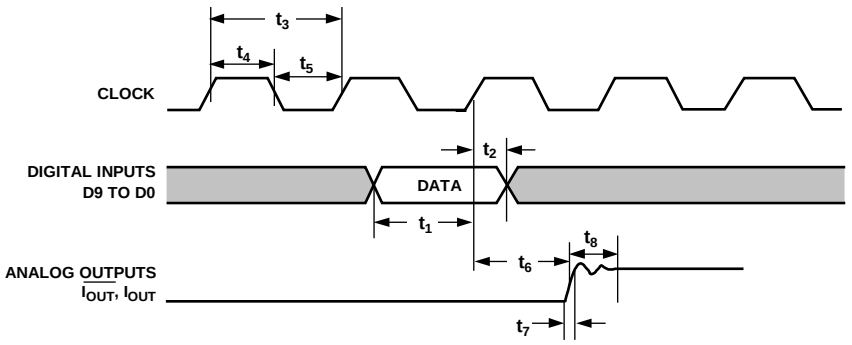


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{AA} to GND	7 V
Voltage on Any Digital Pin	GND − 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range(T_S)	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase Soldering (1 Minute)	220°C
I_{OUT} to GND[1]	0 V to V_{AA}

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

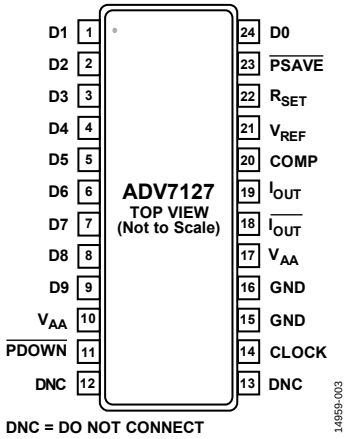


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 9, 24	D0 to D9	Data Inputs (TTL-Compatible). Data is latched on the rising edge of CLOCK. D0 is the least significant data bit. Unused data inputs are connected to either the regular printed circuit board (PCB) power or ground plane. Data inputs are red, green, or blue pixel inputs.
10, 17	V_{AA}	Analog Power Supply (5 V ± 5%). All V_{AA} pins on the ADV7127 must be connected.
11	$\overline{PDOWN}$	Power-Down Control Pin. The ADV7127 completely powers down, including the voltage reference circuit, when $\overline{PDOWN}$ is low.
12, 13	DNC	Do Not Connect. Do not connect to these pins.
14	CLOCK	Clock Input (TTL-Compatible). The rising edge of CLOCK latches D0 to D9 where D0 to D9 can be red, green, or blue pixel data inputs (TTL-compatible). CLOCK is typically the pixel clock rate of the video system. CLOCK is driven by a dedicated TTL buffer.
15, 16	GND	Ground. All GND pins must be connected.
18	$\overline{I_{OUT}}$	Differential Current Output. This pin is capable of directly driving a doubly terminated 75 Ω load. If not required, this output is tied to ground.
19	I_{OUT}	Current Output. This high impedance current source is capable of directly driving a doubly terminated 75 Ω coaxial cable.
20	COMP	Compensation Pin. COMP is a compensation pin for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between COMP and V_{AA}.
21	V_{REF}	Voltage Reference Input. An external 1.23 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 µF decoupling ceramic capacitor is connected between V_{REF} and V_{AA}.
22	R_{SET}	Full-Scale Adjust Control. A resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on I_{OUT} is given by I_{OUT} (mA) = 7968 × V_{REF} (V)/R_{SET} (Ω).
23	$\overline{PSAVE}$	Power Save Control Pin. The device is put into standby mode when $\overline{PSAVE}$ is low. The internal voltage reference circuit is still active.

TYPICAL PERFORMANCE CHARACTERISTICS

5 V

V_{AA} = 5 V, V_{REF} = 1.235 V, I_{OUT} = 17.62 µA, 50 Ω doubly terminated load, differential output loading, T_A = 25°C, unless otherwise noted.

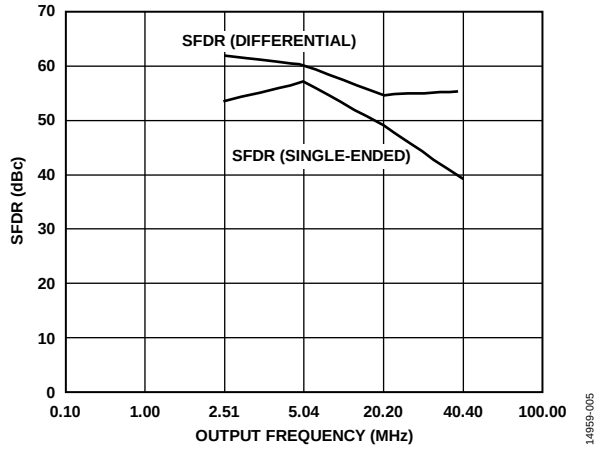


Figure 4. SFDR vs. Output Frequency (f_{OUT}) at f_{CLOCK} = 140 MHz (Single-Ended and Differential)

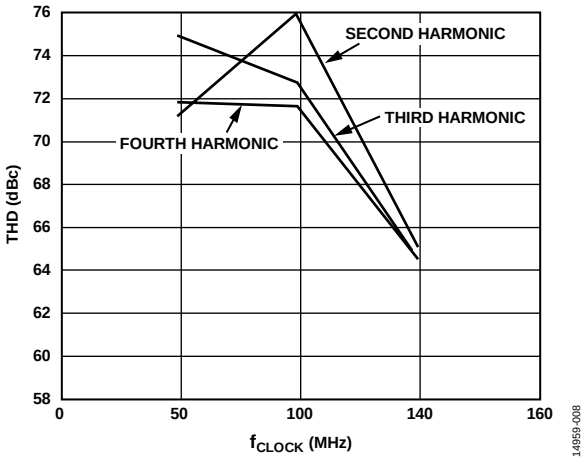


Figure 7. THD vs. f_{CLOCK} at f_{OUT} = 2 MHz (Second, Third, and Fourth Harmonics)

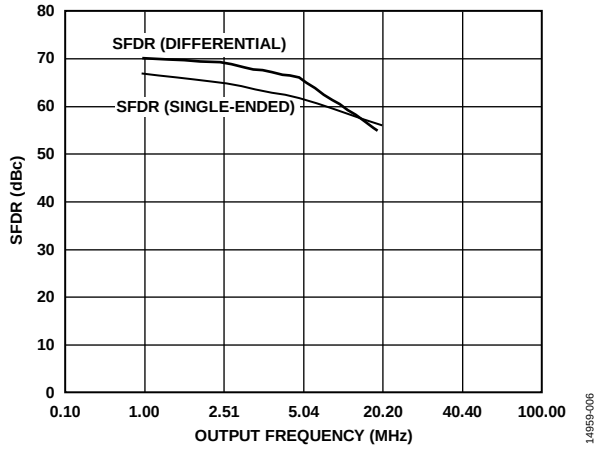


Figure 5. SFDR vs. Output Frequency (f_{OUT}) at f_{CLOCK} = 50 MHz (Single-Ended and Differential)

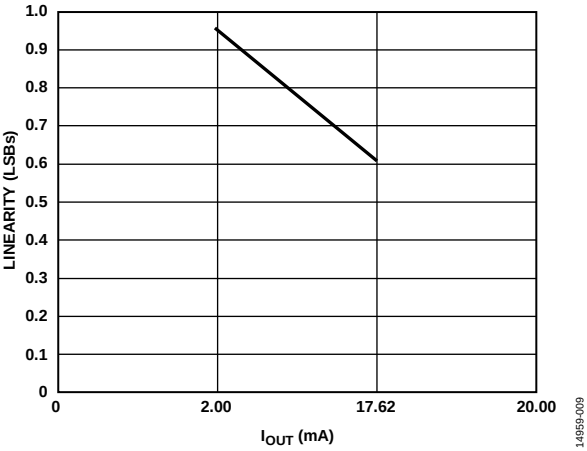


Figure 8. Linearity vs. I_{OUT}

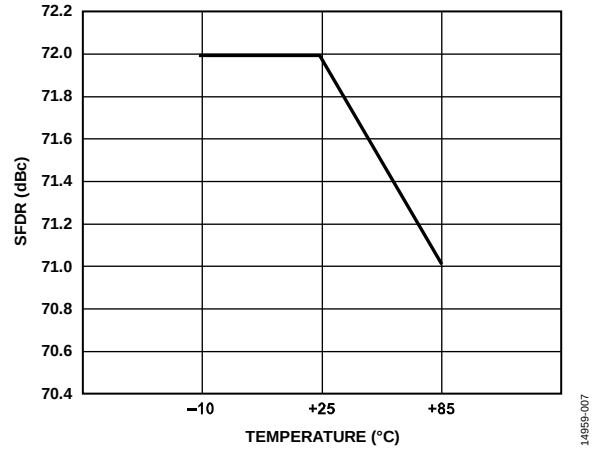


Figure 6. SFDR vs. Temperature at f_{CLOCK} = 50 MHz (f_{OUT} = 1 MHz)

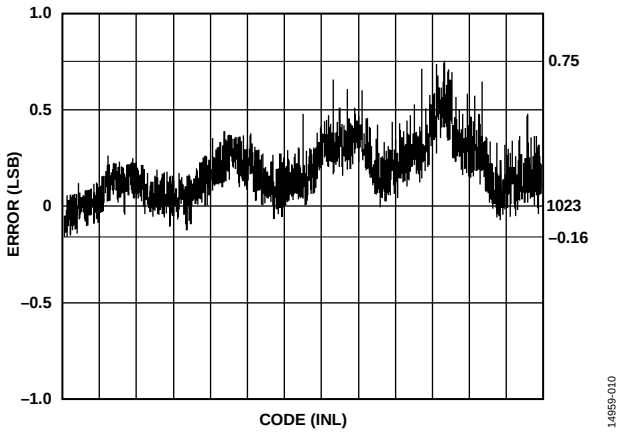


Figure 9. Error vs. Code

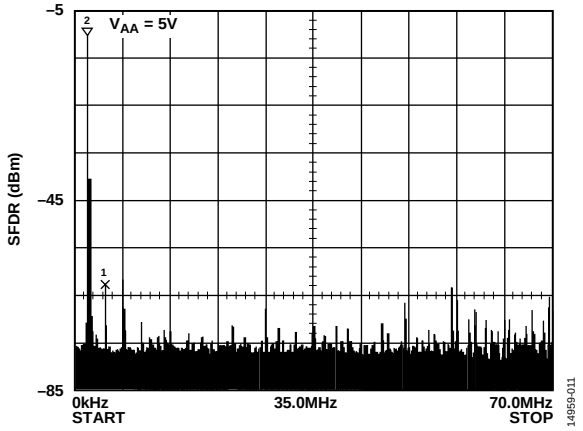


Figure 10. Single Tone SFDR at f_{CLOCK} = 140 MHz (f_{OUT1} = 2 MHz)

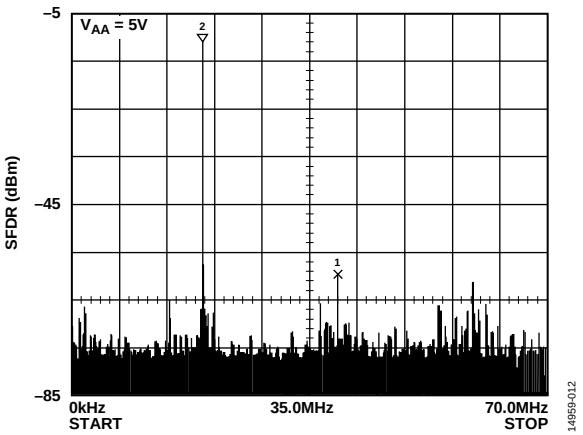


Figure 11. Single Tone SFDR at f_{CLOCK} = 140 MHz (f_{OUT1} = 20 MHz)

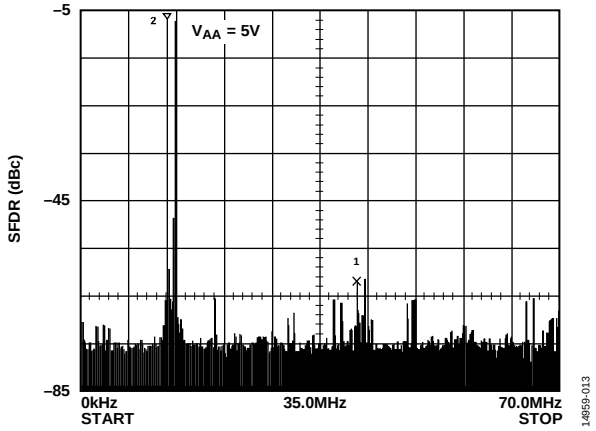


Figure 12. Dual Tone SFDR at f_{CLOCK} = 140 MHz (f_{OUT1} = 13.5 MHz, f_{OUT2} = 14.5 MHz)

3.3 V

V_{AA} = 3 V, V_{REF} = 1.235 V, I_{OUT} = 17.62 µA, 50 Ω doubly terminated load, differential output loading, T_A = 25°C, unless otherwise noted.

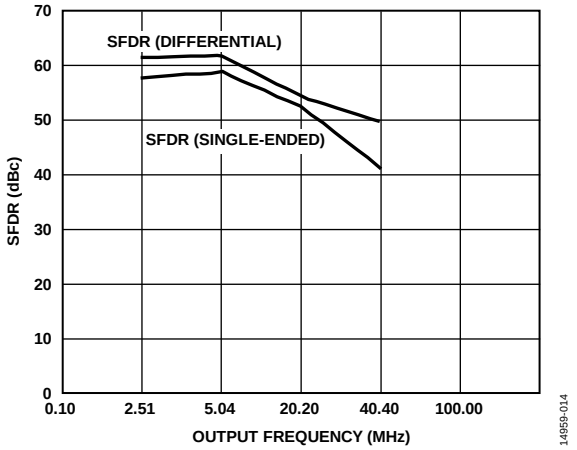


Figure 13. SFDR vs. Output Frequency (f_{OUT}) at f_{CLOCK} = 140 MHz (Single-Ended and Differential)

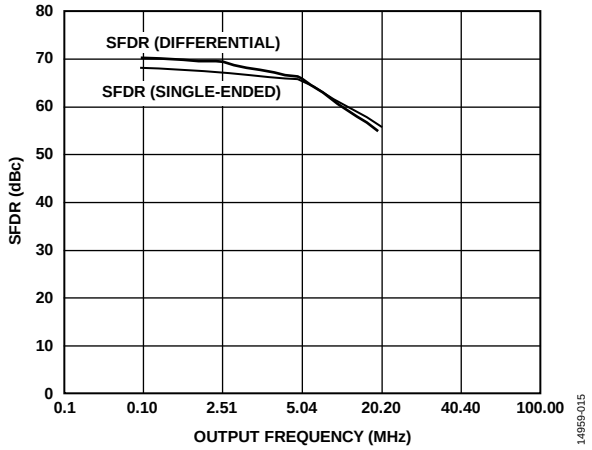


Figure 14. SFDR vs. Output Frequency (f_{OUT}) at f_{CLOCK} = 50 MHz (Single-Ended and Differential)

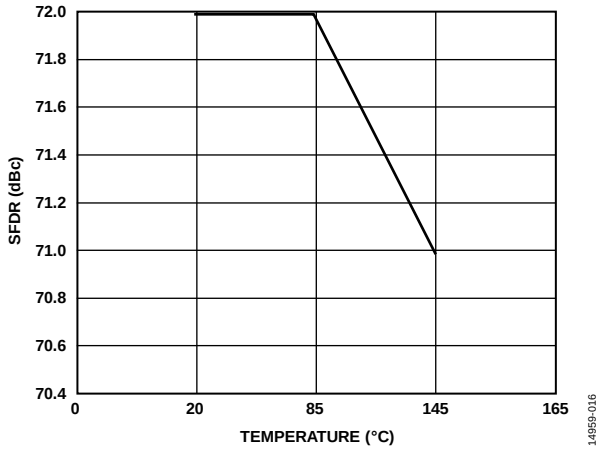


Figure 15. SFDR vs. Temperature at f_{CLOCK} = 50 MHz, (f_{OUT} = 1 MHz)

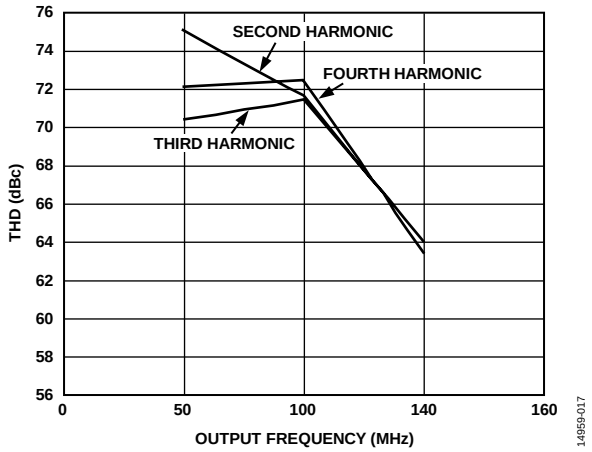


Figure 16. THD vs. f_{CLOCK} at Output Frequency f_{OUT} = 2 MHz (Second, Third, and Fourth Harmonics)

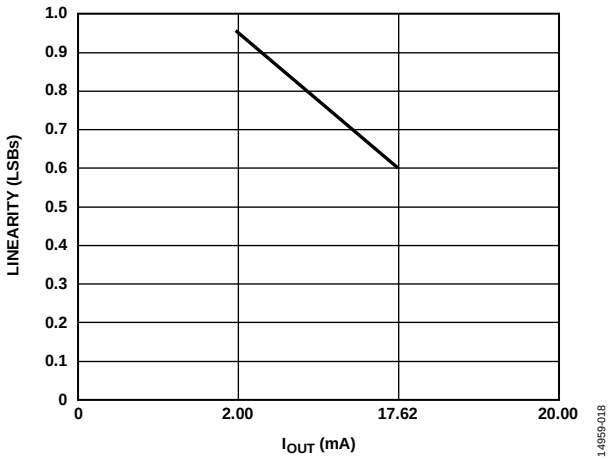


Figure 17. Linearity vs. I_{OUT}

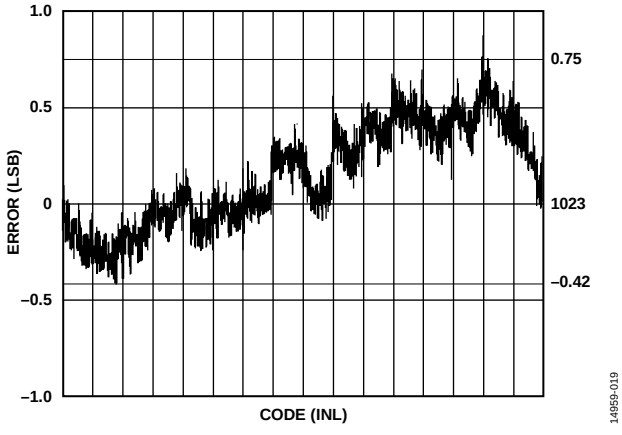


Figure 18. Error vs. Code

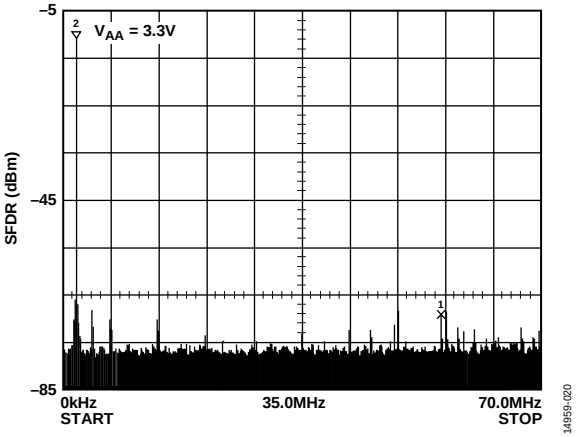


Figure 19. Single Tone SFDR at f_{CLOCK} = 140 MHz (f_{OUT1} = 2 MHz)

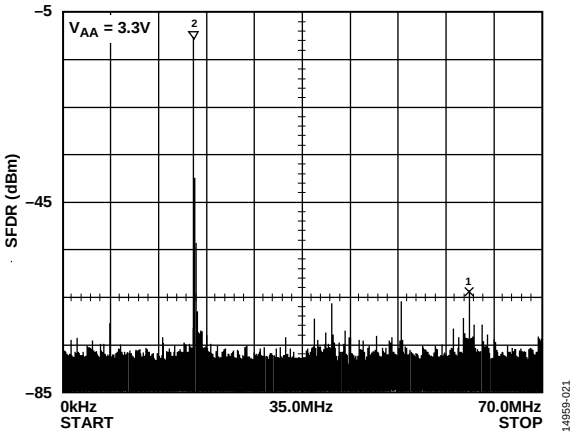


Figure 20. Single Tone SFDR at f_{CLOCK} = 140 MHz (f_{OUT1} = 20 MHz)

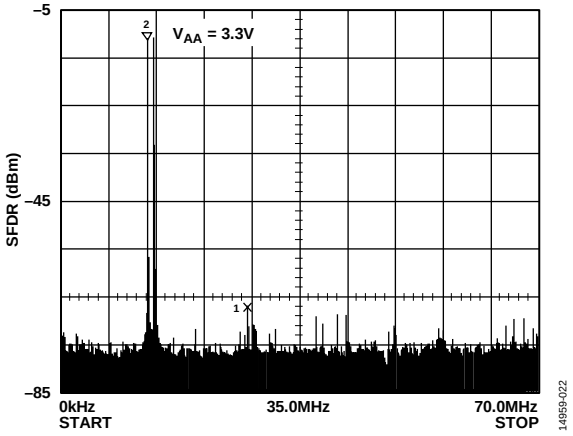


Figure 21. Dual Tone SFDR at f_{CLOCK} = 140 MHz (f_{OUT1} = 13.5 MHz, f_{OUT2} = 14.5 MHz)

TERMINOLOGY

Color Video (RGB)
Color video (RGB) usually refers to the technique of combining the three primary colors of red, green, and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Gray Scale
Gray scale is the discrete levels of video signal between the reference black and reference white levels. A 10-bit DAC contains 1024 different levels, whereas an 8-bit DAC contains 256.

Raster Scan
Raster scan is the most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
Reference black level is the maximum negative polarity amplitude of the video signal.

Reference White Level
Reference white level is the maximum positive polarity amplitude of the video signal.

Video Signal
Video signal is the portion of the composite video signal that varies in gray scale levels between reference white and reference black. It is also referred to as the picture signal, which is the portion that can be visually observed.

THEORY OF OPERATION

The ADV7127 contains one 10-bit DAC, with one input channel containing a 10-bit register. A reference amplifier is also integrated on board the device.

DIGITAL INPUTS

Ten bits of data (color information), D0 to D9, are latched into the device on the rising edge of each clock cycle. This data is presented to the 10-bit DAC and is then converted to an analog output waveform (see Figure 22).

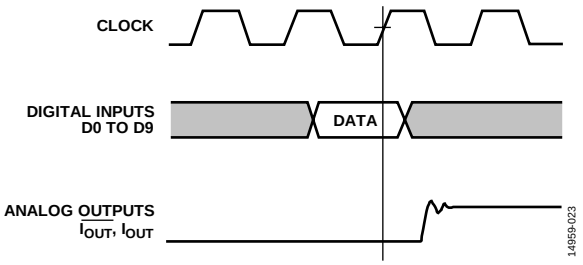


Figure 22. Video Data Input/Output

All of these digital inputs are specified to accept TTL logic levels.

CLOCK INPUT

The CLOCK input of the ADV7127 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and therefore the required CLOCK frequency, is determined by the onscreen resolution, according to the following equation:

Dot Rate = (*Horizontal Resolution* × *Vertical Resolution* × *Refresh Rate*)/*Retrace Factor*

where:
Horizontal Resolution is the number of pixels per line.
Vertical Resolution is the number of lines per frame.
Refresh Rate is the horizontal scan rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system or 30 Hz for an interlaced system.
Retrace Factor is the total blank time factor, which takes into account that the display is blanked for a certain fraction of the total duration of each frame (for example, 0.8).

If there is a graphics system with a 1024 × 1024 resolution, a noninterlaced 60 Hz refresh rate, and a retrace factor of 0.8, then

Dot Rate = (1024 × 1024 × 60)/0.8 = 78.6 MHz

The required CLOCK frequency is 78.6 MHz.

All video data and control inputs are latched into the ADV7127 on the rising edge of CLOCK, as previously described in the Digital Inputs section. It is recommended that the CLOCK input to the ADV7127 be driven by a TTL buffer (for example, 74F244).

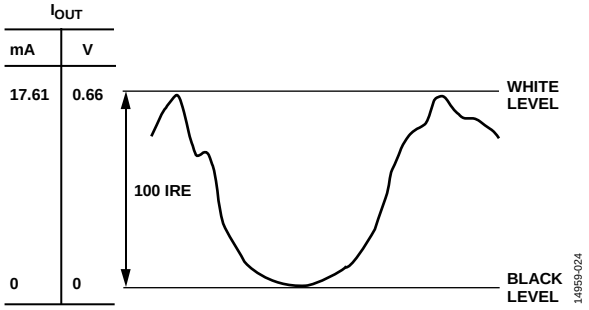


Figure 23. I_{OUT} RS-343A Video Output Waveform

Table 7. Video Output Truth Table (R_{SET} = 560 Ω, R_{LOAD} = 37.5 Ω)

Description Data	I_{OUT} (Ω)	$\overline{I_{OUT}}$ (Ω)	DAC Input
White Level	17.62	0	0x3FF
Video	Video	17.62 – Video	Data
Black Level	0	17.62	0x000

REFERENCE INPUT

The ADV7127 has an on-board voltage reference. The V_{REF} pin is normally terminated to V_{AA} through a 0.1 µF capacitor. Alternatively, the device can, if required, be overdriven by an external 1.23 V reference (AD1580).

A resistance R_{SET} connected between the R_{SET} pin and the GND pin determines the amplitude of the output video level according to the following equation:

$$I_{OUT}\,(\text{mA}) = (7968 \times V_{REF}\,(\text{V}))/R_{SET}\,(\Omega)$$

Using a variable value of R_{SET} allows accurate adjustment of the analog output video levels. Use of a fixed 560 Ω R_{SET} resistor yields the analog output levels quoted in Specifications section. These values typically correspond to the RS-343A video waveform values shown in Figure 23.

DIGITAL-TO-ANALOG CONVERTER

The ADV7127 contains a 10-bit DAC. The DAC is designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = 1) or GND (bit = 0) by a sophisticated decoding scheme. The use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The on-board operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

ANALOG OUTPUT

The analog output of the ADV7127 is a high impedance current source. The current output is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable. Figure 24 shows the required configuration for the output connected into a doubly terminated 75 Ω load. This arrangement develops RS-343A video output voltage levels across a 75 Ω monitor.

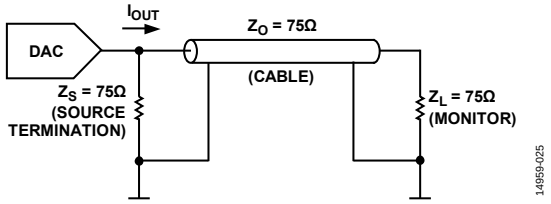


Figure 24. Analog Output Termination for RS-343A

A suggested method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 25. The output current level of the DAC remains unchanged, but the source termination resistance, Z_S, on the DAC is increased from 75 Ω to 150 Ω.

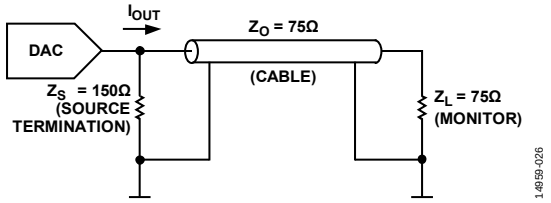


Figure 25. Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in the AN-205 Application Note, *Video Formats and Required Load Terminations*.

Figure 23 shows the video waveforms associated with the current output driving the doubly terminated 75 Ω load of Figure 24.

GRAY SCALE OPERATION

The ADV7127 can be used for standalone, gray scale (monochrome), or composite video applications (that is, only one channel used for video information).

VIDEO OUTPUT BUFFER

The ADV7127 is specified to drive transmission line loads, which is what most monitors are rated as. The analog output configurations to drive such loads are shown in Figure 26. However, in some applications, it may be required to drive long transmission line cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of the output buffers compensates for some cable distortion. Buffers with large full power bandwidths and gains between two and four are required. These buffers need to be able to supply sufficient current over the complete output voltage swing. Analog Devices, Inc., produces a range of suitable op amps for such applications. These include the AD843/AD844/AD847 series of monolithic op amps. In very high frequency applications (80 MHz), the AD8061 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit results in any desired video level.

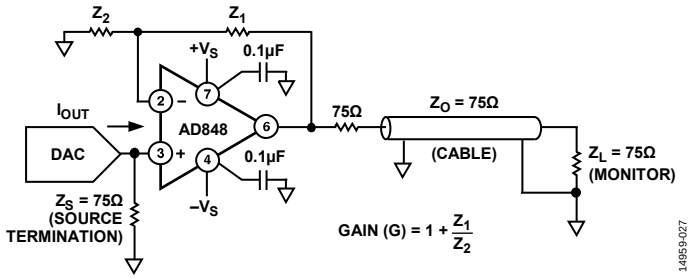


Figure 26. AD848 As an Output Buffer

PCB LAYOUT CONSIDERATIONS

The ADV7127 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7127, it is imperative that great care be given to the PCB layout. Figure 27 shows a recommended connection diagram for the ADV7127.

The PCB layout is optimized for lowest noise on the ADV7127 power and ground lines. Radiated and conducted noise can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins is minimized to inductive ringing.

GROUND PLANES

The ADV7127 and associated analog circuitry have a separate ground plane referred to as the analog ground plane. This ground plane connects to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 27. The ferrite bead is located as close as possible (within 3 inches) to the ADV7127.

The analog ground plane encompasses all ADV7127 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces, and any output amplifiers. The regular PCB ground plane area encompasses all the digital signal traces, excluding the ground pins, leading up to the ADV7127.

POWER PLANES

The PCB layout has two distinct power planes: one for analog circuitry and one for digital circuitry. The analog power plane encompasses the ADV7127 (V_{AA}) and all associated analog circuitry. This power plane is connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 27. This bead is located within 3 inches of the ADV7127.

The PCB power plane provides power to all digital logic on the PCB, and the analog power plane provides power to all ADV7127 power pins, voltage reference circuitry, and any output amplifiers. The PCB power and ground planes do not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane contributes to a reduction in plane to plane noise coupling.

SUPPLY DECOUPLING

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors (see Figure 27).

Optimum performance is achieved by the use of 0.1 µF ceramic capacitors. Each of the two groups of V_{AA} is individually decoupled to ground. The V_{AA} pins (Pin 10 and Pin 17) must be decoupled with capacitors to GND. Decouple the pins by placing the capacitors as close as possible to the device with the capacitor leads as short as possible between the V_{AA} and GND pins, thus minimizing lead inductance.

It is important to note that while the ADV7127 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer must pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) provides an electromagnetic interface (EMI) suppression between the switching power supply and the main PCB. Alternatively, consider using a 3-terminal voltage regulator.

DIGITAL SIGNAL INTERCONNECT

The digital signal lines to the ADV7127 must be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines must not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7127 must be avoided to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs are connected to the regular PCB power plane (V_{CC}) and not the analog power plane.

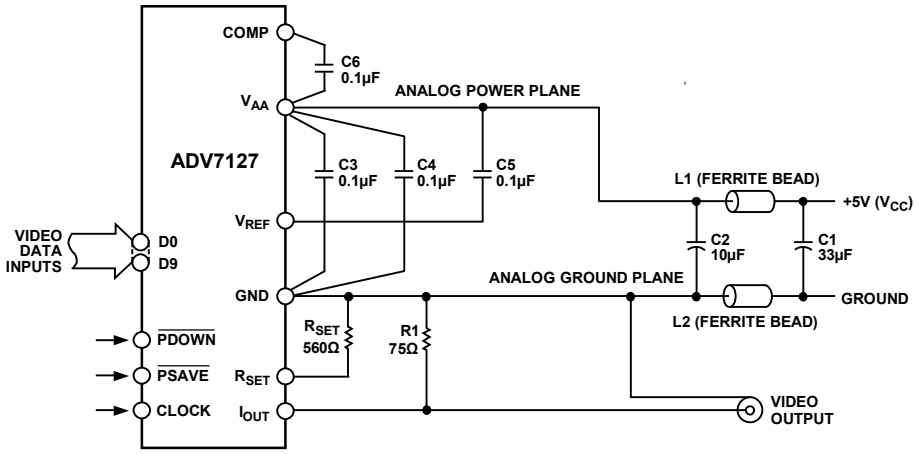
ANALOG SIGNAL INTERCONNECT

The ADV7127 is located as close as possible to the output connectors, which minimizes noise pickup and reflections due to impedance mismatch.

The video output signals overlay the ground plane and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance must be as close as possible to the ADV7127 to minimize reflections.

Additional information on PCB design is available in the AN-333 Application Note, *Design and Layout of a Video Graphics System for Reduced EMI*.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1	33µF TANTALUM CAPACITOR	
C2	10µF TANTALUM	
C3, C4, C5, C6	0.1µF CERAMIC CAPACITOR	
L1, L2	FERRITE BEAD	FAIR-RITE 274300111 OR MURATA BL01/02/03
R1	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	560Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 27. Typical Connection Diagram and Component List

OUTLINE DIMENSIONS

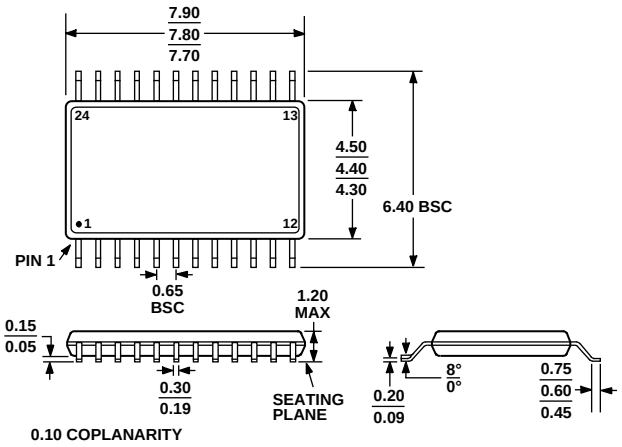


Figure 28. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Speed Options	Temperature Range	Package Description	Package Option
ADV7127JRUZ240	240 MHz	0°C to 70°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADV7127KRUZ50	50 MHz	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADV7127KRUZ50-REEL	50 MHz	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADV7127KRUZ140	140 MHz	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADV7127KRU50	50 MHz	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADV7127KRU50-REEL	50 MHz	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADV7127KRU140	140 MHz	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24

[1] Z = RoHS Compliant Part.

D14959-0-1/17(A)