AD8522–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5.0 V ± 10%, R_L = No Load, –40°C ≤ T_A ≤ +85°C, both DACs tested, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution[1]	N		12			Bits
Relative Accuracy	INL		-1.5	±0.5	+1.5	LSB
Differential Nonlinearity	DNL	Monotonic	-1	±0.5	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+0.5	+3	mV
Full-Scale Voltage[2]	V_{FS}	Data = FFF_H	4.079	4.095	4.111	Volts
Full-Scale Tempco[2, 3]	TCV_{FS}			±15		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching Error	$\Delta V_{FS}A/B$			±1		LSB
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H, $\Delta V_{OUT} \leq 3$ LSB			±5	mA
Load Regulation at Half-Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load[3]	C_L	No Oscillation		500		pF
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current[4]	I_{REF}	$\Delta V_{REF} < 18$ mV			5	mA
Line Rejection	LN_{REJ}			0.025	0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 to 5 mA, Data = 800_H		0.025	0.1	%/mA
LOGIC INPUTS & OUTPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance[3]	C_{IL}				10	pF
Logic Output Voltage Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Logic Output Voltage High	V_{OH}	I_{OH} = 400 µA	3.5			V
TIMING SPECIFICATIONS[3, 5]						
Clock Width High	t_{CH}		35			ns
Clock Width Low	t_{CL}		35			ns
Load Pulse Width	t_{LDW}		25			ns
Data Setup	t_{DS}		10			ns
Data Hold	t_{DH}		20			ns
Clear Pulse Width	t_{CLRW}		20			ns
Load Setup	t_{LD1}		10			ns
Load Hold	t_{LD2}		10			ns
Select	t_{CSS}		30			ns
Deselect	t_{CSH}		30			ns
Clock to SDO Propagation Delay	t_{PD}		20	45	80	ns
AC CHARACTERISTICS[3, 5]						
Voltage Output Settling Time[6]	t_S	To ±1 LSB of Final Value		16		µs
Crosstalk	C_T	Signal Measured at DAC Output, While Changing Opposite $\overline{LDA}/\overline{B}$		38		dB
DAC Glitch	Q	Half-Scale Transition		13		nV s
Digital Feedthrough	D_{FT}	Signal Measured at DAC Output, While Changing Data Without $\overline{LDA}/\overline{B}$		2		nV s
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{DD} = 5.5 V, V_{IH} = 2.4 V or V_{IL} = 0.8 V		3	5	mA
		V_{DD} = 5 V, V_{IL} = 0 V		1	2	mA
Power Dissipation[7]	P_{DISS}	V_{DD} = 5 V, V_{IH} = 2.4 V or V_{IL} = 0.8 V		15	25	mW
		V_{DD} = 5 V, V_{IL} = 0 V		5	10	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES

[1] 1 LSB = 1 mV for 0 V to +4.095 V output range.

[2] Includes internal voltage reference error.

[3] These parameters are guaranteed by design and not subject to production testing.

[4] Very little sink current is available at the V_{REF} pin. Use external buffer if setting up a virtual ground.

[5] All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[6] The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

[7] Power Dissipation is calculated $I_{DD} \times 5$ V.

Specifications subject to change without notice.

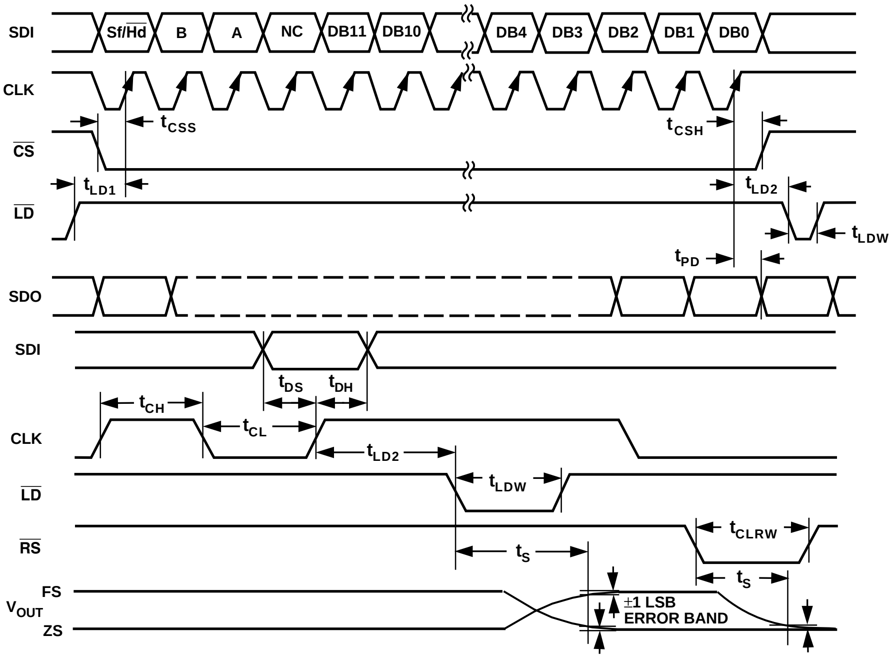


Figure 2. Timing Diagram

SERIAL INPUT REGISTER DATA FORMAT

Last First

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	NC	A	B	Sf/Hd

Table I. Truth Table

Data Word			**Ext Pins**		
Sf/$\overline{\text{Hd}}$	**B**	**A**	**$\overline{\text{LDA}}$**	**$\overline{\text{LDB}}$**	**DAC Register**
Hardware Load:					
L	X	X	↓	↓	Loads DACA + DACB with Data from SR
L	X	X	↓	H	Loads DACA with Data from SR
L	X	X	H	↓	Loads DACB with Data from SR
L	X	X	H	H	No Load
Software Decode Load:					
H	L	L	X	X	No Load
H	H	L	↓	↓	Loads DACB with Data from SR, See Note 1 Below
H	H	L	H	H	No Load
H	L	H	↓	↓	Loads DACA with Data from SR, See Note 1 Below
H	L	H	H	H	No Load
H	H	H	↓	↓	Loads DACA + DACB with Data from SR, See 1 Note Below
H	H	H	H	H	No Load

NOTES

[1] In software mode $\overline{\text{LDA}}$ and $\overline{\text{LDB}}$ perform the same function. They can be tied together or the unused pin should be tied high.

[2] External Pins $\overline{\text{LDA}}$ and $\overline{\text{LDB}}$ should always be high when shifting Data into the shift register.

[3] ↓ symbol denotes negative transition.

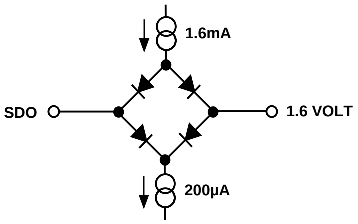
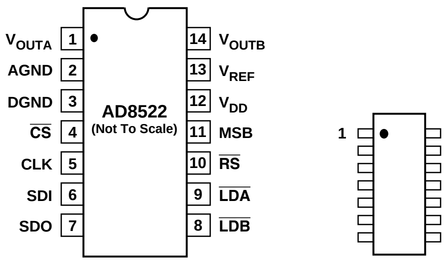


Figure 3. AC Timing SDO Pin Load Circuit

PIN DESCRIPTION

Pin	Function
SDI	Serial Data Input, input data loads directly into the shift register.
CLK	Clock input, positive edge clocks data into shift register.
$\overline{\text{CS}}$	Chip Select, active low input. Prevents shift register loading when high. Does not affect $\overline{\text{LDA}}$ and $\overline{\text{LDB}}$ operation.
$\overline{\text{LDA}}/\overline{\text{B}}$	Load DAC register strobes, active low. Transfers shift register data to DAC register. See truth table for operation. Software decode feature only requires one $\overline{\text{LD}}$ strobe. Tie $\overline{\text{LDA}}$ and $\overline{\text{LDB}}$ together or use one of them with the other pin tied high.
SDO	Serial Data Output. Output of shift register, always active.
$\overline{\text{RS}}$	Resets DAC registers to condition determined by MSB pin. Active low input.
MSB	Digital input: High presets DAC registers to half scale (800_H); Low clears all registers to zero (000_H), when $\overline{\text{RS}}$ is strobed to active low.
V_{DD}	Positive +5 V power supply input. Tolerance ±10%.
AGND	Analog Ground Input.
DGND	Digital Ground Input.
V_{REF}	Reference Voltage Output, 2.5 V nominal.
$V_{OUT\ A/B}$	DAC A/B voltage outputs, 4.095 V full scale, ±5 mA output.

PIN CONFIGURATION



14-Pin Plastic DIP **14-Lead SO-14**

Table II. Truth Tables

$\overline{\text{RS}}$	MSB	DAC Register Preset Register Activity
0	0	Asynchronously Resets DAC Registers to Zero Scale
0	1	Asynchronously Presets DAC Registers to Half Scale (800_H)
1	X	None

$\overline{\text{CS}}$	CLK	Shift Register Shift Register
1	X	No Effect
0	↑	Shifts Register One Bit, SDO Outputs Data from 16 Clocks Earlier

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND & AGND	–0.3 V, +7 V
Logic Inputs and Output to DGND	–0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND	–0.3 V, V_{DD} + 0.3 V
V_{REF} to AGND	–0.3 V, V_{DD} + 0.3 V
AGND to DGND	–0.3 V, V_{DD}
I_{OUT} Short Circuit to GND or V_{DD}	50 mA
Package Power Dissipation	$(T_J \max – T_A)/\theta_{JA}$
Thermal Resistance, θ_{JA}	
14-Pin Plastic DIP Package (N-14)	83°C/W
14-Lead SOIC Package (SO-14)	120°C/W
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8522AN	–40°C to +85°C	14-Pin P-DIP	N-14
AD8522AR	–40°C to +85°C	14-Lead SOIC	SO-14

The AD8522 contains 1482 transistors.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8522 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!

ESD SENSITIVE DEVICE

OPERATION

The AD8522 is a complete ready-to-use dual 12-bit digital-to-analog converter. Only one +5 V power supply is necessary for operation. It contains two voltage-switched, 12-bit, laser-trimmed digital-to-analog converters, a curvature-corrected bandgap reference, rail-to-rail output op amps, input registers, and DAC registers. The serial data interface consists of a serial data input (SDI), clock ($\overline{\text{CLK}}$), and two load strobe pins ($\overline{\text{LDA}}$, $\overline{\text{LDB}}$) with an active low $\overline{\text{CS}}$ strobe. In addition, an asynchronous $\overline{\text{RS}}$ pin will set all DAC register bits to zero causing the V_{OUT} to become zero volts, or to midscale for trimming applications when the MSB pin is programmed to Logic 1. This function is useful for power on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The internal DAC is a 12-bit voltage-mode device with an output that swings from AGND potential to the 2.5 V internal bandgap voltage. It uses a laser-trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage that provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.638 (= 4.095 V/2.5 V) in order to set the 4.095 V full-scale output (1 mV/LSB). See Figure 4 for an equivalent circuit schematic of the analog section.

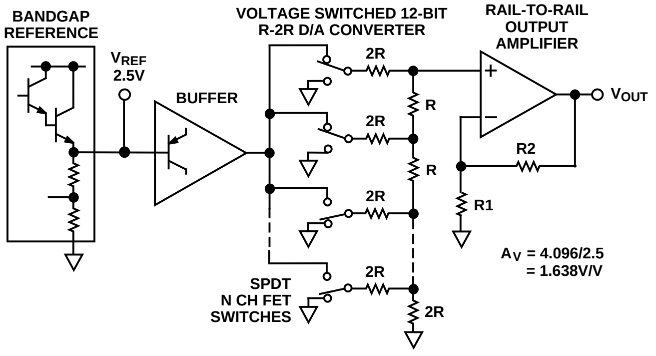


Figure 4. Equivalent AD8522 Schematic of Analog Portion

The op amp has a 16 µs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals versus positive. See the oscilloscope photos in the "Typical Performance Characteristics" section of this data sheet.

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 5 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P channel pull-up device that can supply GND terminated loads, especially important at the –10% supply tolerance value of 4.5 V.

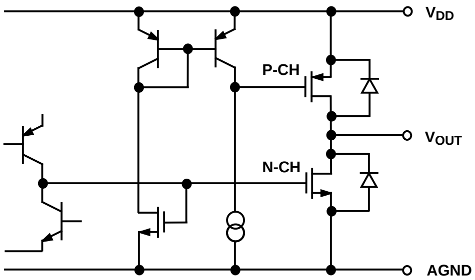


Figure 5. Equivalent Analog Output Circuit

Figures 6 and 7 in the typical performance characteristics section provide information on output swing performance near ground and full scale as a function of load. In addition to resistive load driving capability the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

REFERENCE SECTION

The internal 2.5 V curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. The voltage generated by the reference is available at the V_{REF} pin. Since V_{REF} is *not* intended to drive heavy external loads, it must be buffered. The equivalent emitter follower output circuit of the V_{REF} pin is shown in Figure 4.

Bypassing the V_{REF} pin will improve noise performance; however, bypassing is not required for proper operation. Figure 10 shows broad band noise performance.

POWER SUPPLY

The very low power consumption of the AD8522 is a direct result of a circuit design optimizing use of a CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors good analog accuracy is achieved.

For power consumption sensitive applications it is important to note that the internal power consumption of the AD8522 is strongly dependent on the actual input voltage levels present on the SDI, CLK, $\overline{\text{CS}}$, MSB, $\overline{\text{LDA}}$, $\overline{\text{LDB}}$ and $\overline{\text{RS}}$ pins. Since these inputs are standard CMOS logic structures, they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. Consequently for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A V_{INL} = 0 V on the logic input pins provides the lowest standby dissipation of 1 mA with a +5 V power supply.

As with any analog system, it is recommended that the AD8522 power supply be bypassed on the same PC card that contains the chip. Figure 12 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifiers used in the AD8522 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.5 V to +5.5 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the AD8522 is possible down to +4.3 V. The minimum operating supply voltage versus load current plot, in Figure 7, provides information for operation below V_{DD} = +4.5 V.

TIMING AND CONTROL

The AD8522 has a 16-bit serial input register that accepts clocked in data when the CS pin is active low. The DAC registers are updated by the Load Enable ($\overline{\text{LDA}}$ and $\overline{\text{LDB}}$) pins.

The AD8522 offers two modes of data loading. The first mode, hardware-load, directs the data currently clocked into the serial shift register into either the DAC A or the DAC B register or both depending on the external active low strobing of the $\overline{\text{LDA}}$ or $\overline{\text{LDB}}$ pin. Serial data register bit Sf/$\overline{\text{Hd}}$ must be low for this mode to be in effect.

The second mode of operation is software-load which is designed to minimize the number of control lines connected to the AD8522. In this mode of operation the $\overline{\text{LDA}}$ and $\overline{\text{LDB}}$ pins act as one control input taking the present contents of the serial input register and transferring the 12 bits of data into the decoded address determined by the address bits A and B in the serial input register.

Unipolar Output Operation

This is the basic mode of operation for the AD8522. The AD8522 has been designed to drive loads as low as 820 Ω in parallel with 500 pF. The code table for this operation is shown in Table III.

Table III. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+4.095
801	2049	+2.049
800	2048	+2.048
7FF	2047	+2.047
000	0	0

Typical Performance Characteristics

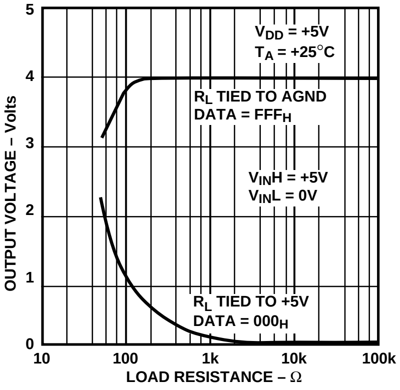


Figure 6. Output Swing vs. Load

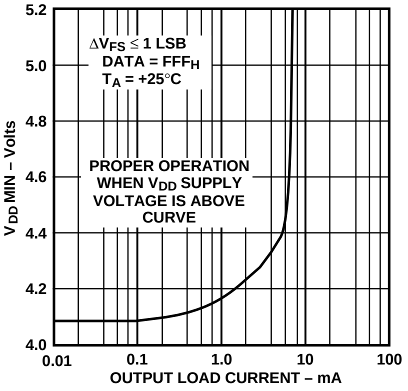


Figure 7. Minimum Supply Voltage vs. Load Current

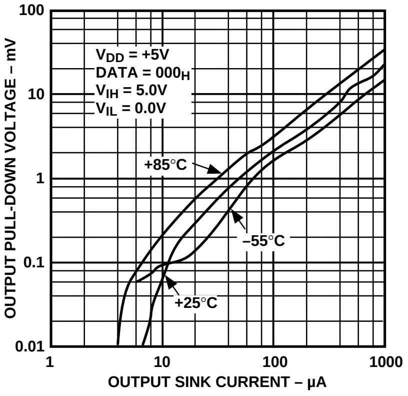


Figure 8. Pull-Down Voltage vs. Output Sink Current Capability

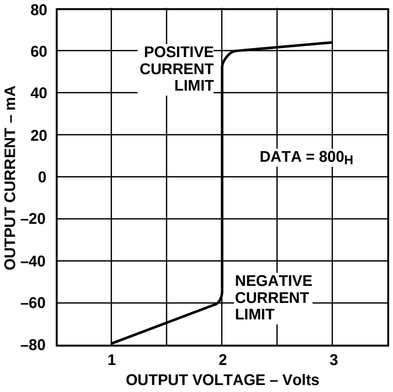


Figure 9. I_{OUT} vs. V_{OUT}

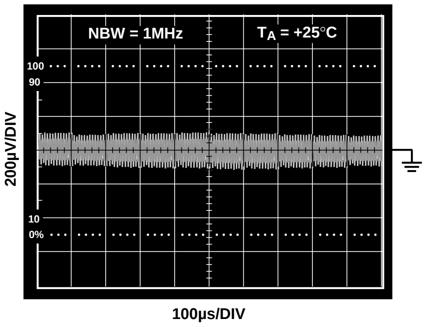


Figure 10. Broadband Noise

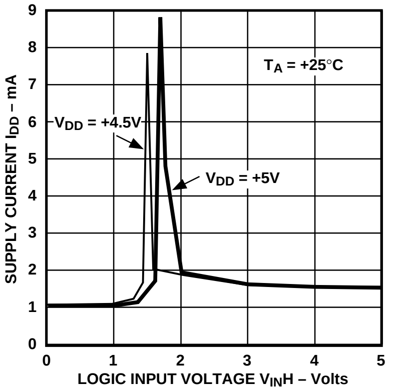


Figure 11. Supply Current vs. Logic Input Voltage

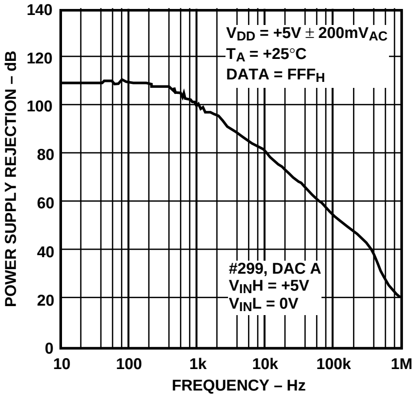


Figure 12. Power Supply Rejection vs. Frequency

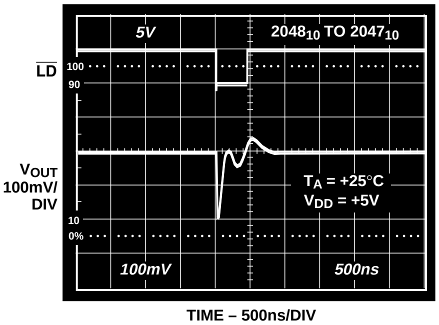


Figure 13. Midscale Transition Performance

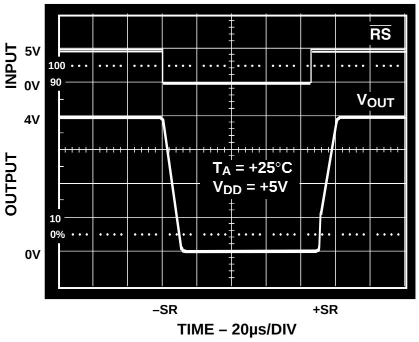


Figure 14. Large Signal Settling Time

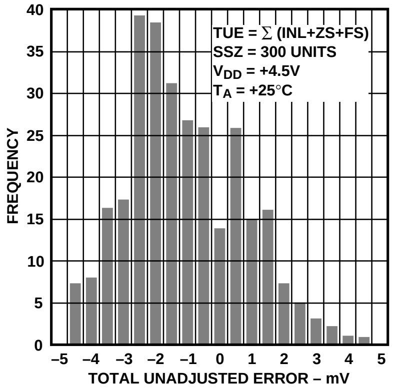


Figure 15. Total Unadjusted Error Histogram

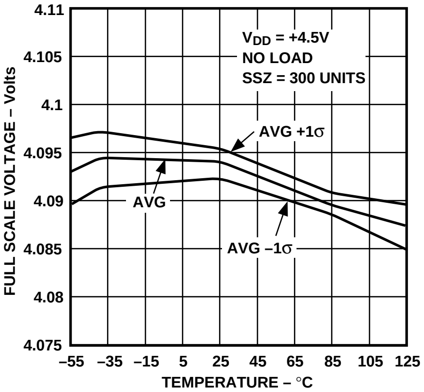


Figure 16. Full-Scale Voltage vs. Temperature

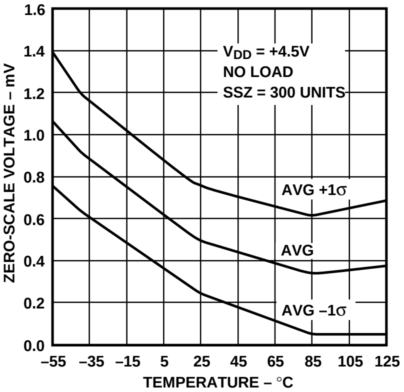


Figure 17. Zero-Scale Voltage vs. Temperature

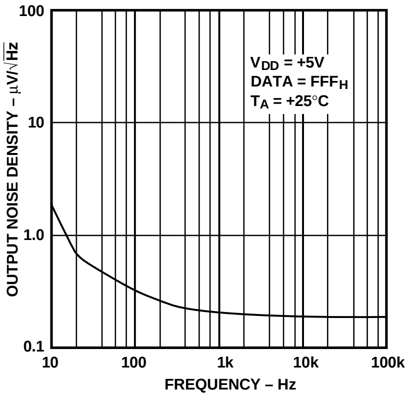


Figure 18. Output Voltage Noise Density vs. Frequency

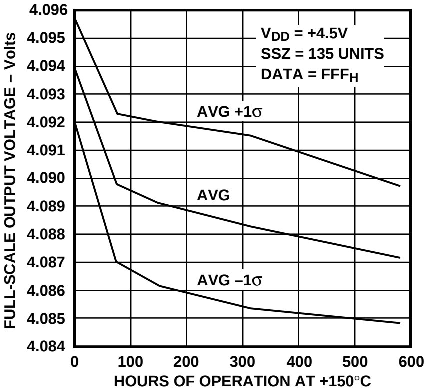


Figure 19. Long Term Drift Accelerated by Burn-In

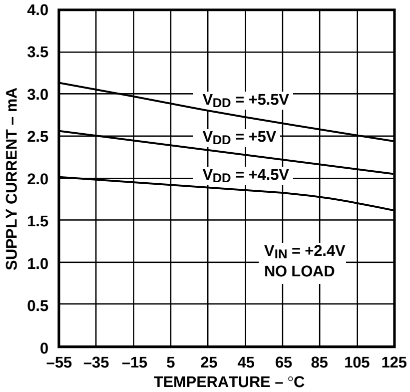


Figure 20. Supply Current vs. Temperature

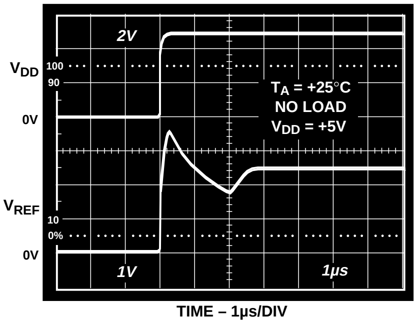


Figure 21. Reference Startup vs. Time

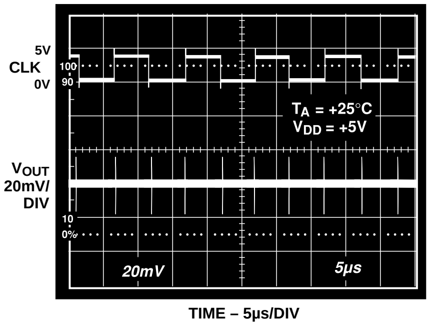


Figure 22. Digital Feedthrough vs. Time

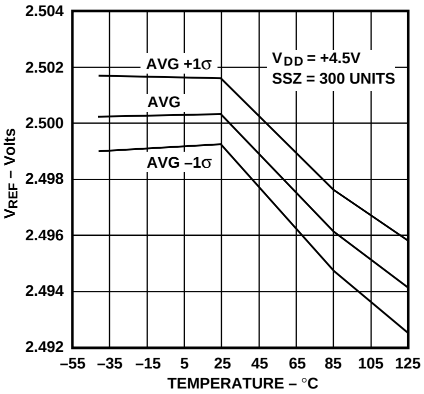


Figure 23. Reference Voltage vs. Temperature

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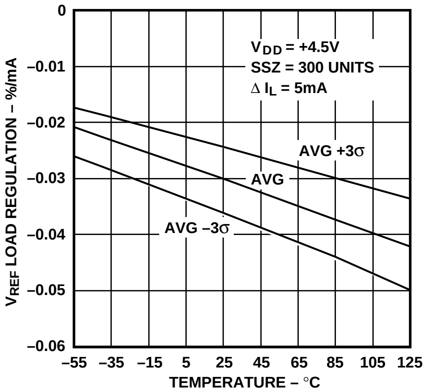


Figure 24. Reference Load Regulation vs. Temperature

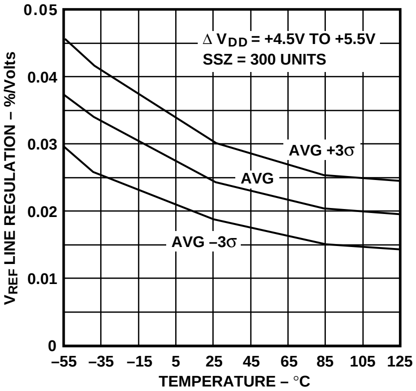
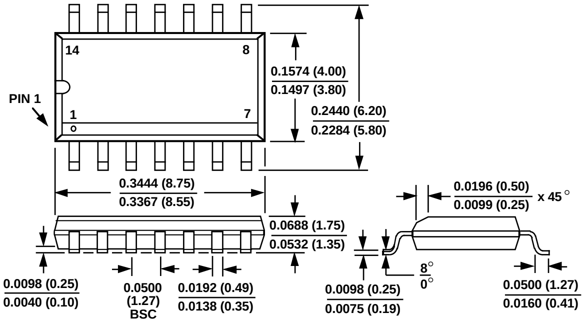


Figure 25. Reference Line Regulation vs. Temperature

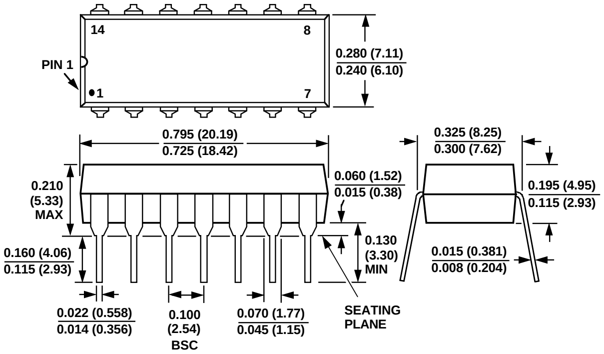
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Narrow Body SOIC (SO-14)



14-Lead Epoxy DIP (N-14)



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