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AD8369—SPECIFICATIONS (V_S = 5 V, T = 25°C, R_S = 200 Ω, R_L = 1000 Ω, Frequency = 70 MHz, at maximum gain, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range	3 dB Bandwidth	LF*		600	MHz
GAIN CONTROL INTERFACE					
Voltage Gain Span			45		dB
Maximum Gain	All bits high (1 1 1 1)		40		dB
Minimum Gain	All bits low (0 0 0 0)		–5		dB
Gain Step Size			3		dB
Gain Step Accuracy	Over entire gain range, with respect to 3 dB step		±0.05		dB
Gain Step Response Time	Step = 3 dB, settling to 10% of final value		30		ns
INPUT STAGE					
Input Resistance	From INHI to INLO		200		Ω
	From INHI to COMM, from INLO to COMM		100		Ω
Input Capacitance	From INHI to INLO		0.1		pF
	From INHI to COMM, from INLO to COMM		1.1		pF
Input Noise Spectral Density			2		$nV/\sqrt{Hz}$
Input Common-Mode DC Voltage	Measured at pin CMDC		1.7		V
Maximum Linear Input	$\lvert V_{INHI} - V_{INLO} \rvert$ at Minimum Gain		2.2		V
OUTPUT STAGE					
Output Resistance	From OPHI to OPLO		200		Ω
	From OPHI to COMM, from OPLO to COMM		100		Ω
Output Capacitance	From OPHI to OPLO		0.25		pF
	From OPHI to COMM, from OPLO to COMM		1.5		pF
Common-Mode DC Voltage	No input signal		$V_S/2$		V
Slew Rate	Output step = 1 V		1200		V/µs
POWER INTERFACE					
Supply Voltage		3.0		5.5	V
Quiescent Current	PWUP high		37	42	mA
vs. Temperature	–40°C ≤ T_A ≤ 85°C			52	mA
Disable Current	PWUP low		400	750	µA
vs. Temperature	–40°C ≤ T_A ≤ 85°C			1	mA
POWER UP INTERFACE	Pin PWUP				
Enable Threshold				1.0	V
Disable Threshold		2.2			V
Response Time	Time delay following low to high transition on PWUP until output settles to within 10% of final value		7		µs
Input Bias Current	PWUP = 5 V		160		µA
DIGITAL INTERFACE	Pins SENB, BIT0, BIT1, BIT2, BIT3, and DENB				
Low Condition				2.0	V
High Condition		3.0			V
Input Bias Current	Low input		150		µA
Frequency = 10 MHz					
Voltage Gain			40.5		dB
Gain Flatness	Within ±10 MHz of 10 MHz		±0.05*		dB
Noise Figure			7.0		dB
Output IP3	f1 = 9.945 MHz, f2 = 10.550 MHz		+22		dBV rms
			+22		dBm
IMD_3	f1 = 9.945 MHz, f2 = 10.550 MHz				
	$V_{OPHI} - V_{OPLO}$ = 1 V p-p composite		–74		dBc
Harmonic Distortion	Second-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–72		dBc
	Third-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–71		dBc
P1dB	For ±1 dB deviation from linear gain		+3		dBV rms
			+3		dBm

*The low frequency high-pass corner is determined by the capacitor on pin FILT, C_{FILT}. See the Theory of Operation section for details.

SPECIFICATIONS (Continued)

Parameter	Conditions	Min	Typ	Max	Unit
Frequency = 70 MHz					
Voltage Gain			40.5		dB
Gain Flatness	Within ±20 MHz of 70 MHz		±0.1		dB
Noise Figure			7.0		dB
Output IP3	f1 = 69.3 MHz, f2 = 70.7 MHz		+19.5		dBV rms
			+19.5		dBm
IMD_3	f1 = 69.3 MHz, f2 = 70.7 MHz				
	$V_{OPHI} - V_{OPLO}$ = 1 V p-p composite		–69		dBc
Harmonic Distortion	Second-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–68		dBc
	Third-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–64		dBc
P1dB	For ±1 dB deviation from linear gain		+3		dBV rms
			+3		dBm
Frequency = 140 MHz					
Voltage Gain			40.0		dB
Gain Flatness	Within ±20 MHz of 140 MHz		±0.10		dB
Noise Figure			7.0		dB
Output IP3	f1 = 139.55 MHz, f2 = 140.45 MHz		+17		dBV rms
			+17		dBm
IMD_3	f1 = 139.55 MHz, f2 = 140.45 MHz				
	$V_{OPHI} - V_{OPLO}$ = 1 V p-p composite		–64		dBc
Harmonic Distortion	Second-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–63		dBc
	Third-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–55		dBc
P1dB	For ±1 dB deviation from linear gain		+3		dBV rms
			+3		dBm
Frequency = 190 MHz					
Voltage Gain			39.7		dB
Gain Flatness	Within ±20 MHz of 190 MHz		±0.1		dB
Noise Figure			7.2		dB
Output IP3	f1 = 189.55 MHz, f2 = 190.45 MHz		+15.5		dBV rms
			+15.5		dBm
IMD_3	f1 = 189.55 MHz, f2 = 190.45 MHz				
	$V_{OPHI} - V_{OPLO}$ = 1 V p-p composite		–61		dBc
Harmonic Distortion	Second-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–57		dBc
	Third-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–51		dBc
P1dB	For ±1 dB deviation from linear gain		+2		dBV rms
			+2		dBm
Frequency = 240 MHz					
Voltage Gain			39.3		dB
Gain Flatness	Within ±20 MHz of 240 MHz		±0.1		dB
Noise Figure			7.2		dB
Output IP3	f1 = 239.55 MHz, f2 = 240.45 MHz		+14		dBV rms
			+14		dBm
IMD_3	f1 = 239.55 MHz, f2 = 240.45 MHz				
	$V_{OPHI} - V_{OPLO}$ = 1 V p-p composite		–58		dBc
Harmonic Distortion	Second-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–50		dBc
	Third-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–49		dBc
P1dB	For ±1 dB deviation from linear gain		+1.5		dBV rms
			+1.5		dBm
Frequency = 320 MHz					
Voltage Gain			39.0		dB
Gain Flatness	Within ±20 MHz of 320 MHz		±0.15		dB
Noise Figure			7.4		dB
Output IP3	f1 = 319.55 MHz, f2 = 320.45 MHz		+11.5		dBV rms
			+11.5		dBm
IMD_3	f1 = 319.55 MHz, f2 = 320.45 MHz				
	$V_{OPHI} - V_{OPLO}$ = 1 V p-p composite		–53		dBc
Harmonic Distortion	Second-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–47		dBc
	Third-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–49		dBc
P1dB	For ±1 dB deviation from linear gain		+1.0		dBV rms
			+1.0		dBm

SPECIFICATIONS (Continued)

Parameter	Conditions	Min	Typ	Max	Unit
Frequency = 380 MHz					
Voltage Gain			38.5		dB
Gain Flatness	Within ±20 MHz of 380 MHz		±0.15		dB
Noise Figure			7.8		dB
Output IP3	f1 = 379.55 MHz, f2 = 380.45 MHz		+8.5		dBV rms
			+8.5		dBm
IMD_3	f1 = 379.55 MHz, f2 = 380.45 MHz,				
	$V_{OPHI} - V_{OPLO}$ = 1 V p-p composite		–47		dBc
Harmonic Distortion	Second-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–45		dBc
	Third-Order, $V_{OPHI} - V_{OPLO}$ = 1 V p-p		–49		dBc
P1dB	For ±1 dB deviation from linear gain		+0.5		dBV rms
			+0.5		dBm

Specifications subject to change without notice.

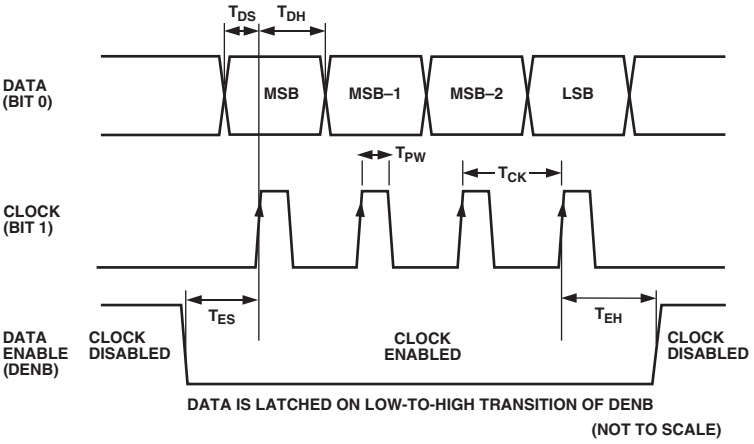
TIMING SPECIFICATIONS

SERIAL PROGRAMMING TIMING REQUIREMENTS
(V_S = 5 V, T = 25°C)

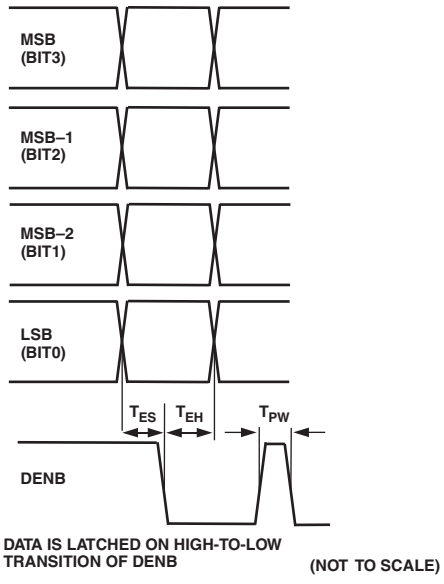
Parameter	Typ	Unit
Minimum Clock Pulsewidth (T_{PW})	10	ns
Minimum Clock Period (T_{CK})	20	ns
Minimum Setup Time Data vs. Clock (T_{DS})	2	ns
Minimum Setup Time Data Enable vs. Clock (T_{ES})	2	ns
Minimum Hold Time Clock vs. Data Enable (T_{EH})	2	ns
Minimum Hold Time Data vs. Clock (T_{DH})	4	ns

PARALLEL PROGRAMMING TIMING REQUIREMENTS
(V_S = 5 V, T = 25°C)

Parameter	Typ	Unit
Minimum Setup Time Data Enable vs. Data (T_{ES})	2	ns
Minimum Hold Time Data Enable vs. Data (T_{EH})	2	ns
Minimum Data Enable Width (T_{PW})	4	ns



Serial Programming Timing



Parallel Programming Timing

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V_S, VPOS . . . . . 5.5 V
PWUP . . . . . V_S + 200 mV
BIT0, BIT1, BIT2, BIT3, DENB, SENB . . . . . V_S + 200 mV
Input Voltage, $V_{INHI} - V_{INLO}$ . . . . . 4 V
Input Voltage, V_{INHI} or V_{INLO} with respect to COMM . . 4.5 V
Input Voltage, $V_{INHI} - V_{INLO}$ with respect to COMM
. . . . . COMM – 200 mV
Internal Power Dissipation . . . . . 265 mW
θ_{JA} . . . . . 121.48°C/W
Maximum Junction Temperature . . . . . 125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (soldering 60 sec) . . . . . to 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

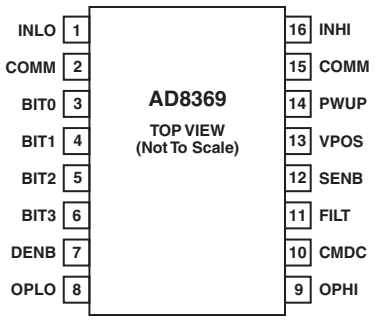
Table I. Typical Voltage Gain vs. Gain Code (V_S = 5 V, f = 70 MHz)

Gain Code	BIT3	BIT2	BIT1	BIT0	Typical Gain (dB) R_L = 1 kΩ	Typical Gain (dB) R_L = 200 Ω
0	0	0	0	0	–5	–10
1	0	0	0	1	–2	–7
2	0	0	1	0	1	–4
3	0	0	1	1	4	–1
4	0	1	0	0	7	2
5	0	1	0	1	10	5
6	0	1	1	0	13	8
7	0	1	1	1	16	11
8	1	0	0	0	19	14
9	1	0	0	1	22	17
10	1	0	1	0	25	20
11	1	0	1	1	28	23
12	1	1	0	0	31	26
13	1	1	0	1	34	29
14	1	1	1	0	37	32
15	1	1	1	1	40	35

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8369 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

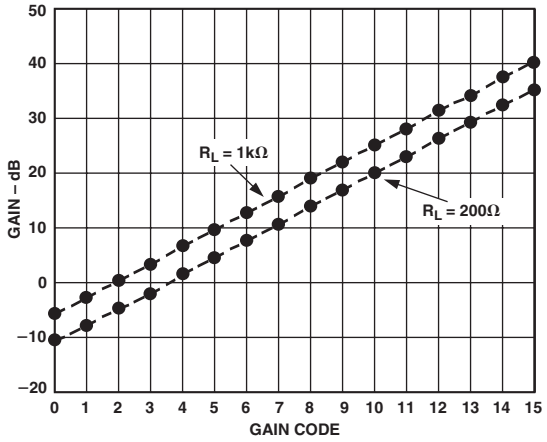
PIN CONFIGURATION



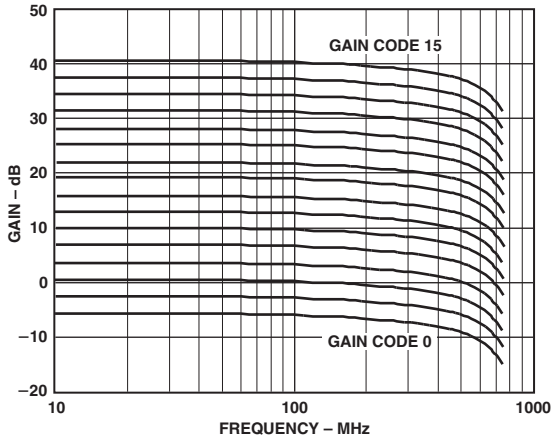
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	INLO	Balanced Differential Input. Internally biased, should be ac-coupled.
2	COMM	Device Common. Connect to low impedance ground.
3	BIT0	Gain Selection Least Significant Bit. Used as DATA input signal when in serial mode of operation.
4	BIT1	Gain Selection Control Bit. Used as CLOCK input pin when in serial mode of operation.
5	BIT2	Gain Selection Control Bit. Inactive when in serial mode of operation.
6	BIT3	Gain Selection Most Significant Bit. Inactive when in serial mode of operation.
7	DENB	Data Enable Pin. Writes data to register. See Timing Specifications for details.
8	OPLO	Balanced Differential Output. Biased to midsupply, should be ac-coupled.
9	OPHI	Balanced Differential Output. Biased to midsupply, should be ac-coupled.
10	CMDC	Common-Mode Decoupling Pin. Connect bypass capacitor to ground for additional common-mode supply decoupling beyond the existing internal decoupling.
11	FILT	High-Pass Filter Connection. Used to set high-pass corner frequency.
12	SENB	Serial or Parallel Interface Select. Connect SENB to VPOS for serial operation. Connect SENB to COMM for parallel operation.
13	VPOS	Positive Supply Voltage, V_S = +3 V to +5.5 V.
14	PWUP	Power-Up Pin. Connect PWUP to VPOS to power up the device. Connect PWUP to COMM to power-down.
15	COMM	Device Common. Connect to a low impedance ground.
16	INHI	Balanced Differential Input. Internally biased, should be ac-coupled.

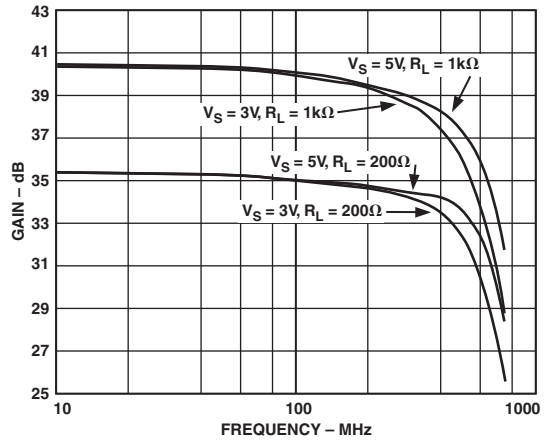
(V_S = 5 V, T = 25°C, R_S = 200 Ω, Maximum gain, unless otherwise noted.)



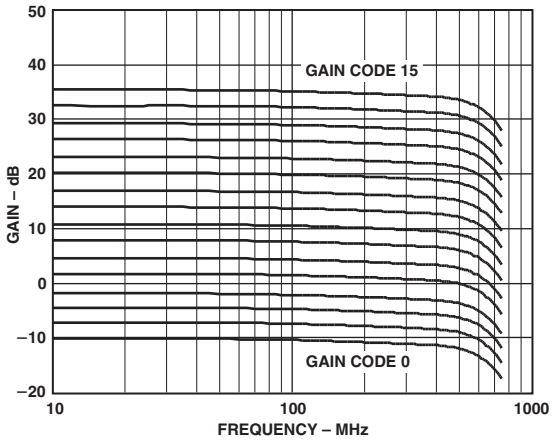
TPC 1. Gain vs. Gain Code at 70 MHz



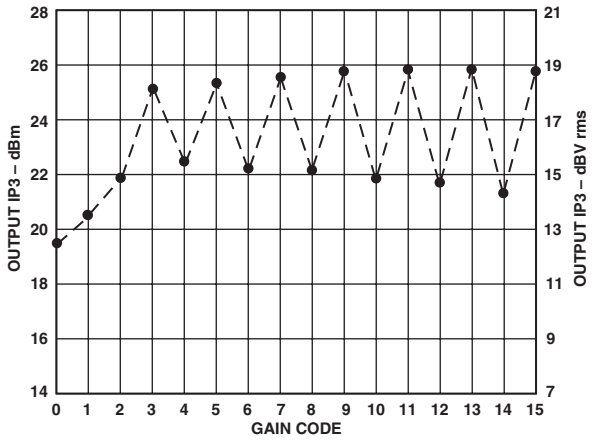
TPC 4. Gain vs. Frequency by Gain Code, R_L = 1 kΩ



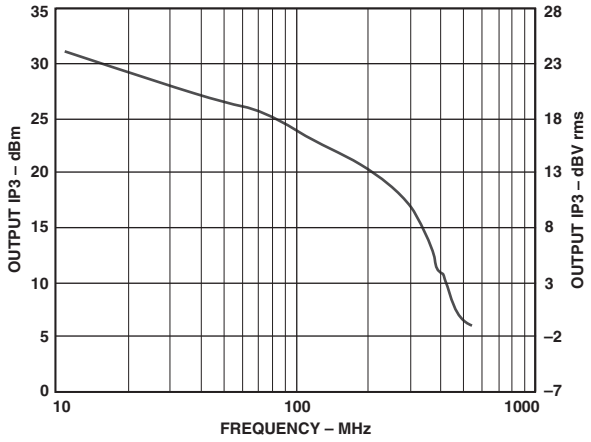
TPC 2. Maximum Gain vs. Frequency by R_L and Supply Voltage



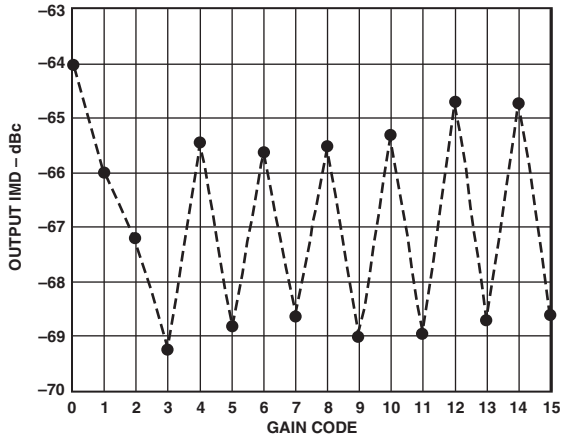
TPC 5. Gain vs. Frequency by Gain Code, R_L = 200 Ω



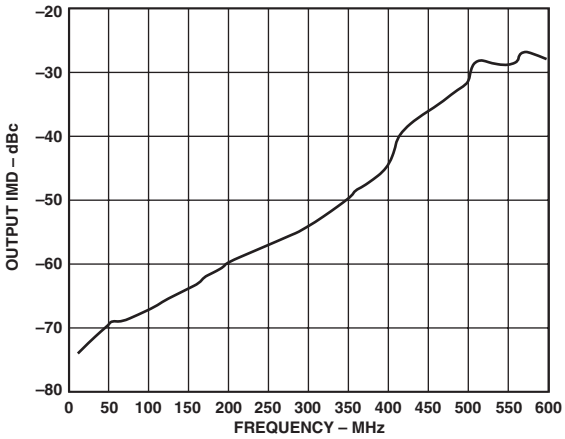
TPC 3. Output IP3 vs. Gain Code at 70 MHz, V_S = 5 V, R_L = 200 Ω



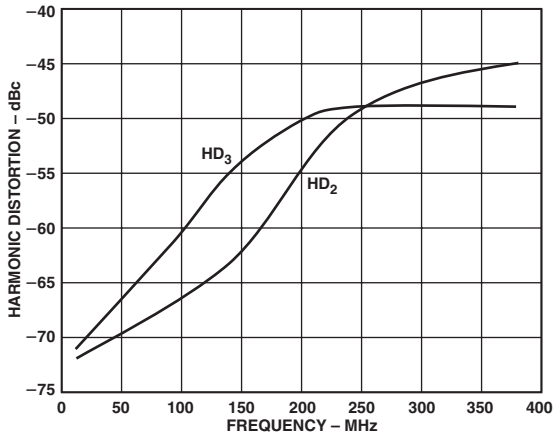
TPC 6. Output IP3 vs. Frequency, V_S = 5 V, R_L = 200 Ω Maximum Gain



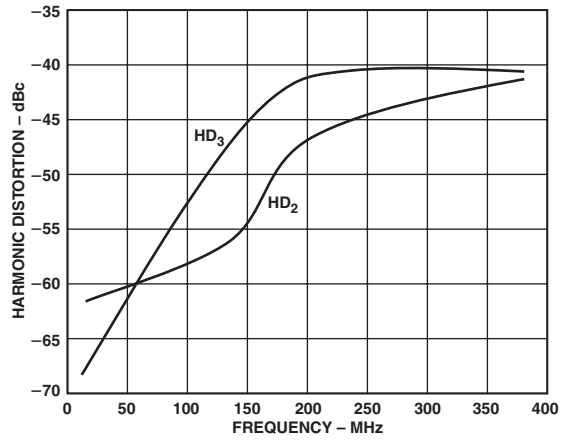
TPC 7. Two-Tone, IMD_3 vs. Gain Code at 70 MHz, $V_{OPHI} – V_{OPLO}$ = 1 V p-p, V_S = 5 V, R_L = 1 kΩ



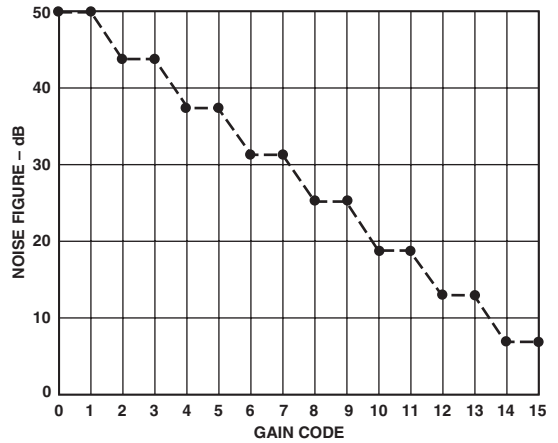
TPC 10. Two-Tone IMD_3 vs. Frequency $V_{OPHI} – V_{OPLO}$ = 1 V p-p, V_S = 5 V, R_L = 1 kΩ, Maximum Gain



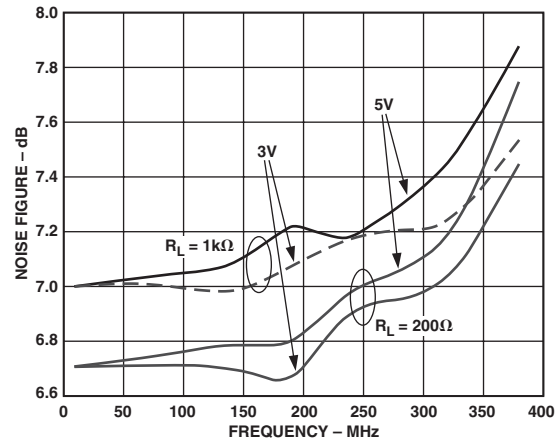
TPC 8. Harmonic Distortion at $V_{OPHI} – V_{OPLO}$ = 1 V p-p vs. Frequency, V_S = 5 V, R_L = 1 kΩ, Maximum Gain



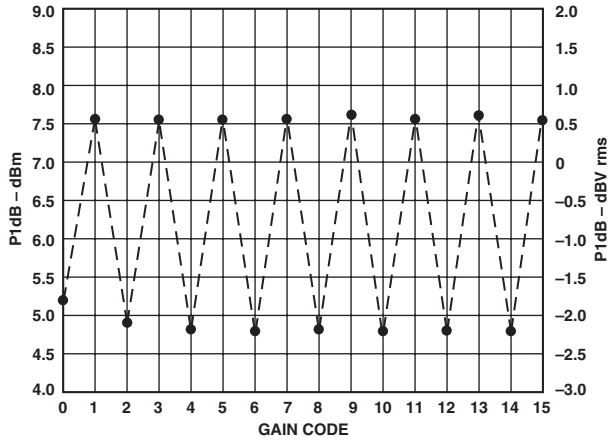
TPC 11. Harmonic Distortion at $V_{OPHI} – V_{OPLO}$ = 1 V p-p vs. Frequency, V_S = 5 V, R_L = 200 Ω, Maximum Gain



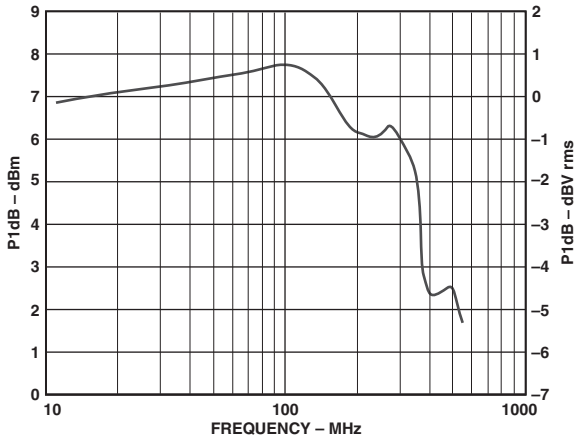
TPC 9. Noise Figure vs. Gain Code at 70 MHz, V_S = 5 V, R_L = 200 Ω



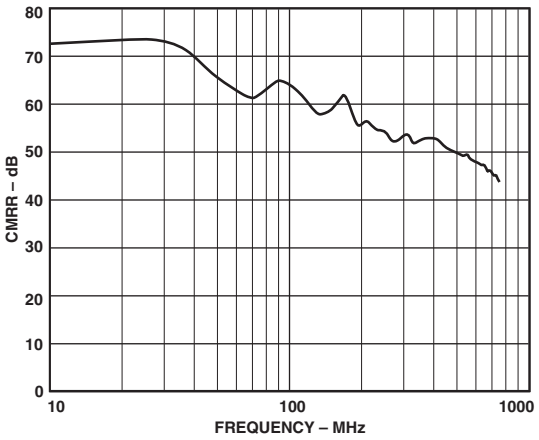
TPC 12. Noise Figure vs. Frequency by R_L and Supply Voltage at Maximum Gain



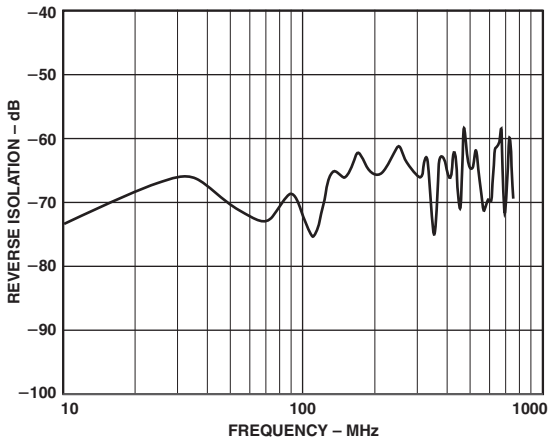
TPC 13. Output P1dB vs. Gain Code at 70 MHz, V_S = 5 V, R_L = 200 Ω



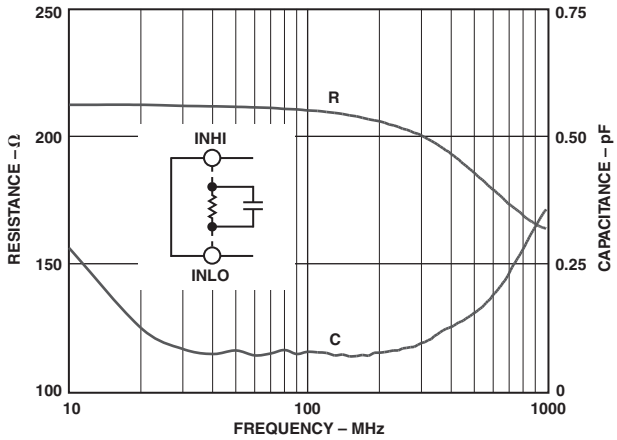
TPC 16. Output P1dB vs. Frequency, V_S = 5 V, R_L = 200 Ω, Maximum Gain



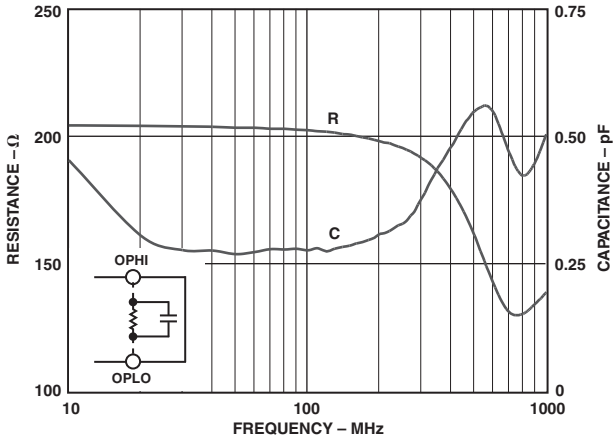
TPC 14. Common-Mode Rejection Ratio vs. Frequency at Maximum Gain, V_S = 5 V, R_L = 200 Ω (Refer to Appendix for Definition)



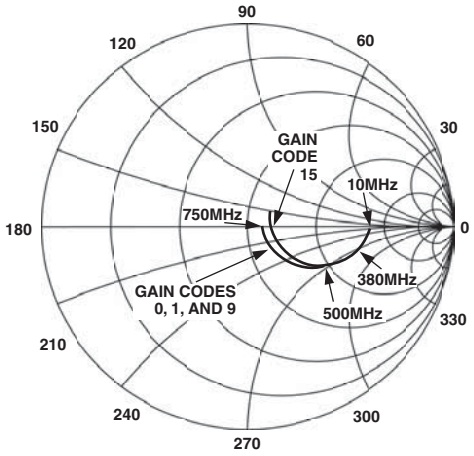
TPC 17. Reverse Isolation vs. Frequency at Maximum Gain, V_S = 5 V, R_L = 200 Ω (Refer to Appendix for Definition)



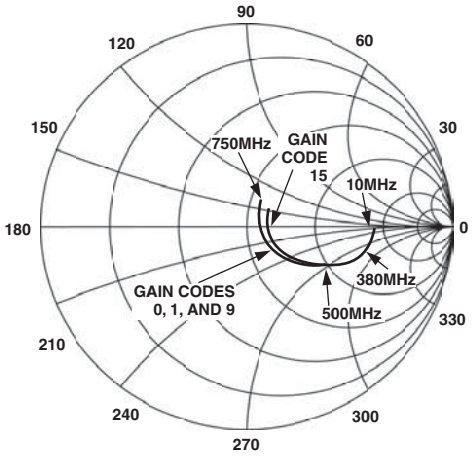
TPC 15. Equivalent Input Resistance and Capacitance vs. Frequency at Maximum Gain



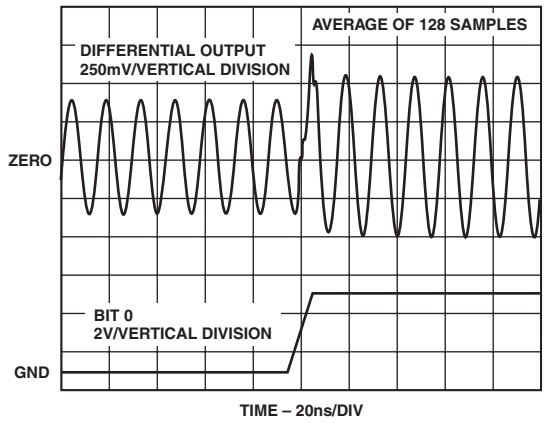
TPC 18. Equivalent Output Resistance and Capacitance vs. Frequency at Maximum Gain



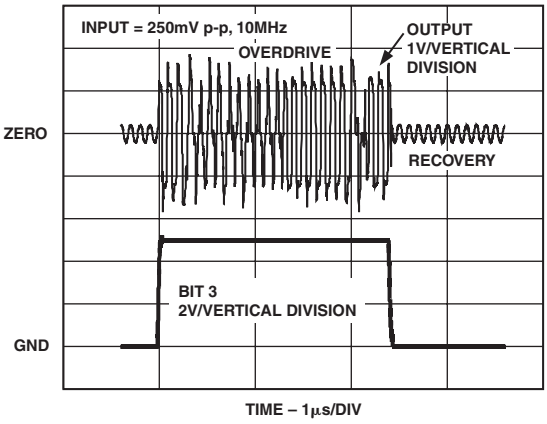
TPC 19. Differential Input Reflection Coefficient, S_{11}, Z_O = 50 Ω Differential, Selected Gain Codes



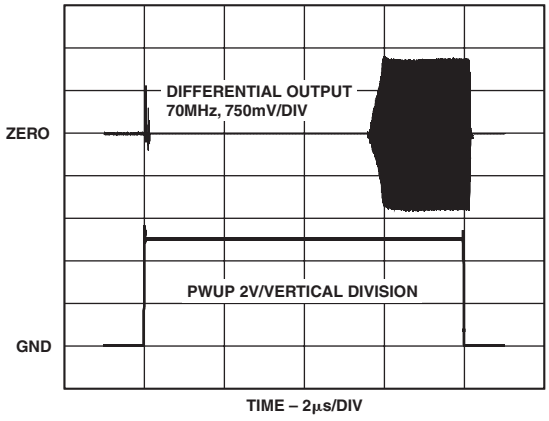
TPC 22. Differential Output Reflection Coefficient, S_{22}, Z_O = 50 Ω Differential, Selected Gain Codes



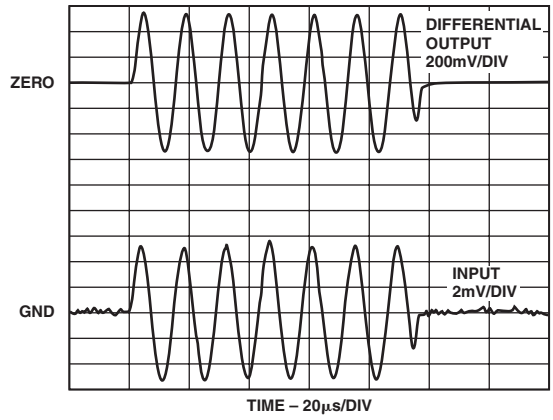
TPC 20. Gain Step Time Domain Response, 3 dB Step, V_S = 5 V, R_L = 1 kΩ, Parallel Transparent Mode



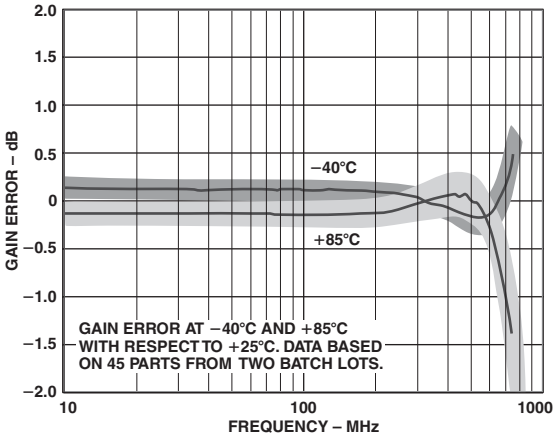
TPC 23. Overdrive Recovery, Maximum Gain, V_S = 5 V, R_L = 1 kΩ, Parallel Transparent Mode



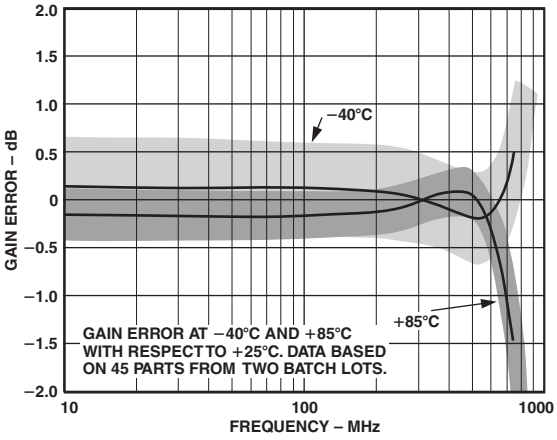
TPC 21. PWUP Time Domain Response, Maximum Gain, V_S = 5 V, R_L = 1 kΩ



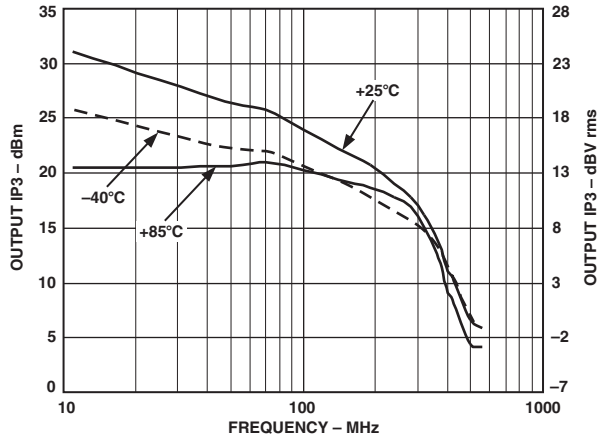
TPC 24. Pulse Response, Maximum Gain, V_S = 5 V, R_L = 1 kΩ



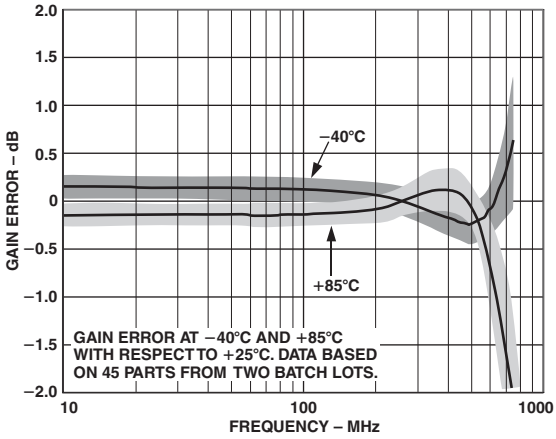
TPC 25. Gain Error Due to Temperature Change vs. Frequency, 3 Sigma to Either Side of Mean, V_S = 5 V, R_L = 1 kΩ, Maximum Gain



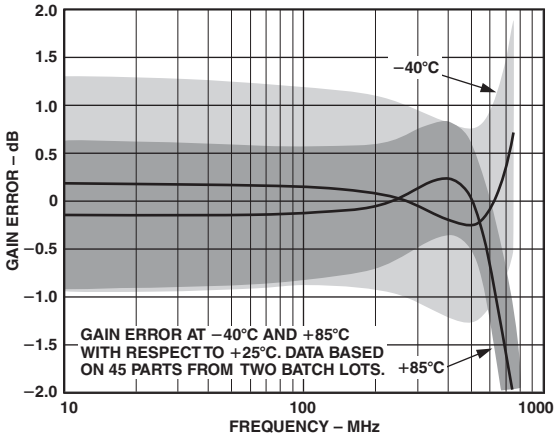
TPC 26. Gain Error Due to Temperature Change vs. Frequency, 3 Sigma to Either Side of Mean, V_S = 3 V, R_L = 1 kΩ, Maximum Gain



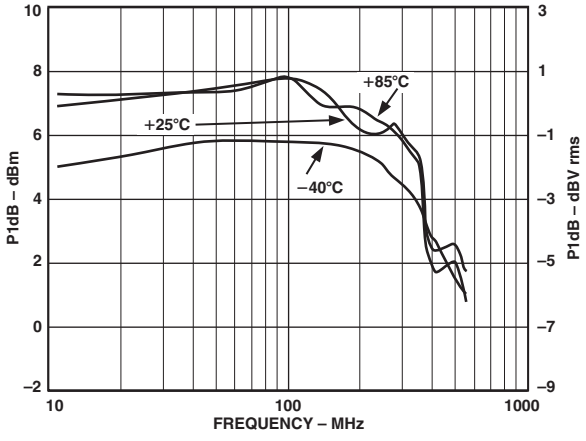
TPC 27. IP3 vs. Frequency by Temperature, V_S = 5 V, R_L = 200 Ω, Maximum Gain



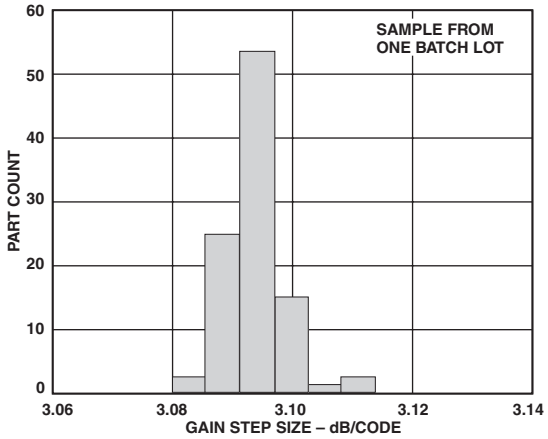
TPC 28. Gain Error Due to Temperature Change vs. Frequency, 3 Sigma to Either Side of Mean, V_S = 5 V, R_L = 200 Ω, Maximum Gain



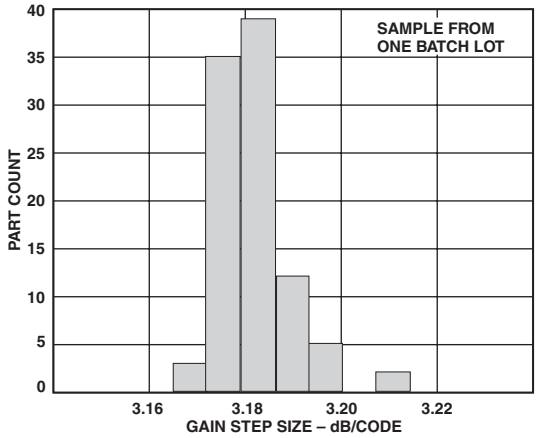
TPC 29. Gain Error Due to Temperature Change vs. Frequency, 3 Sigma to Either Side of Mean, V_S = 3 V, R_L = 200 Ω, Maximum Gain



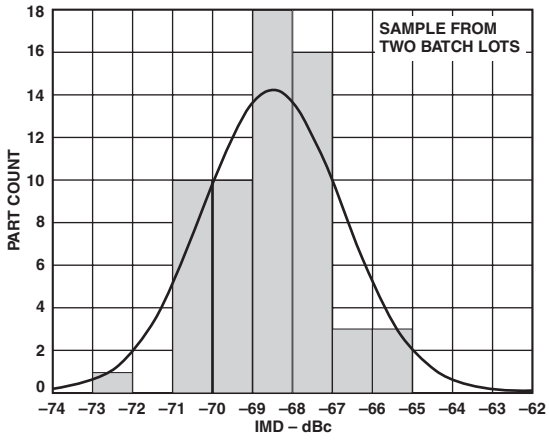
TPC 30. Output P1dB vs. Frequency by Temperature, V_S = 5 V, R_L = 200 Ω, Maximum Gain



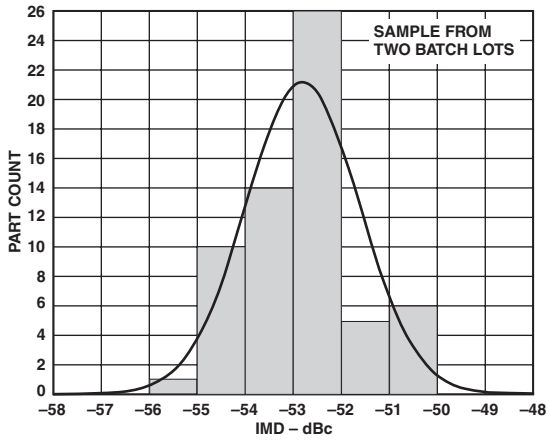
TPC 31. Distribution of Gain Step Size, 70 MHz, V_S = 5 V



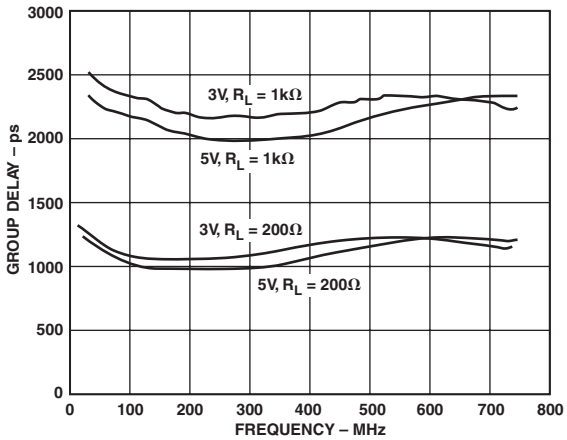
TPC 34. Distribution of Gain Step Size, 320 MHz, V_S = 5 V



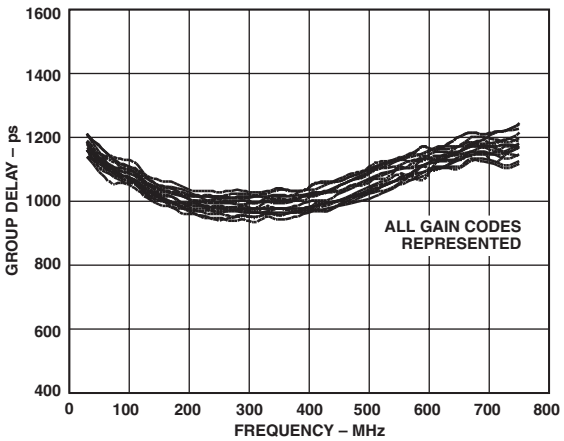
TPC 32. Distribution of IMD_3, 70 MHz, R_L = 1 kΩ, V_{OPHI} – V_{OPLO} = 1 V p-p Composite, V_S = 5 V, Maximum Gain



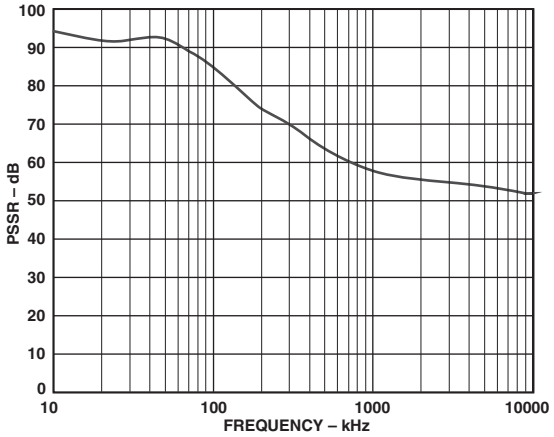
TPC 35. Distribution of IMD_3, 320 MHz, R_L = 1 kΩ, V_{OPHI} – V_{OPLO} = 1 V p-p Composite, V_S = 5 V, Maximum Gain



TPC 33. Group Delay vs. Frequency by R_L and Supply Voltage at Maximum Gain



TPC 36. Group Delay vs. Frequency by Gain Code, V_S = 5 V, R_L = 1 kΩ, Maximum Gain



TPC 37. Power Supply Rejection Ratio, V_S = 5 V, R_L = 1 kΩ, Maximum Gain

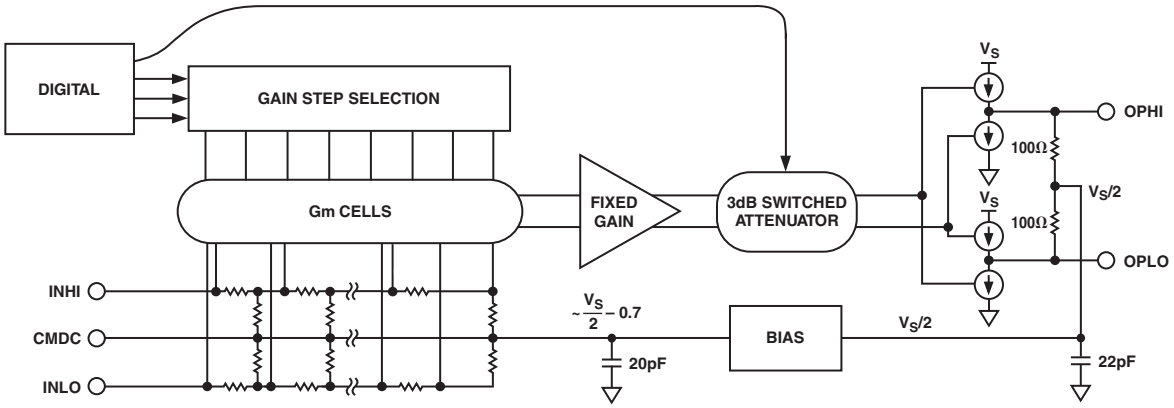


Figure 1. General Block Diagram, Control and Signal Paths Are Differential

THEORY OF OPERATION

The AD8369 is a digitally controlled fully differential VGA based on a variation of Analog Devices' patented X-AMP architecture (Figure 1). It provides accurate gain control over a 45 dB span with a constant –3 dB bandwidth of 600 MHz.

The 3 dB gain steps can be controlled by a user-selectable parallel- or serial-mode digital interface. A single pin (SENB) selects the mode. The AD8369 is designed for optimal operation when used in a fully differential system, although single-ended operation is also possible. Its nominal input and output impedances are 200 Ω.

Input Attenuator and Output 3 dB Step

The AD8369 is comprised of a seven-stage R-2R ladder network (eight taps) and a selected Gm stage followed by a fixed-gain differential amplifier. The ladder provides a total attenuation of 42 dB in 6 dB steps. The full signal is applied to the amplifier using the first tap; at the second tap, the signal is 6 dB lower and so on. A further 3 dB interpolating gain step is introduced at the output of the fixed gain amplifier, providing the full 45 dB of gain span.

Fixed Gain Amplifier

The fixed gain amplifier is driven by the tap point of the R-2R ladder network via the selected Gm cell. The output stage is a complementary pair of current sources, loaded with internal 100 Ω resistors to ac ground which provides a 200 Ω differential output impedance. The low frequency gain of the AD8369 can be approximated by the equation:

$$\frac{V_{OUT}}{V_{IN}} = 0.6\left(\frac{200R_L}{200+R_L}\right)\left(\frac{1}{\sqrt{2^{(15-n)}}}\right)$$

where R_L is the external load resistor in ohms and n is the gain code; 0 is the minimum gain code and 15 is the maximum gain code. The external load, which is in parallel combination with the internal 200 Ω output resistor, affects the overall gain and peak output swing. *Note that the external load has no effect on the gain step size.*

Input and Output Interfaces

The dc working points of the differential input and output interfaces of the AD8369 are internally biased. The inputs INHI and INLO are biased to a diode drop below $V_S/2$ (~1.7 V for a 5 V positive supply) to meet isolation and headroom constraints, while the outputs OPHI and OPLO are centered on the supply midpoint, $V_S/2$, to provide the maximum output swing.

The internal $V_S/2$ reference and the CMDC reference are buffered and decoupled to ground via internal capacitors. The input bias voltage, derived from this $V_S/2$ reference, is brought

out to pin CMDC for decoupling to ground. An external capacitor from CMDC to COMM of 0.01 µF or more is recommended to lower the input common-mode impedance of the AD8369 and improve single-ended operation.

Signals must be ac-coupled at the input, either via a pair of capacitors or a transformer. These may not be needed when the source has no dc path to ground, such as a SAW filter. The output may need dc blocking capacitors when driving dc-grounded loads, but it can be directly coupled to an ADC, provided that the common-mode levels are compatible.

The input and output resistances form a high-pass filter in combination with any external ac-coupling capacitors that should be chosen to minimize signal roll-off at low frequencies. For example, using input-coupling capacitors of 0.1 µF, each driving a 100 Ω input node (200 Ω differential), the –3 dB high-pass corner frequency is at:

$$\frac{1}{2\pi(10^{-7})(100)} = 16\,\text{kHz}$$

It is important to note that the input and output resistances are subject to process variations of up to ±20%. This will affect the high-pass corner frequencies and the overall gain when driven from, or loaded by, a finite impedance (see the Reducing Gain Sensitivity to Input and Output Impedance Variation section).

Noise and Distortion

It is a common aspect of this style of VGAs, however implemented, that the effective noise figure worsens as the gain is reduced. The AD8369 uses a fixed gain amplifier, having a certain invariant noise spectral density, preceded by an attenuator. Thus, the noise figure increases simply by 6 dB per tap point, from a starting point of 7 dB at full gain.

However, unlike voltage-controlled amplifiers that must necessarily invoke nonlinear elements in the signal path, the distortion in a step-gain amplifier can be very low and is essentially independent of the gain setting. Note that the postamplifier 3 dB step does not affect the noise performance, but it has some bearing on the output third-order intercept (OIP3). See TPCs 3 and 9.

Offset Control Loop

The AD8369 uses a control loop to null offsets at the input. If left uncorrected, these offsets, in conjunction with the gain of the AD8369, would reduce the available voltage swing at the output. The control loop samples the differential output voltage error and feeds nulling currents back into the input stage. The nominal high-pass corner frequency of this loop is internally set to 520 kHz, but it is subject to process variations of up to ±20%. This corner frequency can be reduced by adding an external capacitor from the FILT pin to ground, in parallel to an internal 30 pF capacitor. For example, an external capacitor of 0.1 µF would lower the high-pass corner by a factor of 30/100,030, to approximately 156 Hz. This frequency should be chosen to be at least one decade below the lowest component of interest in the input spectrum.

Digital Control

The gain of the AD8369 is controlled via a serial or parallel interface, as shown in Figure 2. Serial or parallel operation is selected via the SENB pin. Setting SENB to a logic low (< $V_S/2$) selects parallel operation, while a logic high on SENB (> $V_S/2$) selects serial operation. The AD8369 has two control registers, the gain control register and the shift register. The gain control register is a latch that holds the data that sets the amplifier gain. The shift registers are composed of four flip-flops that accept the serial data stream.

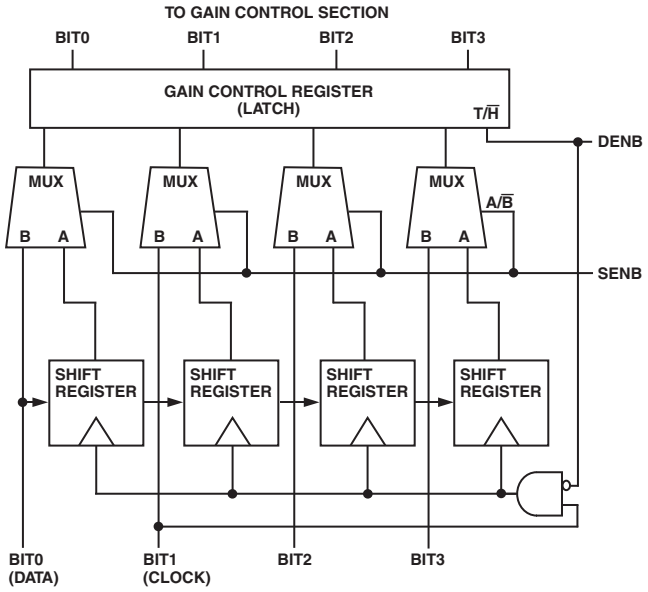


Figure 2. Digital Interface Block Diagram

In parallel operation, the 4-bit parallel data is placed on pins BIT3 through BIT0 and passed along to the gain control register via the mux. Data is latched into the gain control register on the falling edge of the input to DENB, subject to meeting the specified setup and hold times. If this pin is held high (> $V_S/2$), any changes in the parallel data will result in a change in the gain, after propagation delays. This is referred to as the transparent mode of operation. If DENB is held low, the last 4-bit word in the gain control register will remain latched regardless of the signals at the data inputs.

In serial operation, the BIT0 pin is used for data input while the BIT1 pin is the clock input. Data is loaded into the serial shift registers on the rising edge of the clock when DENB is low. Given the required setup and hold times are observed, four rising edge transitions of the clock will fully load the shift register. On the rising edge of DENB, the 4-bit word in the shift register is passed into the gain control register. While this pin is held high, the clock input to the shift registers is turned off. Once DENB is taken low, the shift register clock is again enabled and the last 4-bit word prior to enabling the clock will be latched into the gain control registers. This enables the loading of a new 4-bit gain control word without interruption of the signal path. Only when DENB goes high is data transferred from the shift registers to the gain control registers. If no connections are made to the digital control pins, internal 40 kΩ resistors pull these pins to levels that set the AD8369 to its minimum gain condition.

At power-up or chip enable, if the AD8369 is in parallel mode and DENB is held low, the gain control register will come up in an indeterminate state. To avoid this, DENB should be held high with valid data present during power-up when operating in the parallel mode. In serial mode, the data in the gain control interface powers up with a random gain code independent of the DENB pin. Serial mode operation requires at least four clock cycles and the transition of DENB from low to high for valid data to be present at the gain control register.

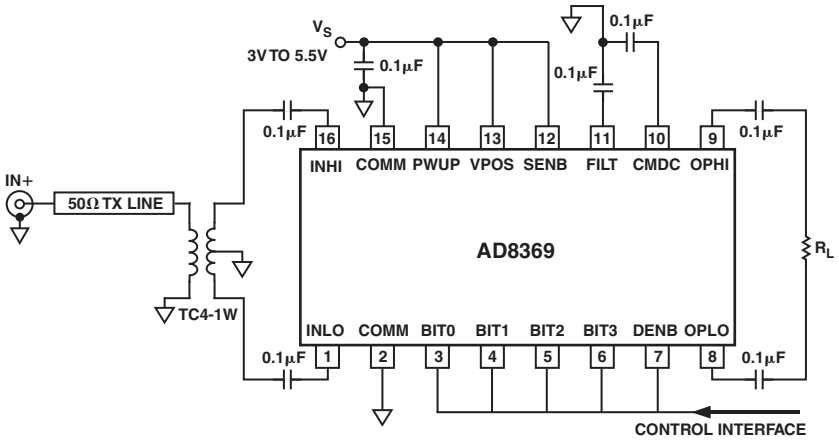


Figure 3. Basic Connections

BASIC CONNECTIONS

Figure 3 shows the minimum connections required for basic operation of the AD8369. Supply voltages of between +3 V and +5.5 V are permissible. The supply to the VPOS pin should be decoupled with at least one low inductance surface-mount ceramic capacitor of 0.1 µF placed as close as possible to the device. More effective decoupling is provided by placing a 100 pF capacitor in parallel and including a 4.7 Ω resistor in series with the supply. Attention should be paid to voltage drops. A ferrite bead is a better choice than the resistor where a smaller drop is required.

Input-Output Interface

A broadband 50 Ω input termination can be achieved by using a 1:2 turns-ratio transformer, as shown in Figure 3. This also can be used to convert a single-ended input signal to a balanced differential form at the inputs of the AD8369.

As in all high frequency applications, the trace impedance should be maintained right up to the input pins by careful design of the PC board traces, as described in the PCB Layout Considerations section.

Reducing Gain Sensitivity to Input and Output Impedance Variation

The lot-to-lot variations in gain mentioned previously can, in principle, be eliminated by adjustments to the source and load.

Define a term α as a function of the input and output resistances of the AD8369 and the source and load resistances presented to it:

$$R_{SOURCE} = \alpha\left(R_{INPUT}\right)$$
$$R_{OUTPUT} = \alpha\left(R_{LOAD}\right)$$

For a 50 Ω source, α = 0.25. Then the load resistance for zero sensitivity to variations must be 800 Ω. Put more simply:

$$\left(R_{SOURCE}\right)\left(R_{LOAD}\right) = \left(R_{INPUT}\right)\left(R_{OUTPUT}\right) = 200^2$$

In general, there is a loss factor, 1/(1+ α), at each interface so the overall gain reduction due to source and output loading is $40 \log_{10} (1 + \alpha)$. In this case, the input and output loss factors are 0.8 (1.94 dB) at each interface so the overall gain is reduced by 3.88 dB.

Operation from a Single-Sided Source

While there are distinct benefits of driving the AD8369 with a well-balanced input, in terms of distortion and gain conformance at high frequencies, satisfactory operation will often be possible when a single-sided source is ac-coupled directly to pin INHI, and pin INLO is ac-grounded via a second capacitor. This mode of operation takes advantage of the good HF common-mode rejection of the input system. The capacitor values are, as always, selected to ensure adequate transmission at low frequencies.

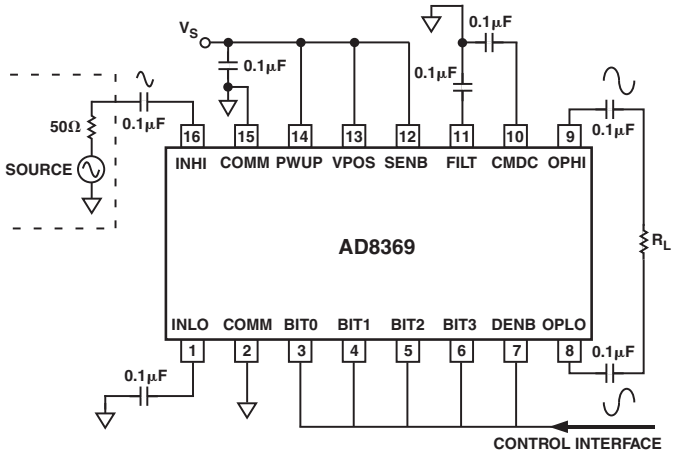


Figure 4. Single-Ended-to-Differential Application Example

For example, suppose the input signal in Figure 4 is a 140 MHz sinusoid from a ground-referenced 50 Ω source. The 0.1 µF coupling capacitors present a very low reactance at this frequency (11 mΩ) so that essentially all of the ac voltage is delivered to the differential inputs of the AD8369. It will be apparent that, in addition to the use of adequate coupling capacitance, the external capacitor used to extend the low frequency range of the offset control loop, C_{FILT}, must also be large enough to prevent the offset control loop from attempting to track the ac signal fluctuations.

Interfacing to an ADC

The AD8369 can be used to effectively increase the dynamic range of an ADC in a direct IF sampling receiver application. Figure 5 provides an example of an interface to an ADC designed for an IF of 70 MHz. It comprises a low-pass filter that attenuates harmonics while providing an impedance transformation from 200 Ω to 1 kΩ. This impedance transformation allows the AD8369 to operate much below its peak output swing in the pass band, which significantly reduces distortion.

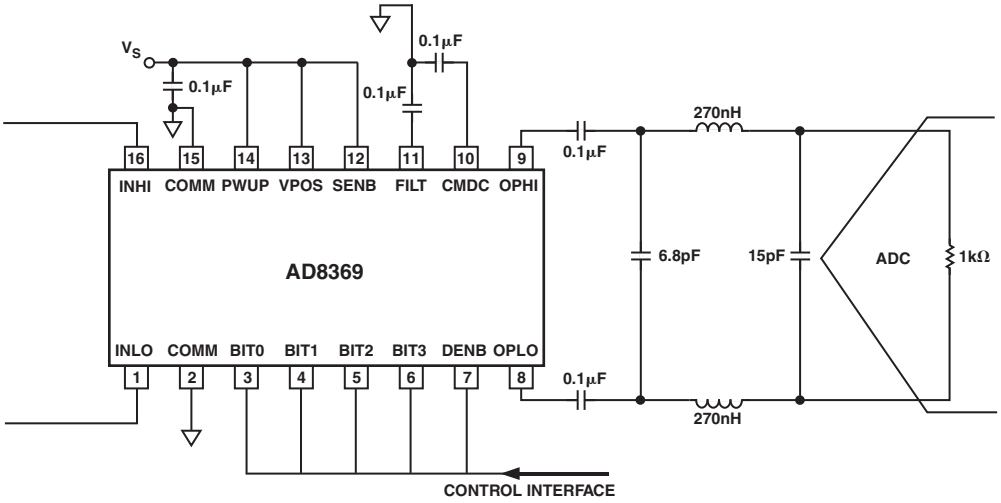


Figure 5. AD8369 to ADC Interface

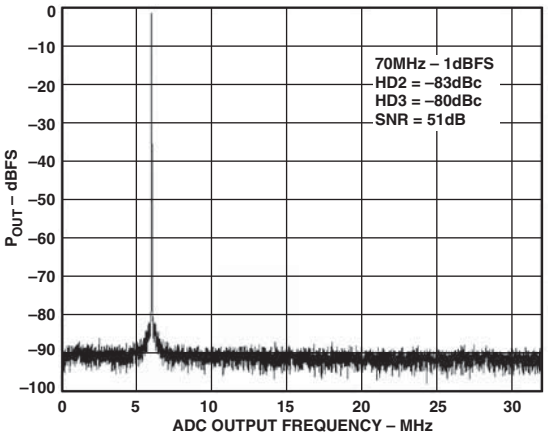


Figure 6. Single-Tone 70 MHz, –1 dBFS

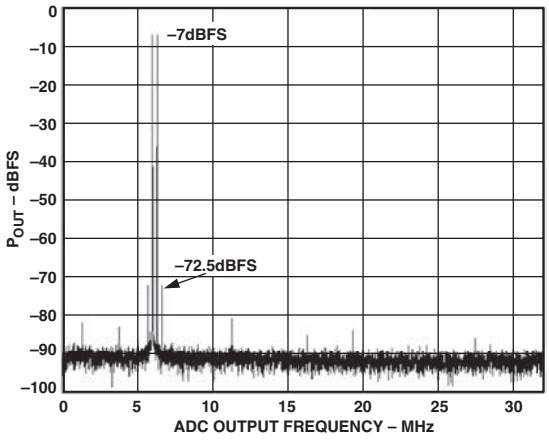


Figure 7. Two-Tone, 70 MHz, 70.3 MHz, –7 dBFS

A high performance 14-bit ADC, the AD6645, is used for illustrative purposes and is sampling at 64 MSPs with a full-scale input of 2.2 V p-p. Typically, an SNR of 51 dB and an SFDR of almost –90 dBFS are realized by this configuration. Figure 6 shows an FFT of the AD8369 delivering a single tone at –1 dBFS (that is, 2 V p-p) at the input of the ADC with an HD2 of –83 dBc and HD3 of –80 dBc. Figure 7 shows that the two-tone, third-order intermodulation distortion level is –65.5 dBc.

PCB Layout Considerations

Each input and output pin of the AD8369 presents 100 Ω relative to their respective ac grounds. To ensure that signal integrity is not seriously impaired by the printed circuit board, the relevant connection traces should provide a characteristic impedance of 100 Ω to the ground plane. This can be achieved through proper layout. Figure 8 shows the cross section of a PC board and Table II shows the dimensions that will provide a 100 Ω line impedance.

Table II. Dimensions Required for 100 Ω Characteristic Impedance Microstrip Line in FR-4

ϵ_r (FR-4)	4.6
W	22 mils
H	53 mils
T	2.1 mils

Key considerations when laying out an RF trace with a controlled impedance include:

- Space the ground plane to either side of the signal trace at least 3 line-widths away to ensure that a microstrip (vertical dielectric) line is formed, rather than a coplanar (lateral dielectric) waveguide.
- Ensure that the width of the microstrip line is constant and that there are as few discontinuations (component pads, etc.) as possible along the length of the line. Width variations cause impedance discontinuities in the line and may result in unwanted reflections.
- Do not use silkscreen over the signal line; this will alter the line impedance.
- Keep the length of the input and output connection lines as short as possible.

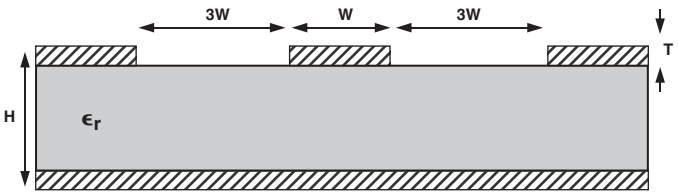


Figure 8. Cross-Sectional View of a PC Board

The AD8369 contains both digital and analog sections. Care should be taken to ensure that the digital and analog sections are adequately isolated on the PC board. The use of separate ground planes for each section connected at only one point via a ferrite bead inductor will ensure that the digital pulses do not adversely affect the analog section of the AD8369.

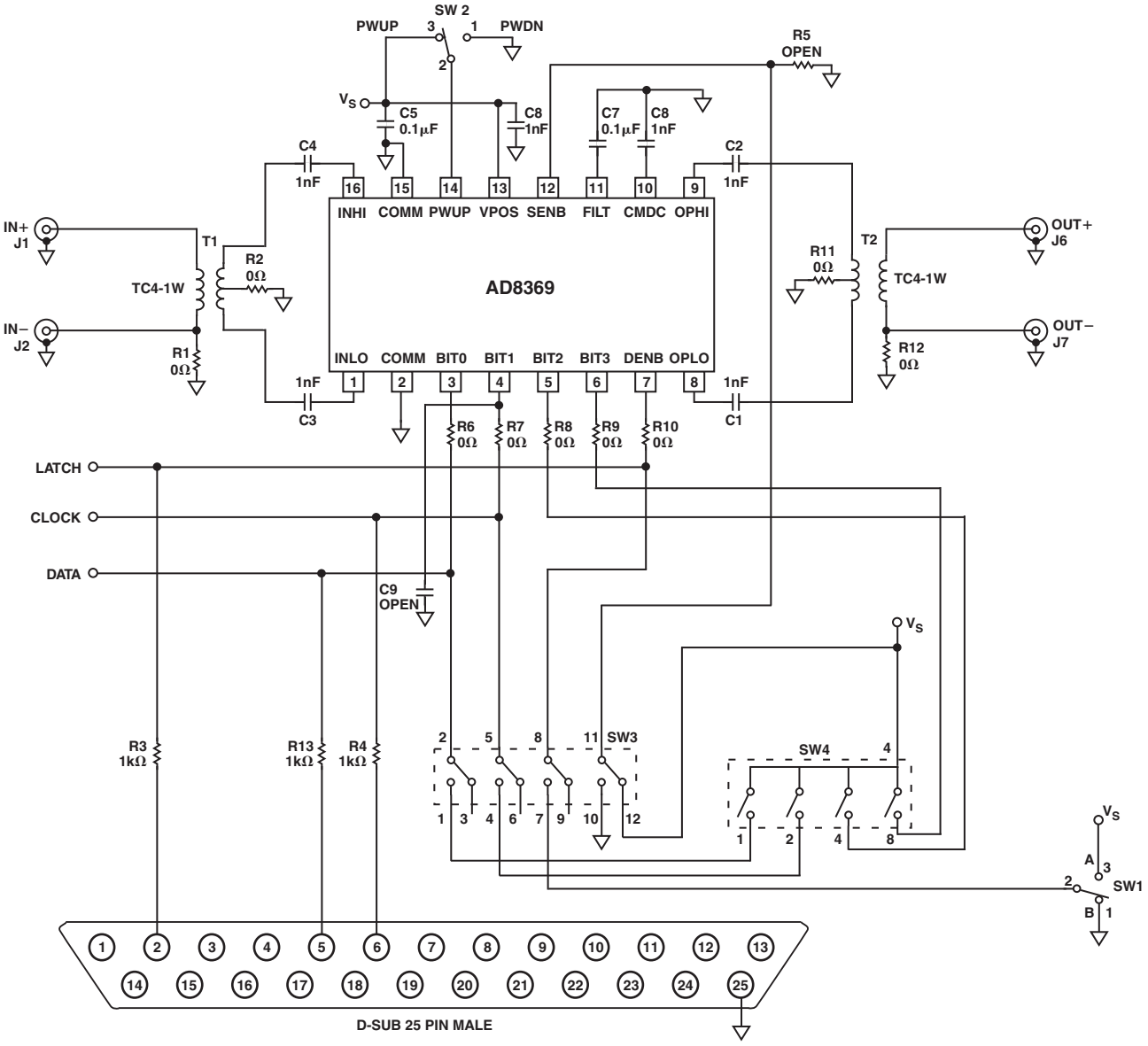


Figure 9. Evaluation Board Schematic

Evaluation Board

The evaluation board allows for quick testing of the AD8369 using standard 50 Ω test equipment. The schematic is shown in Figure 9. Transformers T1 and T2 are used to transform 50 Ω source and load impedances to the desired 200 Ω reference level. This allows for broadband operation of the device without the need to pay close attention to impedance matching (see Table III).

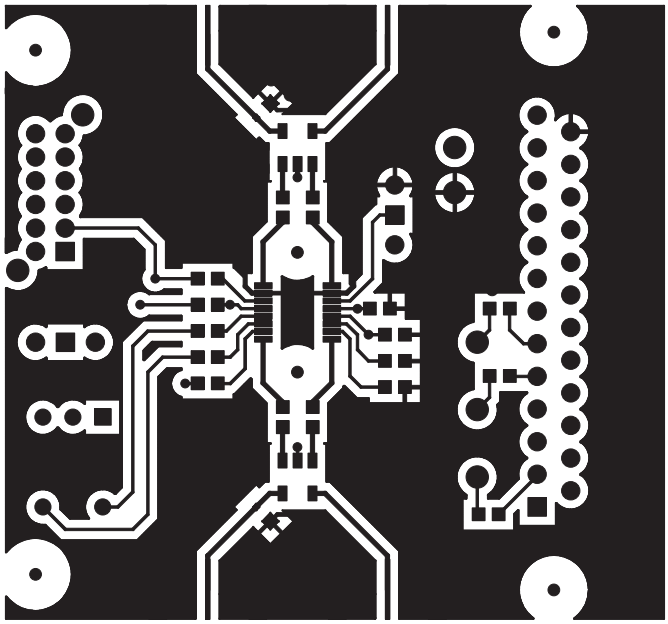


Figure 10. Evaluation Board Layout

Evaluation Board Software

The evaluation board comes with the AD8369 control software that allows for serial gain control from most computers. The evaluation board is connected via a cable to the parallel port of the computer. By simply adjusting the slider bar in the control software, the gain code is automatically updated to the AD8369. On some older PCs, it may be necessary to use 5 kΩ pull-up resistors to VPOS on DATA, CLOCK, and LATCH depending upon the capabilities of the port transceiver.

It is necessary to set SW3 on the evaluation board to "SER" for the control software to function normally.

A screen shot of the evaluation software interface is shown in Figure 11.

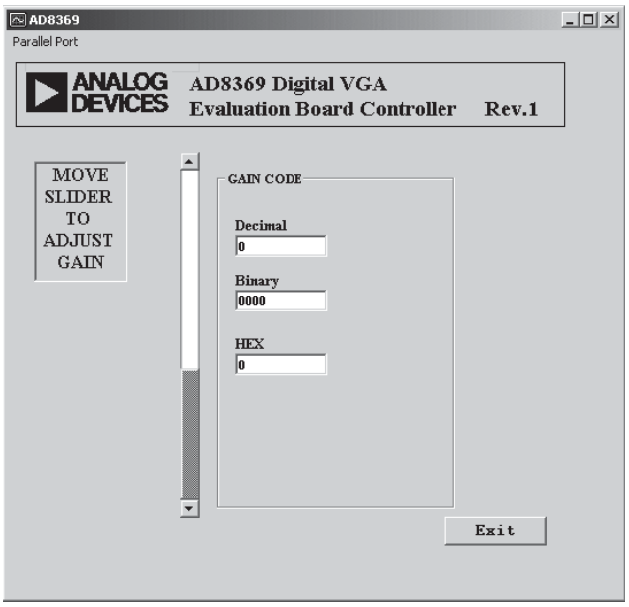


Figure 11. Evaluation Software Interface

Table III. AD8369 Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Supply and Ground Vector Pins	Not Applicable
SW1	Data Enable: Set to Position A when in serial mode of operation, set to Position B when in parallel mode of operation.	Not Applicable
SW2	Device Enable: When in the PWDN position, the PWUP pin will be connected to ground and the AD8369 will be disabled. The device is enabled when the switch is in the PWUP position, connecting the PWUP pin to VPOS.	Not Applicable
SW3, R5	Serial/Parallel Selection. The device will respond to serial control inputs from connector P1 when the switch is in the SER position. Parallel operation is achieved when in the PAR position. Device can be hardwired for parallel mode of operation by placing the 0 Ω resistor in position R5.	Not Applicable R5 = Open (Size 0603)
SW4	Parallel Interface Control. Used to hardwire BIT0 through BIT3 to the desired gain code when in parallel mode of operation. The switch functions as a hexadecimal to binary encoder (Gain Code 0 = 0000, Gain Code 15 = 1111).	Not Applicable
J1, J2, J6, J7	Input and Output Signal Connectors. These SMA connectors provide a convenient way to interface the evaluation board with 50 Ω test equipment.	Not Applicable
C1, C2, C3, C4	AC-Coupling Capacitors. Provides ac-coupling of the input and output signals.	C1, C2, C3, C4 = 1 nF (Size 0603)
T1, T2	Impedance Transformers. Used to transform the 200 Ω input and output impedance to 50 Ω.	T1, T2 = TC4-1W (MiniCircuits)
R1, R2, R11, R12	Single-Ended or Differential. R2 and R11 are used to ground the center tap of the secondary windings on transformers T1 and T2. R1 and R12 should be used to ground J2 and J7 when used in single-ended applications. R1 and R12 should be removed for differential operation.	R1, R2, R11, R12 = 0 Ω (Size 0603)
R6, R7, R8, R9, R10	Control Interface Resistors. Simple series resistors for each control interface signal.	R6, R7, R8, R9, R10 = 0 Ω (Size 0603)
C5, C6, C8	Power Supply Decoupling. Nominal supply decoupling consists of a 0.1 µF capacitor to ground followed by a 1 nF capacitor to ground positioned as close to the device as possible. C8 provides additional decoupling of the input common-mode voltage.	C5 = 0.1 µF (Size 0603) C6 = C8 = 1 nF (Size 0603)
C7	High-Pass Filter Capacitor. Used to set high-pass corner frequency of output.	C7 = 0.1 µF (Size 0603)
C9	Clock Filter Capacitor. May be required with some printer ports to minimize overshoot. The clock waveform may be smoothed using a simple filter network established by R7 and C9. Some experimentation may be necessary to determine optimum values.	C9 = Open (Size 0603)

APPENDIX

Characterization Equipment

Two sets of automated characterization equipment were used to obtain the majority of the information contained in this data sheet.

An Agilent N4441A Balanced Measurement System was used to obtain the gain, phase, group delay, reverse isolation, CMRR, and s-parameter information. Except for the s-parameter information, T-attenuator pads were used to match the 50 Ω impedance of the ports of this instrument to the AD8369.

An Anritsu MS4623B "Scorpion" Vector Network Analyzer was used to obtain nonlinear measurements IMD_3, IP3, and P1dB through matching baluns and attenuator networks.

Definitions of Selected Parameters

Common-mode rejection ratio (TPC 14) has been defined for this characterization effort as:

$$\frac{Differential\text{-}Mode, forward gain}{Common\text{-}Mode, forward gain}$$

where the numerator is the gain into a differential load at the output due to a differential source at the input and the denominator is the gain into a common-mode load at the output due to a common-mode source at the input. In terms of mixed-mode s-parameters, this equates to:

$$\frac{SDD21}{SCC21}$$

Reverse isolation (TPC 17) is defined as SDD12.

More information on mixed-mode s-parameters can be obtained in the a reference by Bockelman, D.E. and Eisenstadt, W.R., *Combined Differential and Common-Mode Scattering Parameters: Theory and Simulation.* IEEE Transactions on Microwave Theory and Techniques, v 43, n 7, 1530 (July 1995).

Composite Waveform Assumption

The nonlinear two-tone measurements made for this data sheet, i.e., IMD_3 and IP3, are based on the assumption of a fixed value composite waveform at the output, generally 1 V p-p. The frequencies of interest dictate the use of RF test equipment and because this equipment is generally not designed to work in units of volts, but rather watts and dBm, an assumption was made to simplify equipment setup and operation.

Two sinusoidal tones can be represented as:

$$V_1 = \sin\left(2\pi f_1 t\right)$$

$$V_2 = \sin\left(2\pi f_2 t\right)$$

The average voltage of one tone is:

$$\sqrt{\frac{1}{T}\int_0^T \left(V_1\right)^2 dt} = \frac{1}{\sqrt{2}}$$

where T is the period of the waveform. The average voltage of the two-tone composite signal is:

$$\sqrt{\frac{1}{T}\int_0^T \left(V_1 + V_2\right)^2 dt} = 1$$

So each tone contributes $1/\sqrt{2}$ to the average composite amplitude in terms of voltage. It can be shown that *the average power of this composite waveform is two times greater, or 3dB, than that of the single tone.* This principle can be used to set correct input amplitudes from generators scaled in dBm and is correct if the two tones are of equal amplitude and are not farther than 1 percent apart in frequency.

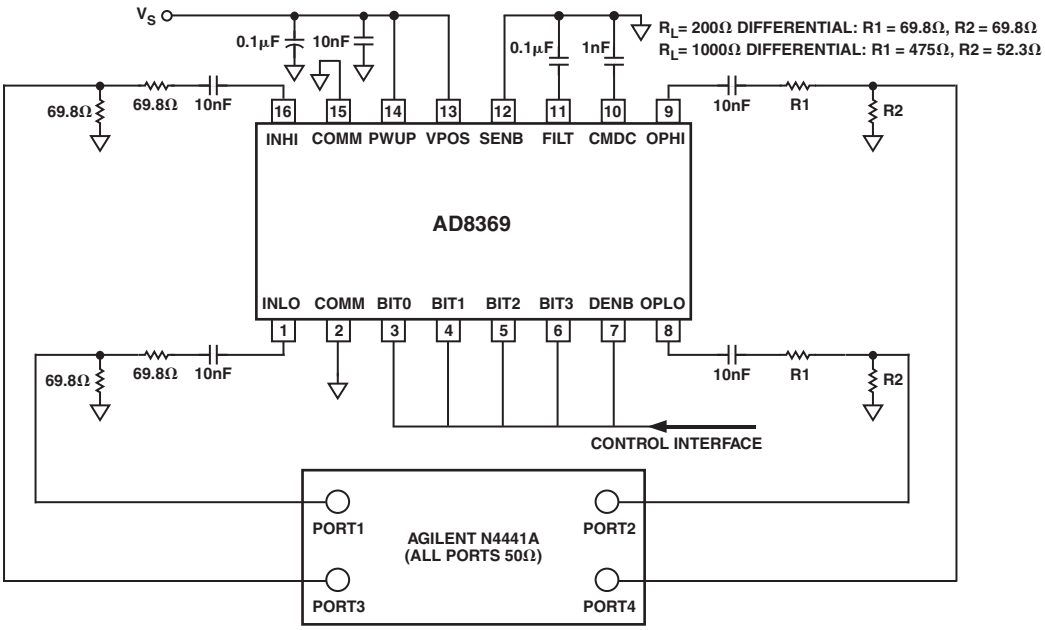


Figure 12. Balanced Measurement System Setup

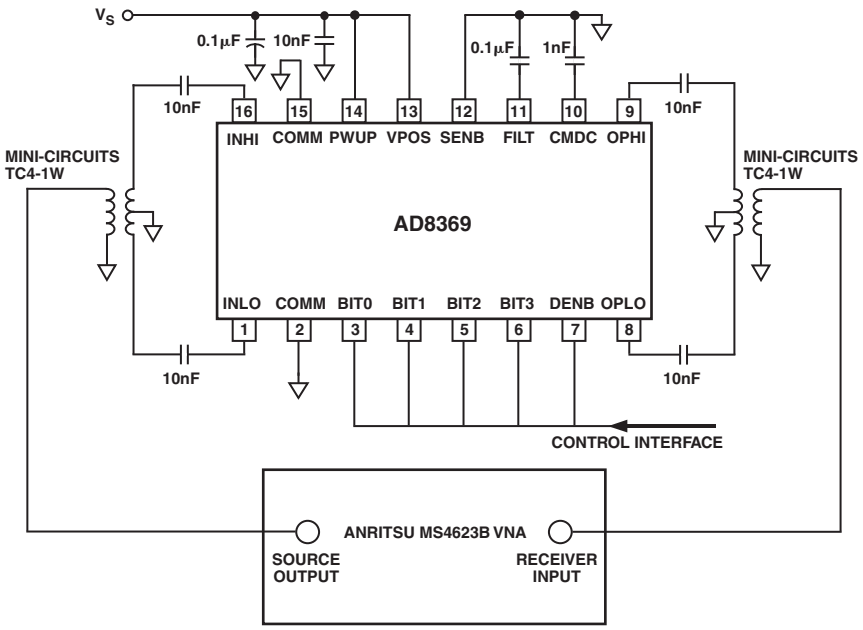


Figure 13. Vector Network Analyzer Setup (200 Ω)

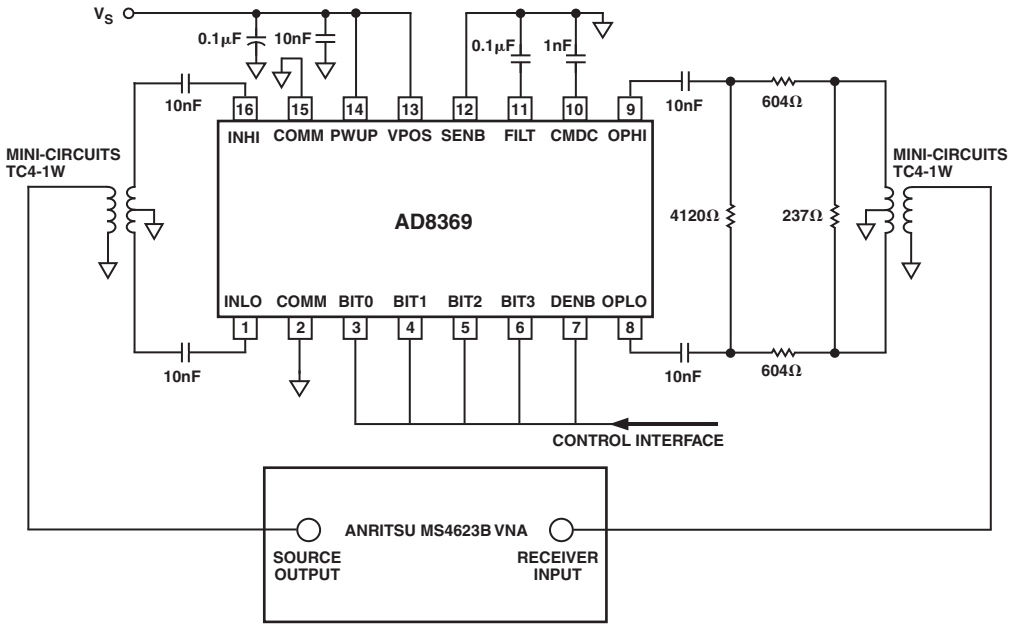


Figure 14. Vector Network Analyzer Setup (1 kΩ)

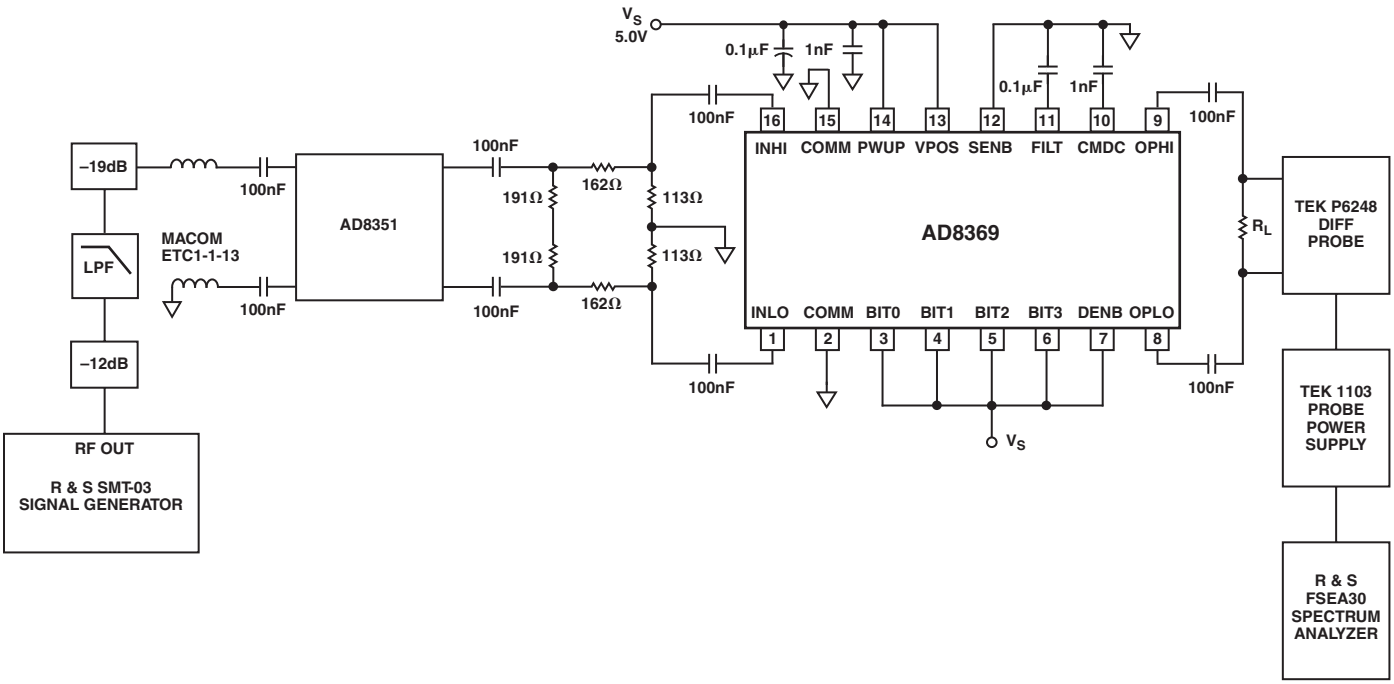


Figure 15. Harmonic Distortion Setup

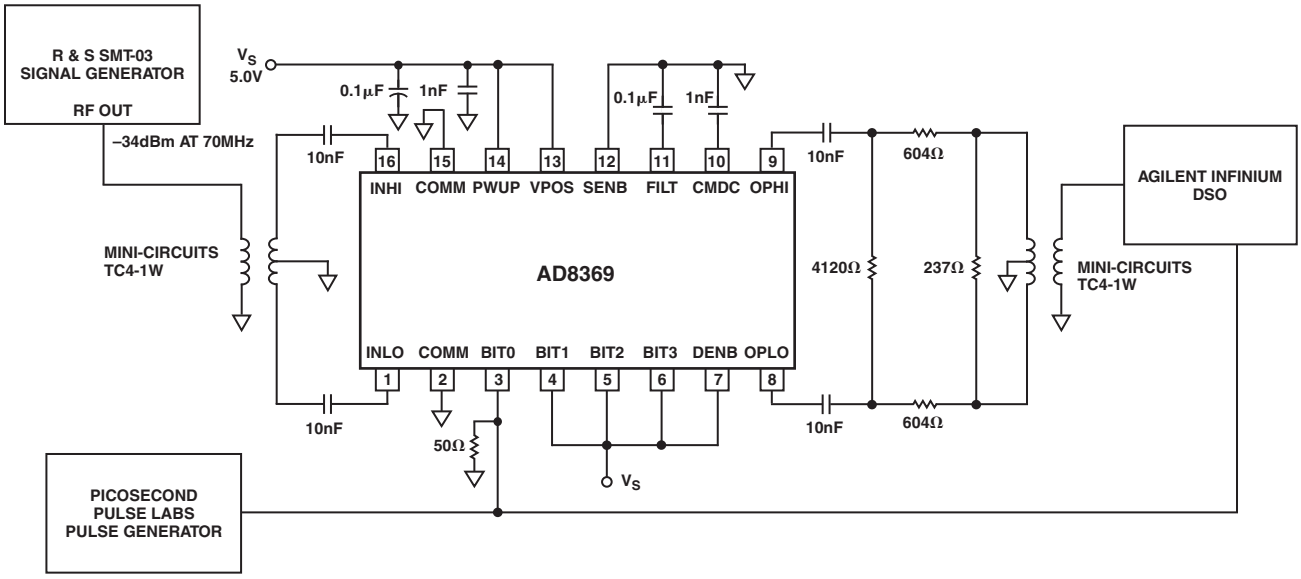


Figure 16. Gain Step Response Setup

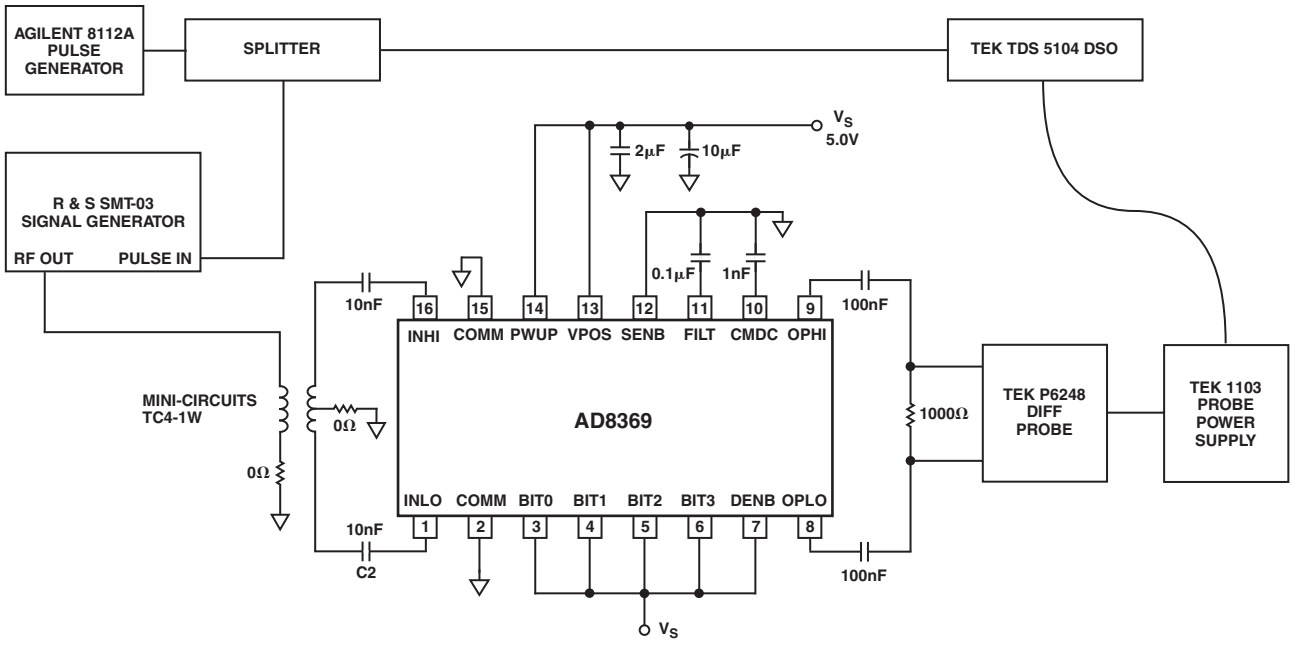


Figure 17. Pulse Response Setup

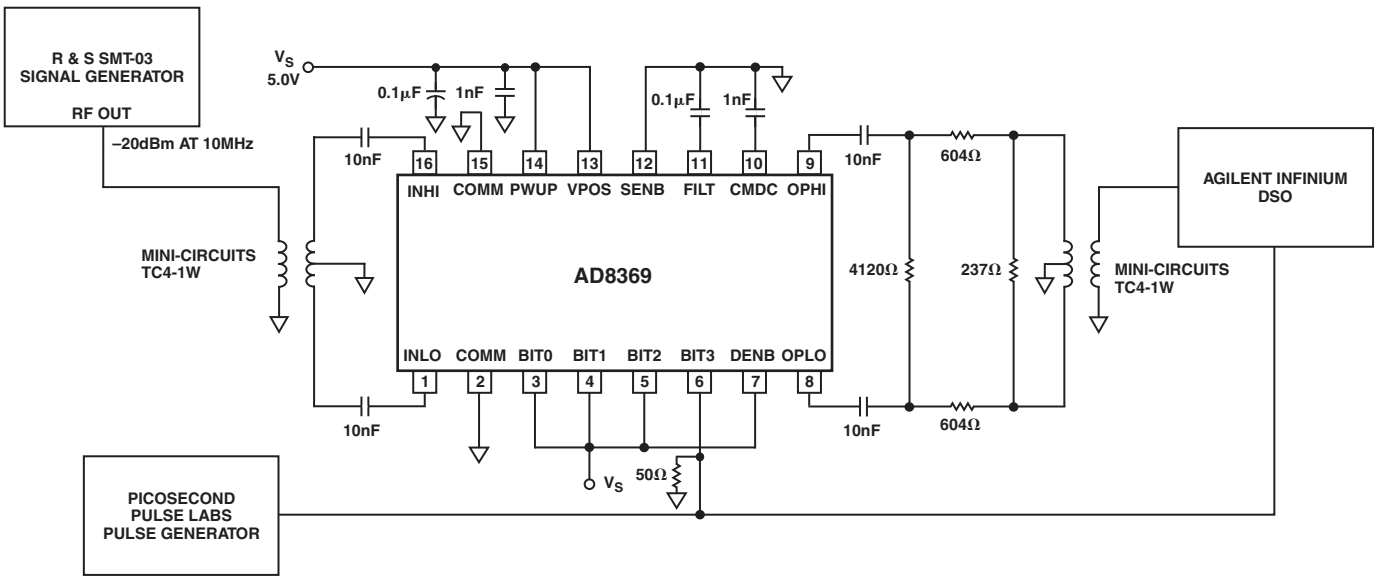
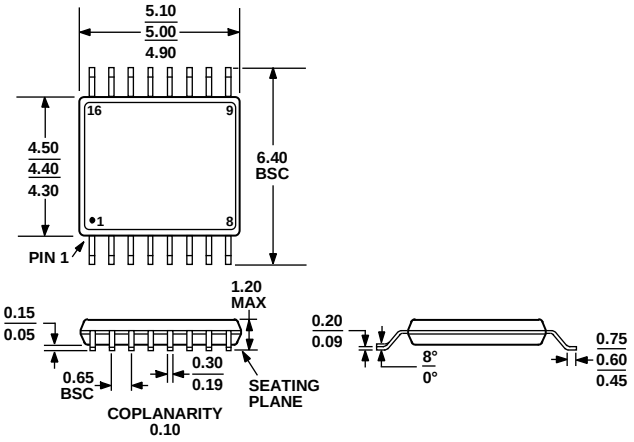


Figure 18. Overdrive Response Setup

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 19. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8369ARUZ	–40°C to +85°C	Tube, 16-Lead TSSOP	RU-16
AD8369ARUZ-REEL7	–40°C to +85°C	16-Lead TSSOP 7" Tape and Reel	
AD8369-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

REVISION HISTORY

9/15—Rev. 0 to Rev. A

Changed θ_{JA} from 150°C/W to 121.48°C/W.....5
Changes to Ordering Guide.....24

D03029-0-9/15(A)