TABLE OF CONTENTS

REVISION HISTORY

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, system impedance Z_O = 200 Ω, V_{MODE} = 5 V, f = 10 MHz, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		LF		500	MHz
GAIN Range			45		dB
INPUT STAGE	Pins INPT and ICOM				
Maximum Input	To avoid input overload		700		mV p-p
Input Resistance	From INPT to ICOM	175	200	225	Ω
GAIN CONTROL INTERFACE	Pin GAIN				
Scaling Factor	V_{MODE} = 5 V, 50 mV ≤ V_{GAIN} ≤ 950 mV		+20		mV/dB
	V_{MODE} = 0 V, 50 mV ≤ V_{GAIN} ≤ 950 mV		−20		mV/dB
Gain Law Conformance	100 mV ≤ V_{GAIN} ≤ 900 mV		±0.2		dB
Maximum Gain	V_{GAIN} = 0.95 V		+42.5		dB
Minimum Gain	V_{GAIN} = 0.05 V		−2.5		dB
V_{GAIN} Step Response	From 0 dB to 30 dB		300		ns
	From 30 dB to 0 dB		300		ns
Small Signal Bandwidth	V_{GAIN} = 0.5 V		5		MHz
OUTPUT STAGE	Pin VOUT				
Maximum Output Voltage Swing	R_L = 1 kΩ		4.3		V p-p
	R_L = 200 Ω		3.5		V p-p
Output Source Resistance	Series resistance of output buffer		50		Ω
Output Centering Voltage[1]			V_S/2		V
SQUARE LAW DETECTOR	Pin DETO				
Output Set Point			354		mV rms
AGC Small Signal Response Time	C_{AGC} = 100 pF, 6 dB gain step		1		µs
POWER INTERFACE	Pins VPSI, VPSO, ICOM, and OCOM				
Supply Voltage		2.7		5.5	V
Total Supply Current	ENBL high, maximum gain, R_L = 200 Ω (includes load current)		26	30	mA
Disable Current vs. Temperature	ENBL low		1.3	1.6	mA
	−40°C ≤ TA ≤ +85°C			1.8	mA
MODE CONTROL INTERFACE	Pin MODE				
Mode LO Threshold	Device in negative slope mode of operation		1.2		V
Mode HI Threshold	Device in positive slope mode of operation		1.4		V
ENABLE INTERFACE	Pin ENBL				
Enable Threshold			2.5		V
Enable Response Time	Time delay following LO to HI transition until device meets full specifications.		1.5		µs
Enable Input Bias Current	ENBL at 5 V		27		µA
	ENBL at 0 V		32		nA
f = 70 MHz					
Gain	Maximum gain		+42.5		dB
	Minimum gain		−3.7		dB
Gain Scaling Factor			19.9		mV/dB
Gain Intercept			−5.6		dB
Noise Figure	Maximum gain		6.2		dB
Output IP3	f1 = 70 MHz, f2 = 71 MHz, V_{GAIN} = 0.5 V		36.5		dBm
			29.5		dBV rms
Output 1 dB Compression Point	V_{GAIN} = 0.5 V		8.5		dBm
			1.5		dBV rms

Parameter	Conditions	Min	Typ	Max	Unit
f = 140 MHz					
Gain	Maximum gain		+43.5		dB
	Minimum gain		−3.6		dB
Gain Scaling Factor			19.7		mV/dB
Gain Intercept			−5.3		dB
Noise Figure	Maximum gain		7.4		dB
Output IP3	f1 = 140 MHz, f2 = 141 MHz, V_{GAIN} = 0.5 V		32.7		dBm
			25.7		dBV rms
Output 1 dB Compression Point	V_{GAIN} = 0.5 V		8.4		dBm
			1.4		dBV rms
f = 190 MHz					
Gain	Maximum gain		+43.5		dB
	Minimum gain		−3.8		dB
Gain Scaling Factor			19.6		mV/dB
Gain Intercept			−5.3		dB
Noise Figure	Maximum gain		7.5		dB
Output IP3	f1 = 190 MHz, f2 = 191 MHz, V_{GAIN} = 0.5 V		30.9		dBm
			23.9		dBV rms
Output 1 dB Compression Point	V_{GAIN} = 0.5 V		8.4		dBm
			1.4		dBV rms
f = 240 MHz					
Gain	Maximum gain		+43		dB
	Minimum gain		−4.1		dB
Gain Scaling Factor			19.7		mV/dB
Gain Intercept			−5.2		dB
Noise Figure	Maximum gain		7.6		dB
Output IP3	f1 = 240 MHz, f2 = 241 MHz, V_{GAIN} = 0.5 V		29.2		dBm
			22.2		dBV rms
Output 1 dB Compression Point	V_{GAIN} = 0.5 V		8.1		dBm
			1.1		dBV rms

[1] The output dc centering voltage is normally set at $V_S/2$ and can be adjusted by applying a voltage to DECL.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPSO, VPSI	5.5 V
ENBL Voltage	V_S + 200 mV
MODE Select Voltage	V_S + 200 mV
V_{GAIN} Control Voltage	1.2 V
Input Voltage	±600 mV
Internal Power Dissipation	250 mW
θ_{JA}	150°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
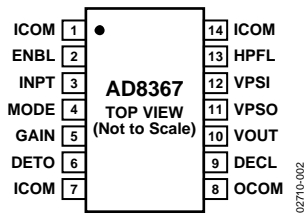
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

```
        ┌──────────────────┐
ICOM  1 │ ●                │ 14  ICOM
ENBL  2 │                  │ 13  HPFL
INPT  3 │   AD8367         │ 12  VPSI
MODE  4 │   TOP VIEW       │ 11  VPSO
GAIN  5 │   (Not to Scale) │ 10  VOUT
DETO  6 │                  │  9  DECL
ICOM  7 │                  │  8  OCOM
        └──────────────────┘
```

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7, 14	ICOM	Signal Common. Connect to low impedance ground.
2	ENBL	A HI Activates the Device.
3	INPT	Signal Input. 200 Ω to ground.
4	MODE	Gain Direction Control. HI for positive slope; LO for negative slope.
5	GAIN	Gain Control Voltage Input.
6	DETO	Detector Output. Provides output current for RSSI function and AGC control.
8	OCOM	Power Common. Connect to low impedance ground.
9	DECL	Output Centering Loop Decoupling Pin.
10	VOUT	Signal Output. To be externally ac-coupled to load.
11	VPSO	Positive Supply Voltage. 2.7 V to 5.5 V. VPSI and VPSO are tied together internally with back-to-back PN junctions. They should be tied together externally and properly bypassed.
12	VPSI	Positive Supply Voltage. 2.7 V to 5.5 V.
13	HPFL	High-Pass Filter Connection. A capacitor to ground sets the corner frequency of the output offset control loop.

TYPICAL PERFORMANCE CHARACTERISTICS

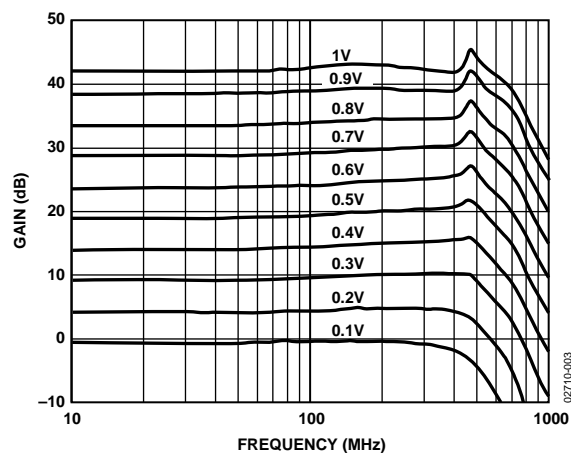V_S = 5 V, T_A = 25°C, system impedance Z_O = 200 Ω, V_{MODE} = 5 V, unless otherwise noted.

Figure 3. Gain vs. Frequency for Values of V_{GAIN}

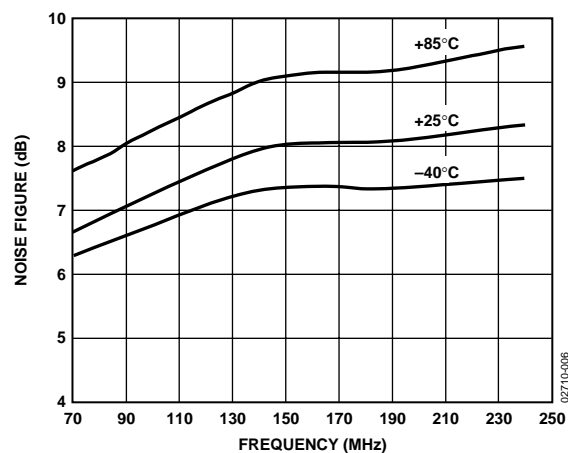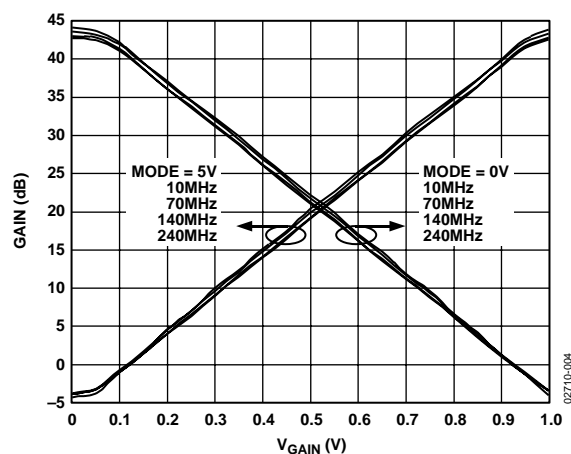Figure 6. NF (re 200 Ω) vs. Frequency at Maximum Gain
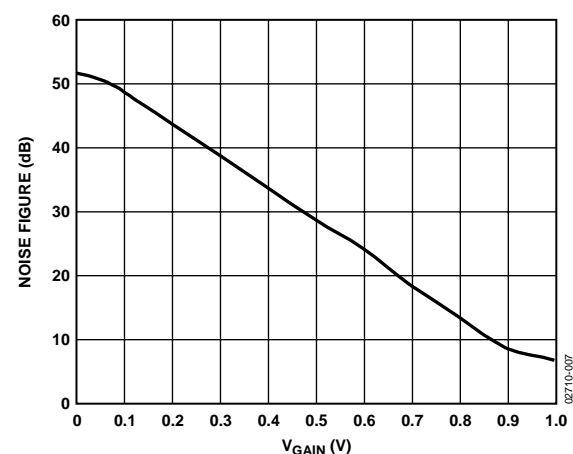

Figure 4. Gain vs. V_{GAIN} (Mode LO and Mode HI)

Figure 7. NF (re 200 Ω) vs. V_{GAIN} at 70 MHz

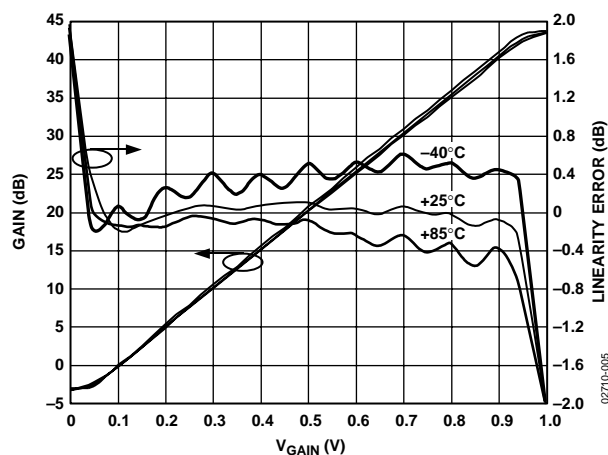Figure 5. Gain Conformance at 70 MHz for T = −40°C, +25°C, and +85°C

Figure 8. OIP3 vs. V_{GAIN}

AD8367

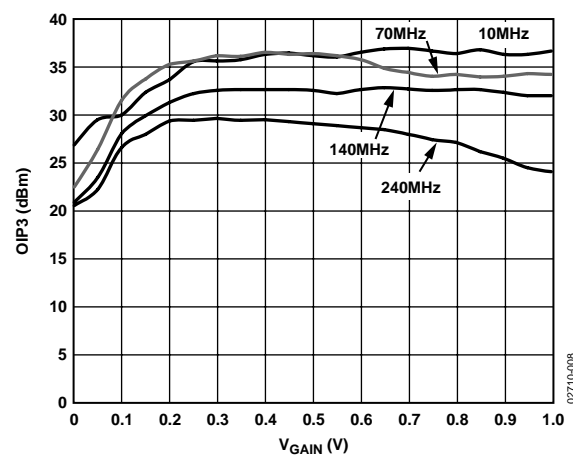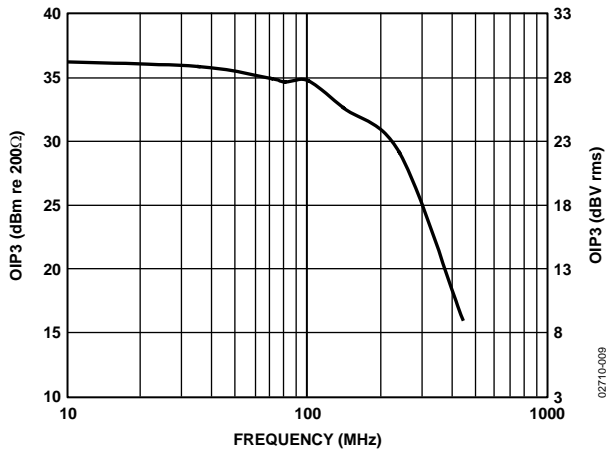Figure 9. OIP3 vs. Frequency for V_{GAIN} = 500 mV

Figure 10. Output P1dB vs. V_{GAIN}

Figure 11. Output P1dB vs. Frequency at V_{GAIN} = 500 mV
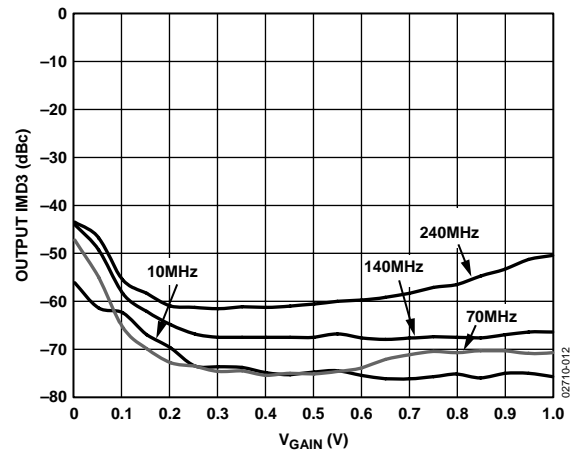

Figure 12. IMD3 vs. Gain (V_{OUT} = 1 V p-p Composite)

Figure 13. Output Compression Point vs. Supply Voltage at 70 MHz, V_{GAIN} = 500 mV
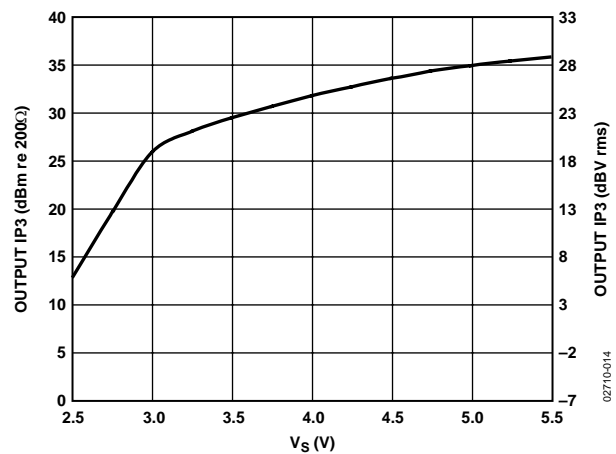
Figure 14. Output Third-Order Intercept vs. Supply Voltage at 70 MHz, V_{GAIN} = 500 mV
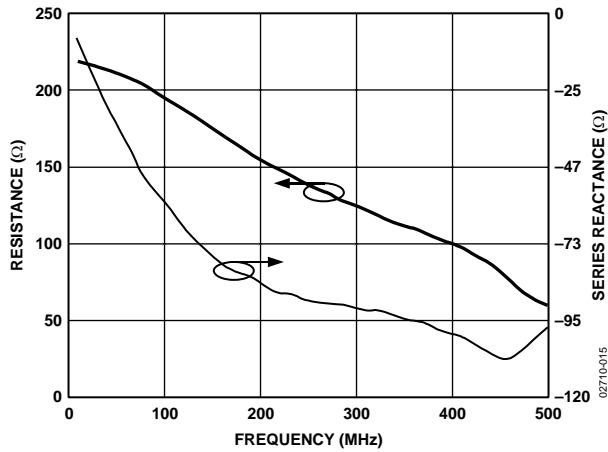
Figure 15. Input Resistance and Series Reactance vs. Frequency at V_{GAIN} = 500 mV
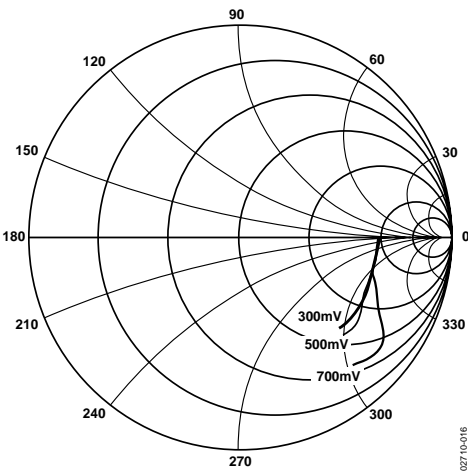
Figure 16. Input Reflection Coefficient vs. Frequency from 10 MHz to 500 MHz for Multiple Values of V_{GAIN}
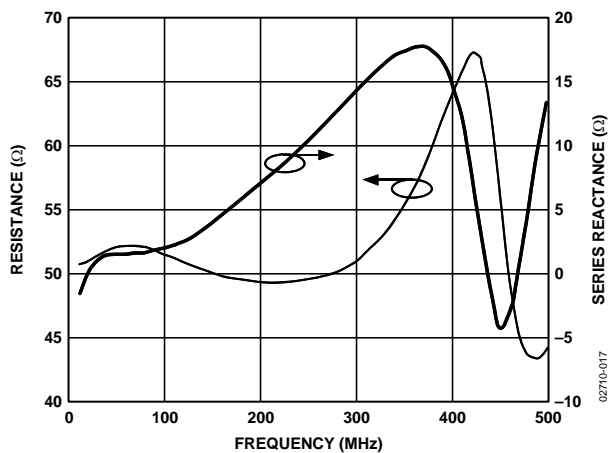
Figure 17. Output Resistance and Series Reactance vs. Frequency at V_{GAIN} = 500 mV
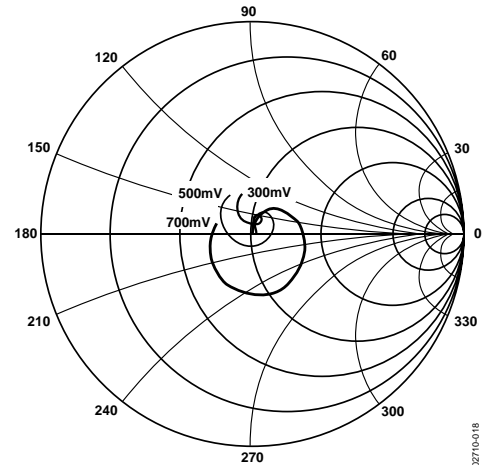
Figure 18. Output Reflection Coefficient vs. Frequency from 10 MHz to 500 MHz for Multiple Values of V_{GAIN}
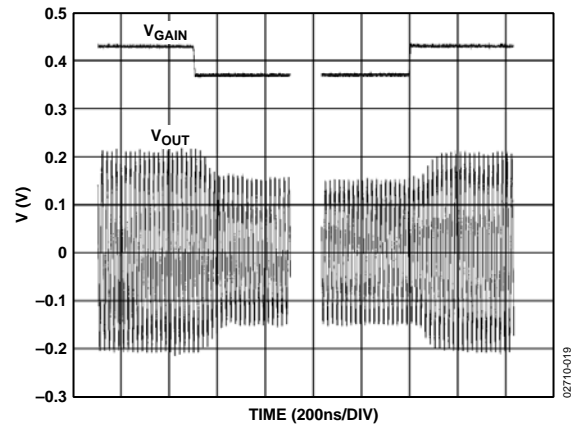
Figure 19. AGA Time Domain Response (3 dB Steps)
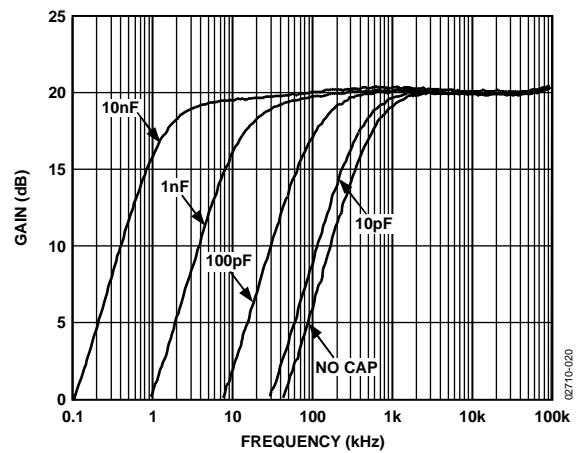
Figure 20. Gain vs. Frequency for Multiple Values of HPFL Capacitor at V_{GAIN} = 500 mV

AD8367
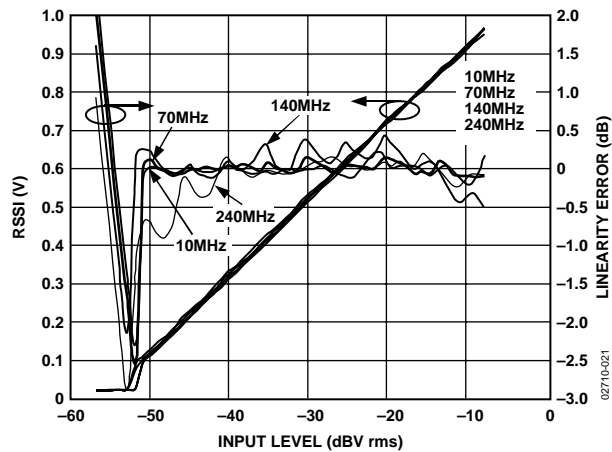
Figure 21. AGC RSSI (Voltage on DETO Pin) vs. Input Power at 10 MHz, 70 MHz, 140 MHz, and 240 MHz
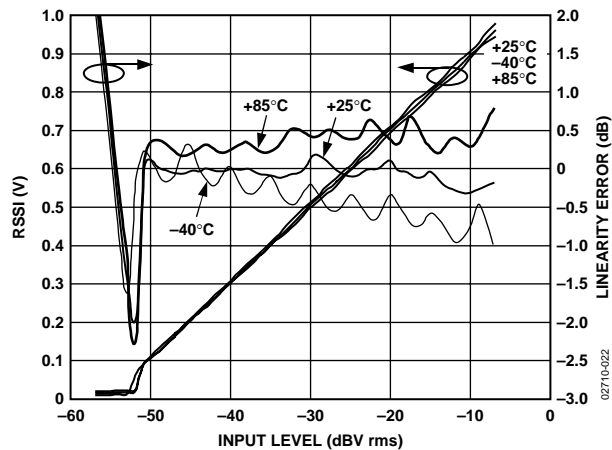
Figure 22. AGC RSSI (Voltage on DETO Pin) vs. Input Power over Temperature at 70 MHz
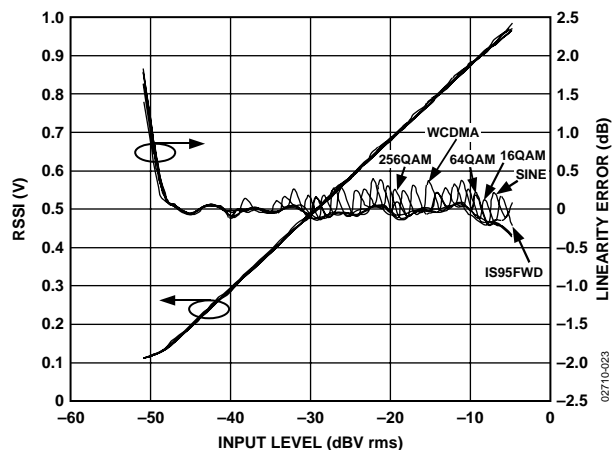
Figure 23. AGC RSSI (Voltage on DETO Pin) vs. Input Power for Various Modulation Schemes
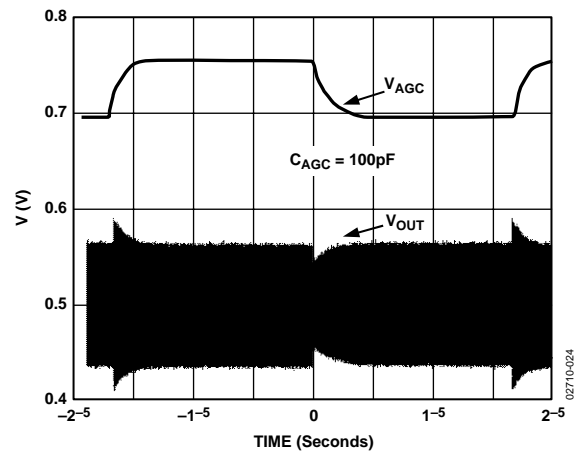
Figure 24. AGC Time Domain Response (3 dB Step)
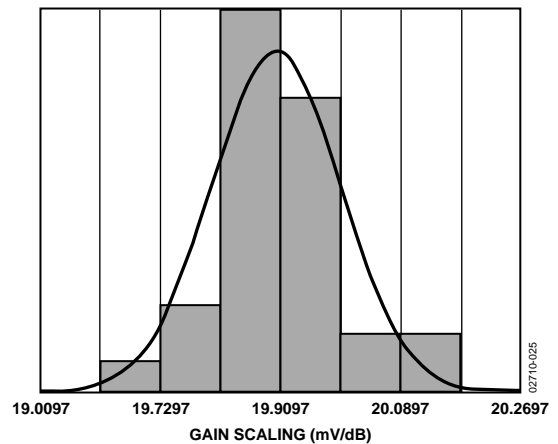
Figure 25. Gain Scaling Distribution at 70 MHz
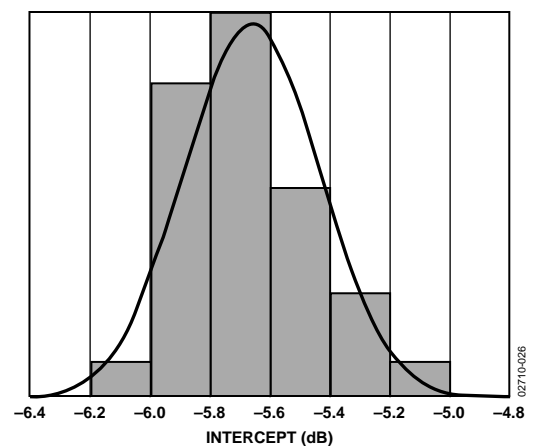
Figure 26. Gain Intercept Distribution at 70 MHz

THEORY OF OPERATION

The AD8367 is a variable gain, single-ended, IF amplifier based on Analog Devices' patented X-AMP architecture. It offers accurate gain control with a 45 dB span and a 3 dB bandwidth of 500 MHz. It can be configured as a traditional VGA with 50 dB/V gain scaling or as an AGC amplifier by using the built in rms detector. Figure 27 is a simplified block diagram of the amplifier. The main signal path consists of a voltage controlled 0 dB to 45 dB variable attenuator followed by a 42.5 dB fixed gain amplifier. The AD8367 is designed to operate optimally in a 200 Ω impedance system.
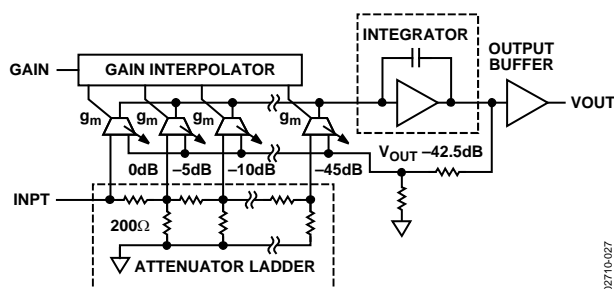
Figure 27. Simplified Architecture

INPUT ATTENUATOR AND GAIN CONTROL

The variable attenuator consists of a 200 Ω single-ended resistive ladder that comprises of nine 5 dB sections and an interpolator that selects the attenuation factor. Each tap point down the ladder network further attenuates the input signal by a fixed decibel factor. Gain control is achieved by sensing different tap points with variable transconductance stages. Based on the gain control voltage, an interpolator selects which stage(s) are active. For example, if only the first stage is active, the 0 dB tap point is sensed; if the last stage is active, the 45 dB tap point is sensed. Attenuation levels that fall between tap points are achieved by having neighboring g_m stages active simultaneously, creating a weighted average of the discrete tap point attenuations. In this way, a smooth, monotonic attenuation function is synthesized, that is, linear-in-dB with a very precise scaling.

The gain of the AD8367 can be an increasing or decreasing function of the control voltage, V_{GAIN}, depending on whether the MODE pin is pulled up to the positive supply or down to ground. When the MODE pin is high, the gain increases with V_{GAIN}, as shown in Figure 28. The ideal linear-in-dB scaled transfer function is given by

$$Gain \text{ (dB)} = 50 \times V_{GAIN} - 5 \tag{1}$$

where V_{GAIN} is expressed in volts.

Equation 1 contains the gain scaling factor of 50 dB/V (20 mV/dB) and the gain intercept of −5 dB, which represents the extrapolated gain for V_{GAIN} = 0 V. The gain ranges from −2.5 dB to +42.5 dB for V_{GAIN} ranging from 50 mV to 950 mV. The

deviation from Equation 1, that is, the gain conformance error, is also illustrated in Figure 28. The ripples in the error are a result of the interpolation action between tap points. The AD8367 provides better than ±0.5 dB of conformance error over >40 dB gain range at 200 MHz and ±1 dB at 400 MHz.
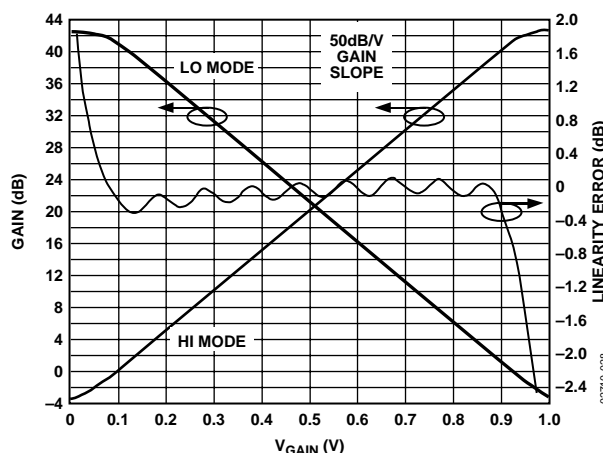
Figure 28. The gain function can be either an increasing or decreasing function of V_{GAIN}, depending on the MODE pin.

The gain is a decreasing function of V_{GAIN} when the MODE pin is low. Figure 28 also illustrates this mode, which is described by

$$Gain \text{ (dB)} = 45 - 50 \times V_{GAIN} \tag{2}$$

This gain mode is required in AGC applications using the built-in, square-law level detector.

INPUT AND OUTPUT INTERFACES

The AD8367 was designed to operate best in a 200 Ω impedance system. Its gain range, conformance law, noise, and distortion assume that 200 Ω source and load impedances are used. Interfacing the AD8367 to other common impedances (from 50 Ω used at radio frequencies to 1 kΩ presented by data converters) can be accomplished using resistive or reactive passive networks, whose design depends on specific system requirements, such as bandwidth, return loss, noise figure, and absolute gain range.

The input impedance of the AD8367 is nominally 200 Ω, determined by the resistive ladder network. This presents a 200 Ω dc resistance to ground, and, in cases where an elevated signal potential is used, ac coupling is necessary. The input signal level must not exceed 700 mV p-p to avoid overloading the input stage. The output impedance is determined by an internal 50 Ω damping resistor, as shown in Figure 29. Despite the fact that the output impedance is 50 Ω, the AD8367 should still be presented with a load of 200 Ω. This implies that the load is mismatched, but doing so preserves the distortion performance of the amplifier.
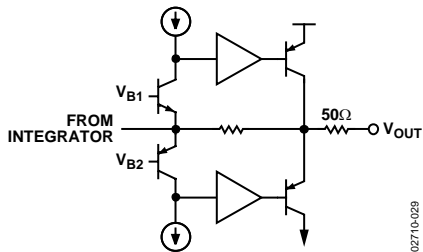
Figure 29. A 50 Ω resistor is added to the output to prevent package resonance.

POWER AND VOLTAGE METRICS

Although power is the traditional metric used in the analysis of cascaded systems, most active circuit blocks fundamentally respond to voltage. The relationship between power and voltage is defined by the impedance level. When input and output impedance levels are the same, power gain and voltage gain are identical. However, when impedance levels change between input and output, they differ. Thus, one must be very careful to use the appropriate gain for system chain analyses. Quantities such as OIP3 are quoted in dBV rms as well as dBm referenced to 200 Ω. The dBV rms unit is defined as decibels relative to 1 V rms. In a 200 Ω environment, the conversion from dBV rms to dBm requires the addition of 7 dB to the dBV rms value. For example, a 2 dBV rms level corresponds to 9 dBm.

NOISE AND DISTORTION

Since the AD8367 consists of a passive variable attenuator followed by a fixed gain amplifier, the noise and distortion characteristics as a function of the gain voltage are easily predicted. The input-referred noise increases in proportion to the attenuation level. Figure 30 shows noise figure, NF, as a function of V_{GAIN} for the MODE pin pulled high. The minimum NF of 7.5 dB occurs at maximum gain and increases 1 dB for every 1 dB reduction in gain. In receiver applications, the minimum NF should occur at the maximum gain where the received signal presumably is weak. At higher levels, a lower gain is needed, and the increased NF becomes less important.

The input-referred distortion varies in a similar manner to the noise. Figure 30 illustrates how the third-order intercept point at the input, IIP3, behaves as a function of V_{GAIN}. The highest IIP3 of 20 dBV rms (27 dBm re 200 Ω) occurs at minimum gain. The IIP3 then decreases 1 dB for every 1 dB increase in gain. At lower levels, a degraded IIP3 is acceptable. Overall, the dynamic range, represented by the difference between IIP3 and NF, remains reasonably constant as a function of gain. The output distortion and compression are essentially independent of the gain. At low gains, when the input level is high, input overload can occur, causing premature distortion.
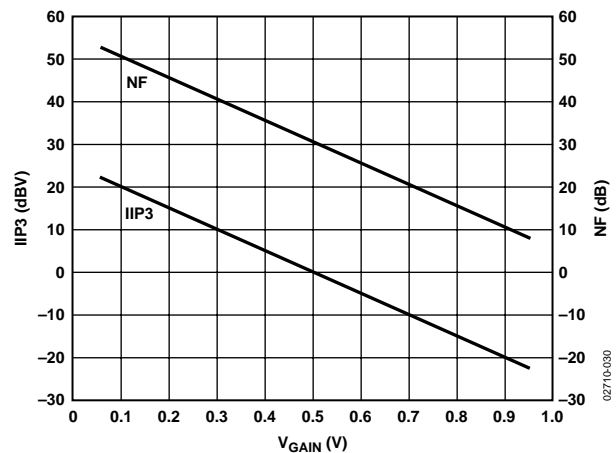
Figure 30. Noise Figure and Input Third-Order Intercept vs. Gain ($R_{SOURCE} = 200 Ω$)

OUTPUT CENTERING

To maximize the ac swing at the output of the AD8367, the output level is centered midway between ground and the supply. This is achieved when the DECL pin is bypassed to ground via a shunt capacitor. The loop acts to suppress deviations from the reference at outputs below its corner frequency while not affecting signals above it, as shown in Figure 31. The maximum corner frequency with no external capacitor is 500 kHz. The corner frequency can be lowered arbitrarily by adding an external capacitor, C_{HP}:

$$f_{HP}(\text{kHz}) = \frac{10}{C_{HP}(\text{nF}) + 0.02} \qquad (3)$$

A 100 Ω in series with the C_{HP} capacitor is recommended to de-Q the resonant tank that is formed by the bond-wire inductance and C_{HP}. Failure to insert this capacitor can potentially cause oscillations at higher frequencies at high gain settings.
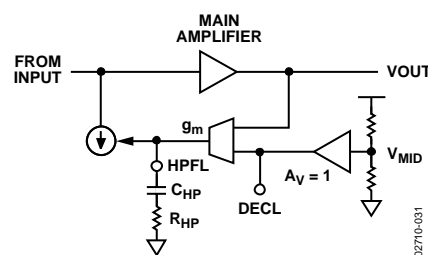
Figure 31. The dc output level is centered to midsupply by a control loop whose corner frequency is determined by C_{HP}.

RMS DETECTION

The AD8367 contains a square-law detector that senses the output signal and compares it to a calibrated setpoint of 354 mV rms, which corresponds to a 1 V p-p sine wave. This setpoint is internally set and cannot be modified to change the AGC setpoint and the resulting VOUT level without using additional external components. This is described in the Modifying the AGC Setpoint section.

Any difference between the output and setpoint generates a current that is integrated by an external capacitor, C_{AGC}, connected from the DETO pin to ground, to provide an AGC control voltage. There is also an internal 5 pF capacitor on the DETO pin.

The resulting voltage is used as an AGC bias. For this application, the MODE pin is pulled low and the DETO pin is tied to the GAIN pin. The output signal level is then regulated to 354 mV rms. The AGC bias represents a calibrated rms measure of the received signal strength (RSSI). Since in AGC mode the output signal is forced to the 354 mV rms setpoint (−9.02 dBV rms), Equation 2 can be recast to express the strength of the received signal, $V_{IN\text{-}RMS}$, in terms of the AGC bias V_{DETO}.

$$V_{IN-RMS} \text{ (dBV rms)} = 54.02 + 50 \times V_{DETO} \qquad (4)$$

where −54.02 dBV rms = −45 dB − 9.02 dBV rms.

For small changes in input signal level, V_{DETO} responds with a characteristic single-pole time constant, τ_{AGC}, which is proportional to C_{AGC}.

$$\tau_{AGC} \text{ (μs)} = 10 \times C_{AGC} \text{ (nf)} \qquad (5)$$

where the internal 5 pF capacitor is lumped with the external capacitor to give C_{AGC}.

APPLICATIONS

The AD8367 can be configured either as a VGA whose gain is controlled externally through the GAIN pin or as an AGC amplifier, using a supply voltage of 2.7 V to 5.5 V. The supply to the VPSO and VPSI pins should be decoupled using a low inductance, 0.1 μF surface-mount, ceramic capacitor as close as possible to the device. Additional supply decoupling can be provided by a small series resistor. A 10 nF capacitor from Pin DECL to Pin OCOM is recommended to decouple the output reference voltage.

INPUT AND OUTPUT MATCHING

The AD8367 is designed to operate in a 200 Ω impedance system. The output amplifier is a low output impedance voltage buffer with a 50 Ω damping resistor to desensitize it from load reactance and parasitics. The quoted performance includes the voltage division between the 50 Ω resistor and the 200 Ω load. The AD8367 can be reactively matched to an impedance other than 200 Ω by using traditional step-up and step down matching networks or high quality transformers. Table 4 lists the 50 Ω S-parameters for the AD8367 at a V_{GAIN} = 750 mV.

Figure 32 illustrates an example where the AD8367 is matched to 50 Ω at 140 MHz. As shown in the Smith Chart, the input matching network shifts the input impedance from Z_{IN} to 50 Ω with an insertion loss of <2 dB over a 5 MHz bandwidth. For the output network, the 50 Ω load is made to present 200 Ω to the AD8367 output. Table 5 provides the component values required for 50 Ω matching at several frequencies of interest.

When added loss and noise can be tolerated, a resistive pad can be used to provide broadband, near-matched impedances at the device terminals and the terminations.

Minimum-loss, L-pad networks are used on the evaluation board (see Figure 45) to allow easy interfacing to standard 50 Ω test equipment. Each pad introduces an 11.5 dB power loss (5.5 dB voltage loss).

f_C = 140MHz, Z_{IN} = 197 − j34.2, R_{SOURCE} = 50Ω
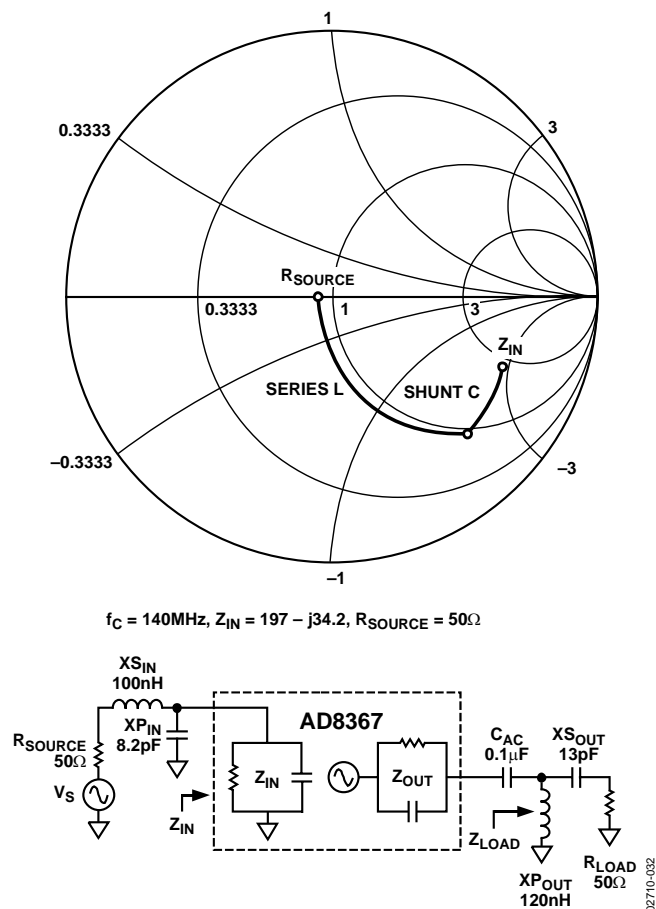
Figure 32. Reactive Matching Example for f = 140 MHz

Table 4. S-Parameters for 200 Ω System for V_S = 5 V and V_{GAIN} = 0.75 V

Frequency (MHz)	S11	S21	S12	S22
10	0.04 ∠ −43.8°	41.1 ∠ 178.8°	0.0003 ∠ 76.1°	0.56 ∠ −179.3°
70	0.09 ∠ −81.5°	43.6 ∠ 163.4°	0.0002 ∠ 63.7°	0.55 ∠ +176.1°
140	0.17 ∠ −103.4°	48.0 ∠ 141.4°	0.0009 ∠ 130.8°	0.56 ∠ +170.2°
190	0.21 ∠ −111.7°	47.5 ∠ 124.0°	0.0017 ∠ 96.8°	0.54 ∠ +166.5°
240	0.26 ∠ −103.8°	48.3 ∠ 107.6°	0.0018 ∠ 113.5°	0.48 ∠ +164.6°

Table 5. Reactive Matching Components for a 50 Ω System where R_{SOURCE} = 50 Ω, R_{LOAD} = 50 Ω

Frequency (MHz)	XS_{IN}	XP_{IN} (pF)	XS_{OUT} (pF)	XP_{OUT}
10	1.5 μH	120	180	1.8 μH
70	220 nH	15	27	270 nH
140	100 nH	8.2	13	120 nH
190	82 nH	2.7	10	100 nH
240	68 nH	1.5	7	82 nH

VGA OPERATION

The AD8367 is a general-purpose VGA suitable for use in a wide variety of applications where voltage control of gain is needed. While having a 500 MHz bandwidth, its use is not limited to high frequency signal processing. Its accurate, temperature- and supply-stable linear-in-dB scaling is valuable wherever it is important to have a more dependable response to the control voltage than is usually offered by VGAs of this sort. For example, there is no preclusion to its use in speech-bandwidth systems.

Figure 33 shows the basic connections. The C_{HP} capacitor at Pin HPFL can be used to alter the high-pass corner frequency of the signal path and is associated with the offset control loop that eliminates the inherent variation in the internal dc balance of the signal path as the gain is varied (offset ripple). This frequency should be chosen to be about a decade below the lowest frequency component of the signal. If made much lower than necessary, the offset loop is not able to track the variations that occur when there are rapid changes in V_{GAIN}. The control of offset is important even when the output is ac-coupled because of the potential reduction of the upper and lower voltage range at this pin.

However, in many applications these components are unnecessary because an internal network provides a default high-pass corner of about 500 kHz. For C_{HP} = 1 nF, the modified corner is at ~10 kHz; it scales downward with increasing capacitance. Figure 20 shows representative response curves for the indicated component values.

Figure 33. Basic Connections for Voltage Controlled Gain Mode

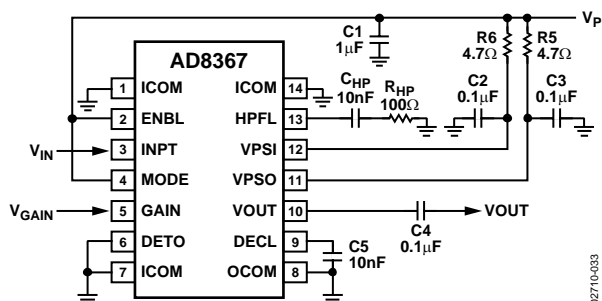## MODULATED GAIN MODE

The AD8367 can be used as a means of modulating the signal level. Keep in mind, however, that the gain is a nonlinear (exponential) function of V_{GAIN}; thus, it is not suitable for normal amplitude-modulation functions. The small signal bandwidth of the gain interface is ~5 MHz, and the slew rate is of the order of ±500 dB/µs. During gain slewing from close to minimum to maximum gain (or vice versa), the internal interpolation processes in an X-AMP-based VGA rapidly scan the full range of gain values. The gain and offset ripple associated with this process can cause transient disturbances in the output. Therefore, it is inadvisable to use high amplitude pulse drives with rise and fall times below 200 ns.

AGC OPERATION

The AD8367 can be used as an AGC amplifier, as shown in Figure 34. For this application, the accurate internal, square-law detector is employed. The output of this detector is a current that varies in polarity, depending on whether the rms value of the output is greater or less than its internally-determined setpoint of 354 mV rms. This is 1 V p-p for sine-wave signals, but the peak amplitude for other signals, such as Gaussian noise, or those carrying complex modulation, is invariably somewhat greater. However, for all waveforms having a crest factor of <5, and when using a supply voltage of 4.5 V to 5.5 V, the rms value is correctly measured and delivered at V_{OUT}. When using lower supplies, the rms value of V_{OUT} is unaffected (the setpoint is determined by a band gap reference), but the peak crest factor capacity is reduced.

The gain pin is connected to the base of a transistor internally and thus requires only 1 µA of current drive. The output of the detector is delivered to Pin DETO. The detector can source up to 60 µA and can sink up to 11 µA. For a sine-wave output signal, and under conditions where the AGC loop is settled, the detector output also takes the form of a sine-wave, but at twice the frequency and having a mean value of 0. If the input to the amplifier increases, the mean of this current also increases and charges the external loop filter capacitor, C_{AGC}, toward more positive voltages. Conversely, a reduction in V_{OUT} below the setpoint of 354 mV rms causes this voltage to fall toward ground. The capacitor voltage is the AGC bias; this can be used as a received signal strength indicator (RSSI) output and is scaled exactly as V_{GAIN}, that is, 20 mV/dB.
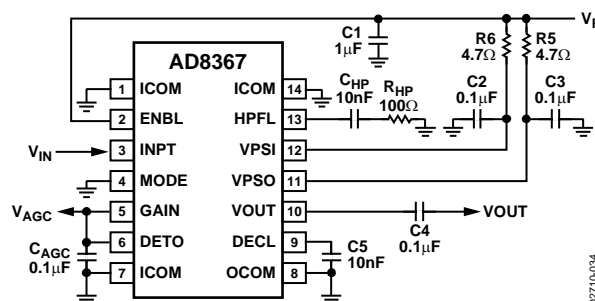
Figure 34. Basic Connections for AGC Operation

A valuable feature of using a square law detector is that the RSSI voltage is a true reflection of signal power and can be converted to an absolute power measurement for any given source impedance. The AD8367 can thus be employed as a true-power meter, or decibel-reading ac voltmeter, as distinct from its basic amplifier function.

The AGC mode of operation requires that the correct gain direction is chosen. Specifically, the gain must fall as V_{AGC} increases to restore the needed balance against the setpoint. Therefore, the MODE pin must be pulled low. This accurate leveling function is shown in Figure 35, where the rms output is

AD8367

held to within 0.1 dB of the setpoint for >35 dB range of input levels.

The dynamics of this loop are controlled by C_{AGC} acting in conjunction with an on-chip equivalent resistance, R_{AGC}, of 10 kΩ which form an effective time-constant $T_{AGC} = R_{AGC} C_{AGC}$. The loop thus operates as a single-pole system with a loop bandwidth of $1/(2\pi T_{AGC})$. Because the gain control function is linear in decibels, this bandwidth is independent of the absolute signal level. Figure 36 illustrates the loop dynamics for a 30 dB change in input signal level with $C_{AGC} = 100$ pF.
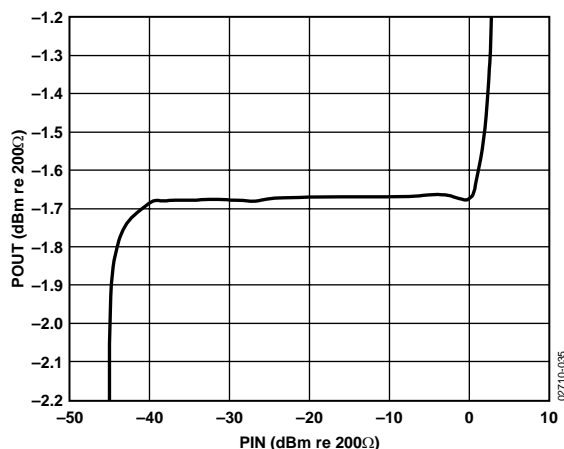
Figure 35. Leveling Accuracy of the AGC Function
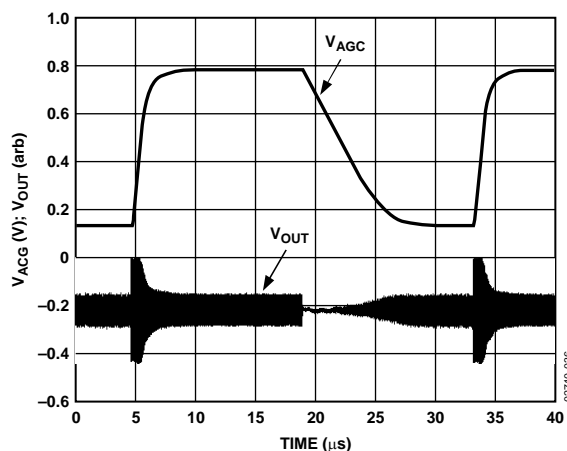
Figure 36. AGC Response to a 32 dB Step in Input Level (f = 50 MHz)

It is important to understand that R_{AGC} does not act as if in shunt with C_{AGC}. Rather, the error-correction process is that of a true integrator, to guarantee an output that is exactly equal in rms amplitude to the specified setpoint. For large changes in input level, the integrating action of this loop is most apparent. The slew rate of V_{AGC} is determined by the peak output current from the detector and the capacitor. Thus, for a representative value of $C_{AGC} = 3$ nF, this rate is about 20 V rms or 10 dB/μs, while the small-signal bandwidth is 1 kHz.

Most AGC loops incorporating a true error-integrating technique have a common weakness. When driven from an increasingly larger signal, the AGC bias increases to reduce the gain. However, eventually the gain falls to its minimum value, for which further increase in this bias has no effect on the gain. That is, the voltage on the loop capacitor is forced progressively higher because the detector output is a current, and the AGC bias is its integral. Consequently, there is always a precipitous increase in this bias voltage when the input to the AD8367 exceeds that value that overdrives the detector, and because the minimum gain is −2.5 dB, that happens for all inputs 2.5 dB greater than the setpoint of ~350 mV rms. If possible, the user should ensure that this limitation is preserved, preferably with a guard-band of 5 dB to 10 dB below overload

In some cases, if driven into AGC overload, the AD8367 requires unusually long times to recover; that is, the voltage at DETO remains at an abnormally high value and the gain is at its lowest value. To avoid this situation, it is recommended that a clamp be placed on the DETO pin, as shown in Figure 37.
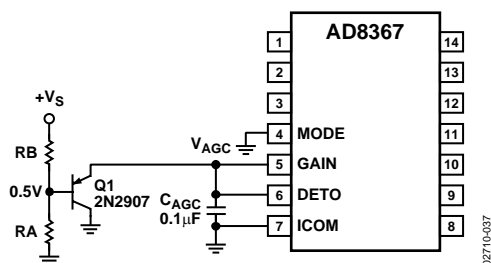
Figure 37. External Clamp to Prevent AGC Overload.
The resistive divider network, RA and RB, should be designed such that the base of Q1 is driven to 0.5 V.

MODIFYING THE AGC SETPOINT

If an AGC setpoint other than the internal one is desired, an external detector must be used. Figure 38 shows a method that uses an external true-rms detector and error integrator to operate the AD8367 as a closed-loop AGC system with a user-settable operating level.

The AD8361 (U2) produces a dc output level that is proportional to the rms value of its input, taken as a sample of the AD8367 (U1) output. This dc voltage is compared to an externally-supplied setpoint voltage, and the difference is integrated by the AD820 (U3) to form the gain control voltage that is applied to the GAIN input of the AD8367 through the divider composed of R4 and R5. This divider is included in order to minimize overload recovery time of the loop by having the integrator saturate at a point that only slightly overdrives the gain control input of the AD8367. The scale factor at V_{AGC} is influenced by the values of R4 and R5; for the values shown, the factor is 86 mV/dB.

Figure 38. Example of Using an External Detector to Form an AGC Loop

Note that in this circuit the AD8367's MODE pin must be pulled high to obtain correct feedback polarity because the integrator inverts the polarity of the feedback signal.

The relationship between the setpoint voltage and the rms output voltage of the AD8367 is

$$V_{OUT-RMS} = V_{SET} \times \frac{(R1 + 225)}{225 \times 7.5} \tag{6}$$

where 225 is the input resistance of the AD8361 and 7.5 is its conversion gain. For $R1 = 200\ \Omega$, this reduces to $V_{OUT-RMS} = V_{SET} \times 0.25$.

Capacitor C2 sets the averaging time for the rms detector. This should be made long enough to provide sufficient smoothing of the detector's output in the presence of the modulation on the RF signal. A level fluctuation of less than 1 dB (<5% to 10%) p-p at the AD8361's output is a reasonable value. A considerably longer time constant needlessly lowers the AGC bandwidth, while a short time constant can degrade the accuracy of the true-rms measurement process. Components C1, R2, and R3 set the control loop's bandwidth and stability. The maximum stable loop bandwidth is limited by the rms detector's averaging time constant as previously discussed.

For an input signal consisting of a 4.096 MS/s QPSK modulated carrier, the relationship between V_{SET} and the output power for this setup is shown in Figure 39. The exponential shape reflects the linear-in-magnitude response of the AD8361. The adjacent channel power ratio (ACPR) as a function of output power is illustrated in Figure 40. The minima occur where the distortion and integrated noise powers cross over.

The component values shown in Figure 38 were chosen for a 64-QAM signal at 500 kS/s at a carrier frequency of 150 MHz. The response time of the loop as shown is roughly 5 ms for an abrupt input level change of 40 dB. Figure 41 shows the dynamic performance of the loop with a step-modulated CW signal applied to the input for a V_{SET} of about 1 V.

For a linear-in-dB response, detectors such as the AD8318 or the AD8362 can be used in place of the AD8361.

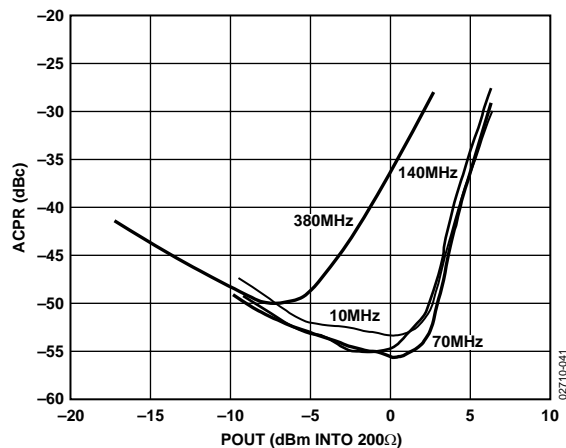Figure 39. AGC Setpoint Voltage vs. Output Power
(QPSK: 4.096 MS/s; α = 0.22; 1 User)

Figure 40. ACPR vs. Output Power for QPSK Waveform
(QPSK: 4.096 MS/s; α = 0.22; 1 User)

Figure 41. AGC Dynamic Response: 8367 AGC with an External Detector

Table 6. Suggested Component Values for External AGC Detector Circuit

Modulation Type	Rate Sys/s	C1 (µF)	C2 (µF)	R2 (kΩ)	R3 (kΩ)
QPSK	1.23 M	0.0022	0.033	150	62
QPSK	4 M	0.0022	0.015	150	39
π/4 DQPSK	24.3 K	0.033	0.68	150	51
64 QAM	100 K	0.015	1.5	150	51
64 QAM	500 K	0.0068	0.33	150	62
64 QAM	4 M	0.0022	0.068	150	100

EVALUATION BOARD

Figure 42 shows the schematic of the AD8367 evaluation board. The board is powered by a single supply of 2.7 V to 5.5 V.

Figure 42. Evaluation Board Schematic

Figure 43. Layout of Component Side

Figure 44. Silkscreen of Component Side

AD8367

Table 7 details the various configuration options of the evaluation board.

Table 7. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP2	Supply and Ground Vector Pins.	Not Applicable
TP3, TP4	Mode and Gain Vector Pins.	Not Applicable
SW1	VGA/AGC Select: Used to select VGA (Position A) or AGC (Position B) mode of operation. SW2 must be set for Position A for AGC mode of operation.	SW1 = A
SW2	MODE Select. Used to select positive or negative VGA slope. Set to Position B for an increasing gain with V_{GAIN}, Position A for decreasing gain law.	SW2 = B
LK1	Device Enable. When LK1 is installed, the ENBL pin is connected to the positive supply and the AD8367 is in operating mode.	LK1 = Installed
R1, R2	Input Interface. R1 and R2 are used to provide an L-pad impedance-transforming network. The broadband matching network transforms a 50 Ω source to match a 200 Ω load with 11.5 dB of insertion loss.	R1 = 57.6 Ω (Size 0603) R2 = 174 Ω (Size 0603)
R3, R4, C4	Output Interface. R3 and R4 are used to transform a 50 Ω load termination to look like a 200 Ω load with 11.5 dB of insertion loss. The ac coupling capacitor, C4, can be increased to obtain a lower high-pass corner frequency.	R3 = 57.6 Ω (Size 0603) R4 = 174 Ω (Size 0603) C4 = 0.1 µF (Size 0603)
C1, C2, C3, R5, R6	Power Supply Decoupling. The nominal supply decoupling consists of a 1 µF capacitor to ground, a 4.7 Ω series resistor, and a 0.1 µF capacitor to ground. The same decoupling network should be used on both the VPSI and VPSO supply lines.	C1 = 1 µF (Size 0603) R5 = R6 = 4.7 Ω (Size 0805) C2 = C3 = 0.1 µF (Size 0603)
C5	Internal Supply Decoupling. Capacitor C5 provides midsupply decoupling.	C5 = 10 nF (Size 0603)
C_{HP}	Filter Capacitor. HPFL capacitor, sets the high-pass corner frequency.	C_{HP} = 0.01 µF (Size 0805) R_{HP} = 0 Ω (Size 0603)
C_{AGC}	AGC Filter Capacitor. Capacitor, CAGC, sets closed-loop AGC response time.	C_{AGC} = 0.1 µF (Size 0805)
R7	Mode Pull-Up Resistor.	R7 = 10 kΩ (Size 0805)
R_{HP}	High-Pass Filter Resistor.	R_{HP} = 100 Ω (Size)

CHARACTERIZATION SETUP AND METHODS

Minimum-loss, L-pad matching networks were used to interface standard 50 Ω. A test equipment to the 200 Ω input impedance during the characterization process. Using a 57.6 Ω shunt resistor followed by a 174 Ω series resistor provides a broadband match between the 50 Ω test equipment and the 200 Ω device impedance, as illustrated in Figure 45. The insertion loss of this network is 11.5 dB.
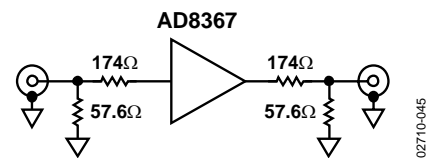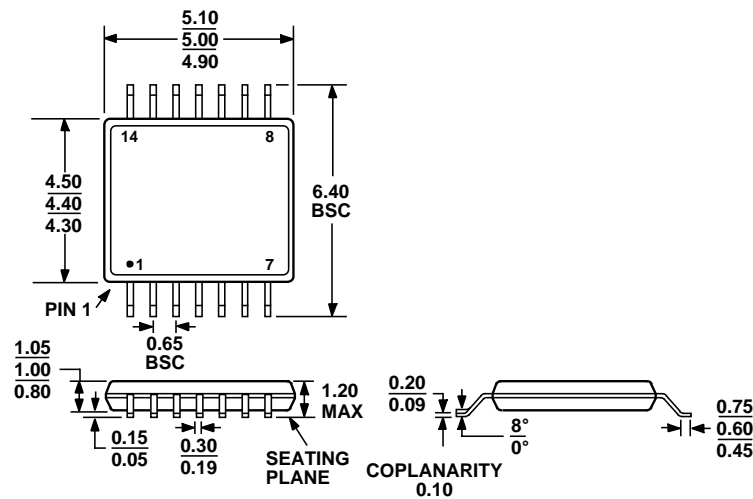

Figure 45. Characterization Test Setup

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-153AB-1

Figure 46. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimension shown millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8367ARU	−40°C to +85°C	14-Lead TSSOP, Tube	RU-14
AD8367ARU-REEL-7	−40°C to +85°C	14-Lead TSSOP, 7" Tape and Reel	RU-14
AD8367ARUZ[1]	−40°C to +85°C	14-Lead TSSOP, Tube	RU-14
AD8367ARUZ-RL7[1]	−40°C to +85°C	14-Lead TSSOP, 7" Tape and Reel	RU-14
AD8367-EVAL		Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

NOTES

ANALOG DEVICES

www.analog.com