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EVALUATION KITS

- Universal Evaluation Board for Single High Speed Operational Amplifiers

DOCUMENTATION

Application Notes

- AN-108: JFET-Input Amps are Unrivaled for Speed and Accuracy
- AN-214: Ground Rules for High Speed Circuits
- AN-356: User's Guide to Applying and Measuring Operational Amplifier Specifications
- AN-402: Replacing Output Clamping Op Amps with Input Clamping Amps
- AN-417: Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems
- AN-581: Biasing and Decoupling Op Amps in Single Supply Applications
- AN-649: Using the Analog Devices Active Filter Design Tool

Data Sheet

- AD825: Low Cost, General-Purpose High Speed JFET Amplifier Data Sheet

User Guides

- UG-755: 8-Lead SOIC Amplifier Evaluation Board User Guide

TOOLS AND SIMULATIONS

- Analog Filter Wizard
- Analog Photodiode Wizard
- Power Dissipation vs Die Temp
- VRMS/dBm/dBu/dBV calculators
- AD825 SPICE Macro Models

REFERENCE MATERIALS

Tutorials

- MT-032: Ideal Voltage Feedback (VFB) Op Amp
- MT-033: Voltage Feedback Op Amp Gain and Bandwidth
- MT-047: Op Amp Noise
- MT-048: Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth
- MT-049: Op Amp Total Output Noise Calculations for Single-Pole System
- MT-050: Op Amp Total Output Noise Calculations for Second-Order System
- MT-052: Op Amp Noise Figure: Don't Be Misled
- MT-053: Op Amp Distortion: HD, THD, THD + N, IMD, SFDR, MTPR
- MT-056: High Speed Voltage Feedback Op Amps
- MT-058: Effects of Feedback Capacitance on VFB and CFB Op Amps
- MT-060: Choosing Between Voltage Feedback and Current Feedback Op Amps

DESIGN RESOURCES

- AD825 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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SPECIFICATIONS

All limits are determined to be at least four standard deviations away from mean value. At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

Table 1.

Parameter	Conditions	V_S	AD825A Min	AD825A Typ	AD825A Max	Unit
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±15 V	23	26		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±15 V	18	21		MHz
−3 dB Bandwidth	Gain = +1	±15 V	44	46		MHz
Slew Rate	R_{LOAD} = 1 kΩ, G = +1	±15 V	125	140		V/µs
Settling Time to 0.1%	0 V to 10 V Step, A_V = −1	±15 V		150	180	ns
to 0.1%	0 V to 10 V Step, A_V = −1	±15 V		180	220	ns
Total Harmonic Distortion	F_C = 1 MHz, G = −1	±15 V		−77		dB
Differential Gain Error	NTSC	±15 V		1.3		%
(R_{LOAD} = 150 Ω)	Gain = +2					
Differential Phase Error	NTSC	±15 V		2.1		Degrees
(R_{LOAD} = 150 Ω)	Gain = +2					
INPUT OFFSET VOLTAGE		±15 V		1	2	mV
	T_{MIN} to T_{MAX}				5	mV
Offset Drift				10		µV/°C
INPUT BIAS CURRENT		±15 V		15	40	pA
	T_{MIN}		5			pA
	T_{MAX}				700	pA
INPUT OFFSET CURRENT		±15 V		20	30	pA
	T_{MIN}		5			pA
	T_{MAX}				440	pA
OPEN-LOOP GAIN	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		70	76		dB
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 1 kΩ		70	76		dB
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 kΩ (50 mA Output)		68	74		dB
COMMON-MODE REJECTION	V_{CM} = ±10	±15 V	71	80		dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		12		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		10		fA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±15 V		±13.5		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 1 kΩ	±15 V	13	±13.3		V
	R_{LOAD} = 500 Ω	±15 V	12.9	±13.2		V
Output Current		±15 V	50			mA
Short-Circuit Current		±15 V		100		mA
INPUT RESISTANCE				5×10^{11}		Ω
INPUT CAPACITANCE				6		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Quiescent Current		±15 V		6.5	7.2	mA
	T_{MIN} to T_{MAX}	±15 V			7.5	mA

All limits are determined to be at least four standard deviations away from mean value. At T_A = 25°C, V_S = ±5 V unless otherwise noted.

Table 2.

			AD825A			
Parameter	**Conditions**	**V_S**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	18	21		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	8	10		MHz
−3 dB Bandwidth	Gain = +1	±5 V	34	37		MHz
Slew Rate	R_{LOAD} = 1 kΩ, G = −1	±5 V	115	130		V/μs
Settling Time to 0.1%	−2.5 V to +2.5 V	±5 V		75	90	ns
to 0.01%	−2.5 V to +2.5 V	±5 V		90	110	ns
Total Harmonic Distortion	F_C = 1 MHz, G = −1	±5 V		−76		dB
Differential Gain Error	NTSC	±5 V		1.2		%
(R_{LOAD} = 150 Ω)	Gain = +2					
Differential Phase Error	NTSC	±5 V		1.4		Degrees
(R_{LOAD} = 150 Ω)	Gain = +2					
INPUT OFFSET VOLTAGE		±5 V		1	2	mV
	T_{MIN} to T_{MAX}				5	mV
Offset Drift				10		μV/°C
INPUT BIAS CURRENT		±5 V		10	30	pA
	T_{MIN}		5			pA
	T_{MAX}				600	pA
INPUT OFFSET CURRENT		±5 V		15	25	pA
	T_{MIN}		5			pA
Offset Current Drift	T_{MAX}				280	pA
OPEN-LOOP GAIN	V_{OUT} = ±2.5	±5 V				
	R_{LOAD} = 500 Ω		64	66		dB
	R_{LOAD} = 150 Ω		64	66		dB
COMMON-MODE REJECTION	V_{CM} = ±2 V	±5 V	69	80		dB
INPUT VOLTAGE NOISE	f = 10 kHz	±5 V		12		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±5 V		10		fA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		± 3.5		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω		+3.2	±3.4		V
	R_{LOAD} = 150 Ω	±5 V	+3.1	±3.2		V
Output Current		±5 V	50			mA
Short-Circuit Current				80		mA
INPUT RESISTANCE				5×10^{11}		Ω
INPUT CAPACITANCE				6		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Quiescent Current		±5 V		6.2	6.8	mA
	T_{MIN} to T_{MAX}	±5 V			7.5	mA
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		76	88		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	
Small Outline (R)	See Figure 6
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	See Figure 6
Storage Temperature Range (R-8, RW-16)	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Specification is for device in free air:
8-lead SOIC package: θ_{JA} = 155°C/W
16-lead SOIC package: θ_{JA} = 85°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

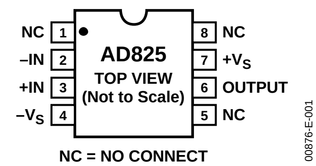


Figure 4. 8-Lead SOIC

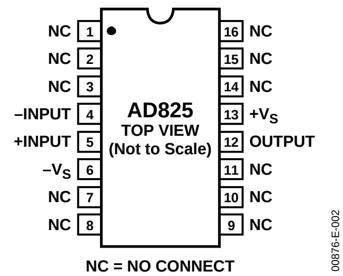


Figure 5. 16-Lead SOIC

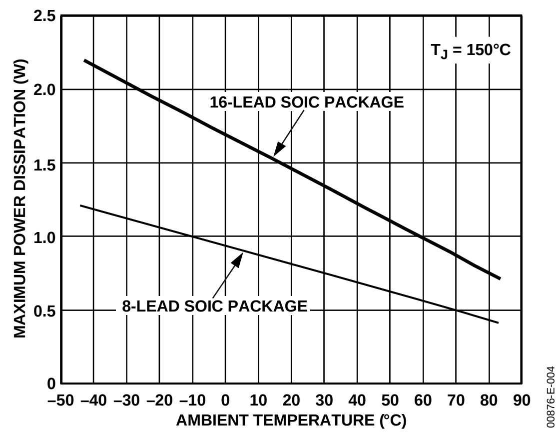
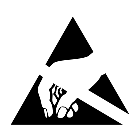


Figure 6. Maximum Power Dissipation vs. Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

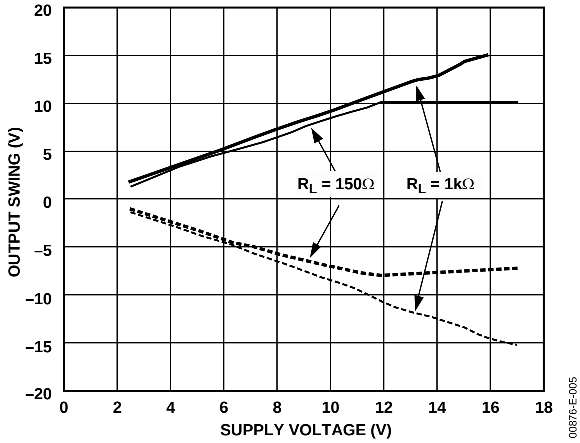


Figure 7. Output Voltage Swing vs. Supply Voltage

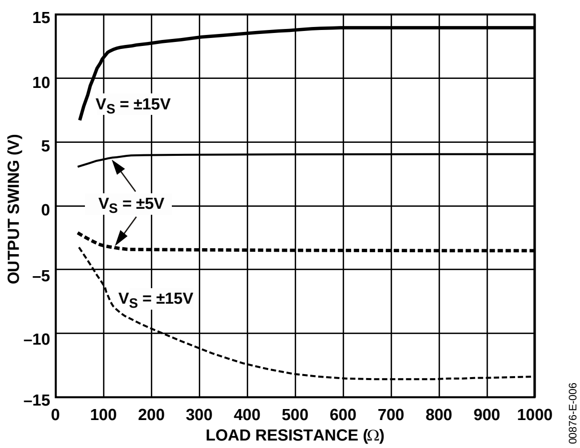


Figure 8. Output Voltage Swing vs. Load Resistance

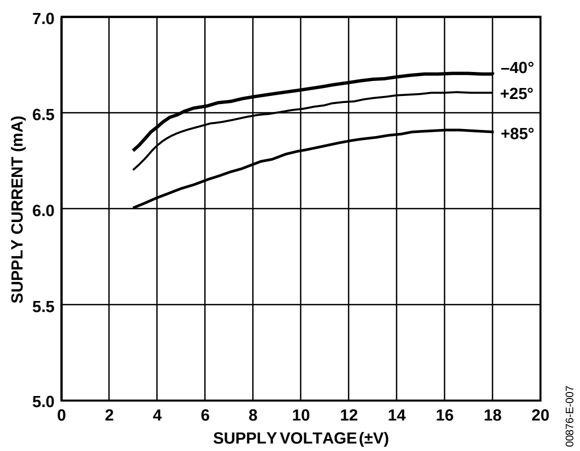


Figure 9. Quiescent Supply Current vs. Supply Voltage for Various Temperatures

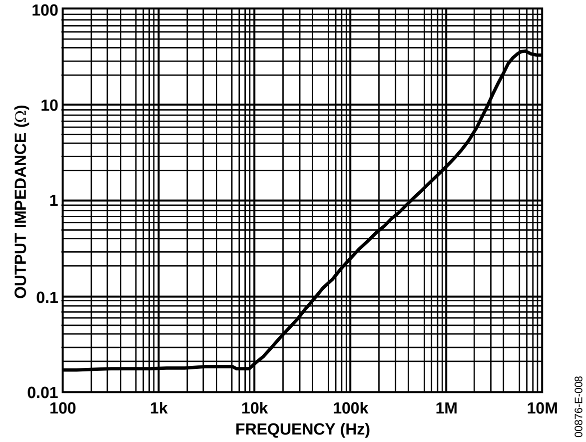


Figure 10. Closed-Loop Output Impedance vs. Frequency

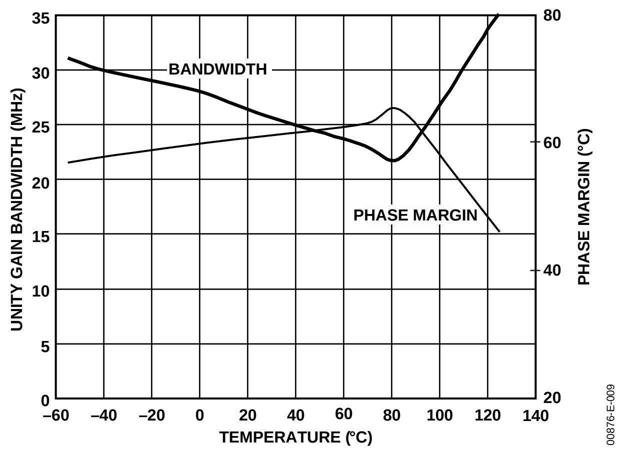


Figure 11. Unity Gain Bandwidth and Phase Margin vs. Temperature

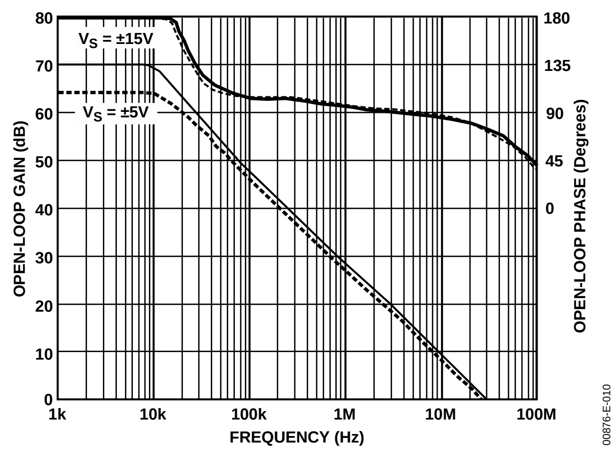


Figure 12. Open-Loop Gain and Phase Margin vs. Frequency

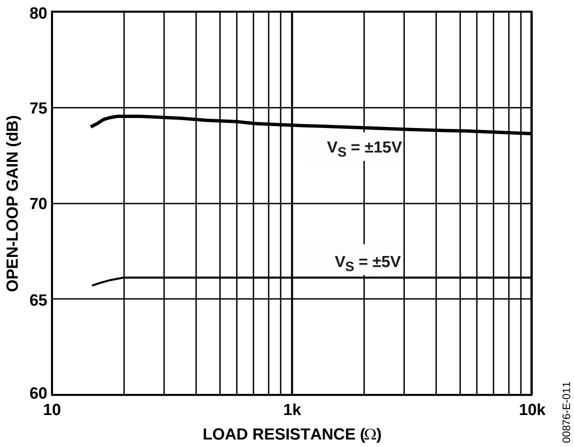


Figure 13. Open-Loop Gain vs. Load Resistance

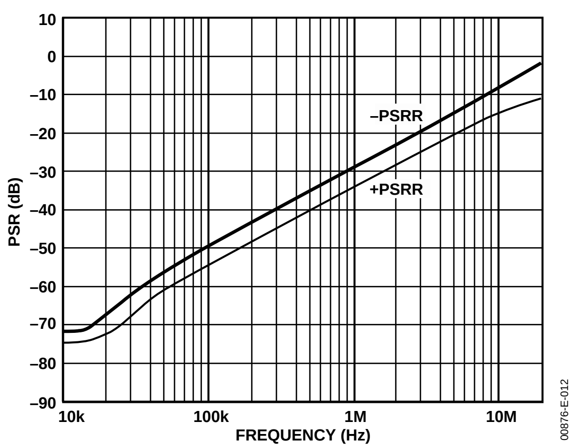


Figure 14. Power Supply Rejection vs. Frequency

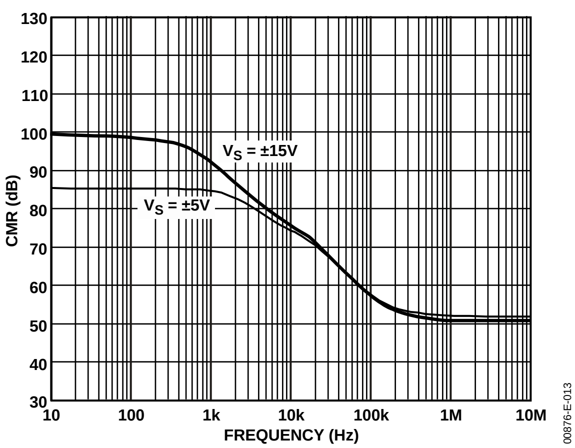


Figure 15. Common-Mode Rejection vs. Frequency

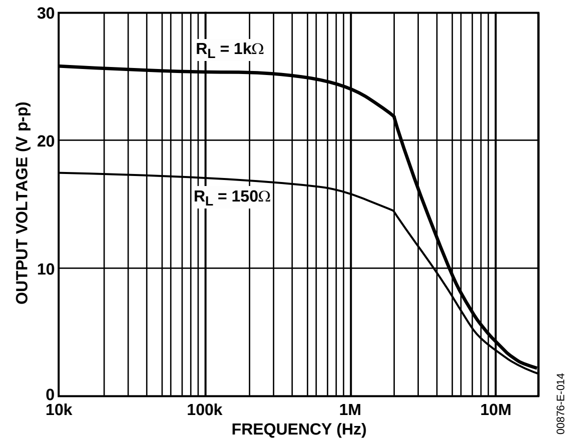


Figure 16. Large Signal Frequency Response; G = +2

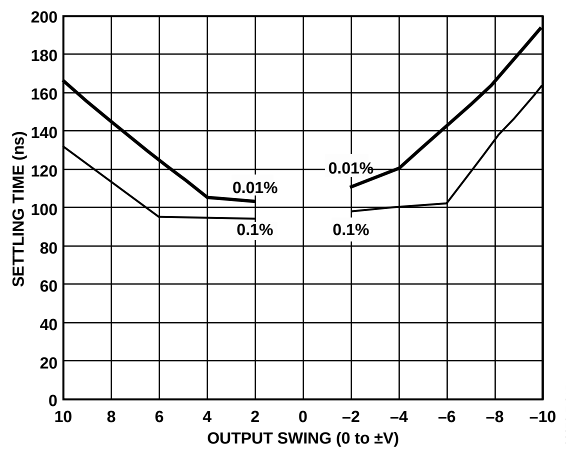


Figure 17. Output Swing and Error vs. Settling Time

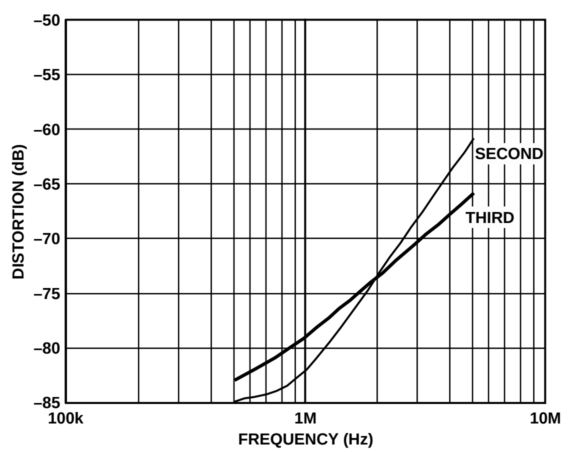


Figure 18. Harmonic Distortion vs. Frequency

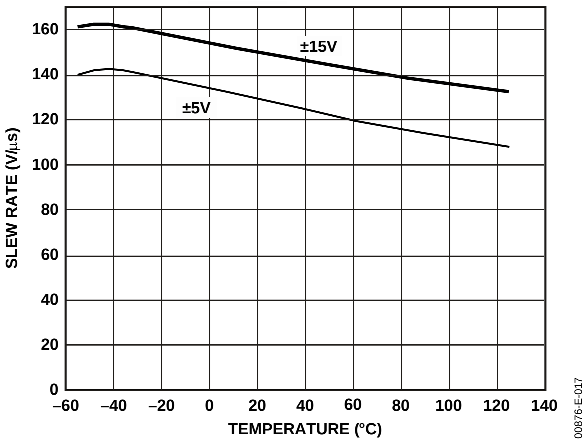


Figure 19. Slew Rate vs. Temperature

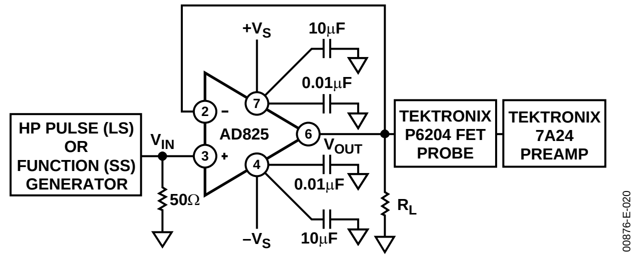


Figure 22. Noninverting Amplifier Connection

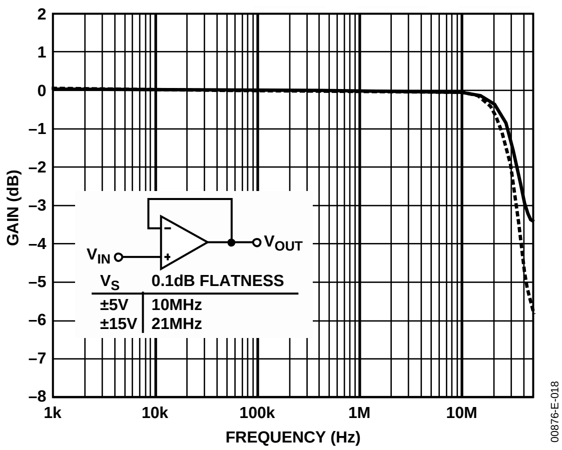


Figure 20. Closed-Loop Gain vs. Frequency, Gain = +1

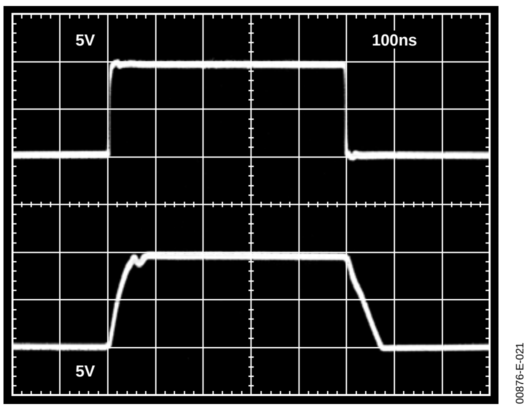


Figure 23. Noninverting Large Signal Pulse Response, R_L = 1 kΩ

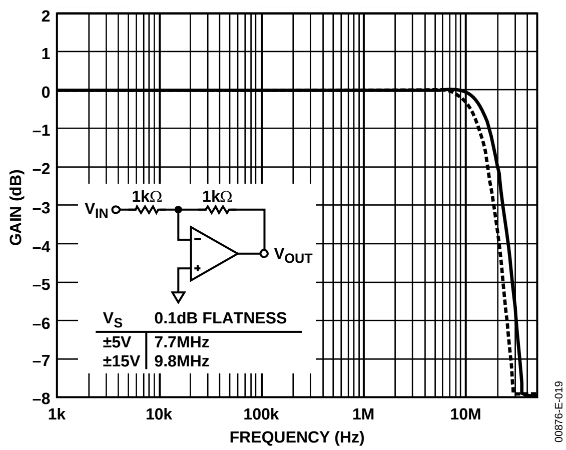


Figure 21. Closed-Loop Gain vs. Frequency, Gain = −1

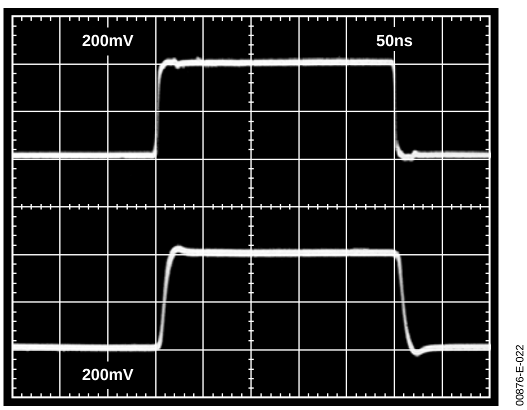


Figure 24. Noninverting Small Signal Pulse Response, R_L = 1 kΩ

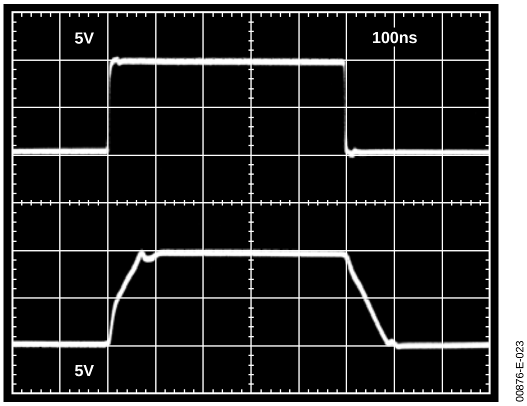


Figure 25. Noninverting Large Signal Pulse Response, $R_L = 150\ \Omega$

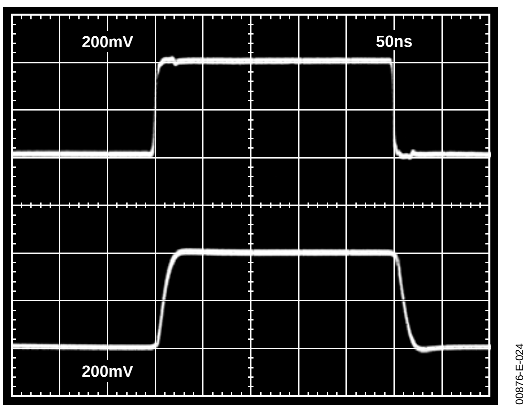


Figure 26. Noninverting Small Signal Pulse Response, $R_L = 150\ \Omega$

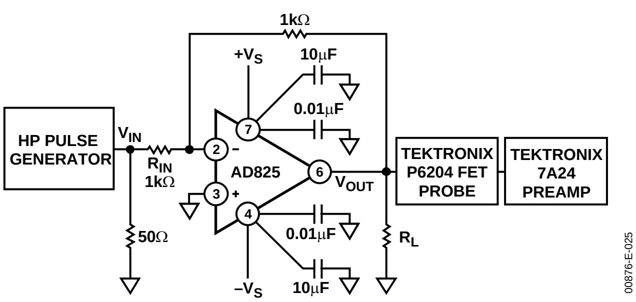


Figure 27. Inverting Amplifier Connection

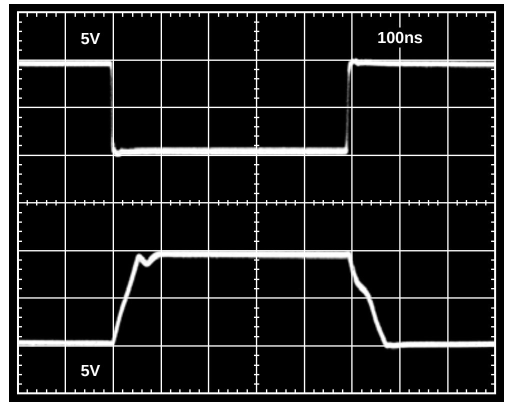


Figure 28. Inverting Large Signal Pulse Response, $R_L = 1\ k\Omega$

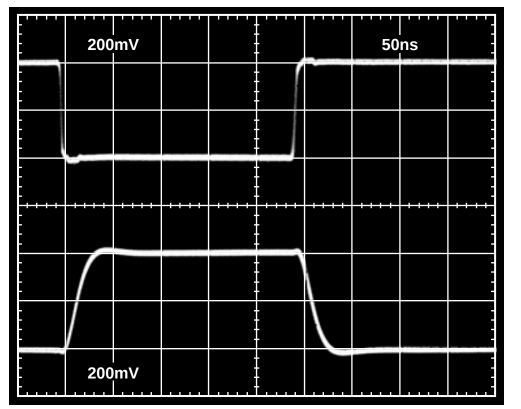


Figure 29. Inverting Small Signal Pulse Response, $R_L = 1\ k\Omega$

DRIVING CAPACITIVE LOADS

The internal compensation of the AD825, together with its high output current drive, permits excellent large signal performance while driving extremely high capacitive loads.

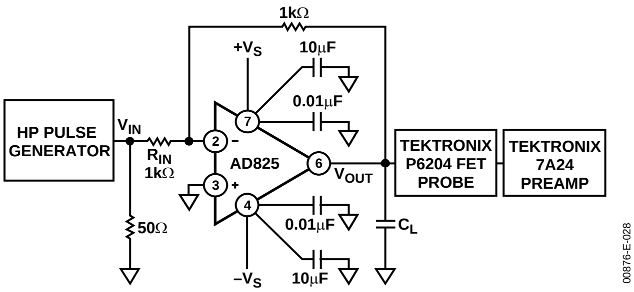


Figure 30. Inverting Amplifier Driving a Capacitive Load

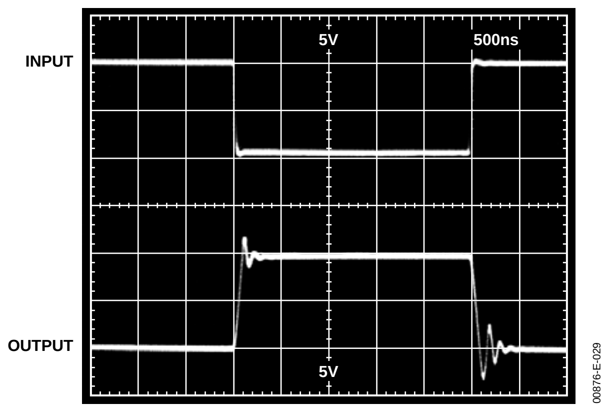


Figure 31. Inverting Amplifier Pulse Response While Driving a 400 pF Capacitive Load

THEORY OF OPERATION

The AD825 is a low cost, wideband, high performance FET input operational amplifier. With its unique input stage design, the AD825 ensures no phase reversal, even for inputs that exceed the power supply voltages, and its output stage is designed to drive heavy capacitive or resistive loads with small changes relative to no load conditions.

The AD825 (Figure 32) consists of common-drain, common-base FET input stage driving a cascoded, common-base matched NPN gain stage. The output buffer stage uses emitter followers in a Class AB amplifier that can deliver large current to the load while maintaining low levels of distortion.

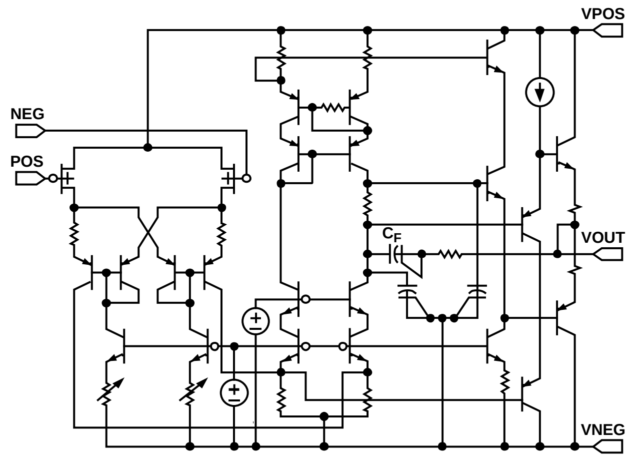


Figure 32. Simplified Schematic

The capacitor, C_F, in the output stage, enables the AD825 to drive heavy capacitive loads. For light loads, the gain of the output buffer is close to unity, C_F is bootstrapped, and not much happens. As the capacitive load is increased, the gain of the output buffer is decreased and the bandwidth of the amplifier is reduced through a portion of C_F adding to the dominant pole. As the capacitive load is further increased, the amplifier's bandwidth continues to drop, maintaining the stability of the AD825.

INPUT CONSIDERATION

The AD825 with its unique input stage ensures no phase reversal for signals as large as or even larger than the supply voltages. Also, layout considerations of the input transistors ensure functionality even with a large differential signal.

The need for a low noise input stage calls for a larger FET transistor. One should consider the additional capacitance that is added to ensure stability. When filters are designed with the AD825, one needs to consider the input capacitance (5 pF to 6 pF) of the AD825 as part of the passive network.

GROUNDING AND BYPASSING

The AD825 is a low input bias current FET amplifier. Its high frequency response makes it useful in applications, such as photodiode interfaces, filters, and audio circuits. When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnects, and resistances should have low inductive paths to ground. Power supply leads should be bypassed to common as close as possible to the amplifier pins. Ceramic capacitors of 0.1 µF are recommended.

SECOND-ORDER LOW-PASS FILTER

A second-order Butterworth low-pass filter can be implemented using the AD825 as shown in Figure 33. The extremely low bias currents of the AD825 allow the use of large resistor values and, consequently, small capacitor values without concern for developing large offset errors. Low current noise is another factor in permitting the use of large resistors without having to worry about the resultant voltage noise.

With the values shown, the corner frequency will be 1 MHz. The equations for component selection are shown below. Note that the noninverting input (and the inverting input) has an input capacitance of 6 pF. As a result, the calculated value of C1 (12 pF) is reduced to 6 pF.

$$C1 = \frac{1.414}{2\pi\, f_{CUTOFF} R1}$$

$$C2\,(farads) = \frac{0.707}{2\pi\, f_{CUTOFF} R1}$$

$$R1 = R2 = User\ Selected\ (Typically\ 10\ \text{k}\Omega\ to\ 100\ \text{k}\Omega)$$

A plot of the filter frequency response is shown in Figure 34; better than 40 dB of high frequency rejection is provided.

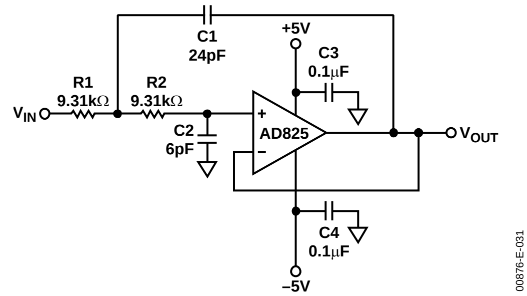


Figure 33. Second-Order Butterworth Low-Pass Filter

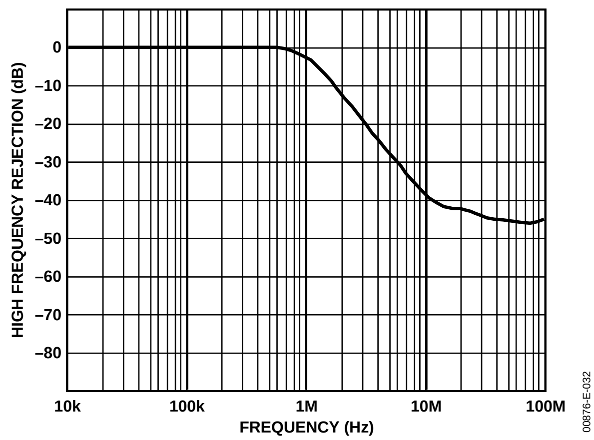


Figure 34. Frequency Response of Second-Order Butterworth Filter

OUTLINE DIMENSIONS

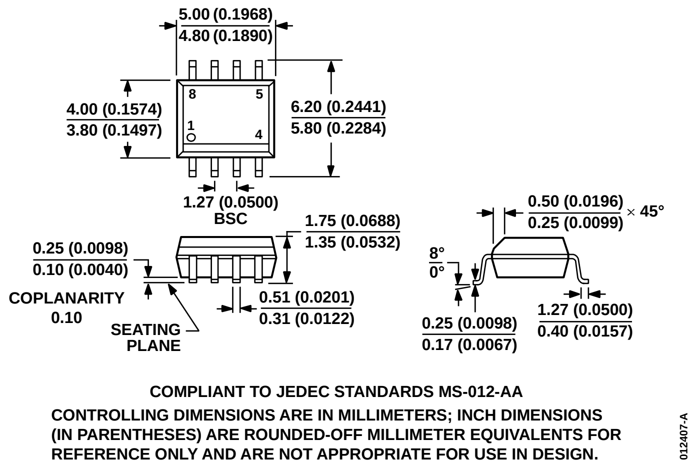


Figure 35. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body (R-8)
Dimensions shown in millimeters (inches)

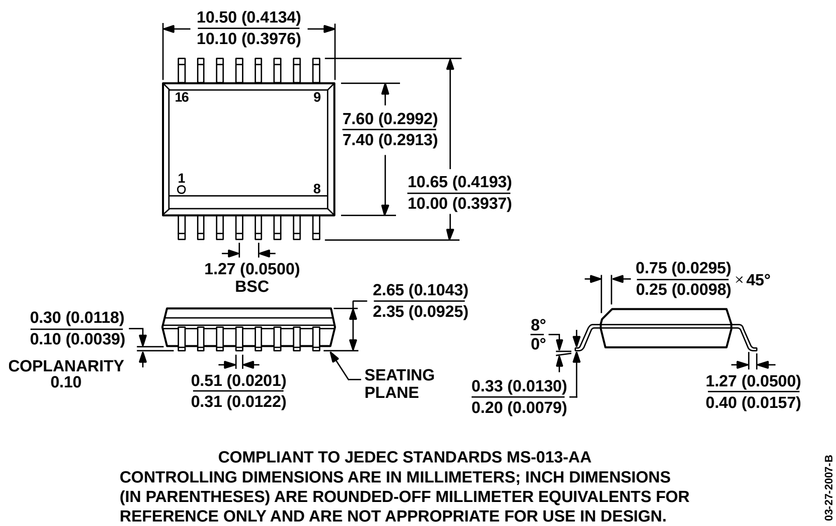


Figure 36. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD825ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD825ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD825ARZ-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD825ARZ-16	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD825ARZ-16-REEL	−40°C to +85°C	16-Lead SOIC_W, 13" Tape and Reel	RW-16
AD825ARZ-16-REEL7	−40°C to +85°C	16-Lead SOIC_W, 7" Tape and Reel	RW-16
AD825AR-EBZ		Evaluation Board	
AD825ACHIPS		Die	

[1] Z = RoHS Compliant Part.

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