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REVISION HISTORY

3/14—Rev. A to Rev. B

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8/10—Rev. 0 to Rev. A

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Updated Outline Dimensions ... 22

5/07—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5V, V_{OCM} = 0 V (AD8146); SYNC LEVEL = 0 V (AD8147/AD8148); T = 25°C; $R_{L, dm}$ = 200 Ω, unless otherwise noted.
T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT AC					
Dynamic Performance					
−3 dB Small Signal Bandwidth	V_O = 0.2 V p-p,				
	AD8146/AD8148		900		MHz
	AD8147		780		MHz
−3 dB Large Signal Bandwidth	V_O = 2 V p-p,				
	AD8146/AD8148		700		MHz
	AD8147		600		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p,				
	AD8146/AD8147		200		MHz
	AD8148		235		MHz
Slew Rate	V_O = 2 V p-p, 25% to 75%		3000		V/µs
Isolation Between Amplifiers	f = 10 MHz				
	AD8146/AD8147		−86		dB
	AD8148		−80		dB
DIFFERENTIAL INPUT DC					
Input Common-Mode Voltage Range			−5 to +5		V
Input Resistance	Differential		1.0		kΩ
	Single-ended input				
	AD8146/AD8147		750		Ω
	AD8148		833		Ω
Input Capacitance	Differential		2		pF
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V				
	AD8146/AD8147/AD8148			−53/−49/−55	dB
DIFFERENTIAL OUTPUT					
Differential Signal Gain	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$; $\Delta V_{IN, dm}$ = ±1 V				
	AD8146/AD8147	1.94		2.00	V/V
	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$; $\Delta V_{IN, dm}$ = ±1 V				
	AD8148	3.8		4.0	V/V
Output Voltage Swing	Each single-ended output				
	AD8146/AD8147/AD8148	−3/−2.25/−3.42		+3.4/+3.4/+3.5	V
Output Offset Voltage		−19		+19	mV
Output Offset Drift	T_{MIN} to T_{MAX}		±8		µV/°C
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{IN, dm}$, $\Delta V_{OUT, dm}$ = 2 V p-p				
	f = 50 MHz				
	AD8146/AD8147		−52		dB
	AD8148		−49		dB
	DC				
	AD8146/AD8148			−41	dB
	AD8147			−44	dB
Output Voltage Noise (RTO)	f = 1 MHz				
	AD8146/AD8147		25		nV/√Hz
	AD8148		42		nV/√Hz
Output Short-Circuit Current	Short to GND, source/sink		+87/−67		mA

Parameter	Conditions	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE (AD8146 ONLY)					
−3 dB Bandwidth	ΔV_{OCM} = 100 mV p-p		340		MHz
Slew Rate	V_{OCM} = −1 V to +1 V, 25% to 75%		800		V/µs
DC Gain	ΔV_{OCM} = ±1 V	0.98		1.00	V/V
V_{OCM} INPUT CHARACTERISTICS (AD8146 ONLY)					
Input Voltage Range			±3		V
Input Resistance			12.5		kΩ
Input Offset Voltage		−36		+36	mV
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V		−48		dB
SYNC DYNAMIC PERFORMANCE (AD8147/AD8148 ONLY)					
Slew Rate	$V_{OUT, cm}$ = −1 V to +1 V; 25% to 75%		1000		V/µs
H_{SYNC} AND V_{SYNC} INPUTS (AD8147/AD8148 ONLY)					
Low-to-High Threshold			1.5 to1.7		V
High-to-Low Threshold			1.5 to1.7		V
SYNC LEVEL INPUT (AD8147/AD8148 ONLY)					
Setting to 0.5 V Pulse Levels			0.5		V
Gain to Red Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$, AD8147/AD8148	0.93/0.96		1.10/1.05	V/V
Gain to Green Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$, AD8147/AD8148	1.91/1.93		2.15/2.08	V/V
Gain to Blue Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$, AD8147/AD8148	−1.10/−1.05		−0.93/−0.96	V/V
POWER SUPPLY					
Operating Range		+4.5		±5.5	V
Quiescent Current, Positive Supply	AD8146/AD8147/AD8148			58/61.5/62.5	mA
	Disabled				
	AD8146			6	mA
	AD8147/AD8148			21.5	mA
Quiescent Current, Negative Supply	AD8146/AD8147/AD8148	−58/−60.5/−62			mA
	Disabled	−37			mA
PSRR	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V				
	AD8146/AD8147/AD8148			−66/−52/−55	dB
OUTPUT PULL-DOWN					
OPD Input Low Voltage			1.1		V
OPD Input High Voltage			2.1		V
OPD Input Bias Current				520	µA
OPD Assert Time			1		µs
OPD Deassert Time			10		ns
Output Voltage When OPD Asserted	Each output, OPD input @ V_S+			−3.8	V

V_S = +5 V or ±2.5 V; V_{OCM} = midsupply (AD8146); SYNC LEVEL = 0 V (AD8147/AD8148); T = 25°C; $R_{L,dm}$ = 200 Ω, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT AC					
Dynamic Performance					
−3 dB Small Signal Bandwidth	V_O = 0.2 V p-p,				
	AD8146		870		MHz
	AD8147/AD8148		680		MHz
−3 dB Large Signal Bandwidth	V_O = 2 V p-p,				
	AD8147		590		MHz
	AD8146/AD8148		620		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p,				
	AD8146/AD8147		165		MHz
	AD8148		200		MHz
DIFFERENTIAL INPUT DC					
Input Common-Mode Voltage Range			0 to 5		V
Input Resistance	Differential		1.0		kΩ
	Single-ended input				
	AD8146/AD8147		750		Ω
	AD8148		833		Ω
Input Capacitance	Differential		2		pF
DC CMRR	$\Delta V_{OUT,dm}/\Delta V_{IN,cm}$; $\Delta V_{IN,cm}$ = ±1 V,				
	AD8146/AD8147/AD8148			−49/−45/−49	dB
DIFFERENTIAL OUTPUT					
Differential Signal Gain	$\Delta V_{OUT,dm}/\Delta V_{IN,dm}$; $\Delta V_{IN,dm}$ = ±1 V,				
	AD8146/AD8147	1.94		2.00	V/V
	$\Delta V_{OUT,dm}/\Delta V_{IN,dm}$; $\Delta V_{IN,dm}$ = ±1 V				
	AD8148	3.80		4.00	V/V
Output Voltage Swing	Each single-ended output, V_S = ±2.5 V	−1.17		+1.24	V
Output Offset Voltage		−17		+17	mV
Output Offset Drift	T_{MIN} to T_{MAX}		±8		µV/°C
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{IN,dm}$, $\Delta V_{OUT,dm}$ = 2 V p-p,				
	f = 50 MHz		−53		dB
	AD8146/AD8147		−49		dB
	AD8148				
	DC				
	AD8146/AD8148			−41	dB
	AD8147			−44	dB
Output Voltage Noise (RTO)	f = 1 MHz				
	AD8146/AD8147		25		nV/√Hz
	AD8148		42		nV/√Hz
Output Short-Circuit Current	Short to GND, source/sink		+63/−48		mA
V_{OCM} DYNAMIC PERFORMANCE (AD8146 ONLY)					
−3 dB Bandwidth	ΔV_{OCM} = 100 mV p-p		310		MHz
Slew Rate	V_{OCM} = −1 V to +1 V, 25% to 75%		800		V/µs
DC Gain	ΔV_{OCM} = ±1 V	0.98		1.00	V/V

Parameter	Conditions	Min	Typ	Max	Unit
V_{OCM} INPUT CHARACTERISTICS (AD8146 ONLY)					
Input Voltage Range			±1.2		V
Input Resistance			12.5		kΩ
Input Offset Voltage		−36		+36	mV
DC CMRR	$\Delta V_{O, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−42		dB
SYNC DYNAMIC PERFORMANCE (AD8147/ AD8148 ONLY)					
Slew Rate	$V_{OUT, cm}$ = −1 V to +1 V; 25% to 75%		800		V/µs
H_{SYNC} AND V_{SYNC} INPUTS (AD8147/AD8148 ONLY)					
Low-to-High Threshold			1.3 to 1.5		V
High-to-Low Threshold			1.3 to 1.5		V
SYNC LEVEL INPUT (AD8147/AD8148 ONLY)					
Setting to 0.5 V Pulse Levels			0.5		V
Gain to Red Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC LEVEL}$, AD8147/AD8148	0.88/0.92		1.07/1.04	V/V
Gain to Green Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC LEVEL}$, AD8147/AD8148	1.83/1.85		2.08/2.00	V/V
Gain to Blue Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC LEVEL}$, AD8147/AD8148	−1.07/−1.04		−0.88/−0.92	V/V
POWER SUPPLY					
Operating Range		+4.5		±5.5	V
Quiescent Current Positive Supply	AD8146/AD8147/AD8148			50/55.5/ 54	mA
	Disable				
	AD8146			4	mA
	AD8147/AD8148			12	mA
Quiescent Current Negative Supply	AD8146/AD8147/AD8148	−50/−55/−53			mA
	Disabled				
	AD8146/AD8147/ AD8148	−14/−18.2/−15			mA
PSRR	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V,				
	AD8146/AD8147/AD8148			−70/−52/-60	dB
OUTPUT PULL-DOWN					
OPD Input Low Voltage			1.0		V
OPD Input High Voltage			2.0		V
OPD Input Bias Current				160	µA
OPD Assert Time			600		ns
OPD Deassert Time			10		ns
Output Voltage When OPD Asserted	Each output, OPD input @ V_S+			−1.6	V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	11 V
All V_{OCM}	$\pm V_S$
Power Dissipation	See Figure 3
Input Common-Mode Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 4. Thermal Resistance with the Underside Pad Connected to the Plane

Package Type/PCB Type	θ_{JA}	Unit
24-Lead LFCSP_WQ/4-Layer	57	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8146/AD8147/AD8148 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8146/AD8147/AD8148. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of differential and common-mode currents flowing to the loads, as well as currents flowing through the internal differential and common-mode feedback loops. The internal resistor tap used in the common-mode feedback loop places a 4 kΩ differential load on the output. Differential feedback, network resistor values are given in the Theory of Operation section and Applications section. RMS output voltages should be considered when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a ground plane to achieve the specified θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 24-lead LFCSP (57°C/W) package on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a ground plane. θ_{JA} values are approximations.

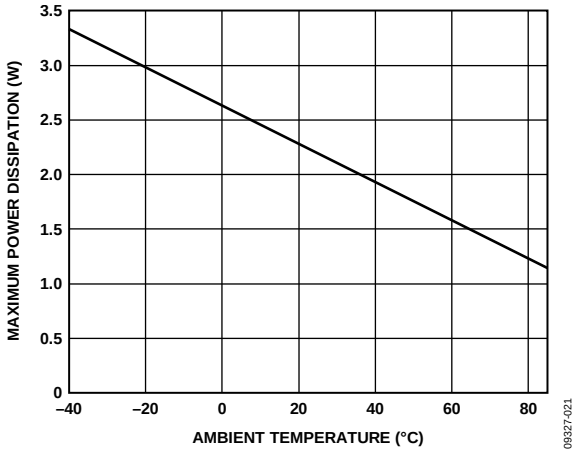
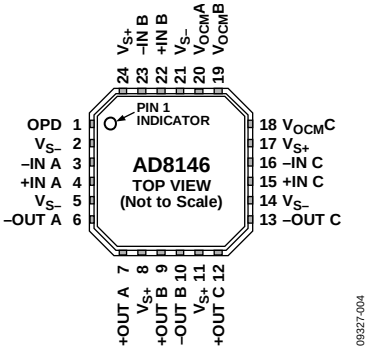


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

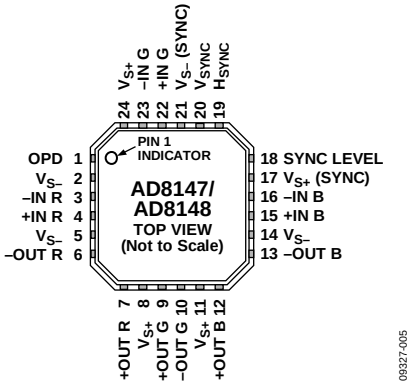


NOTES
1. THE EXPOSED PADDLE ON THE UNDERSIDE OF THE CHIP MUST BE CONNECTED TO A GROUND PLANE.

Figure 4. AD8146 Pin Configuration

Table 5. AD8146 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OPD	Output Pull-Down.
2, 5, 14, 21	V_{S-}	Negative Power Supply Voltage.
3	−IN A	Inverting Input, Amplifier A.
4	+IN A	Noninverting Input, Amplifier A.
6	−OUT A	Negative Output, Amplifier A.
7	+OUT A	Positive Output, Amplifier A.
8, 11, 17, 24	V_{S+}	Positive Power Supply Voltage.
9	+OUT B	Positive Output, Amplifier B.
10	−OUT B	Negative Output, Amplifier B.
12	+OUT C	Positive Output, Amplifier C.
13	−OUT C	Negative Output, Amplifier C.
15	+IN C	Noninverting Input, Amplifier C.
16	−IN C	Inverting Input, Amplifier C.
18	$V_{OCM}C$	The voltage applied to this pin controls output common-mode voltage, Amplifier C.
19	$V_{OCM}B$	The voltage applied to this pin controls output common-mode voltage, Amplifier B.
20	$V_{OCM}A$	The voltage applied to this pin controls output common-mode voltage, Amplifier A.
22	+IN B	Noninverting Input, Amplifier B.
23	−IN B	Inverting Input, Amplifier B.
Exposed Paddle	GND	Signal Ground Reference.



NOTES
1. THE EXPOSED PADDLE ON THE UNDERSIDE OF THE CHIP MUST BE CONNECTED TO A GROUND PLANE.

Figure 5. AD8147/AD8148 Pin Configuration

Table 6. AD8147/AD8148 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OPD	Output Pull-Down.
2, 5, 14	V_{S-}	Negative Power Supply Voltage.
3	−IN R	Inverting Input, Red Amplifier.
4	+IN R	Noninverting Input, Red Amplifier.
6	−OUT R	Negative Output, Red Amplifier.
7	+OUT R	Positive Output, Red Amplifier.
8, 11, 24	V_{S+}	Positive Power Supply Voltage.
9	+OUT G	Positive Output, Green Amplifier.
10	−OUT G	Negative Output, Green Amplifier.
12	+OUT B	Positive Output, Blue Amplifier.
13	−OUT B	Negative Output, Blue Amplifier.
15	+IN B	Noninverting Input, Blue Amplifier.
16	−IN B	Inverting Input, Blue Amplifier.
17	V_{S+} (SYNC)	Positive Power Supply Voltage for Sync.
18	SYNC LEVEL	The voltage applied to this pin controls the amplitude of the sync pulses that are applied to the common-mode voltages.
19	H_{SYNC}	Horizontal Sync Pulse Input.
20	V_{SYNC}	Vertical Sync Pulse Input.
21	V_{S-} (SYNC)	Negative Power Supply Voltage for Sync.
22	+IN G	Noninverting Input, Green Amplifier.
23	−IN G	Inverting Input, Green Amplifier.
Exposed Paddle	GND	Signal Ground Reference.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5V; V_{OCM} = 0 V (AD8146); SYNC LEVEL = 0 V (AD8147/AD8148); T = 25°C; $R_{L, dm}$ = 200 Ω; $C_{L, dm}$ = 0 pF, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +85°C.

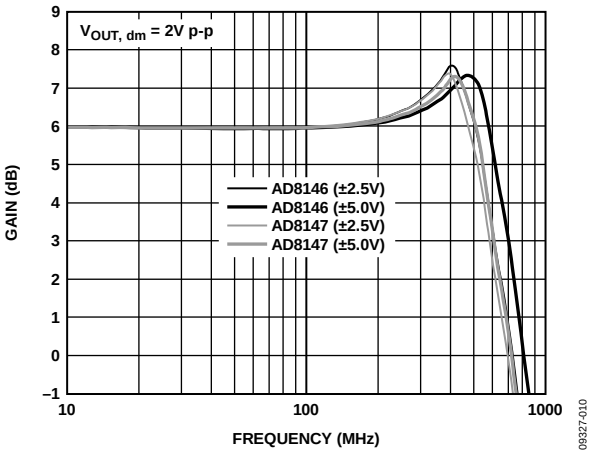


Figure 6. AD8146/AD8147 Large Signal Frequency Response for Various Supplies

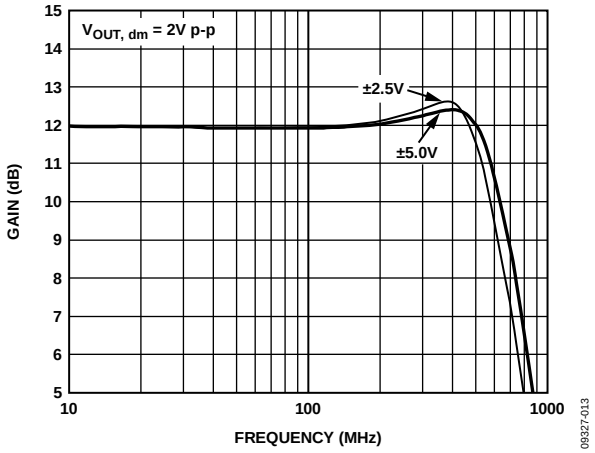


Figure 9. AD8148 Large Signal Frequency Response for Various Supplies

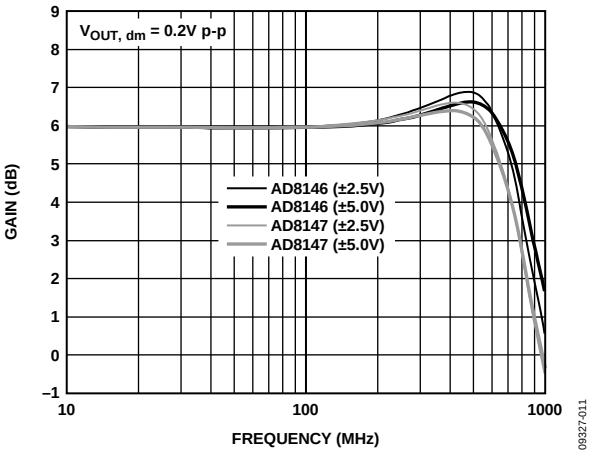


Figure 7. AD8146/AD8147 Small Signal Frequency Response for Various Supplies

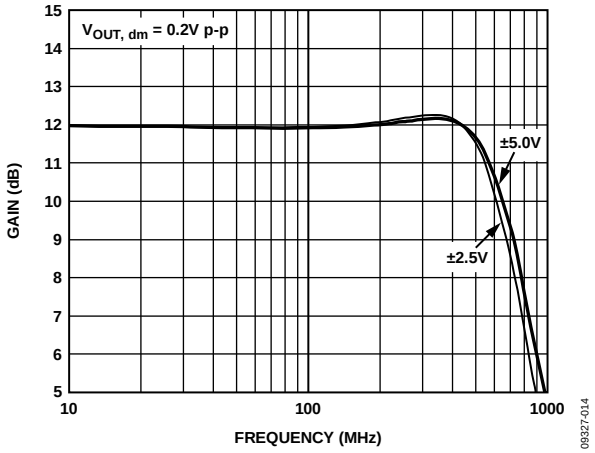


Figure 10. AD8148 Small Signal Frequency Response for Various Supplies

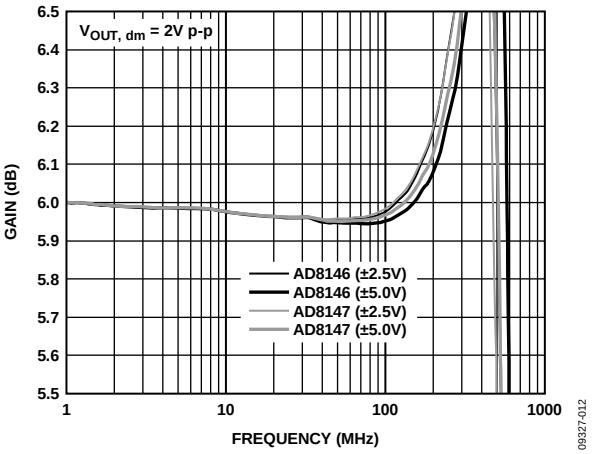


Figure 8. AD8146/AD8147 Large Signal 0.1 dB Flatness for Various Supplies

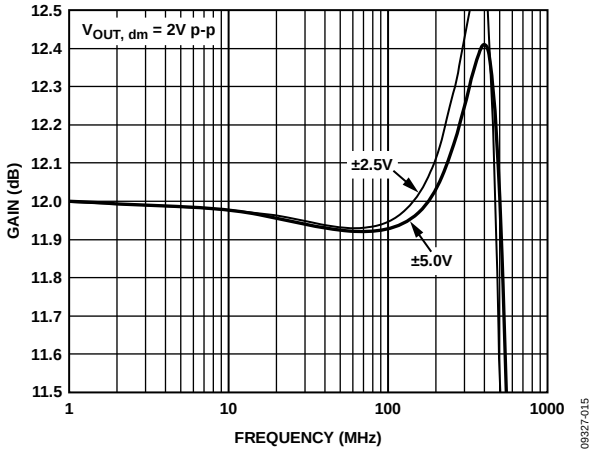


Figure 11. AD8148 Large Signal 0.1 dB Flatness for Various Supplies

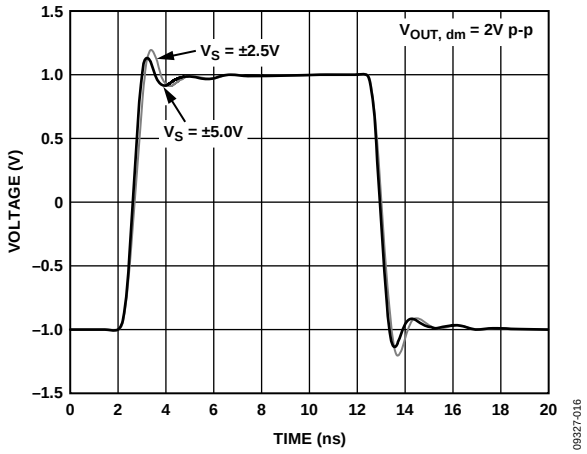


Figure 12. AD8146/AD8147 Large Signal Transient Response for Various Supplies

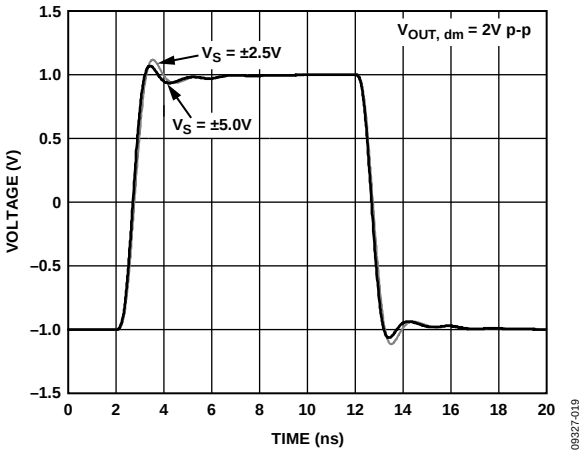


Figure 15. AD8148 Large Signal Transient Response for Various Supplies

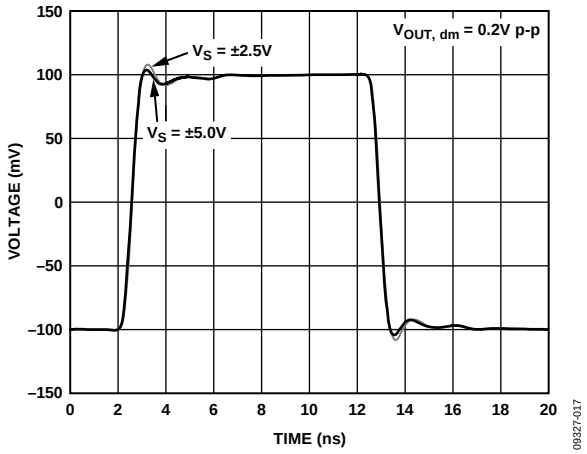


Figure 13. AD8146/AD8147 Small Signal Transient Response for Various Supplies

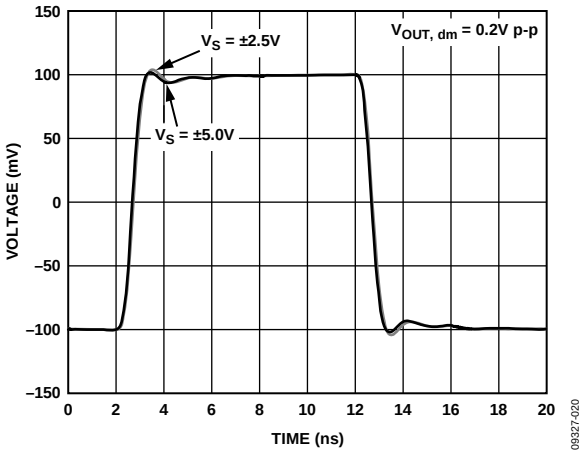


Figure 16. AD8148 Small Signal Transient Response for Various Supplies

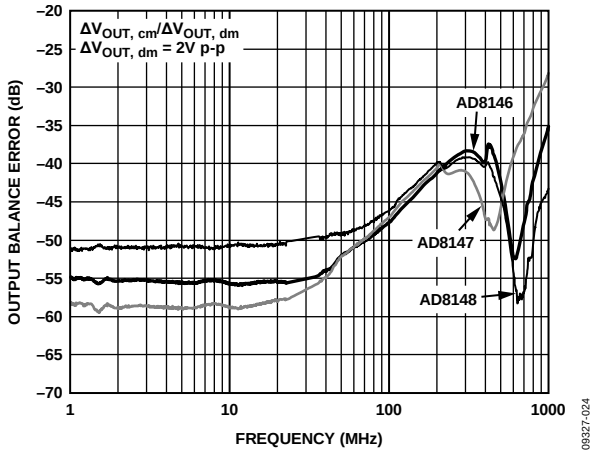


Figure 14. Output Balance vs. Frequency

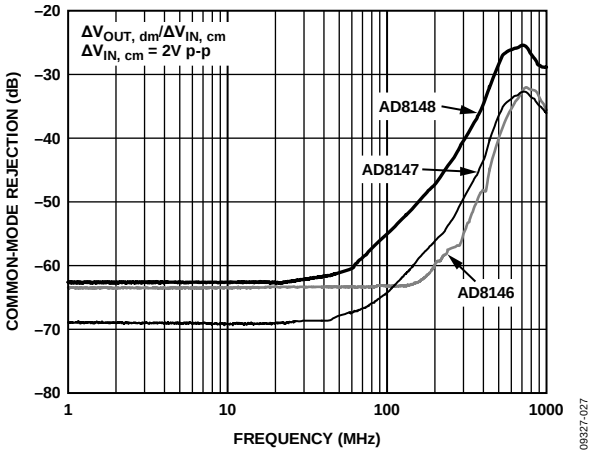


Figure 17. CMRR vs. Frequency

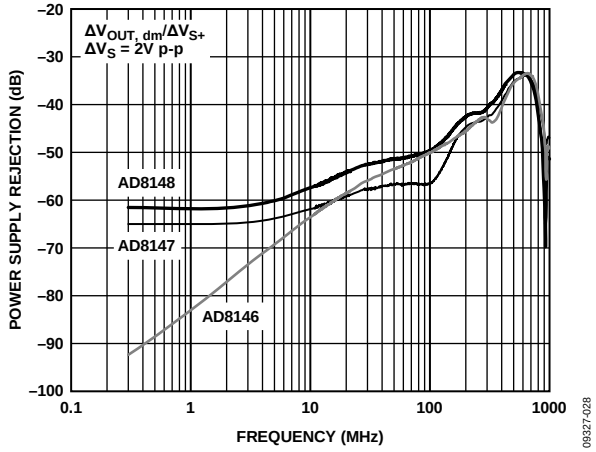


Figure 18. Positive Power Supply Rejection vs. Frequency

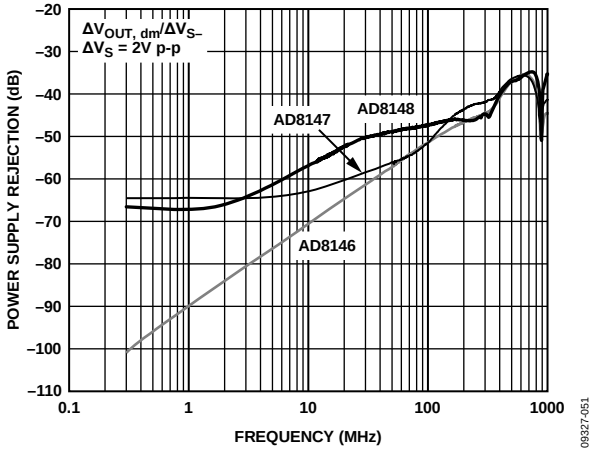


Figure 21. Negative Power Supply Rejection vs. Frequency

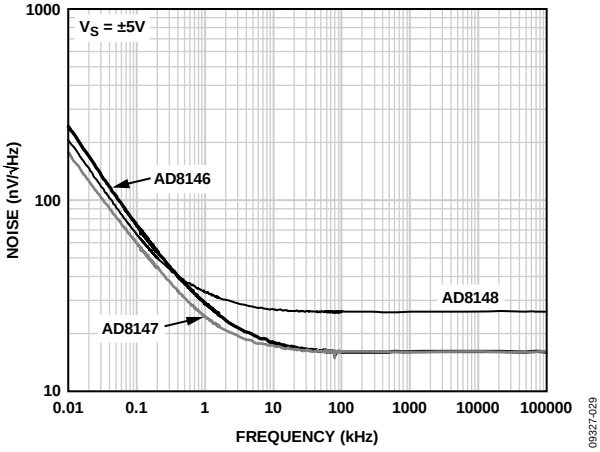


Figure 19. Output-Referred Voltage Noise vs. Frequency

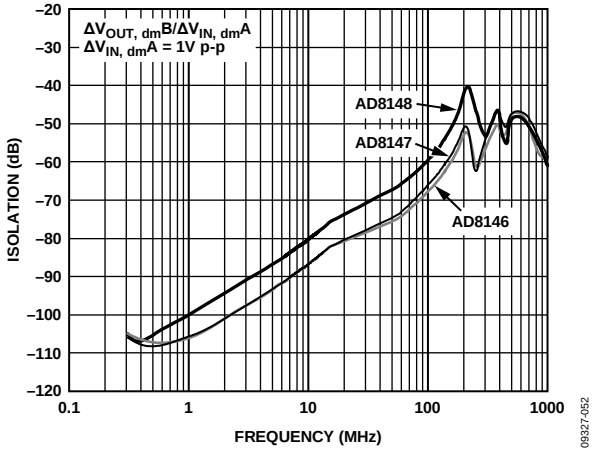


Figure 22. Amplifier-to-Amplifier Isolation vs. Frequency

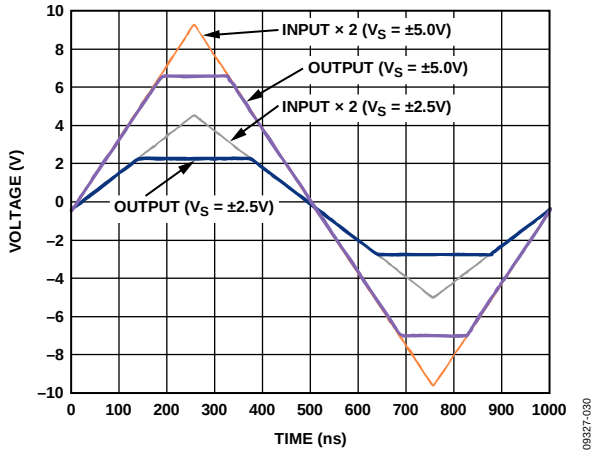


Figure 20. AD8146/AD8147 Output Overdrive Recovery

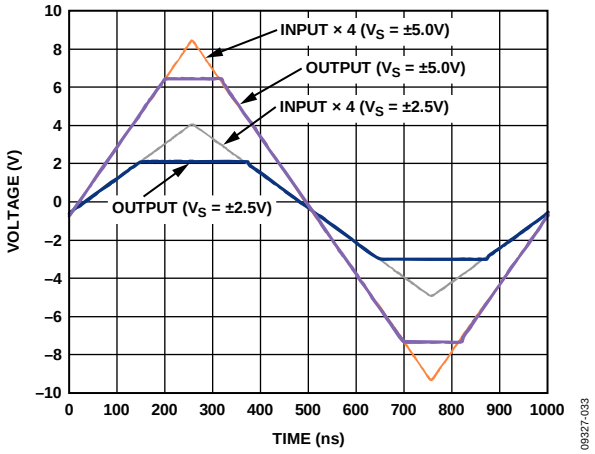


Figure 23. AD8148 Output Overdrive Recovery

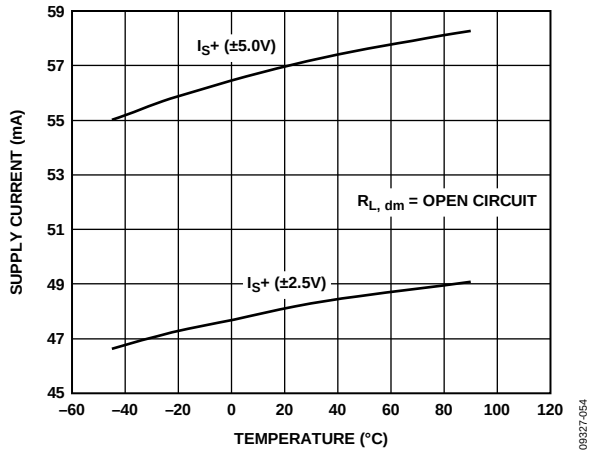


Figure 24. AD8146 Supply Current vs. Temperature

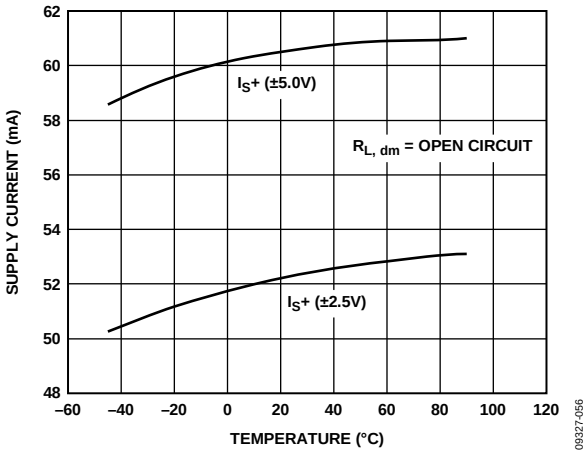


Figure 26. AD8147/AD8148 Supply Current vs. Temperature

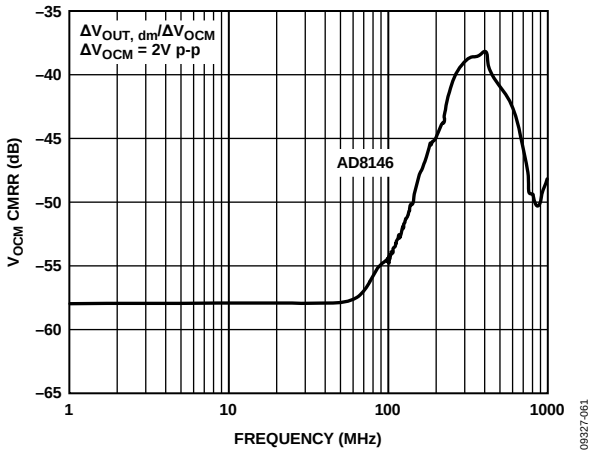


Figure 25. V_{OCM} Common-Mode Rejection Ratio

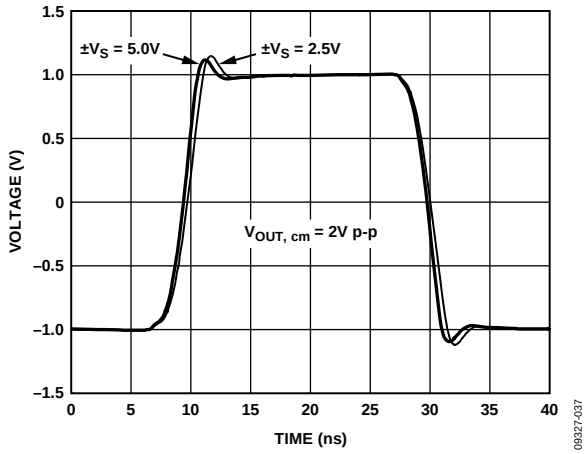


Figure 27. AD8146 Large Signal V_{OCM} Transient Response for Various Supplies

THEORY OF OPERATION

Each differential driver differs from a conventional op amp in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The drivers make it easy to perform single-ended-to-differential conversion, common-mode level shifting, and amplification of differential signals.

Previous differential drivers, both discrete and integrated designs, were based on using two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level shifting has also been difficult with previous differential drivers. Level shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes, the third amplifier was also used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

Each of the drivers uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set by the internal resistors, controls only the differential output voltage. The internal common-mode feedback loop controls only the common-mode output voltage. This architecture makes it easy to transmit signals over the common-mode voltage channels by simply applying the signal voltages to the V_{OCM} inputs. The output common-mode voltage is forced, by internal common-mode feedback, to equal the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The driver architecture results in outputs that are highly balanced over a wide frequency range without requiring external components or adjustments. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude that are exactly 180° apart in phase.

DEFINITION OF TERMS

Differential Voltage

Differential voltage refers to the difference between two node voltages that are balanced with respect to each other. For example, in Figure 28 the output differential voltage (or equivalently output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{OP} - V_{ON})$$

Common-Mode Voltage

Common-mode voltage refers to the average of two node voltages with respect to a common reference. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{OP} + V_{ON})/2$$

Output Balance

Output balance is a measure of how well the differential output signals are matched in amplitude and how close they are to exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential output voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal. By this definition, output balance error is the magnitude of the change in output common-mode voltage divided by the magnitude of the change in output differential mode voltage in response to a differential input signal.

$$Output\ Balance\ Error = \left| \frac{\Delta V_{OUT,\,cm}}{\Delta V_{OUT,\,dm}} \right|$$

ANALYZING AN APPLICATION CIRCUIT

The drivers use high open-loop gain and negative feedback to force their differential and common-mode output voltages to minimize the differential and common-mode input error voltages. The differential input error voltage is defined as the voltage between the differential inputs labeled V_{AP} and V_{AN} in Figure 28. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

CLOSED-LOOP GAIN

The differential mode gain of the circuit in Figure 28 can be described by

$$\left| \frac{V_{OUT,\,dm}}{V_{IN,\,dm}} \right| = \frac{R_F}{R_G}$$

where:

R_F is 1.0 kΩ and R_G is 500 Ω nominally for the AD8146 and AD8147.

R_F is 2.0 kΩ and R_G is 500 Ω nominally for the AD8148.

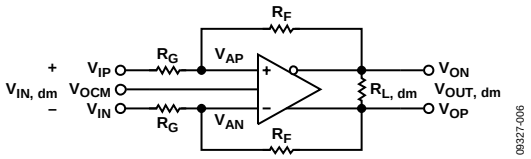


Figure 28. Internal Architecture and Signal Name Definitions

CALCULATING THE INPUT IMPEDANCE

The effective input impedance of a circuit such as that in Figure 28 at V_{IP} and V_{IN} depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the differential input impedance, $R_{IN, dm}$, between the inputs V_{IP} and V_{IN} for all devices is

$$R_{IN,\,dm} = 2 \times R_G$$

In the case of a single-ended input signal (for example, if V_{IN} is grounded and the input signal is applied to V_{IP}), the input impedance becomes

$$R_{IN,\,dm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

The single-ended input impedance of the AD8146 and the AD8147 is therefore 750 Ω, and the single-ended input impedance of the AD8148 is 833 Ω.

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The driver inputs are designed to facilitate level-shifting of ground-referenced input signals on a single power supply. For a single-ended input, this implies, for example, that the voltage at V_{IN} in Figure 28 would be 0 V when the negative power supply voltage of the amplifier is also set to 0 V.

It is important to ensure that the common-mode voltage at the amplifier inputs, V_{AP} and V_{AN}, stays within its specified range. Because voltages V_{AP} and V_{AN} are driven to be essentially equal by negative feedback, the input common-mode voltage of the amplifier can be expressed as a single term, V_{ACM}. V_{ACM} can be calculated as

$$V_{ACM} = \frac{V_{OCM} + 2V_{ICM}}{3}$$

where V_{ICM} is the common-mode voltage of the input signal, that is, $V_{ICM} = (V_{IP} + V_{IN})/2$.

OUTPUT COMMON-MODE CONTROL

The AD8146 allows the user to control each of the three common-mode output levels independently through the three V_{OCM} input pins. The V_{OCM} pins pass a signal to the common-mode output level of each of their respective amplifiers with 330 MHz of small signal bandwidth and an internally fixed gain of 1. In this way, additional control and communication signals can be embedded on the common-mode levels as users see fit.

With no external circuitry, the level at the V_{OCM} input of each amplifier defaults to approximately midsupply. An internal resistive divider with an impedance of approximately 12.5 kΩ sets this level. To limit common-mode noise in dc common-mode applications, external bypass capacitors should be connected from each of the V_{OCM} input pins to ground.

SYNC-ON COMMON-MODE

The AD8147 and AD8148 are specifically targeted at driving RGB video signals over UTP cable using a sync-on common-mode technique. The common-mode outputs of each of the R, G, and B differential outputs are set using circuitry contained within the device. This circuitry embeds the horizontal and vertical sync pulses on the three common-mode outputs in a way that also results in low radiated energy. For a more detailed description of the sync scheme, see the Applications section.

The sync-on common-mode circuit generates a current based on the SYNC LEVEL input pin (Pin 18). With the SYNC LEVEL input tied to GND, the common-mode output of all drivers is set at $(V_{S+} + V_{S-})/2$. Using a resistor divider, a voltage can be applied between GND and SYNC LEVEL that determines the maximum deviation of the common-mode outputs from their midsupply level. If, for instance, SYNC LEVEL = 0.5 V and the supply voltage is 5 V, the common-mode outputs fall within an envelope of 2.5 V ± 0.5 V. The state of each $V_{OUT, cm}$ output based on the H_{SYNC} and V_{SYNC} inputs is determined by the equations defined in the Applications section.

In most cases, the sync-on common-mode circuit can be used by directly applying the H_{SYNC} and V_{SYNC} signals to their respective AD8147 or AD8148 inputs. The logic thresholds of the H_{SYNC} and V_{SYNC} inputs are set to nominally 1.4 V with respect to GND, and the exposed paddles of the AD8147 and AD8148 are used as the GND references for the incoming sync pulses. When ±2.5 V supplies are used, however, external protection is required to limit the positive excursion to less than 2.5 V. For more details, see the Applications section.

The input paths from the H_{SYNC} and V_{SYNC} inputs to the switches in the current mode level-shifting circuit are well matched to eliminate false switching transients, maximizing common-mode balance and minimizing radiated energy.

APPLICATIONS

DRIVING RGB VIDEO SIGNALS OVER CATEGORY-5 UTP CABLE

The foremost application of the drivers is the transmission of RGB video signals over UTP cable in KVM networks. The excellent balance of the differential outputs ensures low radiated energy from each of the twisted pairs. Single-ended video signals are easily converted to differential signals for transmission over the cable, and the internally fixed gain of 2 or 4 automatically compensates for the losses incurred by the source and load terminations. The common topologies used in KVM networks, such as daisy-chained, star, and point-to-point, are supported by the drivers. Figure 29 shows the AD8146 in a triple single-ended-to-differential application when driven from a 75 Ω source, which is typical of how RGB video is driven over an UTP cable.

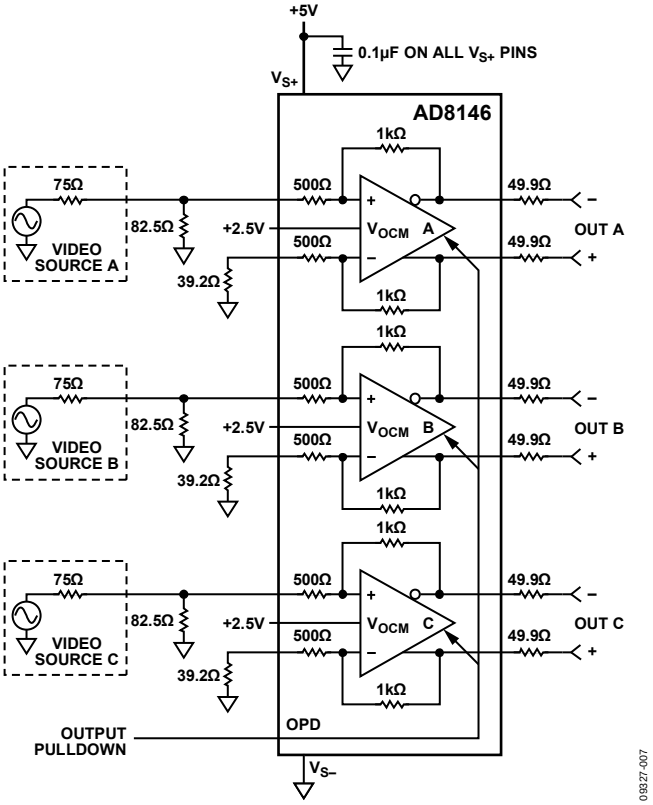
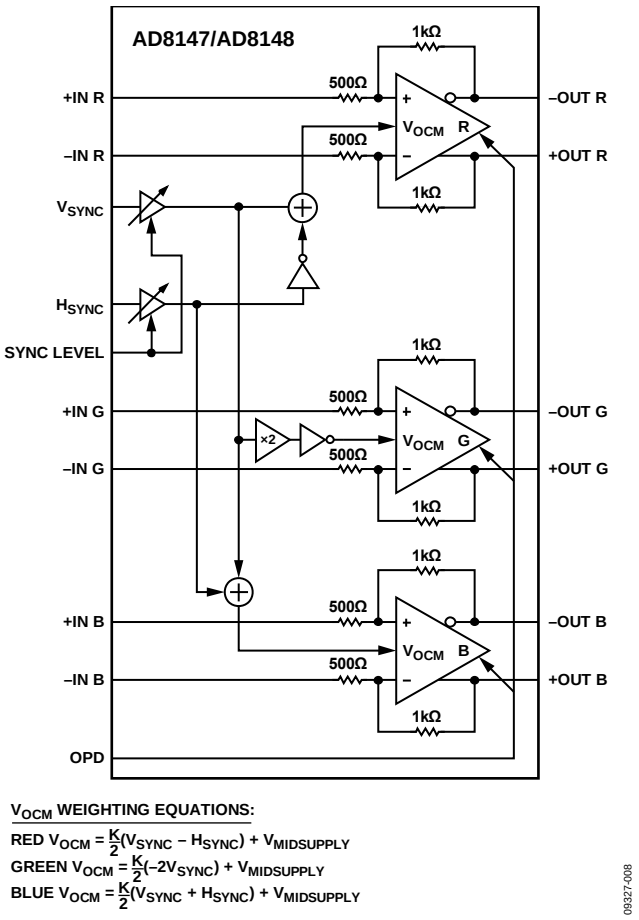


Figure 29. AD8146 in Single-Ended-to-Differential Application

VIDEO SYNC-ON COMMON-MODE

In computer video applications, the horizontal and vertical sync signals are often separate from the video information signals. For example, in typical computer monitor applications, the red, green, and blue (RGB) color signals are transmitted over separate cables, as are the vertical and horizontal sync signals. When transmitting these types of video signals over long distances on UTP cable, it is desirable to reduce the required number of physical channels. One way to do this is to encode the vertical and horizontal sync signals as weighted sums and differences of the output common-mode signals. The RGB color signals are each transmitted differentially over separate physical channels. The fact that the differential and common-mode signals are orthogonal allows the RGB color and sync signals to be separated at the channel's receiver.

Cat-5 cable contains four balanced twisted-pair physical channels that can support both differential and common-mode signals. Transmitting typical computer monitor video over this cable can be accomplished by using three of the twisted pairs for the RGB and sync signals and one wire of the fourth pair as a return path for the Schottky diode bias currents. Each color is transmitted differentially, one on each of the three pairs, and the encoded sync signals are transmitted among the common-mode signals of each of the three pairs. To minimize EMI from the sync signals, the common-mode signals on each of the three pairs produced by the sync encoding scheme induce electric and magnetic fields that for the most part cancel each other. A conceptual block diagram of the sync encoding scheme is presented in Figure 30. Because the AD8147/AD8148 have the sync encoding scheme implemented internally, the user simply applies the horizontal and vertical sync signals to the appropriate inputs. (See the Specifications tables for the high and low levels of the horizontal and vertical sync pulse voltages).



V_{OCM} WEIGHTING EQUATIONS:

RED $V_{OCM} = \frac{K}{2}(V_{SYNC} - H_{SYNC}) + V_{MIDSUPPLY}$

GREEN $V_{OCM} = \frac{K}{2}(-2V_{SYNC}) + V_{MIDSUPPLY}$

BLUE $V_{OCM} = \frac{K}{2}(V_{SYNC} + H_{SYNC}) + V_{MIDSUPPLY}$

Figure 30. AD8147/AD8148 Sync-On Common-Mode Encoding Scheme

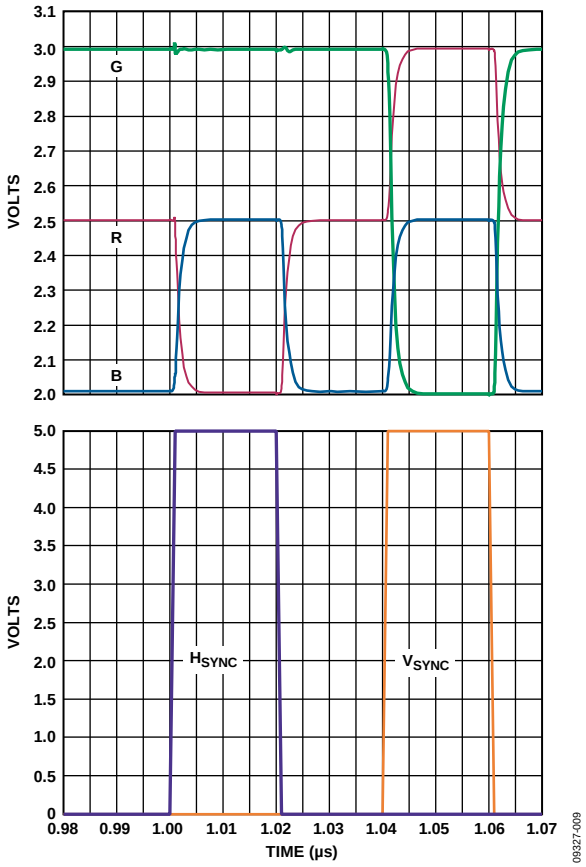


Figure 31. AD8147 Sync-On Common-Mode Signals in Single 5 V Application

The transmitted common-mode sync signal magnitudes are scaled by applying a dc voltage to the SYNC LEVEL input, referenced to GND. The difference between the voltage applied to the SYNC LEVEL input and GND sets the peak deviation of the encoded sync signals about the midsupply, common-mode voltage. For example, with the SYNC LEVEL input set at 500 mV, the deviation of the encoded sync pulses about the nominal midsupply, common-mode voltage is typically ±500 mV. The equations in Figure 30 describe how the V_{SYNC} and H_{SYNC} signals are encoded on each color's midsupply common-mode signal. In these equations, the weights of the V_{SYNC} and H_{SYNC} signals are ±1 (+1 for high and −1 for low), and the constant K is equal to the peak deviation of the encoded sync signals.

Figure 31 shows how the sync signals appear on each common-mode voltage in a single 5 V supply application when the voltage applied to the SYNC LEVEL input is 500 mV, which is the typical setting for most applications.

Sync pulse amplitudes applied to the AD8147 and AD8148 must be less than or equal to the positive supply voltage. In low positive supply applications, such as those that use ±2.5 V supplies, external limiting may be required because many logic families produce amplitudes up to 5 V. Figure 32 illustrates how to use a monolithic triple diode to limit a sync pulse with 5 V amplitude to an amplitude of approximately 2 V.

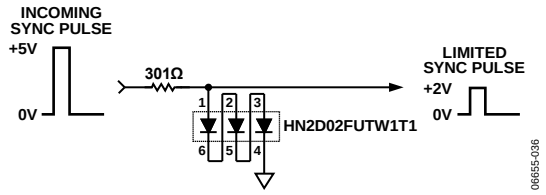


Figure 32. Limiting Sync Pulse Amplitude in Low Positive Supply Applications

DRIVING TWO UTP CABLES WITH ONE DRIVER

Some applications require driving two UTP cables with a single driver. Each individual driver of the AD8146/AD8147/AD8148 is capable of driving two doubly terminated cables, which places a differential load of 100 Ω across the outputs of the driver. Figure 33 illustrates how to drive two cables.

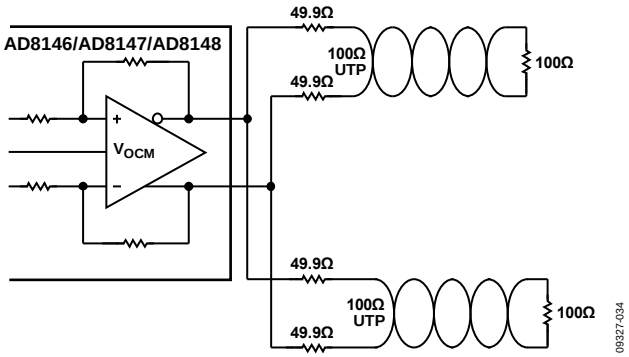


Figure 33. Driving Two UTP Cables With One Driver

Driver bandwidth is affected to a small degree when driving the 100 Ω load presented by the two cables, as compared with driving a typical 200 Ω load. Figure 34 illustrates the AD8146/AD8147/AD8148 bandwidths when driving a 100 Ω load.

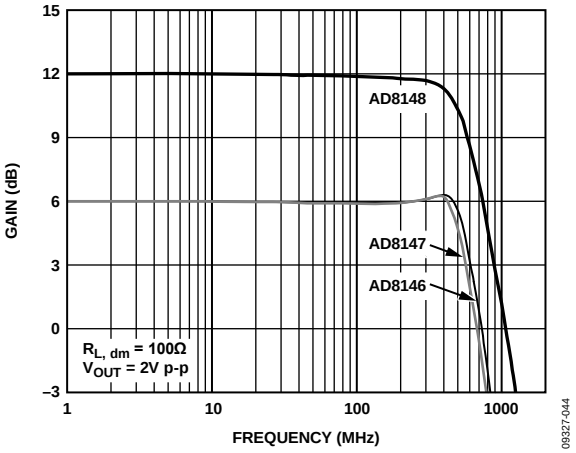


Figure 34. Large Signal Frequency Response Driving 100 Ω Loads

USING THE AD8146 AS A RECEIVER

While the AD8146 excels as a differential driver, it can also be used as a differential-to-differential receiver applied as an input buffer that protects a more sophisticated device, such as a differential crosspoint switch. See Figure 35 for an illustration of this type of application.

Because the AD8146 V_{OCM} input pins are uncommitted, any incoming common-mode signal, such as encoded sync pulses, can be reproduced at the AD8146 outputs by stripping it from the received signal and applying it directly to the V_{OCM} pin. The two series 54.9 Ω resistors form a differential termination resistor of 109.8 Ω, which when loaded with the 1 kΩ differential input resistance of the AD8146, provides an overall termination of approximately 100 Ω. The received common-mode voltages are available at the center taps between the two resistors.

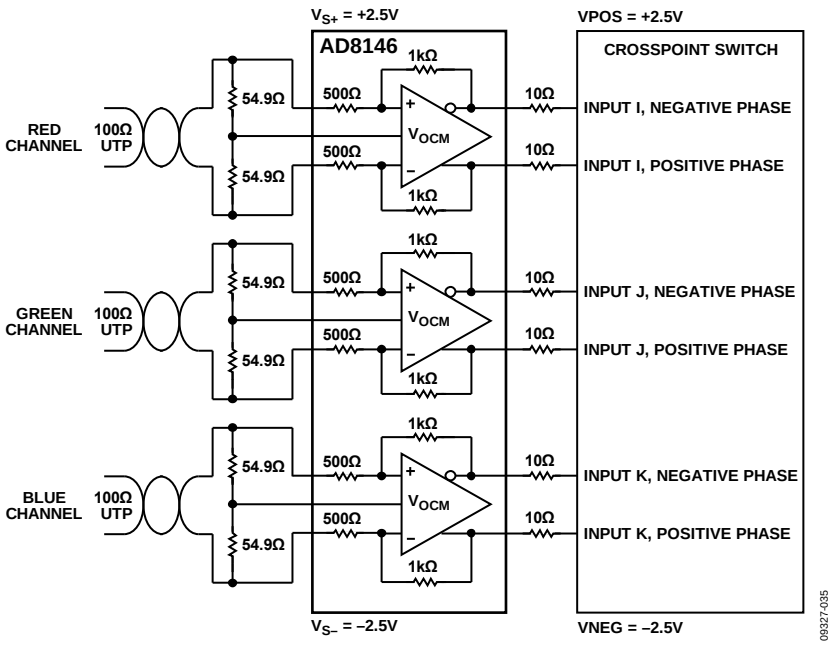


Figure 35. Using the AD8146 as a Differential Receiver

Terminations are not required between the AD8146 and the switch if the interconnection lengths are kept short (less than two inches). The 10 Ω series resistors buffer the input capacitance of the switch (typically 2 pF) and produce a low-pass rolloff that is down by only 0.025 dB at 600 MHz.

OUTPUT PULL-DOWN (OPD)

The output pull-down feature, when used in conjunction with series Schottky diodes, offers a convenient means to multiplex a number of driver outputs together to form a video network. The OPD pin is a binary input that controls the state of the outputs. Its binary input level is referenced to GND (see the Specifications section for the logic levels). When the OPD input is driven to its low state, the output is enabled and operates in normal fashion. In this state, the V_{OCM} input can be used to provide a positive bias on the series diodes, allowing the drivers to transmit signals over the network. When the OPD input is driven to its high state, the outputs of the drivers are forced to a low voltage, irrespective of the level on the V_{OCM} input, reverse-biasing the series diodes and thus presenting high impedance to the network. This feature allows a three-state output to be realized that maintains its high impedance state even when the drivers are not powered.

It is recommended that the output pull-down feature only be used in conjunction with series diodes in such a way as to ensure that the diodes are reverse-biased when the output pull-down feature is asserted, because some loading conditions can prevent the output voltage from being pulled all the way down.

LAYOUT AND POWER SUPPLY DECOUPLING CONSIDERATIONS

Standard high speed PCB layout practices should be adhered to when designing with the drivers. A solid ground plane is required and good wideband power supply decoupling networks should be placed as close as possible to the supply pins. Small surface-mount ceramic capacitors are recommended for these networks, and tantalum capacitors are recommended for bulk supply decoupling.

Source termination resistors on the differential outputs must be placed as close as possible to the output pins to minimize load capacitance due to the PCB traces.

DRIVING A CAPACITIVE LOAD

A purely capacitive load can react with the output impedance of any amplifier to produce an undesirable phase shift, which reduces phase margin and results in high frequency ringing in the pulse response. The best way to minimize this effect is to place a small resistor in series with each of the outputs of the amplifier to buffer the load capacitance. Most applications include 49.9 Ω source termination resistors, which effectively buffer any stray load capacitance.

Under no circumstances should capacitance be intentionally added to an output to introduce frequency domain peaking. Figure 36 and Figure 37 illustrate how adding just 5 pF of excessive load capacitance influences time and frequency domain responses.

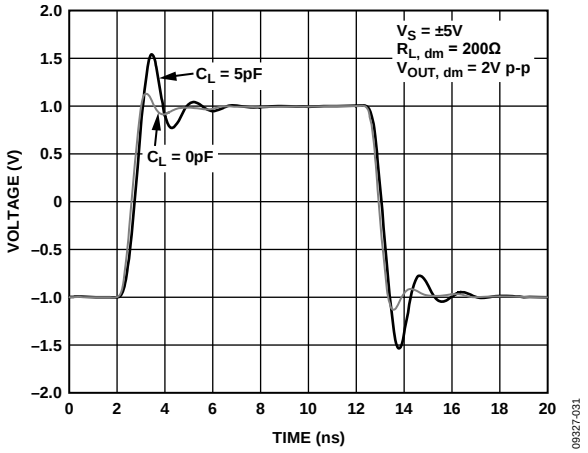


Figure 36. Large Signal Transient Responses at Various Capacitive Loads

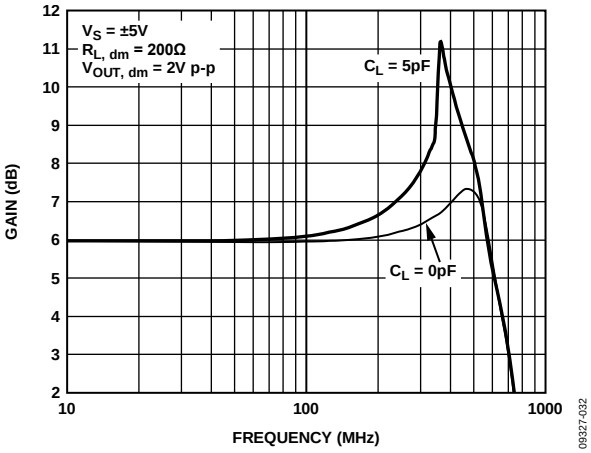


Figure 37. Large Signal Frequency Responses at Various Capacitive Loads

While high frequency peaking is desirable in some cable equalization applications, it should be implemented using methods that do not compromise the stability of the driver and that do not depend on amplifier parasitic elements. The parasitic elements are affected by process variations and cannot be depended upon for circuit designs. The amplifier may break into oscillation when excess load capacitance is intentionally added. For more information on this topic, see the Adding Pre-Emphasis to the section for a description on how to introduce a controlled amount of pre-emphasis for 30 meters of UTP using the AD8148.

ADDING PRE-EMPHASIS TO THE AD8148

UTP cables exhibit loss characteristics that are low pass in nature and are exponential functions of the square root of the frequency. Over wideband video bandwidths, the losses are predominantly due to the skin effect, which causes the resistance of the cable to increase with frequency. Even though the loss characteristics are nonlinear, suitable linear networks can be designed to approximately compensate for the losses.

Placing the compensation network at the transmitting end of the cable is referred to as pre-emphasis, because the higher frequencies are emphasized, or boosted, before they are sent, to compensate for the low-pass response of the cable. Because the higher frequencies experience more loss than the lower frequencies as they pass through the cable, the high and low frequencies arrive at approximately the same level and at the end of the cable when a properly designed pre-emphasis network is used at the transmitter. The ideal cascaded frequency response of the pre-emphasis network and the cable is therefore nominally flat.

Because the AD8148 has an internally set, closed-loop gain of 4 (12 dB), it is possible to reduce the gain at low frequencies using external frequency selective components, then use these components to provide increasing gain with increasing frequency, back to a value close to 12 dB. These components, along with the AD8148, form the pre-emphasis network. When properly designed, the combined frequency response of the pre-emphasis network and cable is approximately flat with a gain of 2 (6 dB).

Figure 38 illustrates how to construct a pre-emphasis network using the AD8148 that compensates for 30 meters of UTP cable. The network in the lower leg is required to match the transfer function of the two feedback loops.

At dc, the capacitors are open circuits, and the network has a gain of approximately 6.5 dB. (The additional 0.5 dB is added to compensate for the cable flat loss that occurs at frequencies below where the skin effect begins to take effect.) Moving up in frequency, the 30 pF capacitor begins to take effect and introduces a zero into the frequency response, causing the gain to increase with frequency. Continuing to move up in frequency, the 30 pF capacitor becomes an effective short, and the 487 Ω resistor goes in parallel with the 442 Ω resistor, forming a pole in the response. Continuing to move up in frequency, the 18 pF capacitor takes effect, introducing another zero, and causes the gain to further increase with frequency until it becomes an effective short, and the gain starts to flatten out until the amplifier response begins to roll off. The gain does not reach 12 dB before the amplifier begins to roll off because the 12 dB value is a high frequency asymptote. The pole and zero locations cited in the previous discussion are qualitative, but the discussion describes the basic principles involved with the operation of the pre-emphasis network.

Figure 39 illustrates the frequency response of the pre-emphasis network.

Figure 40 illustrates the frequency response of the pre-emphasis circuit cascaded with the cable compared with that of the cable alone. It can be seen that the overall response is flat to within ±0.4 dB. The ±0.4 dB ripple in the response is due to the fact that the pre-emphasis network is linear, comprised of two real-axis pole/zero pairs, and the cable response is nonlinear.

EXPOSED PADDLE (EP)

The 24-lead LFCSP has an exposed paddle on the underside of its body. To achieve the specified thermal resistance, it must have a good thermal connection to one of the PCB planes. The exposed paddle must therefore be soldered to a pad on the top of the board that is connected to an inner plane with several thermal vias. The AD8147/AD8148 use the paddle as a ground reference; therefore, for these parts, the PCB plane used must be the ground plane.

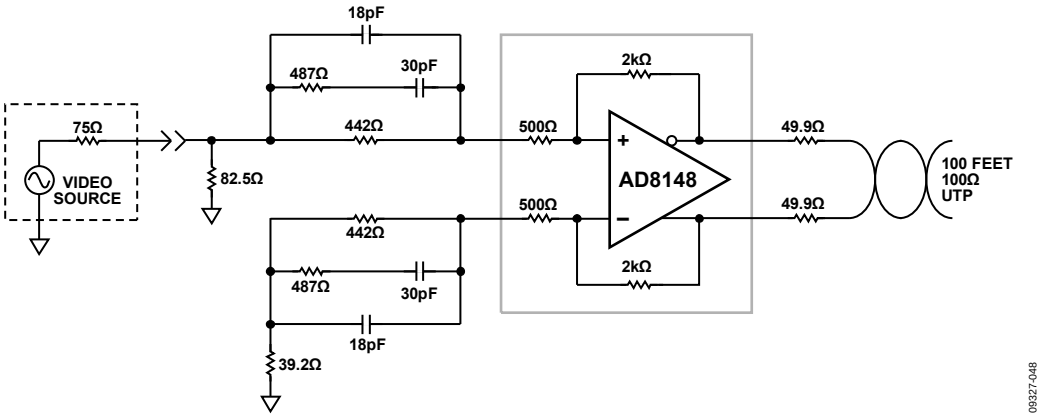


Figure 38. Pre-Emphasis Network Using the AD8148 for 30 Meters of UTP Cable

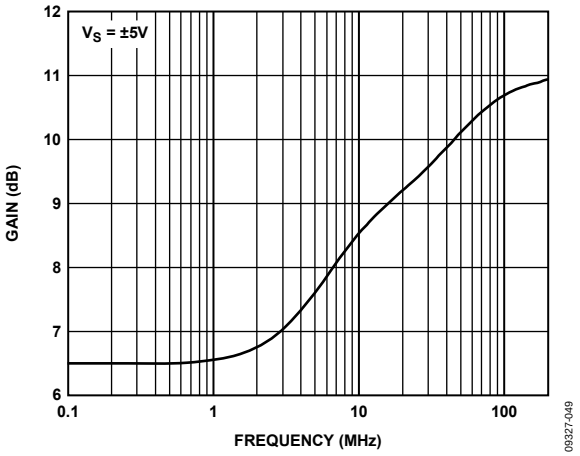


Figure 39. AD8148 Pre-Emphasis Network Frequency Response

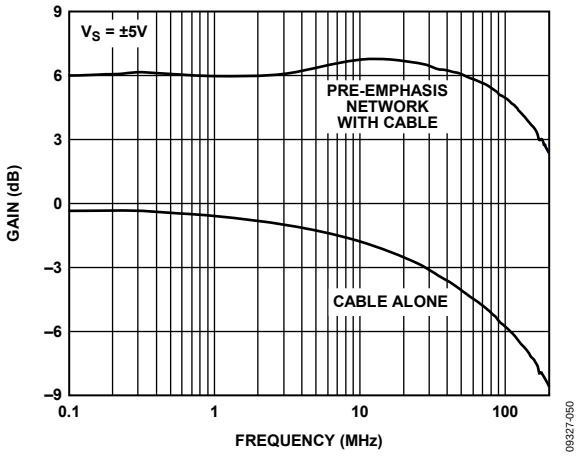


Figure 40. AD8148 Pre-Emphasis Network Cascaded With 30 Meters of UTP Cable vs. UTP Cable Alone

OUTLINE DIMENSIONS

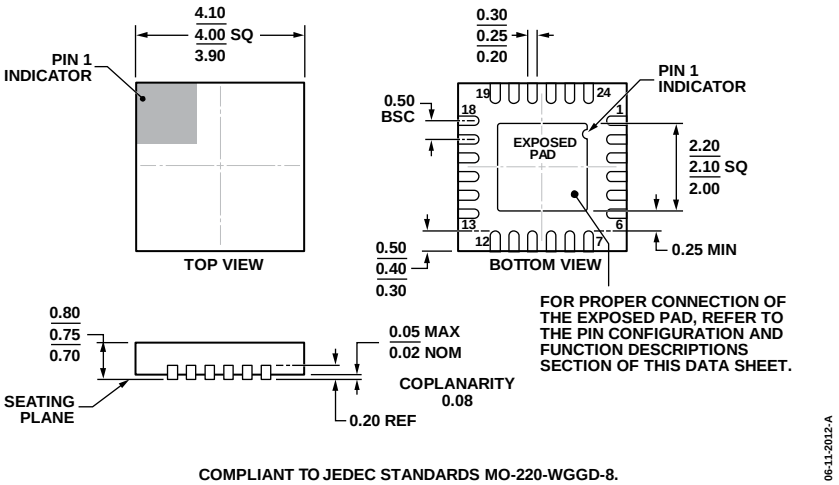


Figure 41. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8146ACPZ-R2	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
AD8146ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
AD8146ACPZ-RL	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
AD8147ACPZ-R2	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
AD8147ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
AD8147ACPZ-RL	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
AD8147-EVALZ		Evaluation Board	
AD8148ACPZ-R2	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
AD8148ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
AD8148ACPZ-RL	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10

[1] Z = RoHS Compliant Part.

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