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12/2015—Rev. C to Rev. D

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SPECIFICATIONS

AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{INx} - V_{INxN}$	0		2 V_{REF}	V
Common-Mode Input Voltage	V_{INxN}	−0.1		+0.5	V
Analog Input CMRR	f_{IN} = 100 kHz		55		dB
Input Current	500 kSPS throughput		45		µA
Input Impedance [1]					
THROUGHPUT SPEED					
Complete Cycle (2 Channels)	Normal mode	2			µs
Throughput Rate	Normal mode	0		500	kSPS
Complete Cycle (2 Channels)	Impulse mode	2.25		2.25	µs
Throughput Rate	Impulse mode	0		444	kSPS
DC ACCURACY					
Integral Linearity Error [2]		−6		+6	LSB [3]
No Missing Codes		15			Bits
Transition Noise			0.8		LSB
Full-Scale Error [4]	T_{MIN} to T_{MAX}		±0.25	±0.5	% of FSR
Full-Scale Error Drift [4]			±2		ppm/°C
Unipolar Zero Error [4]	T_{MIN} to T_{MAX}			±0.25	% of FSR
Unipolar Zero Error Drift [4]			±0.8		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		±0.8		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 100 kHz		86		dB [5]
Spurious-Free Dynamic Range	f_{IN} = 100 kHz		98		dB
Total Harmonic Distortion	f_{IN} = 100 kHz		−96		dB
Signal-to-Noise and Distortion	f_{IN} = 100 kHz		86		dB
	f_{IN} = 100 kHz, −60 dB input		30		dB
Channel-to-Channel Isolation	f_{IN} = 100 kHz		−92		dB
−3 dB Input Bandwidth			10		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Delay Matching			30		ps
Aperture Jitter			5		ps rms
Transient Response	Full-scale step			250	ns
REFERENCE					
External Reference Voltage Range		2.3	2.5	AVDD/2	V
External Reference Current Drain	500 kSPS throughput		180		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.8	V
V_{IH}		+2.0		DVDD + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format [6]					
Pipeline Delay [7]					
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	OVDD − 0.2			V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25[8]	V
Operating Current[9]	500 kSPS throughput				
AVDD			15.5		mA
DVDD			8.5		mA
OVDD			100		µA
Power Dissipation	500 kSPS throughput[9]		120	135	mW
	10 kSPS throughput[10]		2.6		mW
	444 kSPS throughput[10]		114	125	mW
TEMPERATURE RANGE[11]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] See the Analog Inputs section.
[2] Linearity is tested using endpoints, not best fit.
[3] LSB means least significant bit. With the 0 V to 5 V input range, 1 LSB is 76.294 µV.
[4] See the Terminology section. These specifications do not include the error contribution from the external reference.
[5] All specifications in dB are referred to as full-scale input, FS. Tested with an input signal at 0.5 dB below full scale unless otherwise specified.
[6] Parallel or serial 16 bit.
[7] Conversion results are available immediately after completed conversion.
[8] The maximum should be the minimum of 5.25 V and DVDD + 0.3 V.
[9] In normal mode; tested in parallel reading mode.
[10] In impulse mode; tested in parallel reading mode.
[11] Consult sales for extended temperature range.

TIMING SPECIFICATIONS

AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION AND RESET (See Figure 22 and Figure 23)					
Convert Pulse Width	t_1	5			ns
Time Between Conversions					
(Normal Mode/Impulse Mode)	t_2	2/2.25			µs
$\overline{CNVST}$ Low to BUSY High Delay	t_3			32	ns
BUSY High All Modes Except in Master Serial Read After Convert Mode					
(Normal Mode/Impulse Mode)	t_4			1.75/2	µs
Aperture Delay	t_5		2		ns
End of Conversions to BUSY Low Delay	t_6	10			ns
Conversion Time					
(Normal Mode/Impulse Mode)	t_7			1.75/2	µs
Acquisition Time	t_8	250			ns
RESET Pulse Width	t_9	10			ns
$\overline{CNVST}$ Low to $\overline{EOC}$ High Delay	t_{10}			30	ns
$\overline{EOC}$ High for Channel A Conversion					
(Normal Mode/Impulse Mode)	t_{11}			1/1.25	µs
$\overline{EOC}$ Low after Channel A Conversion	t_{12}	45			ns
$\overline{EOC}$ High for Channel B Conversion	t_{13}			0.75	µs
Channel Selection Setup Time	t_{14}	250			ns
Channel Selection Hold Time	t_{15}			30	ns
PARALLEL INTERFACE MODES (See Figure 24 to Figure 28)					
$\overline{CNVST}$ Low to DATA Valid Delay	t_{16}			1.75/2	µs
DATA Valid to BUSY Low Delay	t_{17}	14			ns
Bus Access Request to DATA Valid	t_{18}			40	ns
Bus Relinquish Time	t_{19}	5		15	ns
A/$\overline{B}$ Low to Data Valid Delay	t_{20}			40	ns
MASTER SERIAL INTERFACE MODES (See Figure 29 and Figure 30)					
$\overline{CS}$ Low to SYNC Valid Delay	t_{21}			10	ns
$\overline{CS}$ Low to Internal SCLK Valid Delay[1]	t_{22}			10	ns
$\overline{CS}$ Low to SDOUT Delay	t_{23}			10	ns
$\overline{CNVST}$ Low to SYNC Delay, Read During Convert					
(Normal Mode/Impulse Mode)	t_{24}		250/500		ns
SYNC Asserted to SCLK First Edge Delay	t_{25}	3			ns
Internal SCK Period[2]	t_{26}	23		40	ns
Internal SCLK High[2]	t_{27}	12			ns
Internal SCLK Low[2]	t_{28}	7			ns
SDOUT Valid Setup Time[2]	t_{29}	4			ns
SDOUT Valid Hold Time[2]	t_{30}	2			ns
SCLK Last Edge to SYNC Delay[2]	t_{31}	1			ns
$\overline{CS}$ High to SYNC HI-Z	t_{32}			10	ns
$\overline{CS}$ High to Internal SCLK HI-Z	t_{33}			10	ns
$\overline{CS}$ High to SDOUT HI-Z	t_{34}			10	ns
BUSY High in Master Serial Read after Convert[2]	t_{35}		See Table 4		
$\overline{CNVST}$ Low to SYNC Asserted Delay					
(Normal Mode/Impulse Mode)	t_{36}		0.75/1		µs
SYNC Deasserted to BUSY Low Delay	t_{37}		25		ns

Parameter	Symbol	Min	Typ	Max	Unit
SLAVE SERIAL INTERFACE MODES (See Figure 32 and Figure 33)					
External SCLK Setup Time	t_{38}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{39}	3		18	ns
SDIN Setup Time	t_{40}	5			ns
SDIN Hold Time	t_{41}	5			ns
External SCLK Period	t_{42}	25			ns
External SCLK High	t_{43}	10			ns
External SCLK Low	t_{44}	10			ns

[1] In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise C_L is 60 pF maximum.
[2] In serial master read during convert mode. See Table 4 for serial master read after convert mode.

Table 4. Serial Clock Timings in Master Read After Convert

DIVSCLK[1]		0	0	1	1	
DIVSCLK[0]	Symbol	0	1	0	1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{25}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{26}	25	50	100	200	ns
Internal SCLK Period Typical	t_{26}	40	70	140	280	ns
Internal SCLK High Minimum	t_{27}	12	22	50	100	ns
Internal SCLK Low Minimum	t_{28}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{29}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{30}	2	4	30	80	ns
SCLK Last Edge to SYNC Delay Minimum	t_{31}	1	3	30	80	ns
Busy High Width Maximum (Normal)	t_{35}	3.25	4.25	6.25	10.75	µs
Busy High Width Maximum (Impulse)	t_{35}	3.5	4.5	6.5	11	µs

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Value
Analog Input	
INAx[1], INBx[1], REFx, INxN, REFGND	AVDD + 0.3 V to AGND − 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD, OVDD	−0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD	±7 V
DVDD to OVDD	−0.3 V to +7 V
Digital Inputs	−0.3 V to DVDD + 0.3 V
Internal Power Dissipation[2]	700 mW
Internal Power Dissipation[3]	2.5 W
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] See the Analog Inputs section.
[2] Specification is for device in free air: 48-lead LQFP, θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[3] Specification is for device in free air: 48-lead LFCSP, θ_{JA} = 26°C/W.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

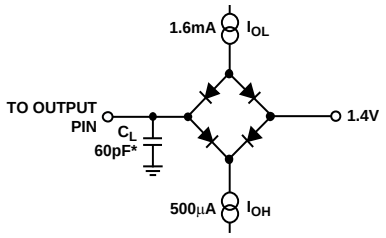


Figure 2. Load Circuit for Digital Interface Timing

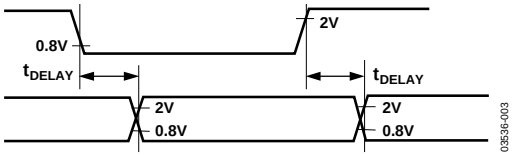


Figure 3. Voltage Reference Levels for Timing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

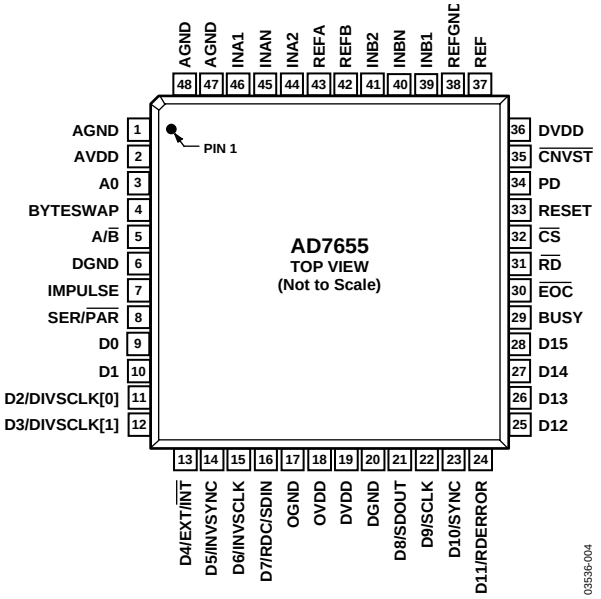


Figure 4. 48-Lead LQFP Pin Configuration

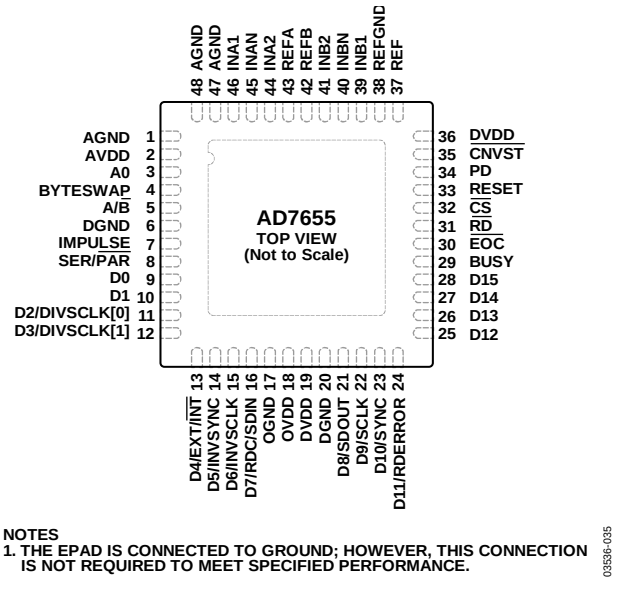


Figure 5. 48-Lead LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 47, 48	AGND	P	Analog Power Ground Pin.
2	AVDD	P	Input Analog Power Pin. Nominally 5 V.
3	A0	DI	Multiplexer Select. When LOW, the analog inputs INA1 and INB1 are sampled simultaneously, then converted. When HIGH, the analog inputs INA2 and INB2 are sampled simultaneously, then converted.
4	BYTESWAP	DI	Parallel Mode Selection (8 Bit, 16 Bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	A/$\overline{B}$	DI	Data Channel Selection. In parallel mode, when LOW, the data from Channel B is read. When HIGH, the data from Channel A is read. In serial mode, when HIGH, Channel A is output first followed by Channel B. When LOW, Channel B is output first followed by Channel A.
6, 20	DGND	P	Digital Power Ground.
7	IMPULSE	DI	Mode Selection. When HIGH, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, these outputs are in high impedance.
11, 12	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/$\overline{PAR}$ is LOW, these outputs are used as Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, EXT/$\overline{INT}$ is LOW, and RDC/SDIN is LOW, which is the serial master read after convert mode. These inputs, part of the serial port, are used to slow down the internal serial clock that clocks the data output. In the other serial modes, these inputs are not used.
13	D[4] or EXT/$\overline{INT}$	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock called, respectively, master and slave mode. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D[5] or INVSYNC	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal in Master modes. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.

Pin No.	Mnemonic	Type[1]	Description
15	D[6]	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 6 of the parallel port data output bus.
	or INVSCLK		When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave modes.
16	D[7]	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus.
	or RDC/SDIN		When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input, depending on the state of EXT/$\overline{INT}$.
			When EXT/$\overline{INT}$ is HIGH, RDC/SDIN can be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 32 SCLK periods after the initiation of the read sequence.
			When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the previous data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (5 V or 3 V).
19, 36	DVDD	P	Digital Power. Nominally at 5 V.
21	D[8]	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus.
	or SDOUT		When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in a 32-bit on-chip register. The AD7655 provides the two conversion results, MSB first, from its internal shift register. The order of channel outputs is controlled by A/$\overline{B}$. In serial mode, when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK.
			In serial mode, when EXT/$\overline{INT}$ is HIGH:
			If INVSCLK is LOW, SDOUT is updated on the SCLK rising edge and valid on the next falling edge.
			If INVSCLK is HIGH, SDOUT is updated on the SCLK falling edge and valid on the next rising edge.
22	D[9]	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 9 of the Parallel Port Data Output Bus.
	or SCLK		When SER/$\overline{PAR}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, depends upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends on the logic state of the INVSCLK pin.
23	D[10]	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 10 of the Parallel Port Data Output Bus.
	or SYNC		When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW).
			When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and frames SDOUT. After the first channel is output, SYNC is pulsed LOW. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid. After the first channel is output, SYNC is pulsed HIGH.
24	D[11]	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 11 of the Parallel Port Data Output Bus.
	or RDERROR		When SER/$\overline{PAR}$ is HIGH and EXT/$\overline{INT}$ is HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started but not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed HIGH.
25 to 28	D[12:15]	DO	Bit 12 to Bit 15 of the parallel port data output bus. When SER/$\overline{PAR}$ is HIGH, these outputs are in high impedance.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started and remains HIGH until the two conversions are complete and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data ready clock signal.
30	$\overline{EOC}$	DO	End of Convert Output. Goes LOW at each channel conversion.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external serial clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7655. Current conversion, if any, is aborted. If not used, this pin could be tied to DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current conversion is completed.
35	$\overline{CNVST}$	DI	Start Conversion. A falling edge on $\overline{CNVST}$ puts the internal sample-and-hold into the hold state and initiates a conversion. In impulse mode (IMPULSE = HIGH), if $\overline{CNVST}$ is held LOW when the acquisition phase (t8) is complete, the internal sample-and-hold is put into the hold state and a conversion is immediately started.

Pin No.	Mnemonic	Type[1]	Description
37	REF	AI	This input pin is used to provide a reference to the converter.
38	REFGND	AI	Reference Input Analog Ground.
39, 41	INB1, INB2	AI	Channel B Analog Inputs.
40, 45	INBN, INAN	AI	Analog Inputs Ground Senses. Allow to sense each channel ground independently.
42, 43	REFB, REFA	AI	These inputs are the references applied to Channel A and Channel B, respectively.
44, 46	INA2, INA1	AI	Channel A Analog Inputs.
	EPAD		Exposed Pad. The EPAD is connected to ground; however, this connection is not required to meet specified performance

[1] AI = input; DI = digital input; DO = digital output; DI/O = bidirectional digital; P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSBs beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value, and is often specified in terms of resolution for which no missing codes are guaranteed.

Full-Scale Error
The last transition (from 111...10 to 111...11) should occur for an analog voltage 1½ LSBs below the nominal full scale (4.999886 V for the 0 V to 5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

Unipolar Zero Error
The first transition should occur at a level ½ LSB above analog ground (76.29 μV for the 0 V to 5 V range). The unipolar zero error is the deviation of the actual transition from that point.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise and Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and expressed in bits by

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

Aperture Delay
Aperture delay is a measure of acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signals are held for a conversion.

Transient Response
The time required for the AD7655 to achieve its rated accuracy after a full-scale step function is applied to its input.

TYPICAL PERFORMANCE CHARACTERISTICS

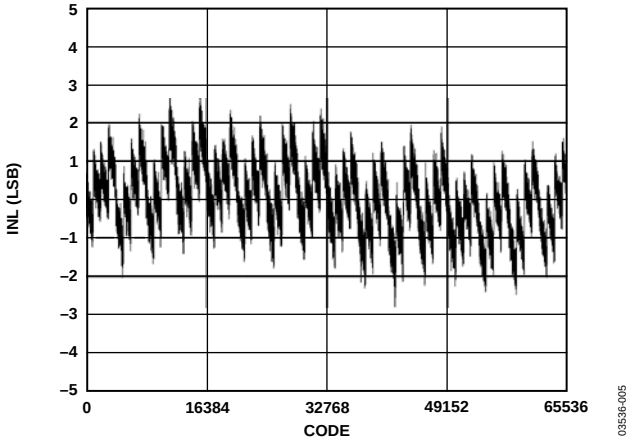


Figure 6. Integral Nonlinearity vs. Code

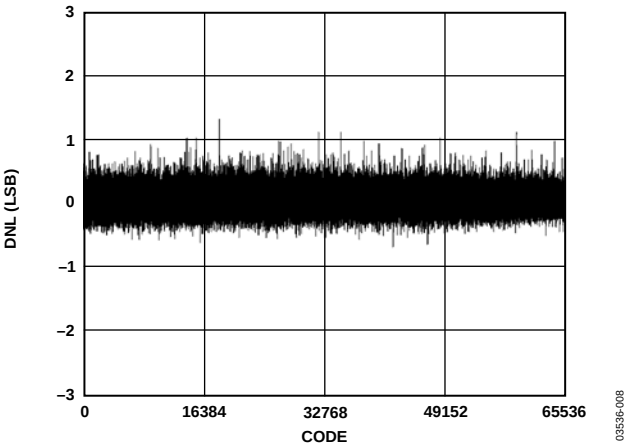


Figure 9. Differential Nonlinearity vs. Code

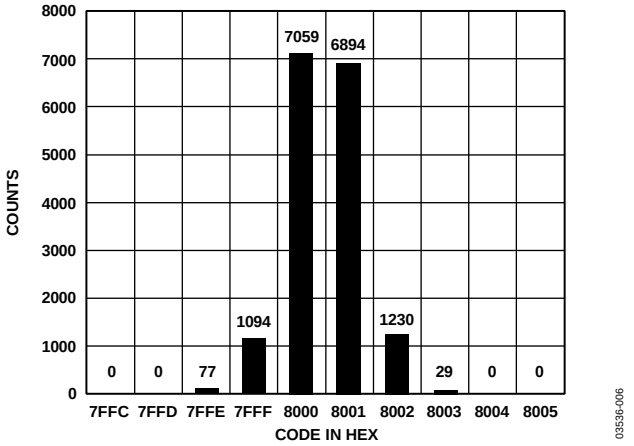


Figure 7. Histogram of 16,384 Conversions of a DC Input at the Code Transition

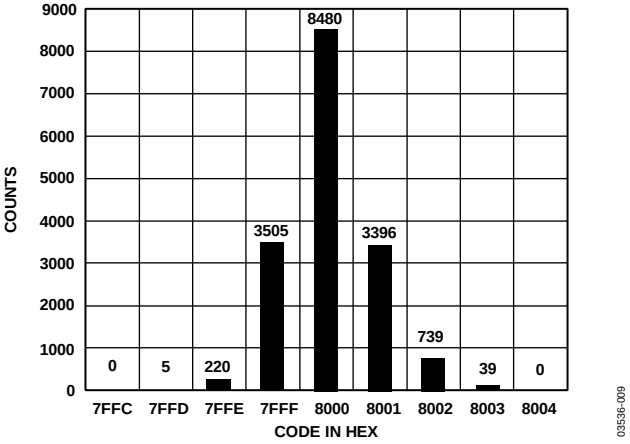


Figure 10. Histogram of 16,384 Conversions of a DC Input at the Code Center

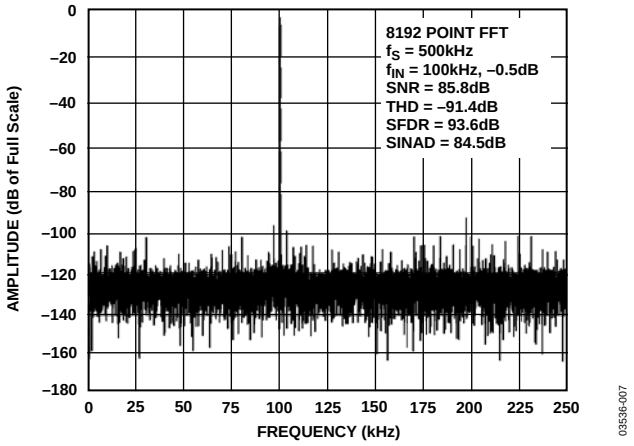


Figure 8. FFT Plot

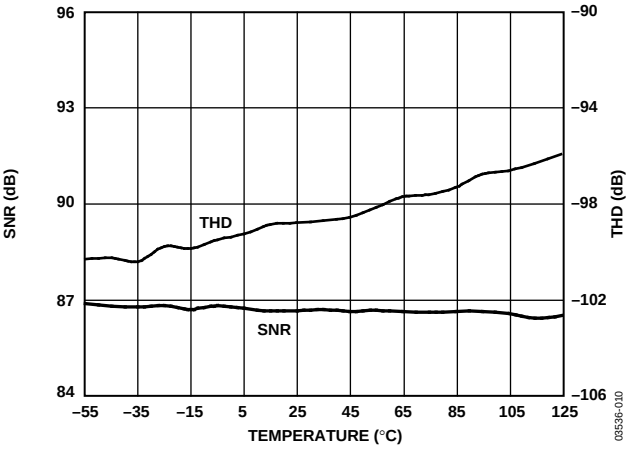


Figure 11. SNR, THD vs. Temperature

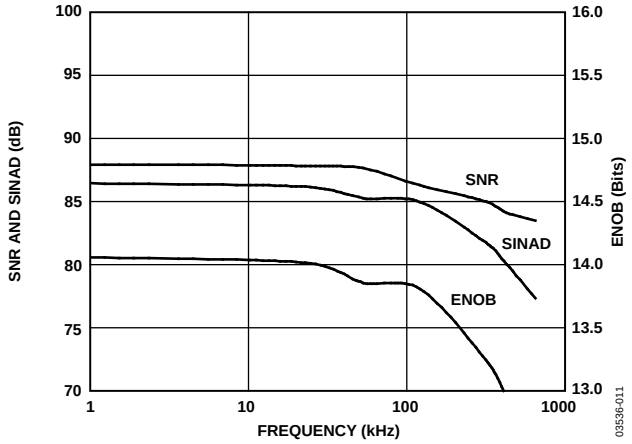


Figure 12. SNR, SINAD, and ENOB vs. Frequency

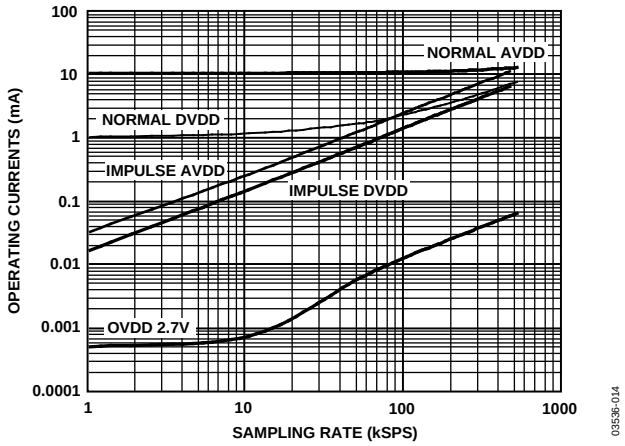


Figure 15. Operating Currents vs. Sample Rate

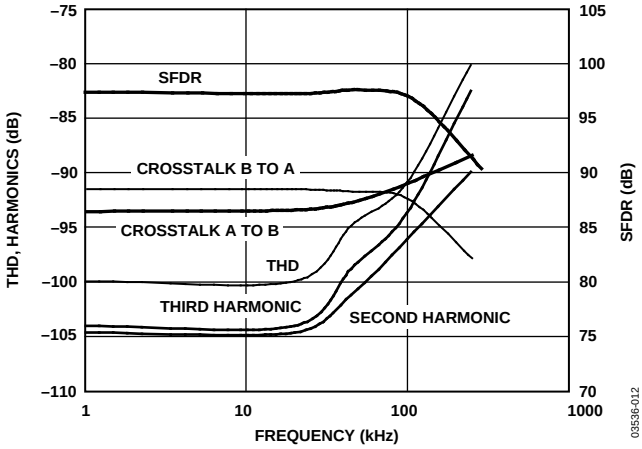


Figure 13. THD, Harmonics, Crosstalk, and SFDR vs. Frequency

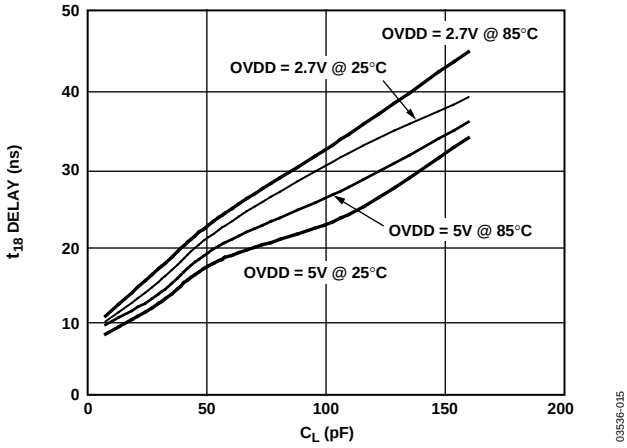


Figure 16. Typical Delay vs. Load Capacitance C_L

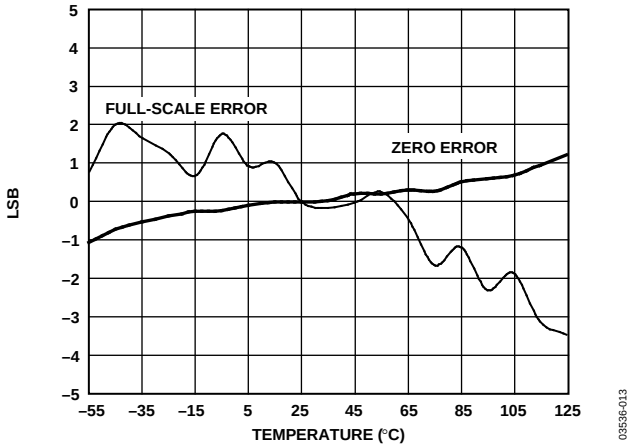


Figure 14. Full-Scale Error and Zero Error vs. Temperature

APPLICATIONS INFORMATION

CIRCUIT INFORMATION

The AD7655 is a very fast, low power, single-supply, precise simultaneous sampling 16-bit ADC.

The AD7655 provides the user with two on-chip, track-and-hold, successive approximation ADCs that do not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications. The AD7655 can also be used as a 4-channel ADC with two pairs simultaneously sampled.

The AD7655 can be operated from a single 5 V supply and be interfaced to either 5 V or 3 V digital logic. It is housed in a 48-lead LQFP or a tiny, 48-lead LFCSP that combines space savings and allows flexible configurations as either a serial or parallel interface. The AD7655 is pin-to-pin compatible with PulSAR ADCs.

MODES OF OPERATION

The AD7655 features two modes of operation, normal mode and impulse mode. Each of these modes is suitable for specific applications.

Normal mode is the fastest mode (500 kSPS). Except when it is powered down (PD = HIGH), the power dissipation is almost independent of the sampling rate.

Impulse mode, the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 444 kSPS. When operating at 10 kSPS, for example, it typically consumes only 2.6 mW. This feature makes the AD7655 ideal for battery-powered applications.

TRANSFER FUNCTIONS

The AD7655 data format is straight binary. The ideal transfer characteristic for the AD7655 is shown in Figure 17 and Table 7. The LSB size is $2 \times V_{REF}/65536$, which is about 76.3 µV.

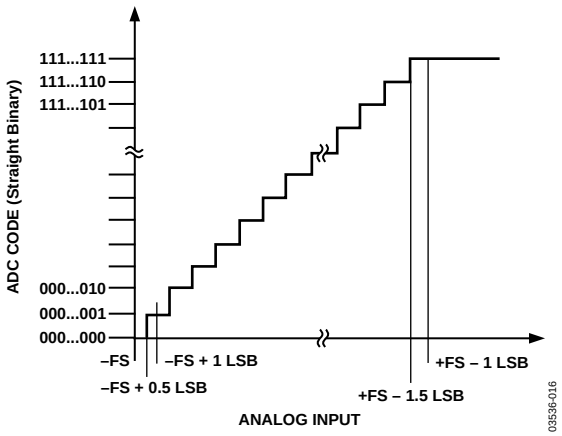
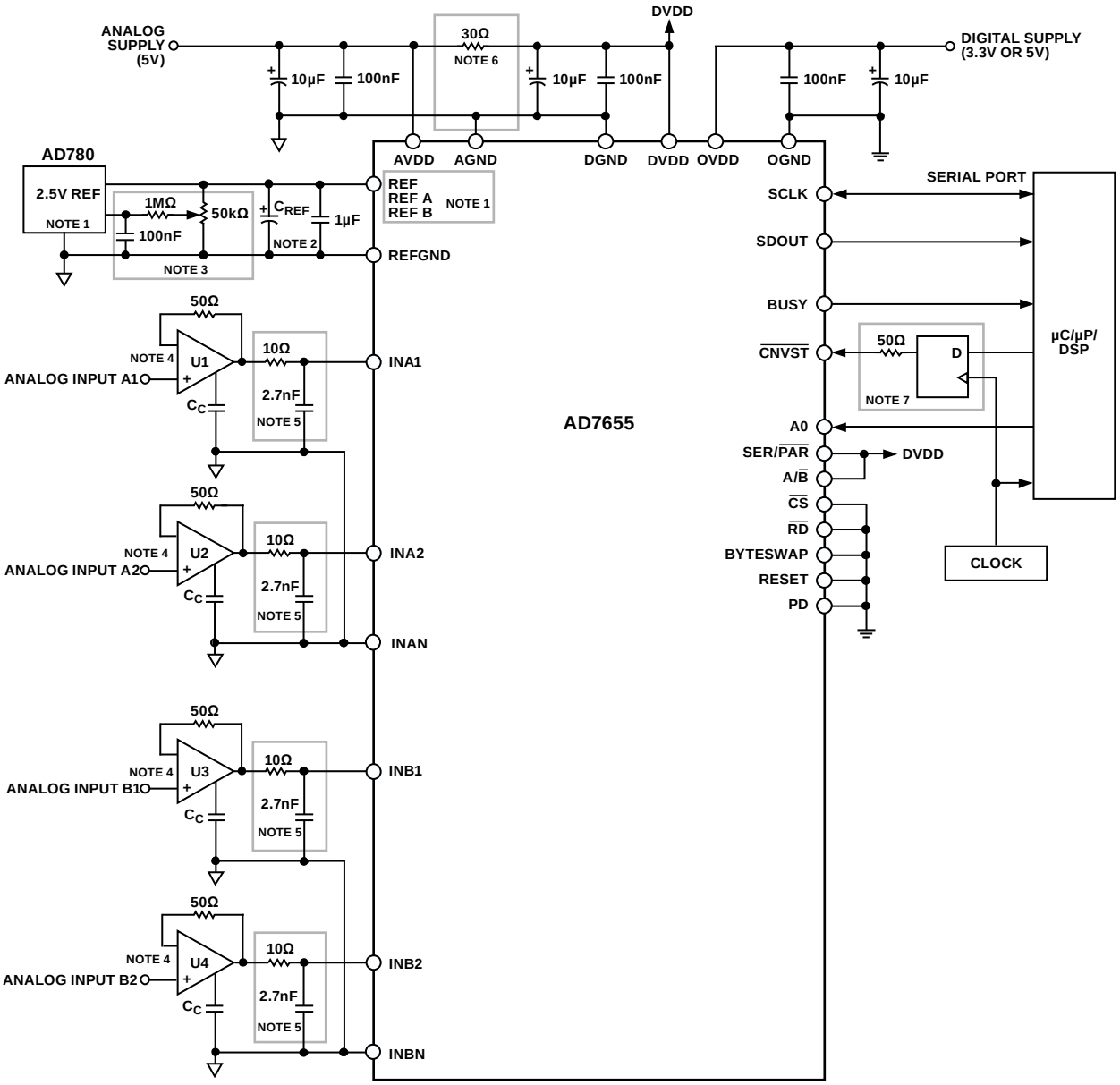


Figure 17. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 2.5 V	Digital Output Code
FSR − 1 LSB	4.999924 V	0xFFFF[1]
FSR − 2 LSB	4.999847 V	0xFFFE
Midscale + 1 LSB	2.500076 V	0x8001
Midscale	2.5 V	0x8000
Midscale − 1 LSB	2.499924 V	0x7FFF
−FSR + 1 LSB	−76.29 µV	0x0001
−FSR	0 V	0x0000[2]

[1] This is also the code for overrange analog input: ($V_{INx} - V_{INxN}$ above $2 \times (V_{REF} - V_{REFGND})$).
[2] This is also the code for underrange analog input (V_{INx} below V_{INxN}).



NOTES
1. SEE VOLTAGE REFERENCE INPUT SECTION.
2. WITH THE RECOMMENDED VOLTAGE REFERENCES, C_{REF} IS 47µF. SEE VOLTAGE REFERENCE INPUT SECTION.
3. OPTIONAL CIRCUITRY FOR HARDWARE GAIN CALIBRATION.
4. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
5. SEE ANALOG INPUTS SECTION.
6. OPTIONAL, SEE POWER SUPPLY SECTION.
7. OPTIONAL LOW JITTER CNVST. SEE CONVERSION CONTROL SECTION.

03536-017

Figure 18. Typical Connection Diagram (Serial Interface)

TYPICAL CONNECTION DIAGRAM

Figure 18 shows a typical connection diagram for the AD7655. Some of the circuitry shown in this diagram is optional and is discussed in the following sections.

ANALOG INPUTS

Figure 19 shows a simplified analog input section of the AD7655.

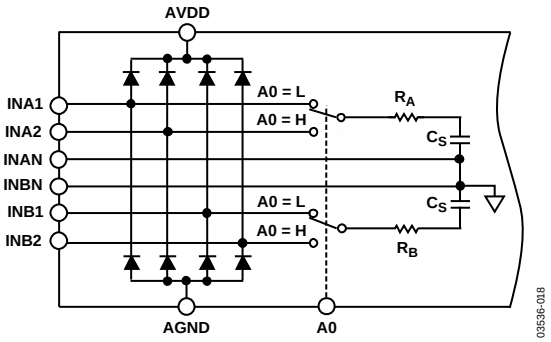


Figure 19. Simplified Analog Input

The diodes shown in Figure 19 provide ESD protection for the inputs. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs. This causes the diodes to become forward biased and start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. This condition can occur when the input buffer (U1) or (U2) supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

This analog input structure allows the sampling of the differential signal between INx and INxN. Unlike other converters, the INxN is sampled at the same time as the INx input. By using differential inputs, small signals common to both inputs are rejected.

During the acquisition phase, for ac signals, the AD7655 behaves like a one-pole RC filter consisting of the equivalent resistance R_A, R_B, and C_S. The resistors R_A and R_B are typically 500 Ω and are a lumped component made up of some serial resistors and the on resistance of the switches. The C_S capacitor is typically 32 pF and is mainly the ADC sampling capacitor. This one-pole filter with a typical −3 dB cutoff frequency of 10 MHz reduces undesirable aliasing effects and limits the noise coming from the inputs.

Because the input impedance of the AD7655 is very high, the AD7655 can be driven directly by a low impedance source without gain error. To further improve the noise filtering of the AD7655 analog input circuit, an external, one-pole RC filter between the amplifier output and the ADC input, as shown in Figure 18, can be used. However, the source impedance has to be kept low because it affects the ac performance, especially the total harmonic distortion. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD degrades when the source impedance increases.

INPUT CHANNEL MULTIPLEXER

The AD7655 allows the choice of simultaneously sampling the inputs pairs INA1/INB1 or INA2/INB2 with the A0 multiplexer input. When A0 is low, the input pairs INA1/INB1 are selected, and when A0 is high, the input pairs INA2/INB2 are selected. Note that INAx is always converted before INBx regardless of the state of the digital interface channel selection $A/\overline{B}$ pin. Also note that the channel selection control, A0, should not be changed during the acquisition phase of the converter. Refer to the Conversion Control section and Figure 22 for timing details.

DRIVER AMPLIFIER CHOICE

Although the AD7655 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7655. The noise coming from the driver is filtered by the AD7655 analog input circuit one-pole, low-pass filter made by R_A, R_B, and C_S or by an external filter, if one is used.
- The driver needs to have a THD performance suitable to that of the AD7655.
- For multichannel, multiplexed applications, the driver amplifier and the AD7655 analog input circuit together must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the data sheet for the driver amplifier, the settling at 0.1% or 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

The AD8021 meets these requirements and, for almost all applications, is usually appropriate. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type. The AD8022 can be used where a dual version is needed and a gain of +1 is used.

The AD829 is another alternative where high frequency (above 100 kHz) performance is not required. In a gain of +1, it requires an 82 pF NPO or mica type compensation capacitor.

The AD8610 is another option where low bias current is needed in low frequency applications.

Refer to Table 8 for some recommended op amps.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4841-1/ ADA4841-2	Very low noise, low distortion, low power, low frequency
AD829	Very low noise, low frequency
AD8021	Very low noise, high frequency
AD8022	Very low noise, high frequency, dual
AD8605/AD8606/ AD8608/AD8615/ AD8616/AD8618	5 V single supply, low power, low frequency, single/dual/quad
AD8610/AD8620	Low bias current, low frequency, single/dual

VOLTAGE REFERENCE INPUT

The AD7655 requires an external 2.5 V reference. The reference input should be applied to REF, REFA, and REFB. The voltage reference input REF of the AD7655 has a dynamic input impedance; it should therefore be driven by a low impedance source with an efficient decoupling. This decoupling depends on the choice of the voltage reference but usually consists of a 1 µF ceramic capacitor and a low ESR tantalum capacitor connected to the REFA, REFB, and REFGND inputs with minimum parasitic inductance. A value of 47 µF is appropriate for the tantalum capacitor when using one of the recommended reference voltages:

- The low noise, low temperature drift AD780, ADR421, and ADR431 voltage references
- The low cost AD1582 voltage reference

For applications using multiple AD7655 devices with one voltage reference source, it is recommended that the reference source drives each ADC in a star configuration with individual decoupling placed as close as possible to the REF/REFGND inputs. Also, it is recommended that a buffer, such as the AD8031/AD8032, be used in this configuration.

Care should be taken with the reference temperature coefficient of the voltage reference, which directly affects the full-scale accuracy if this parameter is applicable. For instance, a 15 ppm/°C tempco of the reference changes the full-scale accuracy by 1 LSB/°C.

POWER SUPPLY

The AD7655 uses three sets of power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.7 V and DVDD + 0.3 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply, as shown in Figure 18. The AD7655 AVDD and DVDD supplies are independent of power supply sequencing. To ensure the device is free from supply voltage induced latch-up, OVDD must never exceed DVDD by greater than 0.3 V. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 20.

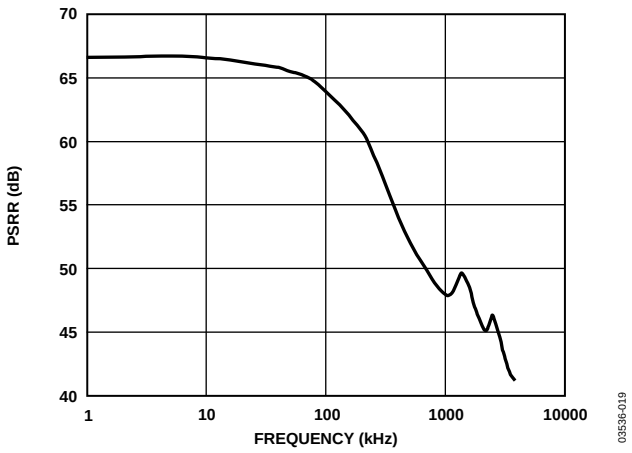


Figure 20. PSRR vs. Frequency

POWER DISSIPATION

In impulse mode, the AD7655 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows significant power savings when the conversion rate is reduced, as shown in Figure 21. This feature makes the AD7655 ideal for very low power battery applications.

Note that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (that is, DVDD and DGND), and OVDD should not exceed DVDD by more than 0.3 V.

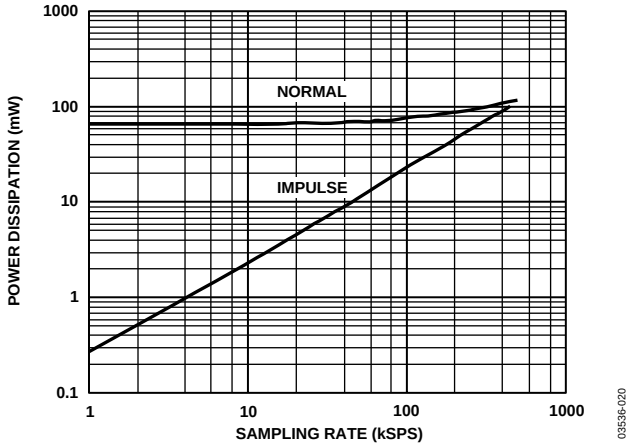


Figure 21. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 22 shows a detailed timing diagram of the conversion process. The AD7655 is controlled by the signal $\overline{CNVST}$, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input, PD, until the conversion is complete. The $\overline{CNVST}$ signal operates independently of the $\overline{CS}$ and $\overline{RD}$ signals.

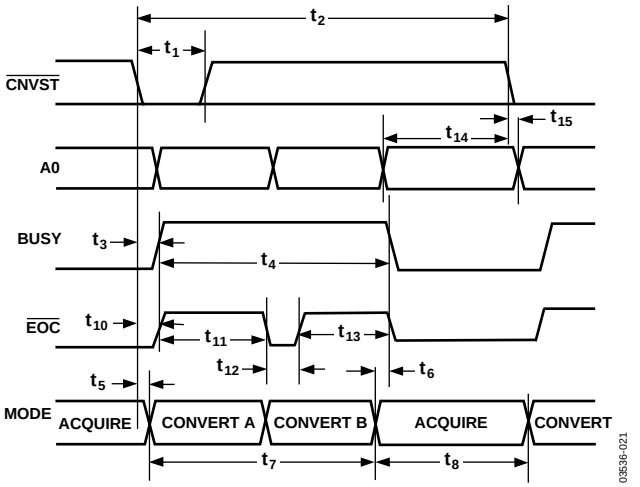


Figure 22. Basic Conversion Timing

Although $\overline{CNVST}$ is a digital signal, it should be designed with special care with fast, clean edges and levels, and with minimum overshoot and undershoot or ringing.

For applications where the SNR is critical, the $\overline{CNVST}$ signal should have very low jitter. One solution is to use a dedicated oscillator for $\overline{CNVST}$ generation or, at least, to clock it with a high frequency low jitter clock, as shown in Figure 18.

In impulse mode, conversions can be automatically initiated. If $\overline{CNVST}$ is held low when BUSY is low, the AD7655 controls the acquisition phase and automatically initiates a new conversion. By keeping $\overline{CNVST}$ low, the AD7655 keeps the conversion process running by itself. Note that the analog input has to be settled when BUSY goes low. Also, at power-up, $\overline{CNVST}$ should be brought low once to initiate the conversion process. In this mode, the AD7655 can sometimes run slightly faster than the guaranteed limits of 444 kSPS in impulse mode. This feature does not exist in normal mode.

DIGITAL INTERFACE

The AD7655 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7655 digital interface accommodates either 3 V or 5 V logic when the OVDD supply pin of the AD7655 is connected to the host system interface digital supply.

The two signals, $\overline{CS}$ and $\overline{RD}$, control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually $\overline{CS}$ allows the selection of each AD7655 in multicircuit applications and is held low in a single AD7655 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus. In parallel mode, signal A/$\overline{B}$ allows the choice of reading either the output of Channel A or Channel B, whereas in serial mode, signal A/$\overline{B}$ controls which channel is output first.

Figure 23 details the timing when using the RESET input. Note the current conversion, if any, is aborted and the data bus is high impedance while RESET is high.

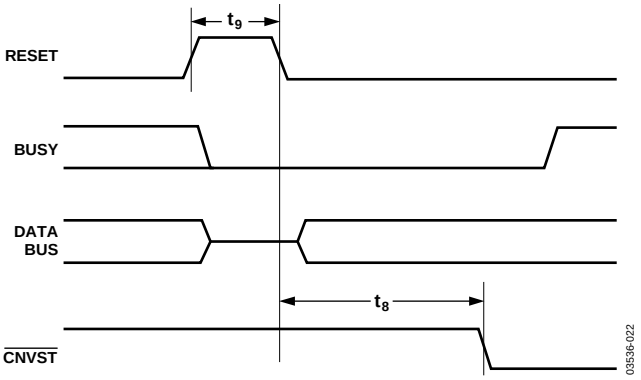


Figure 23. Reset Timing

PARALLEL INTERFACE

The AD7655 is configured to use the parallel interface when SER/$\overline{PAR}$ is held low.

Master Parallel Interface

Data can be read continuously by tying $\overline{CS}$ and $\overline{RD}$ low, thus requiring minimal microprocessor connections. However, in this mode the data bus is always driven and cannot be used in shared bus applications (unless the device is held in RESET). Figure 24 details the timing for this mode.

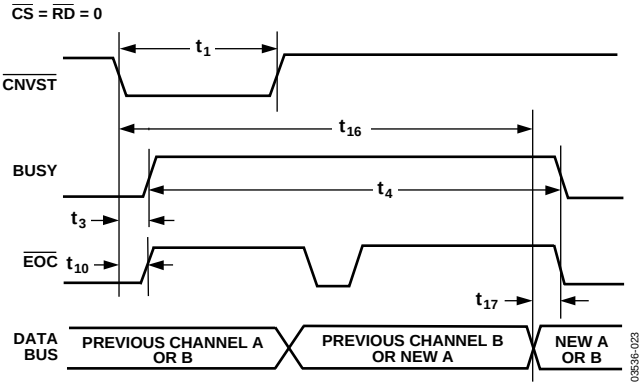


Figure 24. Master Parallel Data Timing for Reading (Continuous Read)

Slave Parallel Interface

In slave parallel reading mode, the data can be read either after each conversion, which is during the next acquisition phase, or during the other channel's conversion, or during the following conversion, as shown in Figure 25 and Figure 26, respectively. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

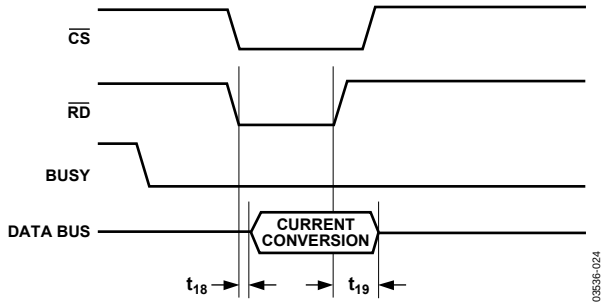


Figure 25. Slave Parallel Data Timing for Reading (Read after Convert)

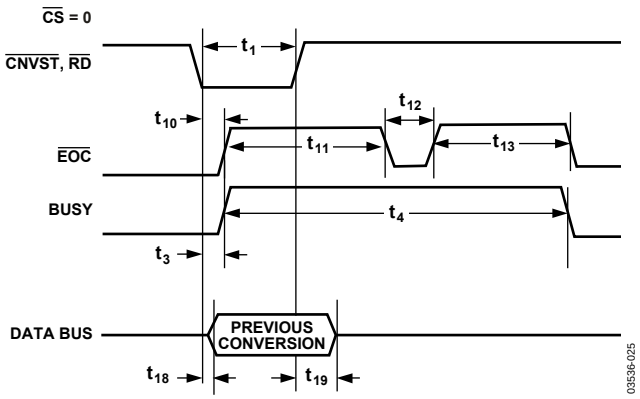


Figure 26. Slave Parallel Data Timing for Reading (Read During Convert)

8-Bit Interface (Master or Slave)

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 27, the LSB byte is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is low. When BYTESWAP is high, the LSB and MSB bytes are swapped, the LSB is output on D[15:8], and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16-bit data can be read in 2 bytes on either D[15:8] or D[7:0].

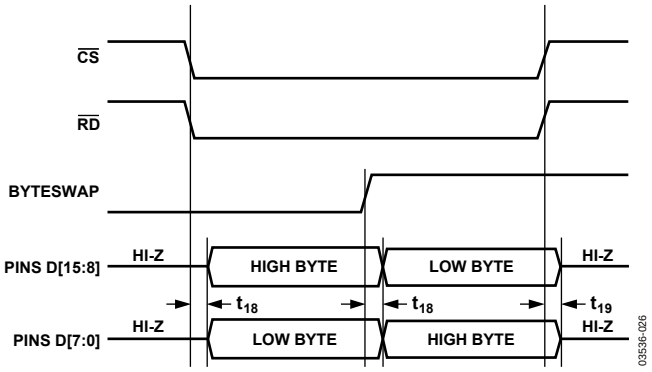


Figure 27. 8-Bit Parallel Interface

Channel A/$\overline{B}$ Output

The A/$\overline{B}$ input controls which channel's conversion results (INAx or INBx) are output on the data bus. The functionality of A/$\overline{B}$ is detailed in Figure 28. When high, the data from Channel A is available on the data bus. When low, the data from Channel B is available on the bus. Note that in parallel reading mode, Channel A can be read immediately after the end of conversion ($\overline{EOC}$), while Channel B is still in its converting phase. However, in any of the serial reading modes Channel A data is updated only after Channel B conversion.

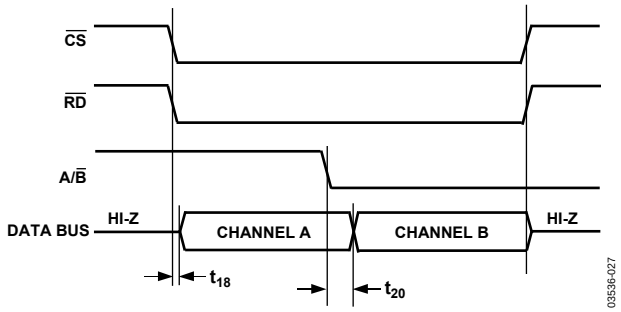


Figure 28. A/$\overline{B}$ Channel Reading

SERIAL INTERFACE

The AD7655 is configured to use the serial interface when the SER/$\overline{PAR}$ is held high. The AD7655 outputs 32 bits of data, MSB first, on the SDOUT pin. The order of the channels being output is also controlled by A/$\overline{B}$. When high, Channel A is output first; when low, Channel B is output first. This data is synchronized with the 32 clock pulses provided on the SCLK pin.

MASTER SERIAL INTERFACE

Internal Clock

The AD7655 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{INT}$ pin is held low. The AD7655 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted, if desired, using the INVSCLK and INVSYNC inputs, respectively. The output data is valid on both the rising and falling edge of the data clock. In this mode, the D7/RDC/SDIN input is used to select between reading after conversion (RDC = low) or reading previous conversion results during conversion (RDC = high). Figure 29 and Figure 30 show the detailed timing diagrams of these two modes.

Usually, because the AD7655 is used with a fast throughput, the master read during convert mode is the most recommended serial mode when it can be used. In this mode, the serial clock and data toggle at appropriate instants, which minimizes potential feed through between digital activity and the critical conversion decisions. The SYNC signal goes low after the LSB of each channel has been output. Note that in this mode, the SCLK period changes because the LSBs require more time to settle, and the SCLK is derived from the SAR conversion clock.

Note that in master read after convert mode, unlike in other modes, the BUSY signal returns low after the 32 bits of data are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width. One advantage of using this mode is that it can accommodate slow digital hosts because the serial clock can be slowed down by using the DIVSCLK[1:0] inputs. Refer to Table 4 for the timing details.

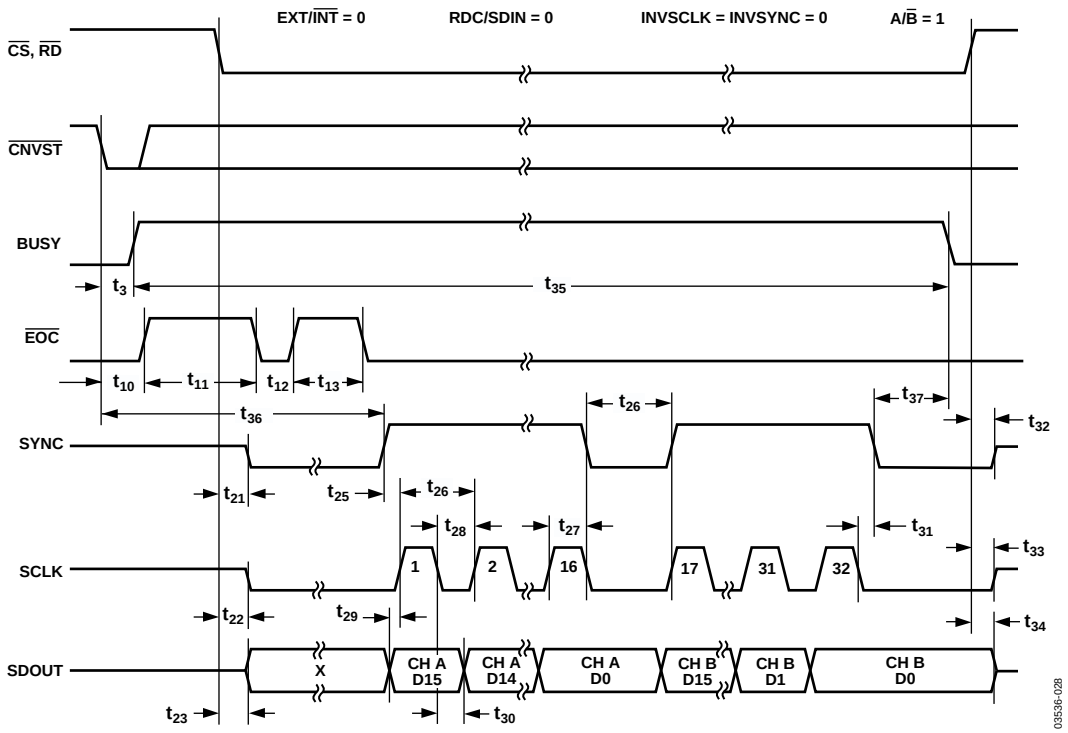


Figure 29. Master Serial Data Timing for Reading (Read After Convert)

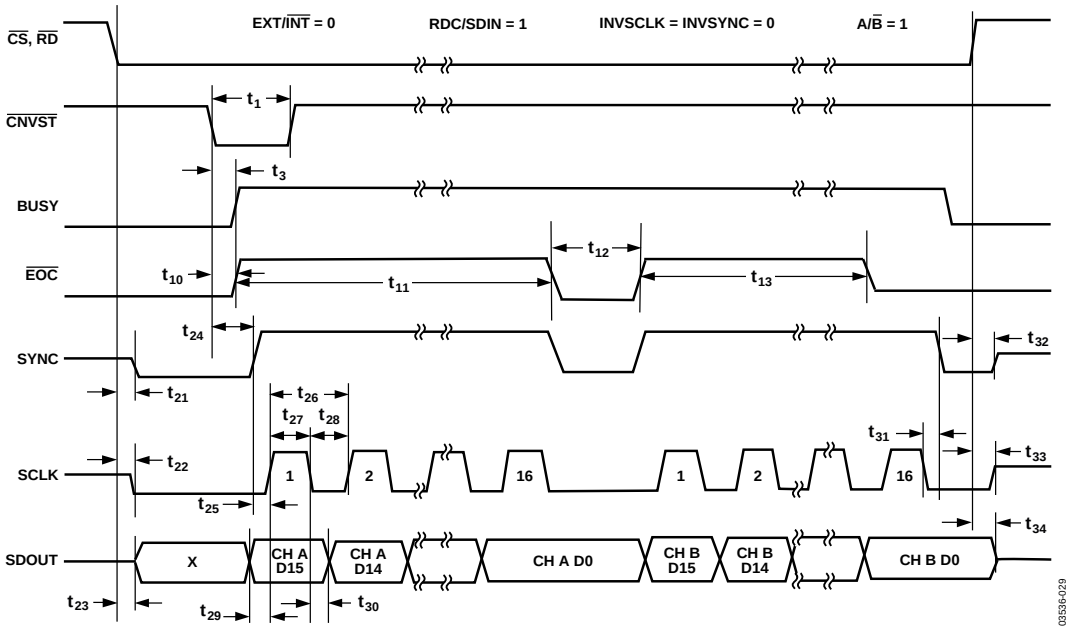


Figure 30. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

SLAVE SERIAL INTERFACE

External Clock

The AD7655 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{INT}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{CS}$. When both $\overline{CS}$ and $\overline{RD}$ are low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 32 and Figure 33 show the detailed timing diagrams of these methods.

While the AD7655 is performing a bit decision, it is important that voltage transients do not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase of each channel, because the AD7655 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of $\overline{EOC}$ high.

External Discontinuous Clock Data Read After Convert

Although the maximum throughput cannot be achieved in this mode, it is the most recommended of the serial slave modes. Figure 32 shows the detailed timing diagrams of this mode. After a conversion is complete, indicated by BUSY returning low, the conversion results can be read while both $\overline{CS}$ and $\overline{RD}$ are low. Data is shifted out from both channels' MSB first, with 32 clock pulses, and is valid on both rising and falling edges of the clock.

Among the advantages of using this mode is that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 40 MHz, which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7655 provides a daisy-chain feature using the RDC/SDIN (serial data in) input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when it is desired, as in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 31. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. Note that the RDC/SDIN input is latched on the edge of SCLK opposite the one used to shift out the data on SDOUT. Therefore, the MSB of the upstream converter follows the LSB of the downstream converter on the next SCLK cycle. The SDIN input should be tied either high or low on the most upstream converter in the chain.

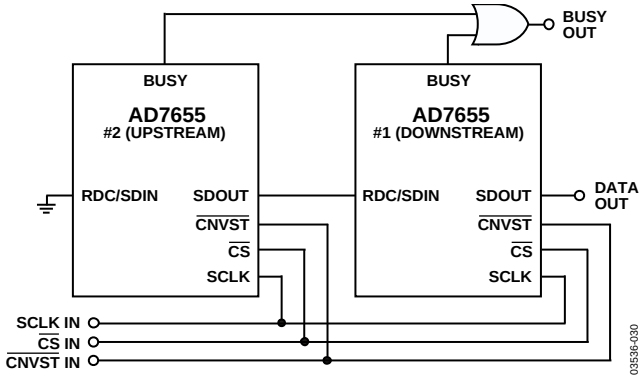


Figure 31. Two AD7655 Devices in a Daisy-Chain Configuration

External Clock Data Read (Previous) During Convert

Figure 33 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 32 clock pulses, and is valid on both the rising and falling edges of the clock. The 32 bits have to be read before the current conversion is completed; otherwise, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode, and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock (at least 32 MHz in impulse mode and 40 MHz in normal mode) is recommended to ensure that all of the bits are read during the first half of each conversion phase ($\overline{EOC}$ high, t_{11}, t_{12}).

It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion has been initiated. This allows the use of a slower clock speed such as 26 MHz in impulse mode and 30 MHz in normal mode.

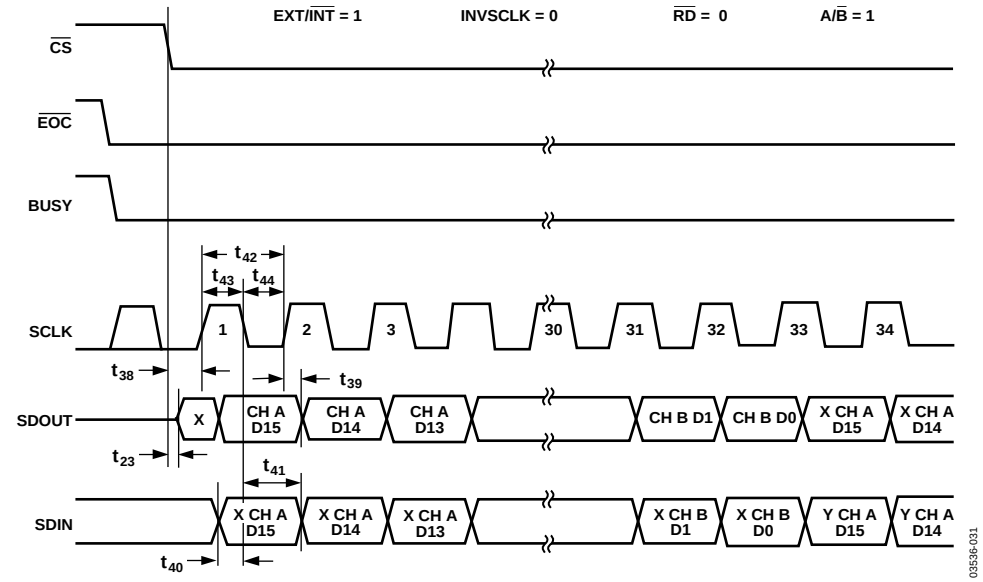


Figure 32. Slave Serial Data Timing for Reading (Read After Convert)

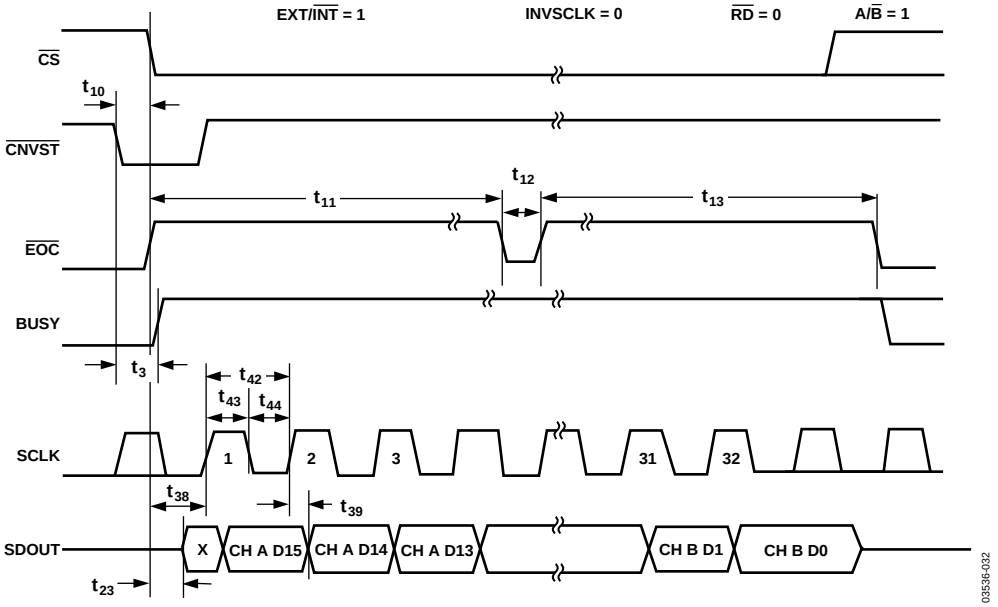


Figure 33. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

MICROPROCESSOR INTERFACING

The AD7655 is ideally suited for traditional dc measurement applications supporting a microprocessor and for ac signal processing applications interfacing to a digital signal processor. The AD7655 is designed to interface with either a parallel 8-bit wide or 16-bit wide interface, a general-purpose serial port, or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7655 to prevent digital noise from coupling into the ADC. The following section describes the use of the AD7655 with an SPI-equipped DSP, the ADSP-2191M.

SPI INTERFACE (ADSP-2191M)

Figure 34 shows an interface diagram between the AD7655 and the SPI1-equipped ADSP-2191M. To accommodate the slower speed of the DSP, the AD7655 acts as a slave device and data must be read after conversion. This mode also allows the daisy-chain feature to be used. The convert command can be initiated in response to an internal timer interrupt. The 32-bit output data is read with two serial peripheral interface (SPI) 16-bit wide accesses.

The reading process can be initiated in response to the end of conversion signal (BUSY going low) using an interrupt line of the DSP. The SPI on the ADSP-2191M is configured for master mode—(MSTR) = 1, Clock Polarity bit (CPOL) = 0, Clock Phase bit (CPHA) = 1, and SPI Interrupt Enable (TIMOD) = 00—by writing to the SPI control register (SPICLTx). To meet all timing requirements, the SPI clock should be limited to 17 Mbps, which allows it to read an ADC result in less than 1 µs. When a higher sampling rate is desired, use of one of the parallel interface modes is recommended.

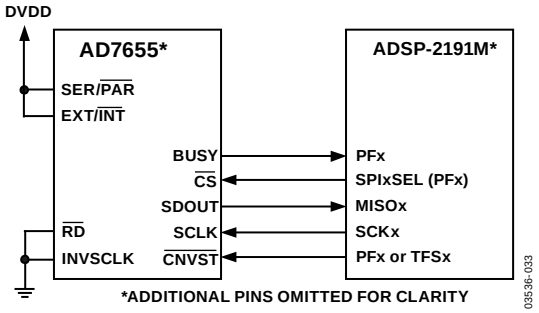


Figure 34. Interfacing the AD7655 to SPI Interface

APPLICATION HINTS

LAYOUT

The AD7655 has very good immunity to noise on the power supplies. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7655 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7655, or as close as possible to the AD7655. If the AD7655 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7655.

Avoid running digital lines under the device because these couple noise onto the die. The analog ground plane should be allowed to run under the AD7655 to avoid noise coupling. Fast switching signals such as $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This reduces the effect of crosstalk through the board.

The power supply lines to the AD7655 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supply impedance presented to the AD7655 and to reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supply pin—AVDD, DVDD, and OVDD—close to, and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located near the ADC to further reduce low frequency ripple.

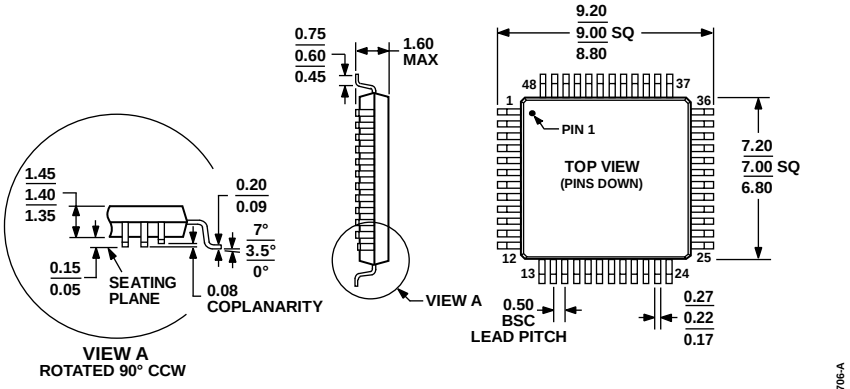
The DVDD supply of the AD7655 can be a separate supply or can come from the analog supply AVDD or the digital interface supply OVDD. When the system digital supply is noisy or when fast switching digital signals are present, if no separate supply is available, the user should connect DVDD to AVDD through an RC filter (see Figure 18) and the system supply to OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD7655 has five ground pins: INGND, REFGND, AGND, DGND, and OGND. INGND is used to sense the analog input signal. REFGND senses the reference voltage and, because it carries pulsed currents, should be a low impedance return to the reference. AGND is the ground to which most internal ADC analog signals are referenced; it must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

EVALUATING THE AD7655 PERFORMANCE

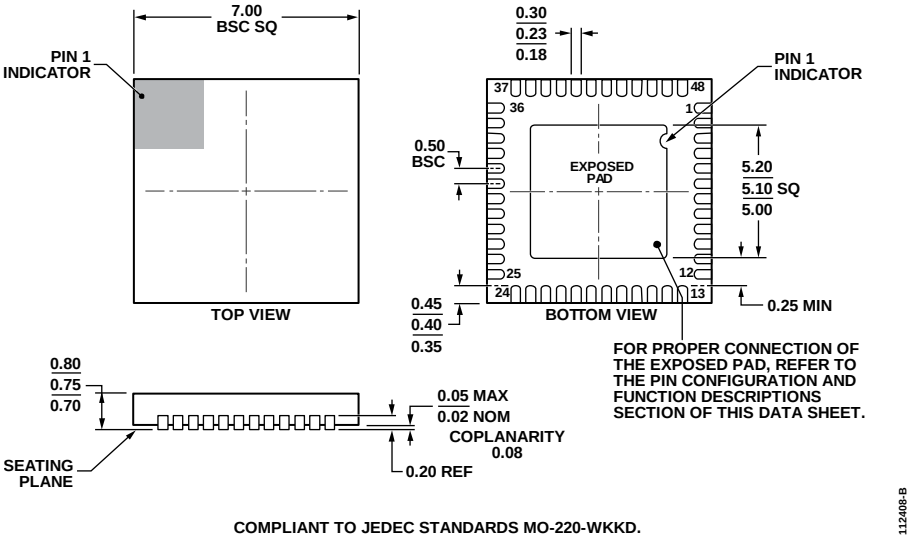
A recommended layout for the AD7655 is outlined in the EVAL-AD7655EDZ evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CED1Z.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 35. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD.

Figure 36. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7655ACPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-4
AD7655ASTZ	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7655ASTZRL	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
EVAL-AD7655EDZ		Evaluation Board	
EVAL-CED1Z		Controller Board	

[1] Z = RoHS Compliant Part.

D03536-0-12/16(E)