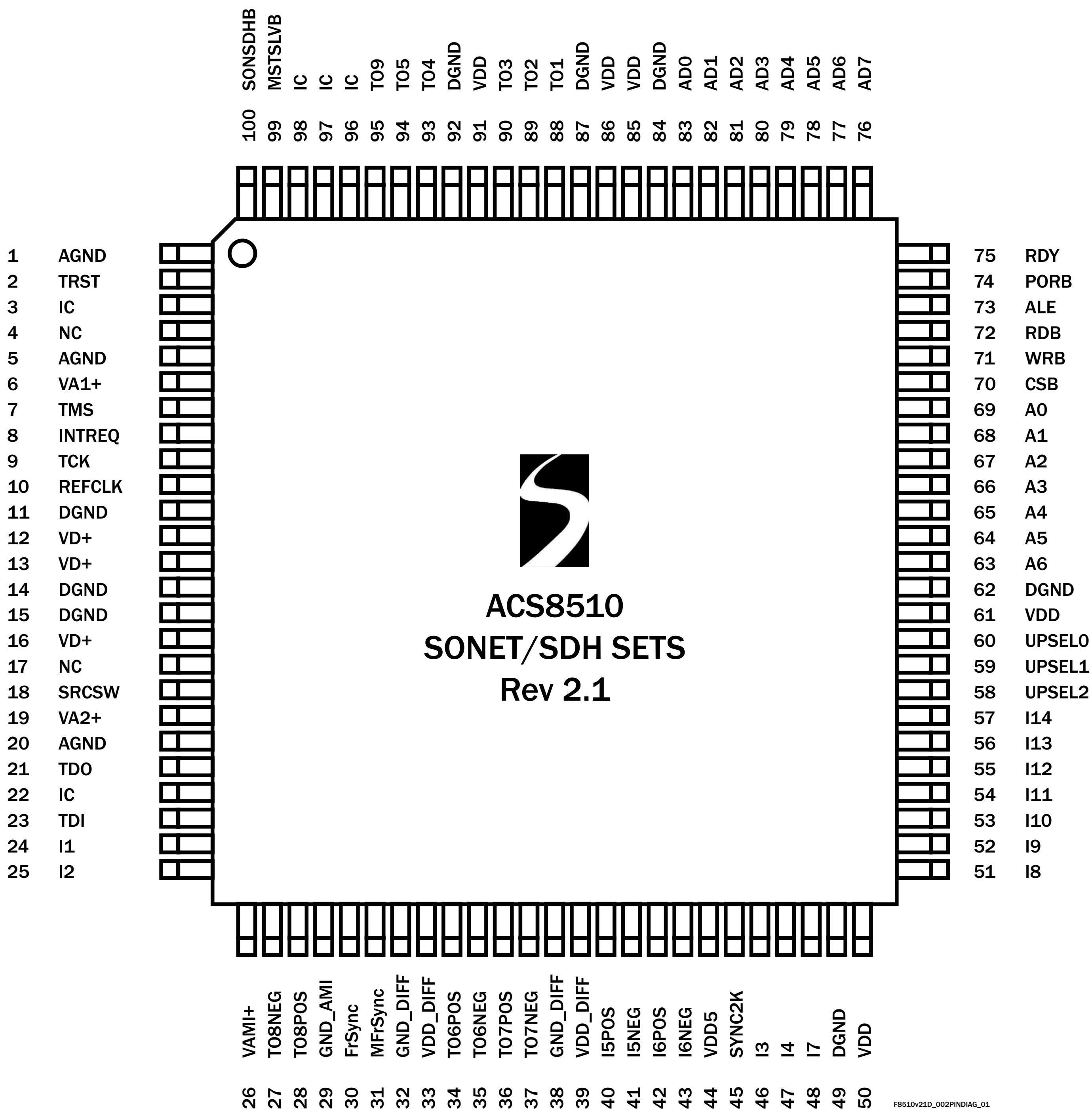
Table of Contents

Section **Page**

Pin Diagram

Figure 2 ACS8510 Rev2.1 Pin Diagram Synchronous Equipment Timing Source for SONET or SDH Network Elements



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
12, 13, 16	VD+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.
26	VAMI+	P	-	Supply Voltage: Digital supply to AMI output, +3.3 Volts ±10%.
33, 39	VDD_DIFF	P	-	Supply Voltage: Digital supply for differential ports, +3.3 Volts ±10%.
44	VDD5	P	-	Digital Supply for +5 Volts Tolerance to Input Pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
50, 61, 85, 86 91	VDD	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.
6	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.
19	VA2+	P	-	Supply Voltage: Analog supply to output PLLs, +3.3 Volts ±10%.
11, 14, 15, 49, 62, 84, 87, 92	DGND	P	-	Supply Ground: Digital ground for logic
29	GND_AMI	P	-	Supply Ground: Digital ground for AMI output.
32, 38	GND_DIFF	P	-	Supply Ground: Digital ground for differential ports.
1, 5, 20	AGND	P	-	Supply Ground: Analog grounds.

Note...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Not Connected or Internally Connected Pins

Pin Number	Symbol	I/O	Type	Description
4, 17	NC	NC	-	Not connected: Leave to Float
3, 22, 96, 97, 98	IC	IC	-	Internally Connected: Leave to Float.

Table 3 Other Pins

Pin Number	Symbol	I/O	Type	Description
2	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for Boundary Scan stand-by mode, still allowing correct device operation. If not used connect to GND or leave floating.
7	TMS	I	TTL^U	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
8	INTREQ	O	TTL/CMOS	Interrupt Request: Active *High* software Interrupt output.
9	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input. If not used connect to GND or leave floating. This pin may require a capacitor placed between the pin and the nearest GND, to reduce noise pickup. A value of 10 pF should be adequate, but the value is dependent on PCB layout.
10	REFCLK	I	TTL	Reference Clock: 12.800 MHz (refer to “Local Oscillator Clock” on page 8).
18	SRCSW	I	TTL_D	Source Switching: Force Fast Source Switching.
21	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK. If not used leave floating.
23	TDI	I	TTL^U	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. If not used connect to VDD or leave floating.
24	I1	I	AMI	Input Reference 1: Composite clock 64 kHz + 8 kHz.
25	I2	I	AMI	Input Reference 2: Composite clock 64 kHz + 8 kHz.
27	TO8NEG	O	AMI	Output Reference 8: Composite clock, 64 kHz + 8 kHz negative pulse.
28	TO8POS	O	AMI	Output Reference 8: Composite clock, 64 kHz + 8 kHz positive pulse.
30	FrSync	O	TTL/CMOS	Output Reference 10: 8 kHz Frame Sync output (square wave).
31	MFrSync	O	TTL/CMOS	Output Reference 11: 2 kHz Multi-Frame Sync output (square wave).
34, 35	TO6POS, TO6NEG	O	LVDS/PECL	Output Reference 6: Programmable, default 38.88 MHz. Also Dig1 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 19.44 MHz, 155.52 MHz, 311.04 MHz. Default type LVDS.
36, 37	TO7POS, TO7NEG	O	PECL/LVDS	Output Reference 7: Programmable, default 19.44 MHz, Also 51.84 Also 51.84 MHz, 77.76 MHz, 155.52 MHz. MHz, 77.76 MHz, 155.52 MHz. default type PECL.
40, 41	I5POS, I5NEG	I	LVDS/PECL	Input Reference 5: Default 19.44 MHz, default type LVDS.
42, 43	I6POS, I6NEG	I	PECL/LVDS	Input Reference 6: Default 19.44 MHz, default type PECL.
45	SYNC2K	I	TTL_D	Synchronize 2 kHz: Connect to 2 kHz Multi-Frame Sync output of partner ACS8510 Rev2.1 in redundancy system.
46	I3	I	TTL_D	Input Reference 3: Programmable, default 8 kHz.
47	I4	I	TTL_D	Input Reference 4: Programmable, default 8 kHz.
48	I7	I	TTL_D	Input Reference 7: Programmable, default 19.44 MHz.
51	I8	I	TTL_D	Input Reference 8: Programmable, default 19.44 MHz.

Table 3 Other Pins (cont...)

Pin Number	Symbol	I/O	Type	Description
52	I9	I	TTL_D	Input Reference 9: Programmable, default 19.44 MHz.
53	I10	I	TTL_D	Input Reference 10: Programmable, default 19.44 MHz.
54	I11	I	TTL_D	Input Reference 11: Programmable, default (Master mode) 1.544/2.048 MHz, default (Slave mode) 6.48 MHz.
55	I12	I	TTL_D	Input Reference 12: Programmable, default 1.544/2.048 MHz.
56	I13	I	TTL_D	Input Reference 13: Programmable, default 1.544/2.048 MHz.
57	I14	I	TTL_D	Input Reference 14: Programmable, default 1.544/2.048 MHz.
58 - 60	UPSEL(2:0)	I	TTL_D	Microprocessor Select: Configures the interface for a particular microprocessor type at reset.
63 - 69	A(6:0)	I	TTL_D	Microprocessor Interface Address: Address bus for the microprocessor interface registers. A(0) is SDI in Serial mode - output in EPROM mode only.
70	CSB	I	TTL^U	Chip Select (Active *Low*): This pin is asserted *Low* by the microprocessor to enable the microprocessor interface - output in EPROM mode only.
71	WRB	I	TTL^U	Write (Active *Low*): This pin is asserted *Low* by the microprocessor to initiate a write cycle. In Motorola mode, WRB = 1 for Read.
72	RDB	I	TTL^U	Read (Active *Low*): This pin is asserted *Low* by the microprocessor to initiate a read cycle.
73	ALE	I	TTL_D	Address Latch Enable: This pin becomes the address latch enable from the microprocessor. When this pin transitions from *High* to *Low*, the address bus inputs are latched into the internal registers. ALE = SCLK in Serial mode.
74	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced *Low*, all internal states are reset back to default values.
75	RDY	O	TTL/CMOS	Ready/Data Acknowledge: This pin is asserted *High* to indicate the device has completed a read or write operation.
76 - 83	AD(7:0)	IO	TTL_D	Address/Data: Multiplexed data/address bus depending on the microprocessor mode selection. AD(0) is SDO in Serial mode.
88	TO1	O	TTL/CMOS	Output Reference 1: Programmable, default 6.48 MHz. Also Dig1 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 19.44 MHz, 25.92 MHz
89	TO2	O	TTL/CMOS	Output Reference 2: Programmable, default 38.88 MHz. Also Dig2 (1.544 MHz/2.048 MHz and 2, 4, 8 x), 25.92 MHz, 51.84 MHz
90	TO3	O	TTL/CMOS	Output Reference 3: 19.44 MHz - fixed.
93	TO4	O	TTL/CMOS	Output Reference 4: 38.88 MHz - fixed.
94	TO5	O	TTL/CMOS	Output Reference 5: 77.76 MHz - fixed.
95	TO9	O	TTL/CMOS	Output Reference 9: 1.544/2.048 MHz, as per ITU G.783[9] BITS requirements.
99	MSTSLVB	I	TTL^U	Master/Slave Select: Sets the initial power up state (or state after a PORB) of the Master/Slave selection register. The register state can be changed after power up by software.

Table 3 Other Pins (cont...)

Pin Number	Symbol	I/O	Type	Description
100	SONSDHB	I	TTL_D	SONET or SDH Frequency Select: Sets the initial power-up state (or state after a PORB) of the SONET/SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5 and Bit 6. When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Functional Description

The ACS8510 Rev2.1 is a highly integrated, single-chip solution for the SETS function in a SONET/SDH Network Element, for the generation of SEC and frame synchronization pulses.

In Free-run mode, the ACS8510 Rev2.1 generates a stable, low noise clock signal from an internal oscillator.

In Locked mode, the ACS8510 Rev2.1 selects the most appropriate input reference source and generates a stable, low-noise clock signal locked to the selected reference.

In Holdover mode, the ACS8510 Rev2.1 generates a stable, low-noise clock signal from the internal oscillator, adjusted to match the last known good frequency of the last selected reference source.

In all modes, the frequency accuracy, jitter and drift performance of the clock meet the requirements of ITU G.812, G.813, G.823, and GR-1244-CORE.

The ACS8510 Rev2.1 supports all three types of reference clock source: recovered line clock (T_{IN1}), PDH network synchronization timing (T_{IN2}) and node synchronization (T_{IN3}). The ACS8510 Rev2.1 generates independent T_{OUT0} and T_{OUT4} clocks, an 8 kHz Frame Synchronization clock and a 2 kHz Multi-Frame Synchronization clock.

The ACS8510 Rev2.1 has a high tolerance to input jitter and wander. The jitter/wander transfer is programmable (0.1 Hz up to 20 Hz cut-off points).

The ACS8510 Rev2.1 supports protection. Two ACS8510 Rev2.1 devices can be configured to provide protection against a single ACS8510 Rev2.1 failure.

The protection maintains alignment of the two ACS8510 Rev2.1 devices (Master and Slave) and

ensures that both ACS8510 Rev2.1 devices maintain the same priority table, choose the same reference input and generate the T_{OUT0} clock, the 8 kHz Frame Synchronization clock and the 2 kHz Multi-Frame Synchronization clock with the same phase.

The ACS8510 Rev2.1 includes a microprocessor port, providing access to the configuration and status registers for device setup and monitoring.

Local Oscillator Clock

The Master system clock on the ACS8510 Rev2.1 should be provided by an external clock oscillator of frequency 12.80 MHz. The clock specification is important for meeting the ITU/ETSI and Telcordia performance requirements for Holdover mode. ITU and ETSI specifications permit a combined drift characteristic, at constant temperature, of all non-temperature related parameters, of up to 10 ppb per day. The same specifications allow a drift of 1 ppm over a temperature range of 0 to +70°C.

Table 4 ITU and ETSI Specification

Parameter	Value
Tolerance	±4.6 ppm over 20 year lifetime
Drift (Frequency Drift over supply voltage range of +2.7 V to +3.3 V)	±0.05 ppm/15 seconds @ constant temp.
	±0.01 ppm/day @ constant temp.
	±1 ppm over temp. range 0 to +70°C

Telcordia specifications are somewhat tighter, requiring a non-temperature-related drift of less than 40 ppb per day and a drift of 280 ppb over the temperature range 0 to +50°C.

Table 5 Telcordia GR-1244 CORE Specification

Parameter	Value
Tolerance	±4.6 ppm over 20 year lifetime

Table 5 Telcordia GR-1244 CORE Specification

Drift (Frequency Drift over supply voltage range of +2.7 V to +3.3 V)	±0.05 ppm/15 seconds @ constant temp.
	±0.04 ppm/15 seconds @ constant temp.
	±0.28 ppm/over temp. range 0 to +50°C

Please contact Semtech for information on crystal oscillator suppliers.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. ± 50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8-bit register locations. The setting of the *conf_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.02 ppm for each LSB step. The default value (in decimal) is 39321. The minimum being 0 and the maximum 65535, gives a -700 ppm to +500 ppm adjustment range of the output frequencies.

For example, if the crystal was oscillating at 12.8 MHz + 5 ppm, then the calibration value in the register to give a -5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be:

39321 - (5 / 0.02) = 39071 (decimal)

Input Interfaces

The ACS8510 Rev2.1 supports up to fourteen input reference clock sources from input types T_{IN1}, T_{IN2} and T_{IN3} using TTL, CMOS, PECL, LVDS and AMI buffer I/O technologies. These interface technologies support +3.3 V and +5 V operation.

Over-Voltage Protection

The ACS8510 Rev2.1 may require Over-Voltage Protection on input reference clock ports according to ITU Recommendation K.41. Semtech protection devices are recommended for this purpose (see separate Semtech data book).

Input Reference Clock Ports

Table 6 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown. Note that SDH and SONET networks use different default frequencies; the network type is pin-selectable using the SONSDHB pin). Specific frequencies and priorities are set by configuration.

Although each input port is shown as belonging to one of the types, T_{IN1}, T_{IN2} or T_{IN3}, they are fully interchangeable as long as the selected speed is within the maximum operating speed of the input port technology.

SDH and SONET networks use different default frequencies; the network type is selectable using the *config_mode* register 34 Hex, bit 2.

For SONET, *config_mode* register 34 Hex, bit 2 = 1, for SDH *config_mode* register 34 Hex, bit 2 = 0. On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 100). Specific frequencies and priorities are set by configuration.

TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies supported are:

- 2 kHz
- 4 kHz
- 8 kHz (and N x 8 kHz)
- 1.544 MHz (SONET)/2.048 MHz (SDH)
- 6.48 MHz,
- 19.44 MHz,
- 25.92 MHz,
- 38.88 MHz,
- 51.84 MHz,
- 77.76 MHz.

The frequency selection is programmed via the *cnfg_ref_source_frequency* register. The internal DPLL will normally lock to the selected input at the frequency of the input, e.g. 19.44 MHz will lock the DPLL phase comparisons at 19.44 MHz. It is, however, possible to utilize an internal pre-divider to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL. This pre-divider can be used in one of 2 ways:

1. Any of the supported spot frequencies can be divided to 8 kHz by setting the *lock8K* bit (bit 6) in the appropriate *cnfg_ref_source_frequency* register location. For good jitter tolerance for all frequencies and for operation at 19.44 MHz and above, use lock8K. It is possible to choose which edge of the 8 kHz input to lock to, by setting the appropriate bit of the *cnfg_control1* register.
2. Any multiple of 8 kHz between 1544 kHz to 100 MHz can be supported by using the *DivN* feature (bit 7 of the *cnfg_ref_source_frequency* register). Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs.

Any reference input with the DivN bit set in the *cnfg_ref_source_frequency* register will employ the internal pre-divider prior to the DPLL locking.

The *cnfg_freq_divn* register contains the divider ratio N where the reference input will get divided by (N+1) where $0<N<2^{14}-1$. The *cnfg_ref_source_frequency* register must be set to the closest supported spot frequency to the input frequency, but must be lower than the input frequency. When using the DivN feature the post-divider frequency must be 8 kHz, which is indicated by setting the *lock8k* bit high (bit 6 in *cnfg_ref_source_frequency* register). Any input set to DivN must have the frequency monitors disabled (If the frequency monitors are disabled, they are disabled for all inputs regardless of the input configurations, in this case only activity monitoring will take place). Whilst any number of inputs can be set to use the DivN feature, only one N can be programmed, hence all inputs using the DivN feature must require the same division to get to 8 kHz.

Table 6 Input Reference Source Selection and Priority Table

Port Number	Channel Number (Bin)	Port Type	Input Port Technology	Frequencies Supported	Default Priority
I_1	0001	T_{IN3}	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	2
I_2	0010	T_{IN3}	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz) Default (SONET): 64/8 kHz Default (SDH): 64/8 kHz	3
I_3	0011	T_{IN3}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	4
I_4	0100	T_{IN3}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	5
I_5	0101	T_{IN1}	LVDS/PECL LVDS default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	6
I_6	0110	T_{IN1}	PECL/LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	7
I_7	0111	T_{IN1}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	8
I_8	1000	T_{IN1}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	9

Table 6 Input Reference Source Selection and Priority Table (cont...)

Port Number	Channel Number (Bin)	Port Type	Input Port Technology	Frequencies Supported	Default Priority
I_9	1001	T_{IN1}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	10
I_10	1010	T_{IN1}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	11
I_11	1011	T_{IN2}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (Master) (SONET): 1.544 MHz Default (Master) (SDH): 2.048 MHz Default (Slave) 6.48 MHz	12/1 (Note (iii))
I_12	1100	T_{IN2}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	13
I_13	1101	T_{IN2}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	14
I_14	1110	T_{IN2}	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 1.544 MHz Default (SDH): 2.048 MHz	15

Notes: (i) TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH is selected using the SONSDHB pin. When the SONSDHB pin is High SONET is selected, when the SONSDHB pin is Low SDH is selected.

(ii) PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz and 311.04 MHz.

(iii) Input port <I_11> is set at 12 on the Master SETS IC and 1 on the Slave SETS IC, as default on power up (or PORB). The default setup of Master or Slave <I_11> priority is determined by the MSTSLVB pin.

DivN Examples

To lock to 2.000 MHz.

1. The *cnfg_ref_source_frequency* register is set to 11XX0001 (binary) to set the DivN, lock8k bits, and the frequency to E1/DS1. (XX = “leaky bucket” ID for this input).
2. The *cnfg_mode* register (34Hex) bit 2 needs to be set to 1 to select SONET frequencies (DS1).
3. The frequency monitors are disabled in *cnfg_monitors* register (48Hex) by writing 00 to bits 0 and 1.
4. The DivN register is set to F9 Hex (249 decimal).

To lock to 10.000 MHz.

1. The *cnfg_ref_source_frequency* register is set to 11XX0010 (binary) to set the DivN, lock8k bits, and the frequency to 6.48 MHz. (XX = “leaky bucket” ID for this input).
2. The frequency monitors are disabled in *cnfg_monitors* register (48Hex) by writing 00 to bits 0 and 1.
3. The DivN register is set to 4E1 Hex (1249 decimal).

PECL and LVDS ports support the spot clock frequencies listed plus 155.52 MHz and 311.04 MHz. The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register. Unused PECL/LVDS differential inputs should be fixed with one input high (VDD) and the other input low (GND), or set in LVDS mode and left floating, in which case one input is internally pulled high and the other low.

An AMI port supports a composite clock, consisting of a 64 kHz AMI clock with 8 kHz boundaries marked by deliberate violations of the AMI coding rules, as specified in ITU recommendation G.703. Departures from the nominal pattern are detected within the ACS8510 Rev2.1, and may cause reference-switching if too frequent. See “DC Characteristics: AMI Input/Output Port” on page 53 for more details. If the AMI port is unused, the pins (I1 and I2) should be tied to GND and the VAMI+ supply pin (pin 26) disconnected.

Input Wander and Jitter Tolerance

The ACS8510 Rev2.1 is compliant to the requirements of all relevant standards, principally ITU Recommendation G.825, ANSI DS1.101-1994 and ETS 300 462-5 (1997).

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Pullin, hold-in and pull-out ranges are specified for each input port in Table 7. Minimum jitter tolerance masks are specified in Figures 3 and 4, and Tables 8 and 9, respectively. The ACS8510 Rev2.1 will tolerate wander and jitter components greater than those shown in Figure 3 and Figure 4, up to a limit determined by a combination of the apparent long-term frequency offset caused by wander and the eye-closure caused by jitter (the input source will be rejected if the offset pushes the frequency outside the hold-in range for long enough to be detected, whilst the signal will also be rejected if the eye closes sufficiently to affect the signal purity). The “8klocking” mode should be engaged for high jitter tolerance according to these masks. All reference clock ports are monitored for quality, including frequency offset and general activity. Single short-term interruptions in selected reference clocks may not cause rearrangements, whilst longer interruptions, or multiple, short-term interruptions, will cause rearrangements, as will frequency offsets which are sufficiently large or sufficiently long to cause loss-of-lock in the phase-locked loop. The failed reference source will be removed from the priority table and declared as unserviceable, until its perceived quality has been restored to an acceptable level.

The registers *sts_curr_inc_offset* (address 0C, 0D, 07) report the frequency of the DPLL with respect to the external TCXO frequency. This is a 19-bit signed number with one LSB representing 0.0003 ppm (range of ±80 ppm). Reading this regularly can show how the currently locked source is varying in value e.g. due to wander on its input.

The ACS8510 Rev2.1 performs automatic frequency monitoring with an acceptable input frequency offset range of ±16.6 ppm. The ACS8510 Rev2.1 DPLL has a programmable frequency limit of ±80 ppm. If the range is programmed to be > 16.6 ppm, the frequency monitors should be disabled so the input reference source is not automatically rejected as out of frequency range..

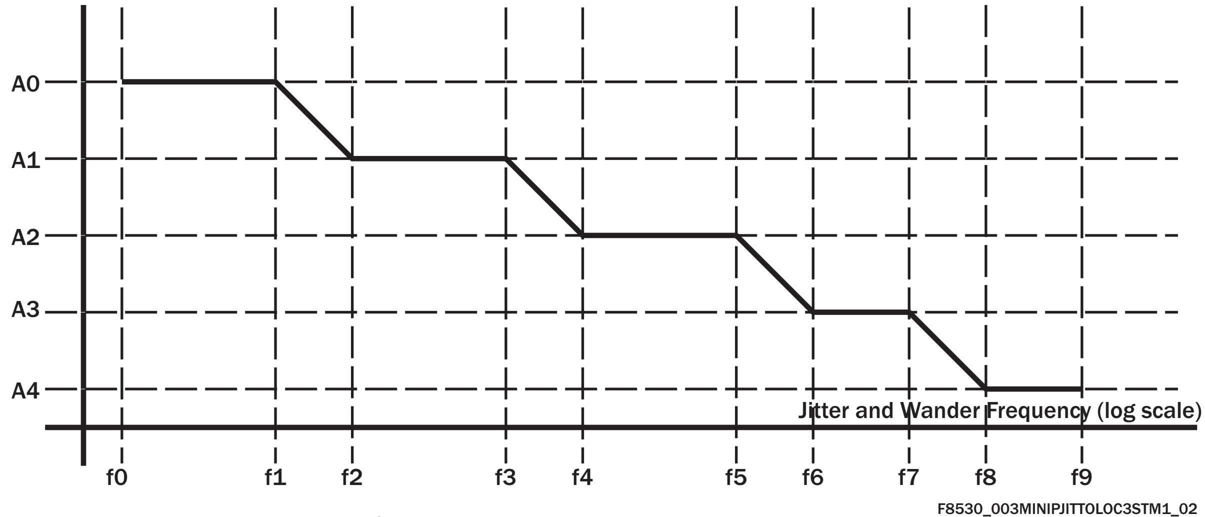
Table 7 Input Reference Source Jitter Tolerance

Jitter Tolerance	Frequency Monitor Acceptance Range	Frequency Acceptance Range (Pull-in)	Frequency Acceptance Range (Hold-in)	Frequency Acceptance Range (Pull-out)
G.703	±16.6 ppm	±4.6 ppm (see Note (i))	±4.6 ppm (see Note (i))	±4.6 ppm (see Note (i))
G.783				
G.823		±9.2 ppm (see Note (ii))	±9.2 ppm (see Note (ii))	±9.2 ppm (see Note (ii))
GR-1244-CORE				

Notes: (i) *The frequency acceptance and generation range will be ±4.6 ppm around the required frequency when the external crystal frequency accuracy is within a tolerance of ±4.6 ppm.*

(ii) *The fundamental acceptance range and generation range is ± 9.2 ppm with an exact external crystal frequency of 12.8 MHz. This is the default DPLL range, the range is also programmable from 0 to 80 ppm in 0.08 ppm steps.*

Figure 3 Minimum Input Jitter Tolerance (OC-3/STM-1)



Note...For inputs supporting G.783[9] compliant sources.)

Table 8 Amplitude and Frequency Values for Jitter Tolerance (OC-3/STM-1)

STM level	Peak to peak amplitude (unit Interval)					Frequency (Hz)									
	A0	A1	A2	A3	A4	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9
STM-1	2800	311	39	1.5	0.15	12 u	178 u	1.6 m	15.6 m	0.125	19.3	500	6.5 k	65 k	1.3m

Frame Sync and MultiFrame Sync Clocks (Part of T_{OUT0})

Frame Sync (8 kHz) and MultiFrame Sync (2 kHz) clocks are provided on outputs T_{O10} (FrSync) and T_{O11} (MFrSync). The FrSync and MFrSync clocks have a 50:50 mark space ratio. These are driven from the T_{OUT0} clock. They are synchronized with their counterparts in a second ACS8510 Rev2.1 device (if used), using the technique described later.

Output Clock Ports

The device supports a set of main output clocks, T_{OUT0} and T_{OUT4}, and a pair of secondary output clocks, “Frame-Sync” and “Multi-Frame-Sync”. The two main output clocks, T_{OUT0} and T_{OUT4}, are independent of each other and are individually selectable. The two secondary output clocks, Frame-Sync and Multi-Frame-Sync, are derived from T_{OUT0}. The frequencies of the output clocks are selectable from a range of pre-defined spot frequencies and a variety of output technologies are supported, as defined in Table 10.

Low-speed Output Clock (T_{OUT4})

The T_{OUT4} clock is supplied on two output ports, T_{O8} and T_{O9}. The former port will provide an AMI signal carrying a composite clock of 64 kHz and 8 kHz, according to ITU Recommendation G.703. The latter port will provide a TTL/CMOS signal at either 1.544 MHz or 2.048 MHz, depending on the setting of the SONSDHB pin.

High-speed Output Clock (Part of T_{OUT0})

The T_{OUT0} port has multiple outputs. Outputs $T_{O1}$and T_{O2} are TTL/CMOS output with a choice of 11 different frequencies up to 51.84 MHz. Outputs T_{O3} to T_{O5} are all TTL/CMOS outputs with fixed frequencies of 19.44 MHz, 38.88 MHz and 77.76 MHz respectively. Output T_{O6} is differential and can support clocks up to 155.52 MHz. Output T_{O7} is also differential and can support clocks up to 155.52 MHz. Each output is individually configured to operate at the frequencies shown in Table 10 (configuration must be consistent between ACS8510 Rev2.1 devices for protection-switching to be effective - output clocks will be phase-aligned between devices). Using the *cnfg_differential_outputs* register, outputs T_{O6} and T_{O7} can be made to be LVDS or PECL compatible.

Figure 4 Minimum Input Jitter Tolerance (DS1/E1)

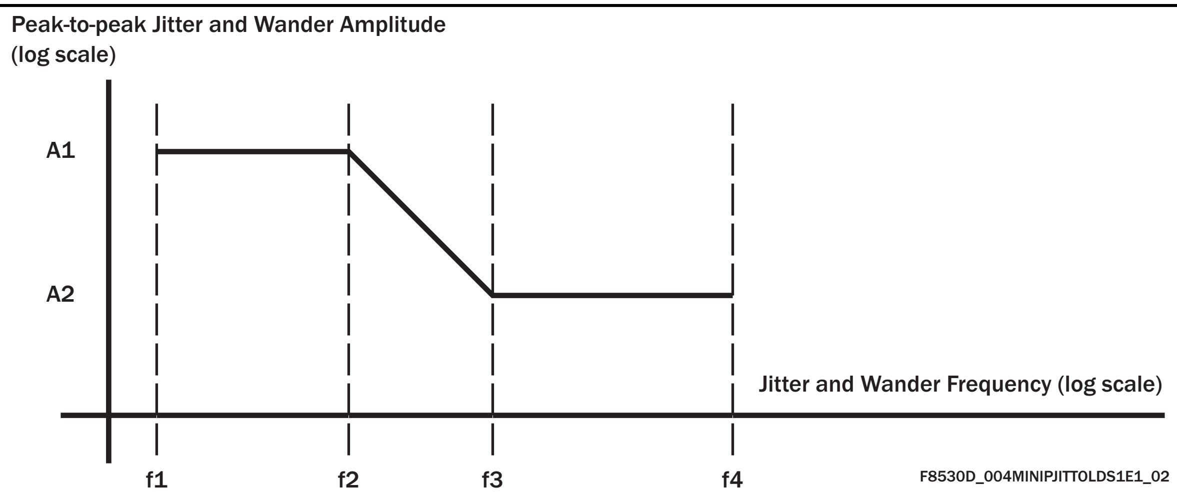


Table 9 Amplitude and Frequency Values for Jitter Tolerance (DS1/E1)

Type	Spec.	Amplitude (UI_{p-p})		Frequency (Hz)			
		A1	A2	F1	F2	F3	F4
DS1	GR-1244-CORE[19]	5	0.1	10	500	8 k	40 k
E1	ITU G.823[13]	1.5	0.2	20	2.4 k	18 k	100k

Low Jitter Multiple E1/DS1 Outputs

This feature added to Rev2.1 is activated using the *cnfg_control1* register. This sends a frequency of twice the Dig2 rate (see reg addr 39h, bits 7:6) to the APLL instead of the normal 77.76 MHz. For this feature to be used, the Dig2 rate must only be set to 12352 kHz/16384 kHz using the *cnfg_T0_output_frequencies* register. The normal OC-3 rate outputs are then replaced with E1/DS1 multiple rates. The E1(SONET)/DS1(SDH) selection is made in the same way as for Dig2 using the *cnfg_T0_output_enable* register.

Table 11 shows the relationship between primary output frequencies and the corresponding output in E1/DS1 mode, and which output they are available from.

Output Wander and Jitter

Wander and jitter present on the output clocks are dependent on:

1. The magnitude of wander and jitter on the selected input reference clock (in Locked mode)
2. The internal wander and jitter transfer characteristic (in Locked mode)
3. The jitter on the local oscillator clock
4. The wander on the local oscillator clock (in Holdover mode).

Wander and jitter are treated in different ways to reflect their differing impacts on network design. Jitter is always strongly attenuated, whilst wander attenuation can be varied to suit the application and operating state. Wander and jitter attenuation is performed using a digital phase locked loop (DPLL) with a programmable bandwidth. This gives a transfer characteristic of a low pass filter, with a programmable pole. It is sometimes necessary to change the filter dynamics to suit particular circumstances - one example being when locking to a new source, the filter can be opened up to reduce locking time and can then be gradually tightened again to remove wander. Since wander represents a relatively long-term deviation from the nominal operating frequency, it affects the rate of supply of data to the network element. Strong wander attenuation limits the rate of consumption of data to within a smaller range, so a larger buffer store is required to prevent data loss. But, since any buffer store potentially

Table 10 Output Reference Source Selection Table

Port Name	Output Port Technology	Frequencies Supported
T_{01}	TTL/CMOS	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 6.48 MHz (default), 12.352 MHz/16.384 MHz, 19.44 MHz, 25.92 MHz
T_{02}	TTL/CMOS	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 12.352 MHz/16.384 MHz, 25.92 MHz, 38.88 MHz (default), 51.84 MHz
T_{03}	TTL/CMOS	19.44 MHz - fixed
T_{04}	TTL/CMOS	38.88 MHz - fixed
T_{05}	TTL/CMOS	77.76 MHz - fixed
T_{06}	LVDS/PECL (LVDS default)	1.544 MHz/2.048 MHz, 3.088 MHz/4.096 MHz, 6.176 MHz/8.192 MHz, 12.352 MHz/16.384 MHz, 19.44 MHz, 38.88 MHz (default), 155.52 MHz, 311.04 MHz
T_{07}	PECL/LVDS (PECL default)	19.44 MHz (default), 51.84 MHz, 77.76 MHz, 155.52 MHz
T_{08}	AMI	64/8 kHz (composite clock, 64 kHz + 8 kHz)
T_{09}	TTL/CMOS	1.544 MHz/2.048 MHz
T_{010}	TTL/CMOS	FrSync, 8 kHz - with a 50:50 MSR
T_{011}	TTL/CMOS	MFrSync, 2 kHz - with a 50:50 MSR

Note...1.544 MHz/2.048 MHz are shown for SONET/SDH respectively. Pin SONSDHB controls default, when High SONET is default.

Table 11 Multiple E1/DS1 Outputs in Relation to Standard Outputs

<table>
<tr><th>Mode</th><th>Freq to APLL</th><th>APLL Multiplier</th><th>APLL Freq</th><th>clk_ filt</th><th>clk_ filt/2</th><th>clk_ filt/4</th><th>clk_ filt/6</th><th>clk_ filt/8</th><th>clk_ filt/12</th><th>clk_ filt/16</th><th>clk_ filt/48</th><th>DPLL Freq</th></tr>
<tr><td>Defaul t</td><td>77.76</td><td>4</td><td>311.04</td><td>311.04</td><td>155.52</td><td>77.76</td><td>51.84</td><td>38.88</td><td>25.92</td><td>19.44</td><td>6.48</td><td>77.76</td></tr>
<tr><td>n value</td><td></td><td></td><td></td><td></td><td></td><td>16</td><td></td><td>8</td><td></td><td>4</td><td></td><td></td></tr>
<tr><td>n x E1</td><td>32.768</td><td>4</td><td>131.072</td><td>131.072</td><td>65.536</td><td>32.768</td><td>21.84533</td><td>16.384</td><td>10.92267</td><td>8.192</td><td>2.730667</td><td>77.76</td></tr>
<tr><td>n x T1</td><td>24.704</td><td>4</td><td>98.816</td><td>98.816</td><td>49.408</td><td>24.704</td><td>16.46933</td><td>12.352</td><td>8.234667</td><td>6.176</td><td>2.058667</td><td>77.76</td></tr>
<tr><td colspan="4" rowspan="7">Frequencies Available by Output</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">T_{01}</td><td></td></tr>
<tr><td></td><td></td><td></td><td colspan="3">T_{02}</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td>T_{03}</td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td>T_{04}</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>T_{05}</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="2">T_{06}</td><td></td><td></td><td>T_{06}</td><td></td><td>T_{06}</td><td></td><td></td></tr>
<tr><td></td><td colspan="3">T_{07}</td><td></td><td></td><td>T_{07}</td><td></td><td></td></tr>
</table>

increases latency, wander may often only need to be removed at specific points within a network where buffer stores are acceptable, such as at digital cross connects. Otherwise, wander is sometimes not required to be attenuated and can be passed through transparently. The ACS8510 Rev2.1 has programmable wander transfer characteristics in a range from 0.1 Hz to 20 Hz. The wander and jitter transfer characteristic is shown in Figure 5.

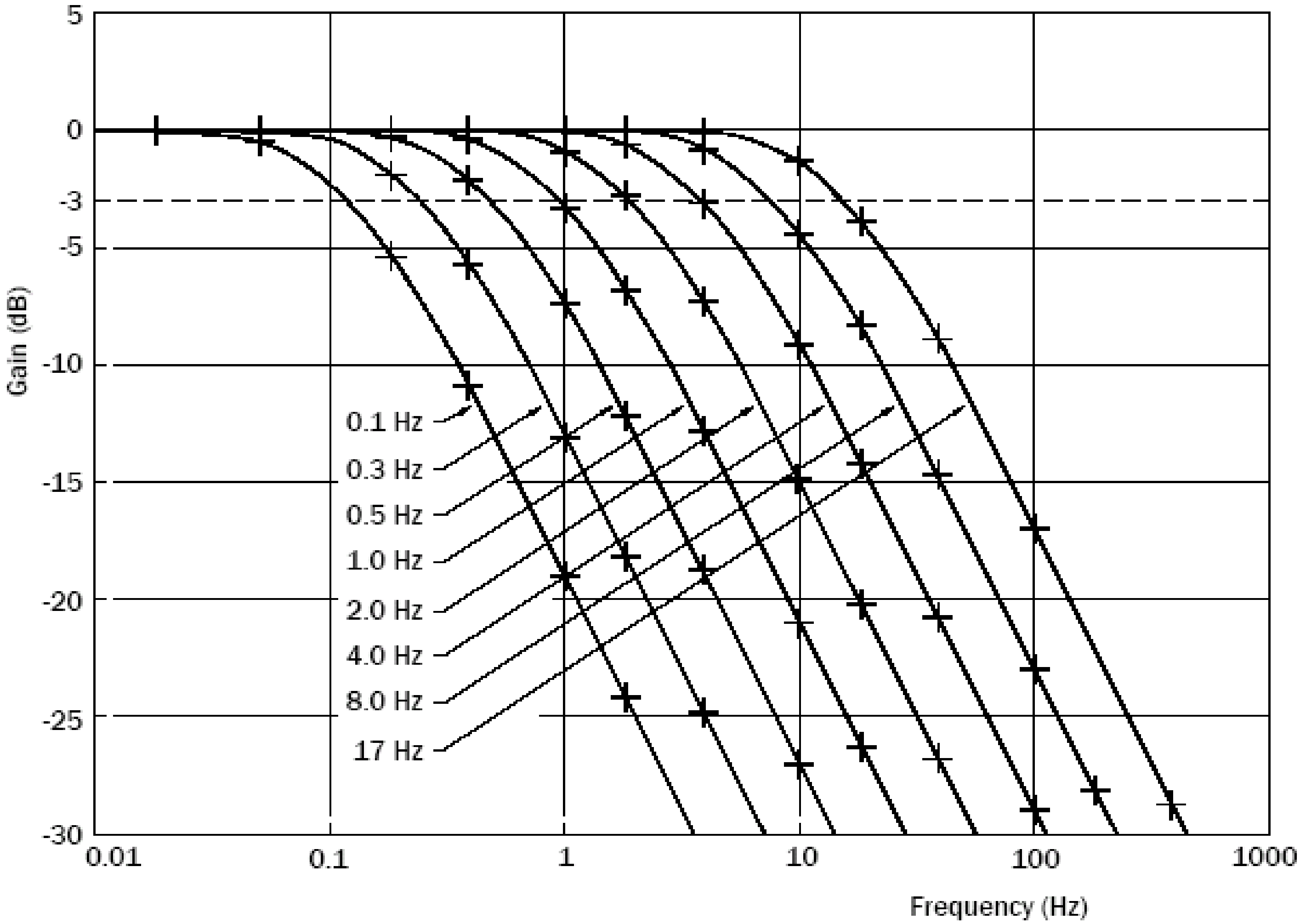
Wander on the local oscillator clock will not have significant effect on the output clock whilst in Locked mode, so long as the DPLL bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal. In Free-run or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator, as specified in the Section “Local Oscillator Clock” on page 8.

Phase Variation

There will be a phase shift across the ACS8510 Rev2.1 between the selected input reference source and the output clock. This phase shift may vary over time but will be constrained to lie within specified limits. The phase shift is characterized using two parameters, MTIE (Maximum Time Interval Error), and TDEV (Time Deviation), which, although being specified in all relevant specifications, differ in acceptable limits in each one. Typical measurements for the ACS8510 Rev2.1 are shown in Figures 6 and 7, for Locked mode operation. Figure 8 shows a typical measurement of Phase Error accumulation in Holdover mode operation.

The required performance for phase variation during Holdover is specified in several ways depending upon the particular circumstances pertaining:

Figure 5 Sample of Wander and Jitter Measured Transfer Characteristics



1. ETSI 300 462-5, Section 9.1, requires that the short term phase error during switchover (i.e., Locked to Holdover to Locked) be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval.
2. ETSI 300 462-5, Section 9.2, requires that the long term phase error in the Holdover mode should not exceed

   $$\{(a1+a2)S+0.5bS^2+c\}$$

   where

   a1 = 50 ns/s (allowance for initial frequency offset)

   a2 = 2000 ns/s (allowance for temperature variation)

   b = 1.16 x 10^{-4} ns/s^2 (allowance for ageing)

   c = 120 ns (allowance for entry into Holdover mode).
3. ANSI Tin1.101-1994, Section 8.2.2, requires that the phase variation be limited so that no more than 255 slips (of 125 μs each) occur during the first day of Holdover. This requires a frequency accuracy better than:

   ((24x60x60)+(255x125μs))/(24x60x60) = 0.37 ppm

   Temperature variation is not restricted, except to within the normal bounds of 0 to 50 °C.
4. Telcordia GR.1244.CORE, Section 5.2., Table 4, shows that an initial frequency offset of 50 ppb is permitted on entering Holdover, whilst a drift over temperature of 280 ppb is allowed; an allowance of 40 ppb is permitted for all other effects.
5. ITU G.822, Section 2.6, requires that the slip rate during category (b) operation (interpreted as being applicable to Holdover mode operation) be limited to less than 30 slips (of 125 μs each) per hour:

   ((((60 x 60)/30)+125μs)/(60x60)) = 1.042 ppm

Figure 6 Maximum Time Interval Error of T_{out0} Output Port

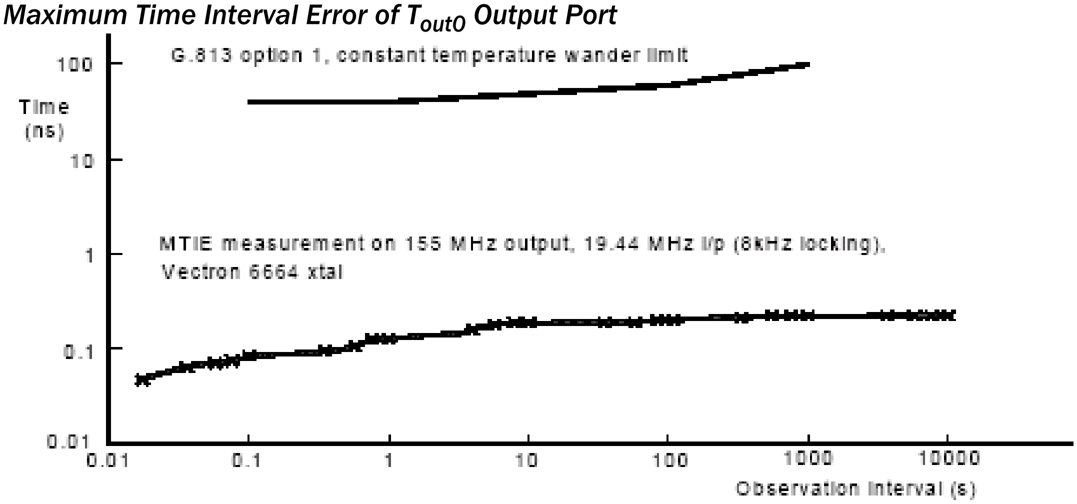


Figure 7 Time Deviation of T_{out0} Output Port

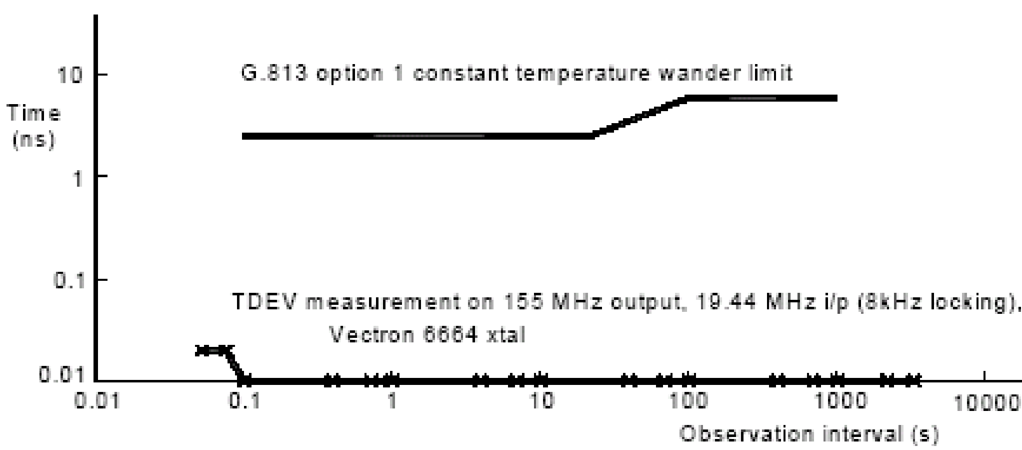
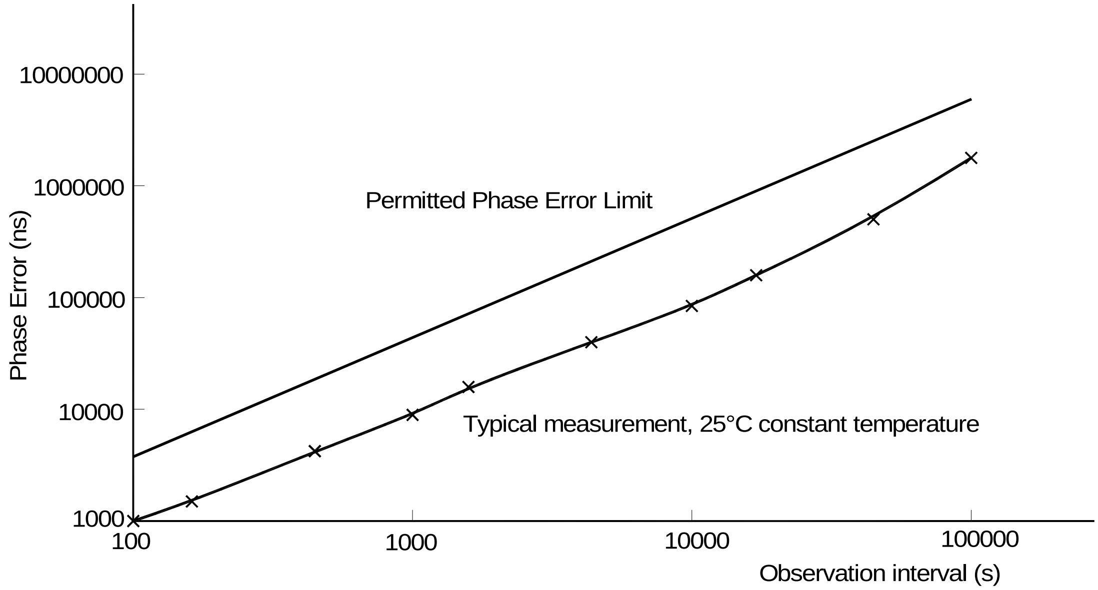


Figure 8 Phase Error Accumulation of T0 PLL Output Port in Holdover Mode



Phase Build-Out

Phase Build-Out (PBO) is the function to minimize phase transients on the output SEC clock during input reference switching. If the currently selected input reference clock source is lost (due to a short interruption, out of frequency detection, or complete loss of reference), the second, next highest priority reference source will be selected. During this transition, the *Lost_Phase* mode is entered.

The typical phase disturbance on clock reference source switching will be less than 12 ns on the ACS8510 Rev2.1. For clock reference switching caused by the main input failing or being disconnected, then the phase disturbance on the output will still be less than the 120 ns allowed for in the G.813 spec. The actual value is dependent on the frequency being locked to.

ITU-T G.813 states that the max allowable short term phase transient response, resulting from a switch from one clock source to another, with Holdover mode entered in between, should be a maximum of 1 μs over a 15 second interval. The maximum phase transient or jump should be less than 120 ns at a rate of change of less than 7.5 ppm and the Holdover performance should be better than 0.05 ppm.

On the ACS8510 Rev2.1, PBO can be enabled, disabled or frozen using the μP interface. By default, it is enabled. When PBO is enabled, it can also be frozen, which will disable the PBO operation on the next input reference switch, but will

remain with the current offset. If PBO is disabled while the device is in the Locked mode, there will be a phase jump on the output SEC clocks as the DPLL locks back to 0 degree phase error.

Microprocessor Interface

The ACS8510 Rev2.1 incorporates a microprocessor interface, which can be configured for the following modes via the bus interface mode control pins UPSEL(2:0) as defined in Table 12.

Table 12 Microprocessor Interface Mode Selection

UPSEL(2:0)	Mode	Description
111 (7)	OFF	Interface disabled
110 (6)	OFF	Interface disabled
101 (5)	SERIAL	Serial uP bus interface
100 (4)	MOTOROLA	Motorola interface
011 (3)	INTEL	Intel compatible bus interface
010 (2)	MULTIPLEXED	Multiplexed bus interface
001 (1)	EPROM	EPROM read mode
000 (0)	OFF	Interface disabled

Motorola Mode

Parallel data + address: this mode is suitable for use with Motorola's 68x0 type bus.

Intel Mode

Parallel data + address: this mode is suitable for use with Intel's 80x86 type bus.

Multiplexed Mode

Data/address: this mode is suitable for use with microprocessors which share bus signals between address and data (e.g., Intel's 80x86 family).

Serial Mode

This mode is suitable for use with microprocessor which use a serial interface.

EPROM Mode

This mode is suitable for simple standalone applications where it is required to change the default loading of the register values to suit different applications.

This can be done by loading values from an external ROM. The data is read from the ROM automatically after power-up when the UPSEL(2:0) pins are set to “001”. Each register value is stored sequentially, with ROM address 0 corresponding to register address 0 and so on.

The value in the *chip_id* location (address 00 & 01) is checked to see if it matches the ID number of the ACS8510 Rev2.1 (value 213E). Upon a successful number match, the remaining data from the ROM is used to set the internal register values. Only 64 locations in the ROM are required.

Register Set

All registers are 8-bits wide, organized with the most-significant bit positioned in the left-most bit, with bit significance decreasing towards the right most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g. flags) upwards. Several data fields are spread across multiple registers; their organization is shown in the register map, Table 13.

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some will be pinsettable. All configuration registers can be read out over the microprocessor port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writeable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Register Access

Most registers are of one of two types, configuration registers or status registers, the exceptions being the *chip_ID* and *chip_revision* registers. Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time and, in some status registers (such as the *sts_interrupts* register), any individual data field may be cleared by writing a “1” into each bit of the field (writing a “0” value into a bit will not affect the value of the bit). A description of each register is given in the Register Map, and Register Map Description.

Interrupt Enable and Clear

Interrupt requests are flagged on pin INTREQ (active High). Bits in the interrupt status register are set (high) by the following conditions:

1. Any reference source becoming valid or going invalid
2. A change in the operating state (e.g. Locked, Holdover etc.)
3. A brief loss of the currently selected reference source
4. An AMI input error

All interrupt sources are maskable via the mask register, each one being enabled by writing a “1” to the appropriate bit. Any unmasked bit set in the interrupt status register will cause the interrupt request pin to be asserted (high). All interrupts are cleared by writing a '1' to the bit(s) to be cleared in the status register. When all pending unmasked interrupts are cleared the interrupt pin will go inactive (low).

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the leaky bucket configuration of the activity monitors. The fastest leaky bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source. Some applications require the facility to switch downstream devices based on the status of the reference sources. In order to provide extra flexibility, it is possible to flag the “main reference failed” interrupt (addr 06, bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to bit 6 of register 48Hex.

Register Map

Shaded areas in the map are “don’t care” and writing either 0 or 1 will not affect any function of the device.

Bits labelled *Set to 0* or *Set to 1* must be set as stated during initialization of the device, either following power up, or after a power on reset (POR). Failure to correctly set these bits may result in the device operating in an unexpected way.

Some registers do not appear in this list. These are either not used, or have test functionality. Do not write to any undefined registers as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Table 13 Register Map

Addr (Hex)	Register Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
00	*chip_id* *(read only)*	Device part number (7:0)							
01		Device part number (15:8)							
02	*chip_revision* *(read only)*	Chip revision number (7:0)							
03	*cnfg_control1* *(read/write)*			Multiple E1/T1 O/P	Analog div sync	Set to 0	8k Edge Polarity	Set to 0	Set to 0
04	*cnfg_control2* *(read/write)*			Phase loss flag limit			Set to 0	Set to 1	Set to 0
05	*sts_interrupts* *(read/write)*	<I_8> valid change	<I_7> valid change	<I_6> valid change	<I_5> valid change	<I_4> valid change	<I_3> valid change	<I_2> valid change	<I_1> valid change
06		Operating mode	Main ref. failed	<I_14> valid change	<I_13> valid change	<I_12> valid change	<I_11> valid change	<I_10> valid change	<I_19> valid change

Table 13 Register Map

Addr (Hex)	Register Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
08	*sts_T4_inputs (read/write)*				T4 ref failed	Ami2 Violation	Ami2 L.O.S.	Ami1 Violation	Ami1 L.O.S.
09	*sts_operating_mode (read only)*						Operating mode (2:0)		
0A	*sts_priority_table (read only)*	Highest priority valid source				Currently selected reference source			
0B		3rd highest priority valid source				2nd highest priority valid source			
0C	*sts_curr_inc_offset (read only)*	Current increment offset (7:0)							
0D		Current increment offset (15:8)							
07							Current increment offset (18:16)		
0E	*sts_sources_valid (read only)*	<I_8>	<I_7>	<I_6>	<I_5>	<I_4>	<I_3>	<I_2>	<I_1>
0F				<I_14>	<I_13>	<I_12>	<I_11>	<I_10>	<I_19>
10	*sts_reference_sources (read/write)*	status <I_2>				status <I_1>			
11		status <I_4>				status <I_3>			
12		status <I_6>				status <I_5>			
13		status <I_8>				status <I_7>			
14		status <I_10>				status <I_9>			
15		status <I_12>				status <I_11>			
16		status <I_14>				status <I_13>			
18	*cnfg_ref_selection_ priority (read/write)*	programmed_priority <I_2>				programmed_priority <I_1>			
19		programmed_priority <I_4>				programmed_priority <I_3>			
1A		programmed_priority <I_6>				programmed_priority <I_5>			
1B		programmed_priority <I_8>				programmed_priority <I_7>			
1C		programmed_priority <I_10>				programmed_priority <I_9>			
1D		programmed_priority <I_12>				programmed_priority <I_11>			
1E		programmed_priority <I_14>				programmed_priority <I_13>			

Table 13 Register Map

Addr (Hex)	Register Name	Data Bit 7 (msb)	6	5	4	3	2	1	0 (lsb)
20	*cnfg_ref_source_ frequency (read/write)*	divn	lock8k	bucket_id <I_1>(1:0)		reference_source_frequency <I_1>(3:0)			
21		divn	lock8k	bucket_id <I_2>(1:0)		reference_source_frequency <I_2>(3:0)			
22		divn	lock8k	bucket_id <I_3>(1:0)		reference_source_frequency <I_3>(3:0)			
23		divn	lock8k	bucket_id <I_4>(1:0)		reference_source_frequency <I_4>(3:0)			
24		divn	lock8k	bucket_id <I_5>(1:0)		reference_source_frequency <I_5>(3:0)			
25		divn	lock8k	bucket_id <I_6>(1:0)		reference_source_frequency <I_6>(3:0)			
26		divn	lock8k	bucket_id <I_7>(1:0)		reference_source_frequency <I_7>(3:0)			
27		divn	lock8k	bucket_id <I_8>(1:0)		reference_source_frequency <I_8>(3:0)			
28		divn	lock8k	bucket_id <I_9>(1:0)		reference_source_frequency <I_9>(3:0)			
29		divn	lock8k	bucket_id <I_10>(1:0)		reference_source_frequency <I_10>(3:0)			
2A		divn	lock8k	bucket_id <I_11>(1:0)		reference_source_frequency <I_11>(3:0)			
2B		divn	lock8k	bucket_id <I_12>(1:0)		reference_source_frequency <I_12>(3:0)			
2C		divn	lock8k	bucket_id <I_13>(1:0)		reference_source_frequency <I_13>(3:0)			
2D		divn	lock8k	bucket_id <I_14>(1:0)		reference_source_frequency <I_14>(3:0)			
30	*cnfg_sts_remote_ sources_ valid (read/write)*	Remote status, channels <8:1>							
31				Remote status, channels <14:9>					
32	*cnfg_operating_mode (read/write)*						Forced operating mode		
33	*cnfg_ref_selection (read/write)*					force_select_reference_source			
34	*cnfg_mode (read/write)*	Auto external 2K enable	Phase alarm timeout enable	Clock edge	Holdover Offset enable	External 2K Sync enable	SONET/ SDH I/P	Master/ Slave	Reversion mode
35	*cnfg_T4 (read/write)*			Squelch	Select T0/T1	Force T1 input source selection (only valid for inputs I_5 to I_10)			
36	*cnfg_differential_inputs (read/write)*							<I_6> PECL	<I_5> PECL
37	*cnfg_uPsel_pins (read only)*						Microprocessor type		
38	*cnfg_T0_output_enable (read/write)*	311.04 MHz on T06	1=SONET 0=SDH for Dig2	1=SONET 0=SDH for Dig1	T01	T02	T03 19.44 MHz	T04 38.88 MHz	T05 77.76 MHz
39	*cnfg_T0_output_ frequencies (read/write)*	Digital2		Digital1		T02		T01	

Table 13 Register Map

Addr (Hex)	Register Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
3A	*cnfg_differential_ outputs (read/write)*	T07 Frequency selection		T06 Frequency selection		T07 LVDS enable	T07 PECL enable	T06 LVDS enable	T06 PECL enable
3B	*cnfg_bandwidth (read/write)*	Auto b/w switch Acq/lock	Acquisition bandwidth			Set to 0	Normal/locked bandwidth		
3C	*cnfg_nominal_frequency (read/write)*	Nominal frequency (7:0)							
3D		Nominal frequency (15:8)							
3E	*cnfg_holdover_offset (read/write)*	Holdover offset (7:0)							
3F		Holdover offset (15:8)							
40		Auto Holdover Averagin					Holdover offset (18:16)		
41	*cnfg_freq_limit (read/write)*	DPLL Frequency offset limit (7:0)							
42								DPLL Frequency offset limit (9:8)	
43	*cnfg_interrupt_mask (read/write)*	<I_8> valid change	<I_7> valid change	<I_6> valid change	<I_5> valid change	<I_4> valid change	<I_3> valid change	<I_2> valid change	<I_1> valid change
44		Operating mode	Main ref. failed	<I_14> valid change	<I_13> valid change	<I_12> valid change	<I_11> valid change	<I_10> valid change	<I_19> valid change
45					T4 ref	Ami2 Violation	Ami2 L.O.S	Ami1 Violation	Ami1 L.O.S
46	*cnfg_freq_divn (read/write)*	Divide-input-by-n ratio (7:0)							
47				Divide-input-by-n ratio (13:8)					
48	*cnfg_monitors (read/write)*		Flag ref lost on TDO	Ultra-fast switching	External source switch enable	Freeze phase buildout	Phase buildout enable	Frequency monitors configuration (1:0)	
50	*cnfg_activ_upper_ threshold0 (read/write)*	Configuration 0: Activity alarm set threshold (7:0)							
51	*cnfg_activ_lower_ threshold0 (read/write)*	Configuration 0: Activity alarm reset threshold (7:0)							
52	*cnfg_bucket_size0 (read/write)*	Configuration 0: Activity alarm bucket size (7:0)							
53	*cnfg_decay_rate0 (read/write)*							Cfg 0:decay_rate (1:0)	

Table 13 Register Map

Addr (Hex)	Register Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
54	*cnfg_activ_upper_ threshold1 (read/write)*	Configuration 1: Activity alarm set threshold (7:0)							
55	*cnfg_activ_lower_ threshold1 (read/write)*	Configuration 1: Activity alarm reset threshold (7:0)							
56	*cnfg_bucket_size1 (read/write)*	Configuration 1: Activity alarm bucket size (7:0)							
57	*cnfg_decay_rate1 (read/write)*							Cfg 1:decay_rate (1:0)	
58	*cnfg_activ_upper_ threshold2 (read/write)*	Configuration 2: Activity alarm set threshold (7:0)							
59	*cnfg_activ_lower_ threshold2 (read/write)*	Configuration 2: Activity alarm reset threshold (7:0)							
5A	*cnfg_bucket_size2 (read/write)*	Configuration 2: Activity alarm bucket size (7:0)							
5B	*cnfg_decay_rate2 (read/write)*							Cfg 2:decay_rate (1:0)	
5C	*cnfg_activ_upper_ threshold3 (read/write)*	Configuration 3: Activity alarm set threshold (7:0)							
5D	*cnfg_activ_lower_ threshold3 (read/write)*	Configuration 3: Activity alarm reset threshold (7:0)							
5E	*cnfg_bucket_size3 (read/write)*	Configuration 3: Activity alarm bucket size (7:0)							
5F	*cnfg_decay_rate3 (read/write)*							Cfg 3:decay_rate (1:0)	
7F	*cnfg_uPsel (read/write)*						Micro-processor type		

Register Map Description

Table 14 Register Description

Addr. (Hex)	Register Name	Description	Default Value (Bin)
	chip_id	This register contains the chip ID = 8510 (decimal)	
00		Bits (7:0) Chip ID bits (7:0	00111110
01		Bits (7:0) Chip ID bits (15:8)	00100001
02	*chip_revision*	This read only register contains the chip revision number This revision = 1 Last revision (engineering samples) = 0	00000001
03	*cnfg_control1*	Bits (7:6) Unused Bit 5 =1 32/24 MHz to APLL: Feeds 2x Dig2 frequency to the APLL instead of the normal 77.76 MHz. Thus the normal OC-3/STM1 outputs are replaced with multiple E1/T1 rates. Note: Dig2 set bits (Reg. 39h Bits (7:6)) must be set to 11 for this mode. =0 77.76MHz to APLL Bit 4 =1 Synchronizes the dividers in the output APLL section to the dividers in the DPLL section such that their phases align. This is necessary in order to have phase alignment between inputs and output clocks at OC-3 derived rates (6.48 MHz to 77.76 MHz). Keeping this bit high may be necessary to avoid the dividers getting out of synchronization when quick changes in frequency occur such as a force into Free-Run. =0 The dividers may get out of phase following step changes in frequency, but in this mode the correct number of high frequency edges is guaranteed within any synchronization period. The output will frequency lock (default). The device will always remain in synchronization 2 seconds from a reset, before the default setting applies. Bits 3 Test control - leave unchanged, or set to 0 Bit 2 =1 When in 8k locking mode the system will lock to the rising input clock edge. =0 When in 8k locking mode the system will lock to the falling input clock edge. Bits (1:0) Test controls - leave unchanged, or set to 00	XX000000
04	*cnfg_control2*	Bits (7:6) Unused Bits (5:3) define the phase loss flag limit. By default set to 4 (100) which corresponds to approximately 140°. A lower value sets a corresponding lower phase limit. The flag limit determines the value at which the DPLL indicates phase lost as a result of input jitter, a phase jump, or a frequency jump on the input Bits (2:0) Test controls - leave unchanged, or set to 010	XX100010
05	*sts_interrupts*	Bits (7:0) <I_8> to <I_1>	00000000
06		Bits (7:0) Operating mode, main ref failed, <I_14> to <I_9>	00000000

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
08	*sts_T4_inputs*	This register holds the status flags of the AMI inputs and the TOUT4 reference. The alarms once set will hold their state until reset. Each bit may be cleared individually by writing a “1” to that bit, thus resetting the interrupt. Writing “0”s will have no effect. These bits can also generate interrupts. Bits (7:5) Unused. Bit 4 =1 T4 reference failed - no valid T_{IN1} input (<I_10>:<I_5>), T4 DPLL cannot lock to source (default) =0 T4 reference good - valid T_{IN1} input available. Bit 3 =1 Ami2 Violation detected =0 Ami2 clear (default) Bit 2 =1 Ami2 Loss of signal =0 Ami2 clear (default) Bit 1 =1 Ami1 Violation detected =0 Ami1 clear (default) Bit 0 =1 Ami1 Loss of signal =0 Ami1 clear (default)	XXX10000
09	*sts_operating_mode*	This read-only register holds the current operating state of the main state machine. Figure 11 shows how the values of the “operating state” variable match with the individual states. Bits (7:3) Unused. Bits (2:0) State 001 Free-Run (default) 010 Holdover 100 Locked 110 Pre-locked 101 Pre-locked2 111 Phase lost	XXXXX001

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
	sts_priority_table	This is a 16-bit read-only register. Bits (15:12) Third highest priority valid source: this is the channel number of the input reference source which is valid and has the next-highest priority to the second-highest-priority valid source. Bits (11:8) Second highest priority valid source: this is the channel number of the input reference source which is valid and has the next-highest priority to the highest-priority valid source. Bits (7:4) Highest priority valid source: this is the channel number of the input reference source which is valid and has the highest priority - it may not be the same as the currently selected reference source (due to failure history or changes in programmed priority). Bits (3:0) Currently selected reference source: this is the channel number of the input reference source which is currently input to DPLL. Note that these registers are updated by the state machine in response to the contents of the *cnfg_ref_selection_priority* register and the ongoing status of individual channels; channel number “0000”, appearing in any of these registers, indicates that no channel is available for that priority.	
0A		Bits (7:4) Highest priority valid source (*sts_priority_table* bits (7:4)) Bits (3:0) Currently selected reference source (*sts_priority_table* bits (3:0))	0000000
0B		Bits (7:4) 3rd-highest priority valid source (*sts_priority_table* bits (15:12)) Bits (3:0) 2nd-highest priority valid source (*sts_priority_table* bits (11:8))	0000000
	sts_curr_inc_offset	This read-only register contains a signed-integer value representing the 19 significant bits of the current increment offset of the digital PLL. The register may be read periodically to build up a historical database for later use during holdover periods (this would only be necessary if an external oscillator which did not meet the stability criteria described in Local Oscillator Clock section is used). The register will read 00000000 immediately after reset.	
0C		Bits (7:0) *sts_curr_inc_offset* bits (7:0)	00000000
0D		Bits (7:0) *sts_curr_inc_offset* bits (15:8)	00000000
07		Bits (7:3) Unused Bits (2:0) *sts_curr_inc_offset* bits (18:16)	XXXXX000
	sts_sources_valid	This register contains a bit to show validity for every reference source. =1 Valid source =0 Invalid source (default)	
0E		Bits (7:0) <I_8> to <I_1>	00000000
0F		Bits (7:6) Unused Bits (5:0) <I_14> to <I_9>	XX000000

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
	sts_reference_sources	This is a 7-byte register which holds the status of each of the 14 input reference sources. The status of each reference source is shown in a 4-bit field. Each bit is active high.To aid status checking, a copy of each status bit 3 is provided in the *sts_sources_valid* register. The status is reported as follows: (Each bit may be cleared individually) Status bit 3 = Source valid (no alarms) (bit 3 is combination of bits (2:0)) (default 0) Status bit 2 = out-of-band alarm (default 1) Status bit 1 = no activity alarm (default 1) Status bit 0 = phase lock alarm (default 0)	
10		Bits (7:4) Status of input reference source <I_2> Bits (3:0) Status of input reference source <I_1>	01100110
11		Bits (7:4) Status of input reference source <I_4> Bits (3:0) Status of input reference source <I_3>	01100110
12		Bits (7:4) Status of input reference source <I_6> Bits (3:0) Status of input reference source <I_5>	01100110
13		Bits (7:4) Status of input reference source <I_8> Bits (3:0) Status of input reference source <I_7>	01100110
14		Bits (7:4) Status of input reference source <I_10> Bits (3:0) Status of input reference source <I_9>	01100110
15		Bits (7:4) Status of input reference source <I_12> Bits (3:0) Status of input reference source <I_11>	01100110
16		Bits (7:4) Status of input reference source <I_14> Bits (3:0) Status of input reference source <I_13>	01100110
	cnfg_ref_selection_ priority	This register holds the priority of each of the 14 input reference sources. The priority values are all relative to each other, with lower-valued numbers taking higher priorities. Only the values “1” to “15” (dec) are valid - “0” disables the reference source. Each reference source should be given a unique number, however two sources given the same priority number will be assigned on a first in first out basis. It is recommended to reserve the priority value “1” as this is used when forcing reference selection via the *cnfg_ref_selection* register. If the user does not intend to use the *cnfg_ref_selection* register then the priority value “1” need not be reserved.	
18		Bits (7:4) Programmed priority of input reference source <I_2> Bits (3:0) Programmed priority of input reference source <I_1>	00110010
19		Bits (7:4) Programmed priority of input reference source <I_4> Bits (3:0) Programmed priority of input reference source <I_3>	01010100
1A		Bits (7:4) Programmed priority of input reference source <I_6> Bits (3:0) Programmed priority of input reference source <I_5>	01110110
1B		Bits (7:4) Programmed priority of input reference source <I_8> Bits (3:0) Programmed priority of input reference source <I_7>	10011000

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
1C	*cnfg_ref_selection_ priority (continued)*	Bits (7:4)Programmed priority of input reference source <I_10> Bits (3:0)Programmed priority of input reference source <I_9>	10111010
1D		Bits (7:4)Programmed priority of input reference source <I_12> Bits (3:0)Programmed priority of input reference source <I_11>	11010001 (MSTSLVB=0) 11011100 (MSTSLVB=1)
1E		Bits (7:4)Programmed priority of input reference source <I_14> Bits (3:0)Programmed priority of input reference source <I_13>	11111110
	cnfg_ref_source_ frequency	This register is used to set up each of the 14 input reference sources. Bits (7:6) of each byte defines the operation undertaken on the input frequency, in accordance with the following key: 00 The input frequency is fed directly into the DPLL. (default). 01 The input frequency is internally divided down to 8 kHz, before being fed into the DPLL. (For high jitter tolerance). 10 Unsupported configuration - do not use. 11 Uses the division coefficient stored in registers 46 and 47 (*cnfg_freq_divn*) to divide the input by this value prior to being fed into the DPLL. The frequency monitors must be disabled. The divided down frequency should equal 8 kHz. The frequency (3:0) should be set to the nearest spot frequency just below the actual input frequency. The DivN feature works for input frequencies between 1.544 MHz and 100 MHz. Bits (5:4) define which leaky bucket group (0-3) is used, as defined in registers 50 to 5F. (default 00). Bits (3:0) defines the frequency of the reference source in accordance with the following: 0000 8 kHz (fixed <I_1>, <I_2>, default <I_3>, <I_4>) 0001 1.544 MHz (SONET)/2.048 MHz (SDH) (as defined by register 34, bit 2) (default <I_12>, <I_13>, <I_14>) 0010 6.48 MHz (default <I_11> when MSTSLVB = 1) 0011 19.44 MHz (default <I_11> when MSTSLVB=0, and <I_5>, <I_6>, <I_7> <I_8>, <I_9>, <I_10>) 0100 25.92 MHz 0101 38.88 MHz 0110 51.84 MHz 0111 77.76 MHz 1000 155.52 MHz 1001 2 kHz 1010 4 kHz	
20		Frequency of reference source <I_1> - fixed at 00000000 for 8 kHz only	00000000
21		Frequency of reference source <I_2> - fixed at 00000000 for 8 kHz only	00000000
22		Frequency of reference source <I_3>	00000000
23		Frequency of reference source <I_4>	00000000

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
24	*cnfg_ref_source_ frequency (continued)*	Frequency of reference source <I_5>	00000011
25		Frequency of reference source <I_6>	00000011
26		Frequency of reference source <I_7>	00000011
27		Frequency of reference source <I_8>	00000011
28		Frequency of reference source <I_9>	00000011
29		Frequency of reference source <I_10>	00000011
2A		Frequency of reference source <I_11>	00000010 (MSTSLVB=0) 00000011 (MSTSLVB=1)
2B		Frequency of reference source <I_12>	00000001
2C		Frequency of reference source <I_13>	00000001
2D		Frequency of reference source <I_14>	00000001
	cnfg_sts_remote_ sources_ valid	This register holds the status of the reference sources supplied to the other device in a master/slave configuration. It is a copy of the other device's *sts_sources_valid* register. The register is part of the protection mechanism.	
30		Bits (7:0) Reference sources <I_8>:<I_1>	11111111
31		Bits (7:6) Unused Bits (5:0) Reference sources <I_14>:<I_9>	XX111111
32	*cnfg_operating_mode*	This register is used to force the device into a desired operating state, represented by the binary values shown in Figure 11. Value 0 (hex) allows the control state machine to operate automatically. Bits (7:3)Unused Bits (2:0)Desired operating state (as per Figure 11)	XXXXX000
33	*cnfg_ref_selection*	This register is used to force the device to select a particular input reference source, irrespective of its priority. Writing to this register temporarily raises the selected input to priority “1”. Provided no other input is already programmed with priority “1”, and revertive mode is on, this source will be selected.. Bits (7:4) Unused. Bits (3:0) Desired reference source (0000 and 1111 disables the force selection, and allows automatic selection of all sources, default is 1111)	XXXx1111

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
34	*cnfg_mode*	This register contains several individual configuration fields, as detailed below: Bit 7 =1 Auto 2 kHz Sync enable: External 2 kHz Sync will be enabled only when the source is locked to 6.48 MHz. Otherwise it will be disabled (default) =0 Auto 2 kHz Sync disable: The user controls this function using bit 3 of this register, as described below. Bit 6 =1 Phase Alarm Timeout enable: The phase alarm will timeout after 100 seconds (default). =0 Phase Alarm Timeout disable: The phase alarm will not timeout and must be reset by software. Bit 5 =1 Rising Clock Edge selected: The device will reference to the rising edge of the external 12.8 MHz crystal oscillator signal =0 Falling edge Edge selected: The device will reference to the falling edge of the external 12.8 MHz crystal oscillator signal (default). Bit 4 =1 Holdover offset enable: The device will adopt the Holdover offset value stored in the *cnfg_holdover_offset* register, in order to set the frequency in Holdover =0 Holdover offset disable: The device will ignore the value and Holdover will freeze the frequency of the DPLL on entering Holdover mode (default). Bit 3 = 1 External 2 kHz Sync Enable: The device will align the phase of its internally generated Frame Sync signal (8 kHz) and MultiFrame Sync signal (2 kHz) with that of the signal supplied to the Sync2K pin. The device should be locked to a 6.48 MHz output from another ACS8510 Rev2.1. = 0 External 2 kHz Sync Disable: The device will ignore the Sync2k pin. Bit 2 = 1 SONET Mode: The device expects the input frequency of any input channel given the value '0001' in the *cnfg_ref_source_frequency* register to be 1544 kHz = 0 SDH Mode: The device expects the input frequency of any input channel given the value "0001" in the *cnfg_ref_source_frequency* register to be 2048 kHz. At start up or reset the bit value will be defaulted to the setting of pin SONSDHB. This setting can subsequently be altered by changing this bit value. Bit 1 = 1 Master Mode: The device will adopt the master mode and make the active decisions of which source to select, etc. This bit is writeable, but its default value is determined by the pin, MSTSLVB. = 0 Slave Mode: The device will adopt the slave mode and will follow the master device. At start up or reset the bit value will be defaulted to the setting of pin MSTSLVB. This setting can subsequently be altered by changing this bit value. Bit 0 = 1 Revertive Mode: The device will switch to the highest priority source available shown in the *sts_priority_table* register, bits (7:4) = 0 Non Revertive Mode: The device will retain the presently selected source (default)	11001000 (MSTSLVB=0) (SONSDHB=0) 11001100 (MSTSLVB=0) (SONSDHB=1) 11000010 (MSTSLVB=1) (SONSDHB=0) 11000110 (MSTSLVB=1) (SONSDHB=1)

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
35	*cnfg_T4*	This controls DPLL _T4 (output on T_{08}/T_{09}) and input source selection: Bits (7:6) Unused Bit 5 =1 DPLL_T4 is turned off (squelched) =0 DPLL_T4 is on (default) Bit 4 Selects which DPLL (T4 or T0) source feeds outputs T_{08}/T_{09}: =1 DPLL_T0 output is fed to outputs T_{08} and T_{09} =0 DPLL_T4 output is fed to outputs T_{08} and T_{09} Bits (3:0) Input source selection. The device will switch to the source shown in this field for the generation of the T_{OUT4} signal. If '0' it will select the highest priority active T_{IN1}.	XX000000
36	*cnfg_differential_inputs*	This register contains two individual configuration fields, as follows: Bits (7:2) Unused Bit 1 =1 Input <I_6> is PECL-compatible (Default) =0 Input <I_6> is LVDS-compatible Bit 0 =1 Input <I_5> is PECL-compatible =0 Input <I_5> is LVDS-compatible (Default)	XXXXXX10
37	*cnfg_uPsel_pins*	This read only register returns a value indicating the microprocessor type selected at power up or reset. This is set by the configuration of the UPSEL pins (pins 58 - 60). If the UPSEL pin configuration is changed while the device is operating no effect will take place, but this register will reflect that change, so indicating the configuration that will be implemented at the next power up or reset. The microprocessor type can be changed with the device operational, though register 7F. Bits (7:3) Unused. Bit (2:0) Microprocessor type 000 OFF (interface disabled) 001 EPROM 010 MULTIPLEXED 011 INTEL 100 MOTOROLA 101 SERIAL 110 OFF (interface disabled) 111 OFF (interface disabled)	Bits(7:3)= XXXXX Bits(2:0)= UPSEL pin configuration

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
38	*cnfg_T0_output_enable*	This register contains several individual configuration fields, as follows: Bit 7 =1 T_{06} output frequency set to 311.04 MHz * =0 T_{06} output frequency set by Address 3A (5:4) (default) Bit 6 =1 SONET mode selected for Dig2 =0 SDH mode selected for Dig2 (default) - see register *cnfg_T0_output_frequencies* Bit 5 =1 SONET mode selected for Dig1 =0 SDH mode selected for Dig1 (default) - see register *cnfg_T0_output_frequencies* Bit 4 =1 Output port T_{01} enabled (default) =0 Output port T_{01} disabled** - see register *cnfg_T0_output_frequencies* Bit 3 =1 Output port T_{02} enabled (default) =0 Output port T_{02} disabled** - see register *cnfg_T0_output_frequencies* Bit 2 =1 Output port T_{03} enabled (19.44 MHz*) (default) =0 Output port T_{03} disabled** Bit 1 =1 Output port T_{04} enabled (38.88 MHz*) (default) =0 Output port T_{04} disabled** Bit 0 =1 Output port T_{05} enabled (77.76 MHz*) (default) =0 Output port T_{05} disabled** Notes: * Defaults frequencies are changed to multiples of E1/T1 if the appropriate bit of the *cnfg_control1* register is set to 1. For details, see Table 10. ** "Disabled" means that the output port holds a static logic value (the port is not Tri-stated).	00011111

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
39	*cnfg_T0_output_ frequencies*	This register holds the frequency selections for each output port, as detailed below.* Bits (7:6) Dig2 00 1544 kHz/2048 kHz (default) 01 3088 kHz/4096 kHz 10 6176 kHz/8192 kHz 11 12352 kHz/16384 kHz Bits (5:4) Dig1 00 1544 kHz/2048 kHz (default) 01 3088 kHz/4096 kHz 10 6176 kHz/8192 kHz 11 12352 kHz/16384 kHz Bits (3:2) T_{02} 00 25.92 MHz 01 51.84 MHz 10 38.88 MHz (default) 11 Dig2 Bits (1:0) T_{01} 00 6.48 MHz (default) 01 25.92 MHz 10 19.44 MHz 11 Dig1 For Dig1/Dig2 the frequency values are shown for SONET/SDH. They are selected via the SONET/SDH bits in register *cnfg_T0_output_enable*. Note: * The above frequencies are changed to multiples of E1/T1 if the appropriate bit of the *cnfg_control1* register is set to 1. For details, see Table 10.	0000100
3A	*cnfg_differential_ outputs*	This register holds the frequency selections and the port-technology type for the differential outputs, T_{06} and T_{07}, as detailed below. Bits (7:6) T_{07} 00 155.52 MHz 01 51.84 MHz 10 77.76 MHz 11 19.44 MHz (default) Bits (5:4) T_{06} 00 38.88 MHz (default) 01 19.44 MHz 10 155.52 MHz 11 Dig1 Bits (3:2)T_{07} 00 Port disabled 01 PECL-compatible (default) 10 LVDS-compatible 11 Unused Bits (1:0) T_{06} 00 Port disabled 01 PECL-compatible 10 LVDS-compatible (default) 11 Unused	11000110

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
3B	*cnfg_bandwidth*	This register contains information used to control the operation of the digital PLL. When bandwidth selection is set to automatic, the DPLL will use the acquisition bandwidth setting when out of lock, and the normal/locked bandwidth setting when in lock. When set to manual, the DPLL will always use the normal/locked bandwidth setting. Bit 7 =1 Automatic operation =0 Manual operation (default) Bits (6:4) Acquisition bandwidth 000 0.1 Hz 001 0.3 Hz 010 0.5Hz 011 1.0 Hz 100 2.0 Hz 101 4.0 Hz 110 8.0 Hz 111 17 Hz (default) Bit (2:0) Loop bandwidth 000 0.1 Hz 001 0.3 Hz 010 0.5 Hz 011 1.0 Hz 100 2.0 Hz 101 4.0 Hz (default) 110 8.0 Hz 111 17 Hz Bit 3 Unused	0111X101
	cnfg_nominal_frequency	This register holds a 16 bit unsigned integer allowing compensation for offset of the crystal oscillator from the nominal 12.8 MHz. See “Crystal Frequency Calibration” on page 9. Default results in 0 ppm adjustment.	
3C		Bits (7:0) *cnfg_nominal_frequency* bits (7:0)	10011001
3D		Bits (7:0) *cnfg_nominal_frequency* bits (15:8)	10011001
	cnfg_holdover_offset	This register holds a 19-bit signed integer, representing the holdover offset value, which can be used to set the holdover mode frequency when enabled via the holdover offset enabled bit in the *cnfg_mode* register.	
3E		Bits (7:0) *cnfg_holdover_offset* bits (7:0)	00000000
3F		Bits (7:0) *cnfg_holdover_offset* bits (15:8)	00000000
40		Bit 7 =1 Auto Holdover Averaging enable. This enables the frequency average to be taken from 32 samples. One sample taken every 32 seconds, after the frequency has been confirmed to be in-band by the frequency monitors. This gives a 17 minute history of the currently locked to reference source for use in Holdover. (default). =0 Auto Holdover Averaging disabled. Bits (6:3) Unused Bits (2:0) *cnfg_holdover_offset* bits (18:16)	1XXXX000

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
	cnfg_freq_limit	This register holds a 10 bit unsigned integer representing the pull-in range of the DPLL. It should be set according to the accuracy of crystal implemented in the application, using the following formula: Frequency range ±(ppm) = (*cnfg_freq_limit* x 0.0785)+0.01647 or *cnfg_freq_limit* = (Frequency range ± (ppm) - 0.01647) / 0.0785 Default value when SRCSW is left unconnected or tied low is ±9.3 ppm. Default value when SRCSW is high is the full range of around ±80 ppm.	
41		Bits (7:0) *cnfg_freq_limit* bits (7:0)	01110101 (SRCSW low) 11111111 (SRCSW high)
42		Bits (7:2) Unused Bits (1:0) *cnfg_freq_limit* bits (9:8)	XXXXXX00 (SRCSW low) XXXXXX11 (SRCSW high)
	cnfg_interrupt_mask	Each bit, if set to 0 will disable the appropriate interrupt source in either the interrupt status register or the *sts_T4_inputs* register.	
43		Bits (7:0) *cnfg_interrupt_mask* bits (7:0)	11111111
44		Bits (7:0) *cnfg_interrupt_mask* bits (15:8)	11111111
45		Bits (7:5) Unused Bits (4:0) *cnfg_interrupt_mask* bits (20:16)	XXX11111
	cnfg_freq_divn	This 14 bit integer is used as the divisor for any input applied to <I_14>:<I_1> to get the phase locking frequency desired. Only active for inputs with the DivN bit set to “1”. This will cause the input frequency to be divided by (N+1) prior to phase comparison, e.g. program N to: ((input freq)/ 8 kHz) -1 The *reference_source_frequency* bits should be set to reflect the closest spot frequency to the input frequency, but must be lower than the input frequency.	
46		Bits (7:0) *cnfg_freq_divn* bits (7:0)	00000000
47		Bits (7:6) Unused Bits (5:0) *cnfg_freq_divn* bits (13:8)	XX000000

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
48	*cnfg_monitors*	This 7 bit register allows global configuration of monitors and control of phase build-out. Bit 7 Unused Bit 6 =1 Enables value of the *main_ref_failed* interrupt to be driven out of pin TDO =0 Disables value of the *main_ref_failed* interrupt from being driven out of pin TDO (default). Bit 5 =1 Enables ultra fast switching: Allows the DPLL to raise an inactivity alarm on the currently selected source after missing only a few cycles. See “Ultra Fast Switching” on page 40. =0 Normal operation (default) Bit 4 =1 Forces locking to <I_3> if pin SRCSW high, or <I_4> if SRCSW low =0 Pin SRCSW ignored and automatic control enabled. Bit 3 =1 Will freeze the output phase relationship with the current input to output phase offset. =0 Allows changes in input to output phase offset (Normal phase buildout mode) (default). Bit 2 =1 Enables phase build out (default). =0 DPLL will always lock to 0° Bits (1:0) are for configuring frequency monitors- 00 = off, 01 = 15 ppm (default), others are reserved for future use.	X0000101 (SRCSW low) X0010101 (SRCSW high)
50	*cnfg_activ_upper_ threshold0*	Bits (7:0) set the value in the leaky bucket that causes the activity alarm to be raised	00000110
51	*cnfg_activ_lower_ threshold0*	Bits (7:0) set the value in the leaky bucket that causes the activity alarm to be cleared	00000100
52	*cnfg_bucket_size0*	Bits (7:0) set the maximum value that the leaky bucket can reach given an inactive input	00001000
53	*cnfg_decay_rate0*	Bits (7:2)Unused Bits (1:0) control the leak rate of the leaky bucket. The fill-rate of the bucket is +1 for every 128 ms interval that has experienced some level of inactivity. The decay rate is programmable in ratios of the fill rate. The ratio can be set to 1:1, 2:1, 4:1, 8:1 by using values of 00, 01, 10, 11 respectively. However, these buckets are not “true” leaky buckets in nature. The bucket stops “leaking” when it is being filled. This means that the fill and decay rates can be the same (00 = 1:1) with the net effect that an active input can be recognized at the same rate as an inactive one.	XXXXXX01
54	*cnfg_activ_upper_ threshold1*	As for Reg. 50 but for bucket 1	00000110

Table 14 Register Description (cont...)

Addr. (Hex)	Register Name	Description	Default Value (Bin)
55	*cnfg_activ_lower_ threshold1*	As for Reg. 51 but for bucket 1	00000100
56	*cnfg_bucket_size1*	As for Reg. 52 but for bucket 1	00001000
57	*cnfg_decay_rate1*	As for Reg. 53 but for bucket 1	XXXXXX01
58	*cnfg_activ_upper_ threshold2*	As for Reg. 50 but for bucket 2	00000110
59	*cnfg_activ_lower_ threshold2*	As for Reg. 51 but for bucket 2	00000100
5A	*cnfg_bucket_size2*	As for Reg. 52 but for bucket 2	00001000
5B	*cnfg_decay_rate2*	As for Reg. 53 but for bucket 2	XXXXXX01
5C	*cnfg_activ_upper_ threshold3*	As for Reg. 50 but for bucket 3	00000110
5D	*cnfg_activ_lower_ threshold3*	As for Reg. 51 but for bucket 3	00000100
5E	*cnfg_bucket_size3*	As for Reg. 52 but for bucket 3	00001000
5F	*cnfg_decay_rate3*	As for Reg. 53 but for bucket 3	XXXXXX01
7F	*cnfg_uPsel*	Bits (7:3) Unused Bits (2:0) can be used to change the mode of the microprocessor interface. The interface will initially be set as the pins UPSEL (pins 58 - 60) - the pin set up can be read via register 37 (*cnfg_uPsel_pins*). At power up or reset the device will default to this setting. This register can be used to change the microprocessor mode after start up, supporting booting from EPROM and subsequently communicating via another mode. At start up the EPROM will down load the pre-programmed settings for all the registers, and as the last operation, action the change of interface with this last register. It is recommended that this function is only used for EPROM start up applications, as subsequent versions of this device may only allow operation in this way. The bits are defined in Table 11 or as given in Reg. 37 of the register map description.	Bits(7:3)= XXXXX Bits(2:0)= Pin dependent

Selection of Input Reference Clock Source

Under normal operation, the input reference sources are selected automatically by an order of priority. But, for special circumstances, such as chip or board testing, the selection may be forced by configuration.

Automatic operation selects a reference source based on its pre-defined priority and its current availability. A table is maintained which lists all reference sources in the order of priority. This is initially downloaded into the ACS8510 Rev2.1 via the microprocessor interface by the Network Manager, and is subsequently modified by the results of the ongoing quality monitoring. In this way, when all the defined sources are active and valid, the source with the highest programmed priority is selected but, if this source fails, the next-highest source is selected, and so on.

Restoration of repaired reference sources is handled carefully to avoid inadvertent disturbance of the output clock. The ACS8510 Rev2.1 has two modes of operation; Revertive and Non-Revertive. In Revertive mode, if a revalidated (or newly validated) source has a higher priority than the reference source which is currently selected, a switchover will take place. Many applications prefer to minimize the clock switching events and choose Non-Revertive mode. In Non-Revertive mode, when a re-validated (or newly validated) source has a higher priority then the selected source will be maintained. The re-validation of the reference source will be flagged in the *sts_sources_valid* register and, if not masked, will generate an interrupt. Selection of the re-validated source can only take place under software control - the software should briefly enable Revertive mode to affect a switch-over to the higher priority source. If the selected source fails under these conditions the device will indicate that it is still locked to the failed reference. It will not select the higher priority source until instructed to do so by the software; by briefly setting the Revertive mode bit. When there is a reference available with higher priority than the selected reference, there will be NO change of reference source as long as the Non-Revertive mode remains on AND the device will remain indicating a locked state on the failed reference. This is the case even if there are lower priority references available or the currently selected reference fails. When the ONLY valid reference sources that are available have a lower priority than the selected reference, a failure of the selected reference will always trigger a switchover, regardless of whether Revertive or Non-Revertive mode has been chosen.

Also, in a Master/Slave redundancy-protection scheme, the Slave device(s) must follow the Master device. The alignment of the Master and Slave devices is part of the protection mechanism. The availability of each source is determined by a combination of local and remote monitoring of each source. Each input reference source supplied to each ACS8510 Rev2.1 device is monitored locally and the results are made available to other devices.

Forced Control Selection

A configuration register, *cnfg_ref_selection*, controls both the choice of automatic or forced selection and the selection itself (when forced selection is required). The forced selection of an input reference source occurs when the *cnfg_ref_selection* variable contains a non-zero value, the value then representing the input port required to be selected. This is not the normal mode of operation, and the *cnfg_ref_selection* variable is defaulted to the all-one value on reset, thereby adopting the automatic selection of the reference source.

Automatic Control Selection

When an automatic selection is required, the *cnfg_ref_selection* register must be set to all zero or all one. The configuration registers, *cnfg_ref_selection_priority*, held in the µP port block, consists of seven, 8 bit registers organised as one 4-bit register per input reference port. Each register holds a 4-bit value which represents the desired priority of that particular port. Unused ports should be given the value, '0000' or '1111', in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the whole of the configuration file will be defaulted to the values defined by Table 6. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each reference source should be given a unique number, the valid values are 1 to 15 (dec). A value of 0 disables the reference source. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis. There is no implied priority based on the channel numbers.

The input port <I_11> is for the connection of the synchronous clock of the T_{OUT0} output of the Master device (or the active-Slave device), to be used to align the T_{OUT0} output with the Master (or active-Slave) device if this device is acting in a subordinate-Slave or subordinate-Master role.

Ultra Fast Switching

A reference source is normally disqualified after the leaky bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented, whereby if register 48H, bit 5 (Ultra Fast Switching), is set then a loss of activity of just a few reference clock cycles will set the “no activity alarm” and cause a reference switch. This can be chosen to cause an interrupt to occur instead of or as well as causing the reference switch. The *sts_interrupts* register 05 Hex Bit 14 (*main_ref_failed*) of the interrupt status register is used to flag inactivity on the reference that the device is locked to much faster than the activity monitors can support. If bit 6 of the *cnfg_monitors* register (flag ref loss on TDO) is set, then the state of this bit is driven onto the TDO pin of the device.

The flagging of the loss of the main reference failure on TDO is simply allowing the status of the *sts_interrupt* bit 14 to be reflected in the state of the TDO output pin. The pin will, therefore remain *High* until the interrupt is cleared. This functionality is not enabled by default so the usual JTAG functions can be used. When JTAG is normally used straight out of power-up, then this feature will have no bearing on the functionality. The TDO flagging feature will need to be disabled if JTAG is not enabled on power-up and the feature has since been enabled.

When the TDO output from the ACS8510 Rev2.1 is connected to the TDI pin of the next device in the JTAG scan chain, the implementation should be such that a logic change caused by the action of the interrupt on the TDI input should not effect the operation when JTAG is not active.

External Protection Switching

Fast external switching between inputs <I_3> and <I_4> can also be triggered directly from a dedicated pin (SRCSW). This mode can be activated either by holding this pin high during reset, or by writing to bit 4 of register address 48Hex. Once external protection switching is enabled, then the value of this pin directly selects either <I_3> (SRCSW high) or <I_4> (SRCSW low). If this mode is activated at reset by pulling the SRCSW pin high, then it configures the default frequency tolerance of <I_3> and <I_4> to +/- 80 ppm (register address 41Hex and 42Hex). Any of these registers can be subsequently set by external software if required.

When external protection switching is enabled, the device will operate as a simple switch. All clock monitoring is disabled and the DPLL will simply be forced to try to lock on to the indicated reference source.

Clock Quality Monitoring

Clock quality is monitored and used to modify the priority tables of the local and remote ACS8510 Rev2.1 devices. The following parameters are monitored:

1. Activity (toggling)

2. Frequency (This monitoring is only performed whenthere is no irregular operation of the clock or loss of clock condition)

In addition, input ports <I_1> and <I_2> carry AMI-encoded composite clocks which are monitored by the AMI-decoder blocks. Loss of signal is declared by the decoders when either the signal amplitude falls below +0.3 V or there is no activity for 1 ms.

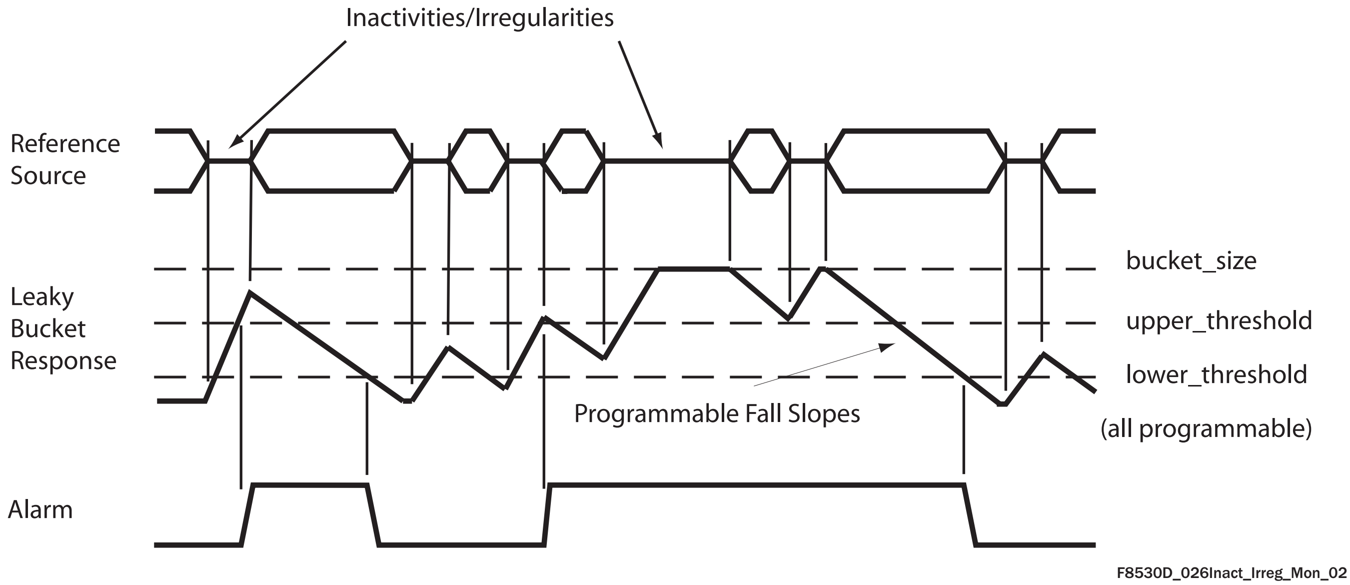
Any reference source which suffers a loss-of-signal, loss-of-activity, loss-of-regularity or clock out-of-band condition will be declared as unavailable.

Clock quality monitoring is a continuous process which is used to identify clock problems. There is a difference in dynamics between the selected clock and the other reference clocks.

Anomalies occurring on non-selected reference sources affect only that source's suitability for selection, whereas anomalies occurring on the selected clock could have a detrimental impact on the accuracy of the output clock.

Anomalies, whether affecting signal purity or signal frequency, could induce jitter or frequency offsets in the output clock, leading to anomalous behavior. Anomalies on the selected clock, therefore, have to be detected

Figure 9 Inactivity and Irregularity Monitoring



Leaky bucket timing

The time taken to raise an inactivity alarm on a reference source that has previously been fully active (leaky bucket empty) will be:

$$\frac{(\textit{cnfg\_activ\_upper\_threshold}\ N)}{8} \quad \text{secs}$$

where N is the number of the relevent leaky bucket configuration. If an input is intermittently inactive then this time can be longer. The default setting of *cnfg_activ_upper_threshold* is 6, therefore the default time is 0.75 s.

The time taken to cancel the activity alarm on a previously completely inactive reference source is calculated as:

$$\frac{2^{(\textit{cnfg\_decay\_rate}\ N)} \times ((\textit{cnfg\_bucket\_size}\ N) - (\textit{cnfg\_activ\_lower\_thrshold}\ N))}{8} \quad \text{secs}$$

where N is the number of the relevent leaky bucket configuration in each case. The default setting are shown in the following:

$$\frac{2^{1} \times (8-4)}{8} = 1.0 \text{ s}$$

as they occur and the phase locked loop must be temporarily isolated until the clock is once again pure. The clock monitoring process cannot be used for this because the high degree of accuracy required dictates that the process be slow. To achieve the immediacy required by the phase locked loop requires an alternative mechanism. The phase locked loop itself contains appropriate circuitry, based around the phase detector, and isolates itself from the selected reference source as soon as a signal impurity is detected. It can likewise respond to frequency offsets outside the permitted range since these result in saturation of the phase detector. When the phase locked loop is isolated from the reference source, it is essentially operating in a Holdover state; this is preferable to feeding the loop with a standby source, either temporarily or permanently, since excessive phase excursions on the output clock are avoided.

Anomalies detected by the phase detector are integrated in a leaky bucket accumulator. Occasional anomalies do not cause the accumulator to cross the alarm setting threshold, so the selected reference source is retained. Persistent anomalies cause the alarm setting threshold to be crossed and result in the selected reference source being rejected.

Activity Monitoring

The ACS8510 Rev2.1 has a combined inactivity and irregularity monitor. The ACS8510 Rev2.1 uses a "leaky bucket" accumulator, which is a digital circuit which mimics the operation of an analog integrator, in which input pulses increase the output amplitude but die away over time. Such integrators are used when alarms have to be triggered either by fairly regular defect events, which occur sufficiently close together, or by defect events which occur in bursts. Events which are sufficiently spread out should not trigger the alarm. By adjusting the alarm setting threshold, the point at which the alarm is triggered can be controlled. The point at which the alarm is cleared depends upon the decay rate and the alarm clearing threshold. On the alarm setting side, if several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur a little more spread out, but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. On the alarm clearing side, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). See Figure 9.

The "leaky bucket" accumulators are programmable for size, alarm set & reset thresholds and decay rate. Each source is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the accumulator is incremented. The accumulator will continue to increment up to the point that it reaches the programmed bucket size. The "fill rate" of the leaky bucket is, therefore, 8 units/second.

The "leak rate" of the leaky bucket is programmable to be in multiples of the fill rate (x1, x0.5, x0.25 and x0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to "leak" at the same time as a "fill" is avoided by preventing a "leak" when a "fill" event occurs. Disqualification of a non-selected reference source is based on inactivity, or on an out of band result from the frequency monitors. The currently selected reference source can be disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the next highest priority, active reference source is selected.

Frequency Monitoring

The ACS8510 Rev2.1 performs frequency monitoring to identify reference sources which have drifted outside the acceptable frequency range of ±16.6 ppm (measured with respect to the output clock). The *sts_reference_sources* out-of-band alarm for a particular reference source is raised when the reference source is outside the acceptable frequency range. The ACS8510 Rev2.1 DPLL has a programmable frequency limit of ±80 ppm. If the range is programmed to be > 16.6 ppm, the frequency monitors should be disabled so the input reference source is not automatically rejected as out of frequency range.

Modes of Operation

The ACS8510 Rev2.1 has three primary modes of operation (Free-run, Locked and Holdover) supported by three secondary, temporary modes (Pre-Locked, Lost_Phase and Pre-Locked2). These are shown in the State Transition Diagram, Figure 11.

The ACS8510 Rev2.1 can operate in Forced or Automatic control. On reset, the ACS8510 Rev2.1 reverts to Automatic Control, where transitions between states are controlled completely automatically. Forced Control can be invoked by configuration, allowing transitions to be performed under external control. This is not the normal mode of operation, but is provided for special occasions such as testing, or where a high degree of hands-on control is required.

Free-run mode

The Free-run mode is typically used following a power-on-reset or a device reset before network synchronization has been achieved. In the Free-run mode, the timing and synchronization signals generated from the ACS8510 Rev2.1 are based on the Master clock frequency provided from the external oscillator and are not synchronized to an input reference source. The frequency of the output clock is a fixed multiple of the frequency of the external oscillator, and the accuracy of the output clock is equal to the accuracy of the Master clock.

The transition from Free-run to Pre-locked occurs when the ACS8510 Rev2.1 selects a reference source.

Pre-Locked mode

The ACS8510 Rev2.1 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE specification, if the selected reference source is of good quality. If the device cannot achieve lock within 100 seconds, it reverts to Free-run mode and another reference source is selected.

Locked mode

The Locked mode is used when an input reference source has been selected and the PLL has had time to lock. When the Locked mode is achieved, the output signal is in phase and locked to the selected input reference source. The selected input reference source is determined by the priority table.

When the ACS8510 Rev2.1 is in Locked mode, the output frequency and phase follows that of the selected input reference source. Variations of the external crystal frequency have a minimal effect on the output frequency. Only the minimum to maximum frequency range is affected. Note that the term, 'in phase', is not applied in the conventional sense when the ACS8510 Rev2.1 is used as a frequency translator (e.g., when the input frequency is 2.048 MHz and the output frequency is 19.44 MHz) as the input and output cycles will be constantly moving past each other; however, this variation will itself be cyclical over time unless the input and output are not locked.

Lost_Phase mode

Lost-phase mode is entered when the current phase error, as measured within the DPLL, is larger than a preset limit (see register 04, bits 5:3), as a result of a frequency or phase transient on the selected reference source.

This mode is similar in behavior to the Pre-locked or Pre-locked(2) modes, although in this mode the DPLL is attempting to regain lock to the same reference rather than attempt lock to a new reference.

If the DPLL cannot regain lock within 100 s, the source is disqualified, and one of the following transitions takes place:

1. Go to Pre-Locked(2);

- If a known-good standby source is available.

2. Go to Holdover;

- If no standby sources are available.

Holdover mode

The Holdover mode is used when the ACS8510 Rev2.1 has been in Locked mode for long enough to acquire stable frequency data, but the final selected reference source has become unavailable and a replacement has not yet been qualified for selection. In Holdover mode, the ACS8510 Rev2.1 provides the timing and synchronization signals to maintain the Network Element (NE), but they are not phase locked to any input reference source.

The timing is based on a stored value of the frequency ratio obtained during the last Locked mode period.

To allow for further development of the way the internal algorithm operates, and to allow for customized switching behavior, the switch to and from Holdover state may be controlled by external software.

The device must be set in either “manual” mode or “automatic” mode:

1. Register *cnfg_mode* bit *holdover offset enable* set high (manual mode). The Holdover frequency is determined by the value in register *cnfg_holdover_offset*. This is a 19 bit signed number, with a LSB resolution of 0.0003 ppm, which gives an adjustment range of ±80 ppm. This value can be derived from a reading of the register *sts_curr_inc_offset* (addr 0D, 0C and 07) which gives, in the same format, an indication of the current output frequency deviation, which would be read when the device is locked. If required, this value could be read by an external microcontroller and averaged over the time required. The averaged value could then be fed to the *cnfg_holdover_offset* register ready for setting of the averaged frequency value when the device enters Holdover mode. The *sts_curr_inc_offset* value is internally derived from the Digital Phase Locked Loop (DPLL) integral path value, which already represents a well averaged measure of the current frequency, depending on the loop bandwidth selected.

2. Register *cnfg_mode* bit *holdover offset enable* set low (automatic mode). In automatic control, the device can be run in one of two ways:

2.1 Register *cnfg_holdover_offset* register 40 bit 7 *auto holdover averaging* is set high. The value is averaged internally over 32 samples at 32 seconds apart, giving the average frequency over approximately the last 20 minutes.

The proportional DPLL path is ignored so that recent signal disturbances do not affect the Holdover frequency value. If the device has been previously correctly locked, missing pulses in the input clock stream fed to the SETS IC are ignored, hence also avoiding any frequency disturbances to the output frequency value when an input clock source fails.

2.2 Register *cnfg_holdover_offset* register 40 bit 7 *auto holdover averaging* is set low. This simply freezes the DPLL at the current frequency (as reported by the *sts_curr_inc_offset* register). The proportional DPLL path is ignored so that recent signal disturbances do not affect the Holdover frequency value.

Automatic control with internal averaging (option 2.1) is the default condition. If the TCXO frequency is varying due to temperature fluctuations in the room, then the instantaneous value can be different from the average value, and then it may be possible to exceed the 0.05 ppm limit (depending on how extreme the temperature fluctuations are). It is advantageous to shield the TCXO to slow down frequency changes due to drift and external temperature fluctuations.

The frequency accuracy of Holdover mode has to meet the ITU-T, ETSI and Telcordia performance requirements. The performance of the external oscillator clock is critical in this mode, although only the frequency stability is important - the stability of the output clock in Holdover is directly related to the stability of the external oscillator.

Pre-Locked(2) mode

This state is very similar to the Pre-Locked state. It is entered from the Holdover state when a reference source has been selected and applied to the phase locked loop. It is also entered if the device is operating in Revertive mode and a higher-priority reference source is restored.

Upon applying a reference source to the phase locked loop, the ACS8510 Rev2.1 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE specification, if the selected reference source is of good quality.

If the device cannot achieve lock within 100 seconds, it reverts to Holdover mode and another reference source is selected.

Protection Facility

The ACS8510 Rev2.1 supports redundancy protection. The primary functions of this include:

- Alignment of the priority tables of both Master and Slave ACS8510 Rev2.1 devices so as to align the selection of reference sources of both Master and Slave ACS8510 Rev2.1 devices.

- Alignment of the phases of the 8 kHz and 2 kHz clocks in both Master and Slave ACS8510 Rev2.1 devices to within one cycle of the 77.76 MHz internal clock.

When two ACS8510 Rev2.1 devices are to be used in a redundancy-protection scheme within an NE, one will be designated as the Master and the other as the Slave. It is expected that an NE will use the T_{OUT0} output for its internal operations because the T_{OUT4} output is intended to feed an SSU/BITS system. An SSU/BITS will not be bothered by phase differences between signals arriving from different sources because it typically incorporates line build-out functions to absorb phase differences on reference inputs. This means that the phasing of the composite clocks between two ACS8510 Rev2.1 devices do not have to be mutually-aligned. The same is not true, however, of the T_{OUT0} output signals (T_{01} - T_{07}, Frame clock and Multi-Frame clock). It is usually important to align the phases of all equivalent T_{OUT0} signals generated by different sources so that switch-over from one device to another does not affect the internal operations of the NE. Both ACS8510 Rev2.1 devices will produce the same signals, which will be routed around the NE to the various consumers (clock sinks). With the possible exception of a through-timing mode, the signals from the Master device will be used by all consumers, unless the Master device fails, when each consumer will switch over to the signals generated by the Slave device.

Switchover to a new T_{OUT0} clock should be as hitless as possible. This requires the signals of both ACS8510 Rev2.1 devices to be phase aligned at each consumer. Phase alignment requires frequency alignment. To ensure that both devices can generate output clocks locked to the same source, both devices are supplied with the same reference sources on the same input ports and will have identical priority tables.

Failures of selected reference sources will result in both ACS8510 Rev2.1 devices making the same updates to their priority tables as availability information will be updated in both devices. Although, in principle, the priority tables will be the same if the same reference sources are used on the same input port on each device, in practice, this is only true if the reference sources actually arrive at each device - failures of a source seen only by one device and not by the other, such as could be caused, for example, by a backplane connector failure, would result in the priority tables becoming misaligned. It is thus necessary to force the priority tables to be aligned under normal operating conditions so that the devices can make the same decisions - this can be achieved by loading the availability seen by one device (via the *sts_reference_sources* register) into the *cnfg_sts_remote_sources_valid* register of the other device. Another factor which could affect hit-less switching is the frequency of the local oscillator clock used by each ACS8510 Rev2.1 device: these clocks are not mutually aligned and, whilst this has no impact on the frequency of the output clocks during locked mode, it could cause the output frequencies to diverge during Holdover mode if no action were taken to avoid it. In order to maintain alignment of the output frequencies of each ACS8510 Rev2.1 device even during Holdover, the Master device's 6.48 MHz output is fed into the Slave device on its <I_11> pin, whilst the Multi-Frame Sync (2 kHz) output is fed to the Sync2k input of the Slave. In this way, the Slave locks to the master's output and remains locked whilst the Master moves between operating states. Only when the Master fails does the Slave use its own reference inputs - should the Master have been in the Holdover state, the Slave device will see the same lack of reference sources and also enter the Holdover state. This scheme also provides a convenient way to phase-align all T_{OUT0} output clocks in Master and Slave devices, and also to detect the failure of the Master device.

If a Master device fails, the Slave has to take over responsibility for the generation of the output clocks, including the 8 kHz and 2 kHz Frame and Multi-Frame clocks. The Slave device is also given responsibility for building the priority table and performing the reference switching operations. The Slave device, therefore, adopts a more active role when the Master has failed. The *cnfg_mode* register 34 (Hex) Bit 1 contains the *Master/Slave* control bit to determine the designation of the device.

To restore redundancy protection, the Master has to be repaired and replaced. When this occurs, the new Master cannot immediately adopt its normal role because it must not cause phase hits on the output clocks. It has, therefore, to adopt a subordinate role to the active Slave device, at least until such time as it has acquired alignment to the 8 kHz and 2 kHz frame and Multi-Frame clocks and the priority table of the Slave device; then, when a switch-back (restoration) is ordered, the Master can take over responsibility. These activities, in Master or Slave operation, are summarized in Table 15 and described in detail in Application Note AN-SETS-2.

Alignment of Priority Tables in Master and Slave ACS8510 Rev2.1

Correct protection will only be achieved by connecting individual reference sources to the same input ports on each device and priority tables in each device must be aligned to each other.

The Master device must take account of the availability of each reference source seen by another device and a Slave device must adopt the same order of priority as the Master device (except that the Slave's highest-priority input is <I_11>). Both devices monitor the reference sources and decide the availability of each source; if the failure of a reference source is seen by both devices, they will both update their priority tables - however, if the reference source failure is only seen by one device and not by both, the priority tables could get out of step: this could be catastrophic if it resulted in two devices choosing different reference sources since any slight differences in frequency variation over time (e.g. wander) would mis-align the phase of the 8 kHz Frame and 2 kHz MultiFrame clocks produced by the individual devices, resulting in phase hits on switch-over. It is therefore important that the same priority table be built by each device, using the reference source availability seen by each device.

The monitoring of the reference sources performed by a Master ACS8510 Rev2.1 results in a list of available sources being placed in a *sts_valid_sources* register. This information is used within the device as one of the masks used to build the device's priority table. The information is passed to the Slave device and used to configure the *cnfg_sts_remote_sources_valid* register so that it can use it as a mask in building its own priority tables. The information is passed between devices using the microprocessor port.

Alignment of the Selection of Reference Sources for T_{OUT4} Generation in the Master and Slave ACS8510 Rev2.1

As stated previously, there is no need to align the phases of the T_{OUT4} outputs in Master and Slave devices. There is a need, however, to ensure that all devices select the same reference source. But, since there is no Holdover mode required for the generation of the T_{OUT4} clock, and every reference source is continuously monitored within each device, it is permissible to rely on external intelligence to command a switchover to an alternative source should the selected one fail. The time delay involved in detecting the failure, indicating it to the outside and selecting a new source, will result only in the SSU/BITS entering its Holdover mode for a short time.

Alignment of the Phases of the 8 kHz and 2 kHz Clocks in both Master and Slave ACS8510 Rev2.1

In addition to aligning the edges of the T_{OUT0} outputs of Master and Slave devices, it is necessary to align the edges of the Frame and MultiFrame clocks. If this is not performed, frame alignment may be lost in distant equipment on switch-over to an alternative device, resulting in anomalous network operation of a very serious nature.

In accordance with the alignment mechanism used with the main T_{OUT0} clock (described in the opening paragraphs of this section), whereby the 6.48 MHz output of the Master device is supplied to the Slave device, the alignment of both the 8 kHz and 2 kHz clocks is accomplished (they are already synchronous to the T_{OUT0} clocks) by feeding the 2 kHz clock of the Master device into the Slave device. The MultiFrame Sync clock output of the Slave device is also fed to the Sync2K input of the Master device. Alignment of the Multi-Frame Sync input occurs only when *cnfg_mode* register, bit 3, address 34Hex External 2 kHz *Sync Enable* is set to 1.

JTAG

The JTAG connections on the ACS8510 Rev2.1 allow a full boundary scan to be made. The JTAG implementation is fully compliant to IEEE 1149.1, with the following minor exceptions, and the user should refer to the standard for further information.

1. The output boundary scan cells do not capture data from the core, and so do not support INTEST. However this does not affect board testing.

2. In common with some other manufacturers, pin TRST is internally pulled low to disable JTAG by default. The standard is to pull high. The polarity of TRST is as the standard: TRST high to enable JTAG boundary scan mode, TRST low for normal operation.

3. The device does not support the optional tri-state capability (HIGHZ). This will be supported on the next revision of the device.

The JTAG timing diagram is shown in Figure 17.

PORB

The Power On Reset (PORB) pin resets the device if forced Low for a power on reset to be initiated. The reset is asynchronous, the minimum Low pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Asserting Reset is required at power on, and may be re-asserted at any time to restore defaults. This is implemented most simplistically by an external capacitor to GND along with the internal pull-up resistor. The ACS8510 Rev2.1 is held in a reset state for 250 ms after the PORB pin has been pulled High. In normal operation PORB should be held High.

Figure 10 Master-Slave Schematic

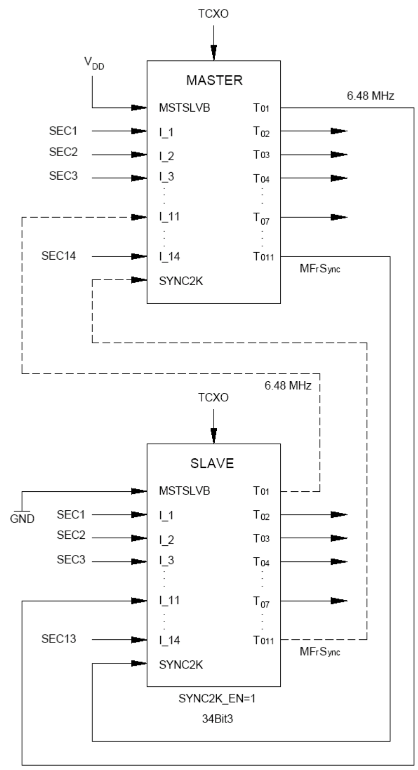


Table 15 Master-Slave Relationship

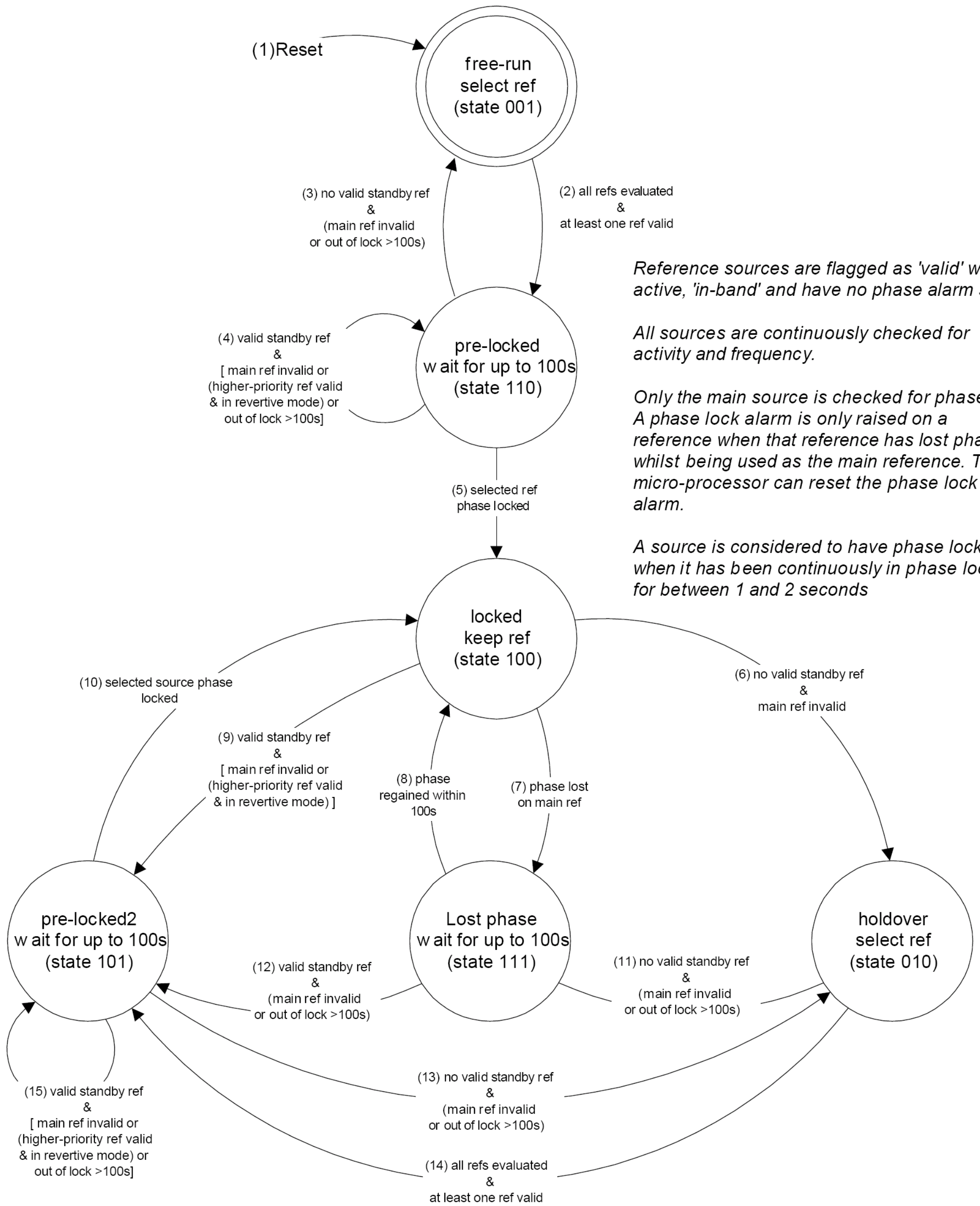
Ref_sources to Master ACS8510 Rev2.1	Ref_sources to Slave ACS8510 Rev2.1	Master ACS8510 Rev2.1 Status	Slave ACS8510 Rev2.1 Status	Master ACS8510 Rev2.1	Slave ACS8510 Rev2.1 Output	Comments
All good	All good	Good	Good	Locked (ref_x)	Locked to Master	
Some Failed	Some others failed	Good	Good	Locked (ref_y)	Locked to Master	
Good	Good	Good	Failed	Locked (ref_x)	Dead	
Good	Good	Failed	Good	Dead	Locked (ref_x)	
Good	Good	Failed	Failed	Dead	Dead	
Failed	Failed	Failed	Good	Holdover	Locked to Master	
Failed	Failed	Good	Failed	Holdover	Dead	
Failed	Failed	Failed	Good	Dead	Holdover	
Failed	Failed	Failed	Failed	Dead	Dead	

Notes: (i) Both ACS8510 Rev2.1 must build a common priority table so that the Slave ACS8510 Rev2.1 can select the same input reference source as the Master ACS8510 Rev2.1 if the Master fails (when the Master is OK, the Slave locks to the Master's output).

(ii) Slave ACS8510 Rev2.1 uses common priority table, built before Master ACS8510 Rev2.1 failed - priority table can be modified asstatus of the input reference sources changes.

(iii) Slave ACS8510 Rev2.1 outputs must remain in phase with those of Master ACS8510 Rev2.1.

Figure 11 Automatic Mode Control State Diagram



Reference sources are flagged as 'valid' when active, 'in-band' and have no phase alarm set.

All sources are continuously checked for activity and frequency.

Only the main source is checked for phase. A phase lock alarm is only raised on a reference when that reference has lost phase whilst being used as the main reference. The micro-processor can reset the phase lock alarm.

A source is considered to have phase locked when it has been continuously in phase lock for between 1 and 2 seconds

Electrical Specification

Maximum Ratings

Important Note: The “Absolute Maximum Ratings”are stress ratings only, and functional operation of the device at conditions other than those indicated in the “Operating Conditions” sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 16 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage VDD, VD+, VA1+, VA2+	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins)	V_{IN}	-	5.5	V
Output Voltage (non-supply pins)	V_{OUT}	-	5.5	V
Ambient Operating Temperature Range	T_A	-40	+85	^oC
Storage Temperature	T_{STOR}	-50	+150	^oC

Operating Conditions

Table 17 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply (dc voltage) VDD, VD+, VA1+, VA2+, VAMI+, VDD_DIFF	V_{DD}	3.0	3.3	3.6	V
Power Supply (dc voltage) VDD5	V_{DD5}	3.0	3.3/5.0	5.5	V
Ambient Temperature Range	T_A	-40	-	+85	^oC
Supply Current (Typical - one 19 MHz output)	I_{DD}	-	130	222	mA
Total Power Dissipation	P_{TOT}	-	430	800	mW

DC Characteristics

Table 18 DC Characteristics: TTL Input Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2.0	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Input Current	I_{IN}	-	-	10	µA

Table 19 DC Characteristics: TTL Input Port with Internal Pull-up

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-up Resistor	PU	30	-	80	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 20 DC Characteristics: TTL Input Port with Internal Pull-down

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2.0	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-down Resistor	PD	30	-	80	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 21 DC Characteristics: TTL Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{OUT} *Low* (I_{OL} = 4 mA)	V_{OL}	0	-	0.4	V
V_{OUT} *High* (I_{OH} = 4 mA)	V_{OH}	2.4	-	-	V
Drive Current	I_D	-	-	4	mA

Table 22 DC Characteristics: PECL Input/Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
PECL Input *Low* Voltage Differential Inputs (Note ii)	V_{ILPECL}	V_{DD}-2.5	-	V_{DD}-0.5	V
PECL Input *High* Voltage Differential Inputs (Note ii)	V_{IHPECL}	V_{DD}-2.4	-	V_{DD}-0.4	V
Input Differential Voltage	V_{IDPECL}	0.1	-	1.4	V
PECL Input *Low* Voltage Single-ended Input (Note iii)	V_{ILPECL_S}	V_{DD}-2.4	-	V_{DD}-1.5	V

Table 22 DC Characteristics: PECL Input/Output Port (cont...)

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
PECL Input *High* Voltage Single-ended Input (Note iii)	V_{ILPECL_S}	V_{DD}-1.3	-	V_{DD}-0.5	V
Input *High* Current Input Differential Voltage V_{ID} = 1.4V	I_{IHPECL}	-10	-	+10	µA
Input *Low* Current Input Differential Voltage V_{ID} = 1.4V	I_{ILPECL}	-10	-	+10	µA
PECL Output *Low* Voltage (Note iv)	V_{OLPECL}	V_{DD}-2.10	-	V_{DD}-1.62	V
PECL Output *High* Voltage (Note iv)	V_{OHPECL}	V_{DD}-1.25	-	V_{DD}-0.88	V
PECL Output Differential Voltage (Note iv)	V_{ODPECL}	580	-	900	mV

Notes: (i) *Unused differential input ports should be left floating and set in LVDS mode, or the positive and negative inputs tied to V_{DD} and GND respectively.*

(ii) *Assuming a differential input voltage of at least 100 mV.*

(iii) *Unused differential input terminated to V_{DD} -1.4 V.*

(iv) *With 50 Ω load on each pin to V_{DD} -2 V, i.e. 82 Ω to GND and 130 Ω to V_{DD}.*

Figure 12 Recommended Line Termination for PECL Input/Output Ports

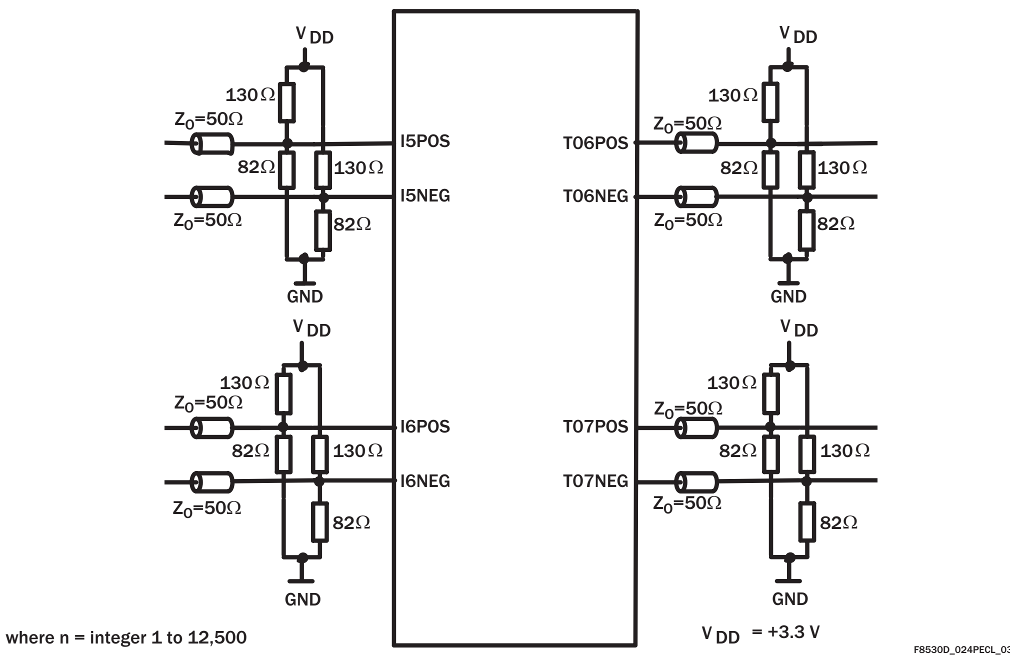


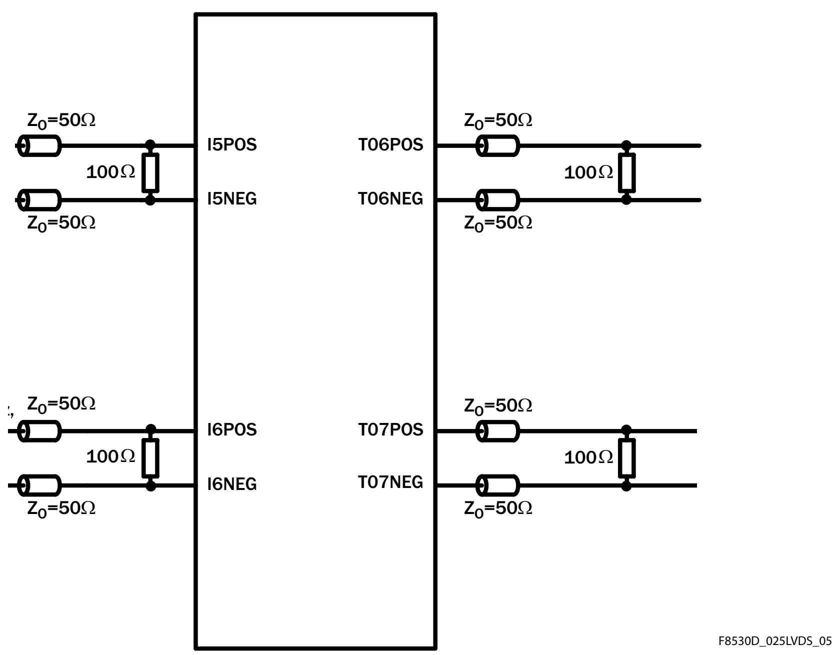
Table 23 DC Characteristics: LVDS Input/Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS Input Voltage Range Differential Input Voltage = 100 mV	V_{VRLVDS}	0	-	2.40	V
LVDS Differential Input Threshold	V_{DITH}	-100	-	+100	mV
LVDS Input Differential Voltage	$V_{IDLVTSDS}$	0.1	-	1.4	V
LVDS Input Termination Resistance Must be placed externally across the LVDS ± input pins of ACS8510 Rev2.1. Resistor should be 100 Ω with 5% tolerance	R_{TERM}	95	100	105	Ω
LVDS Output *High* Voltage (Note (i))	V_{OHLVDS}	-	-	1.585	V
LVDS Output *Low* Voltage (Note (i))	V_{OLLVDS}	0.885	-	-	V
LVDS Differential Output Voltage	V_{ODLVDS}	250	-	450	mV
LVDS Change in Magnitude of Differential Output Voltage for complementary States (Note (i))	$V_{DOSLVDS}$	-	-	25	mV
LVDS Output Offset Voltage Temperature = 25°C (Note (i))	V_{OSLVDS}	1.125	-	1.275	V

Note: (i) *With 100 Ω load between the differential outputs.*

Figure 13 Recommended Line Termination for LVDS Input/Output Ports



DC Characteristics: AMI Input/Output Port

(Across all operating Conditions, unless otherwise stated.)

The Alternate Mark Inversion (AMI) signal is DC balanced and consists of positive and negative pulses with a peak-to-peak voltage of 2.0 ±0.2 V.

The electrical specifications are taken from option a) of Table 2/G.703 - Digital 64 kbit/s centralized clock interface, from ITU G.703[6].

The electrical characteristics of the 64 kbit/s interface are as follows:

Nominal bit rate: 64 kbit/s. The tolerance is determined by the network clock stability.

There should be a symmetrical pair carrying the composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.

Over-voltage protection requirement: refer to Recommendation K.41[16]

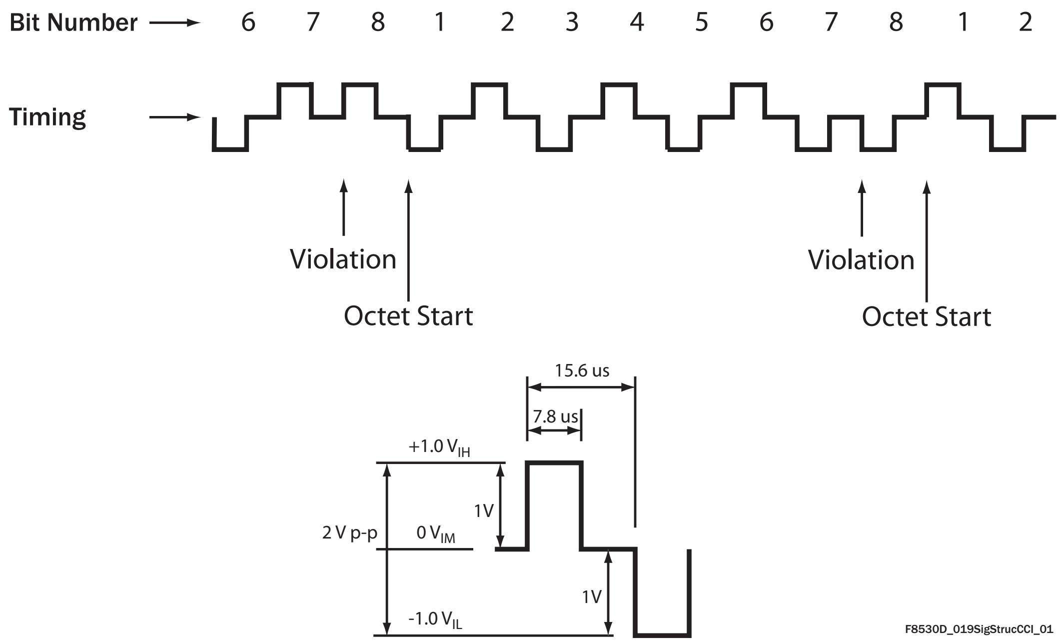
Code conversion rules:
The data signals are coded in AMI code with 100% duty cycle. The composite clock timing signals convey the 64 kHz bit-timing information using AMI coding with a 50% to 70% duty ratio and the 8 kHz octet phase information by introducing violations in the code rule. The structure of the signals and voltage level are shown in Figure 14, Figure 15 and Figure 16.

Table 24 DC Characteristics: AMI Input/Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Pulse Width	t_{PW}	1.56	7.8	14.04	µs
Input Pulse Rise/Fall Time	$t_{R/F}$	-	-	5	µs
AMI Input Voltage *High*	$V_{IH\ AMI}$	2.5	-	V_{DD} + 0.3	V
AMI Input Voltage *Middle*	$V_{VIM\ AMI}$	1.5	1.65	1.8	V
AMI Input Voltage *Low*	$V_{VIL\ AMI}$	0	-	1.4	V
AMI Output Current Drive	I_{AMIOUT}	-	-	20	mA
AMI Output *High* Voltage Output Current = 20mA	$V_{OH\ AMI}$	V_{DD} - 0.16	-	-	V
AMI Output *Low* Voltage Output Current = 20mA	$V_{OL\ AMI}$	-	-	0.16	V
Nominal Test Load Impedance	R_{TEST}	-	110	-	Ω
“Mark” Amplitude After Transformer	V_{MARK}	0.9	1.0	1.1	V
“Space” Amplitude After Transformer	V_{SPACE}	- 0.1	0	0.1	V

Figure 14 Signal Structure of 64 kHz/8 kHz Central Clock Interface)



Note...after suitable input/output transformer (also see G.703[6]).

Figure 15 AMI Input and Output Signal Levels

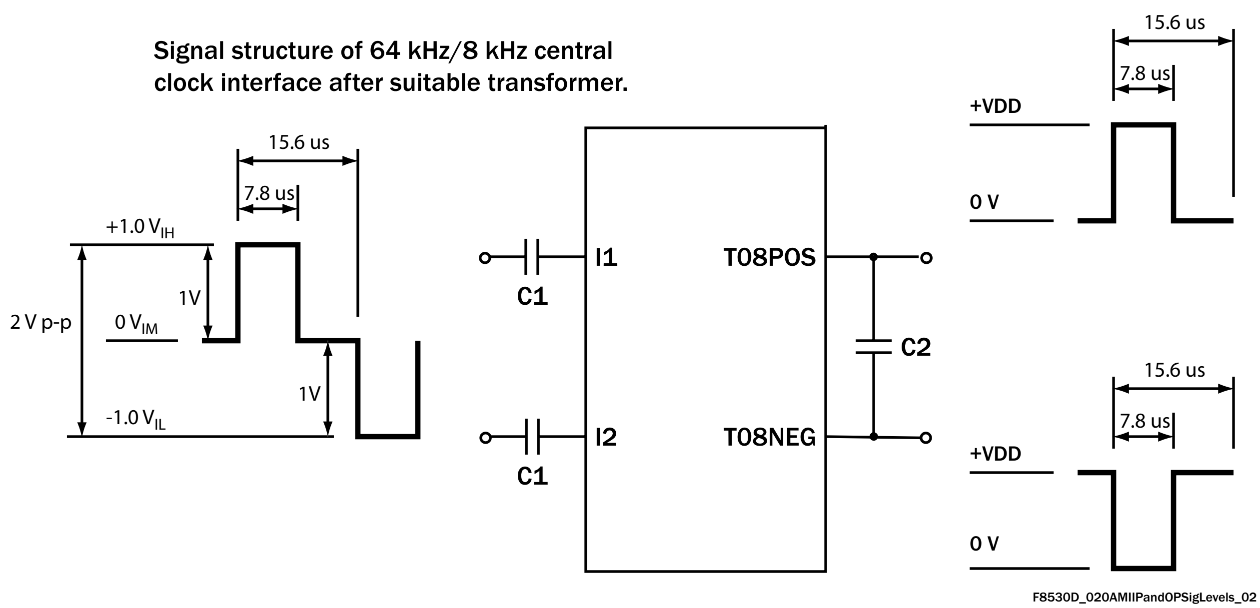
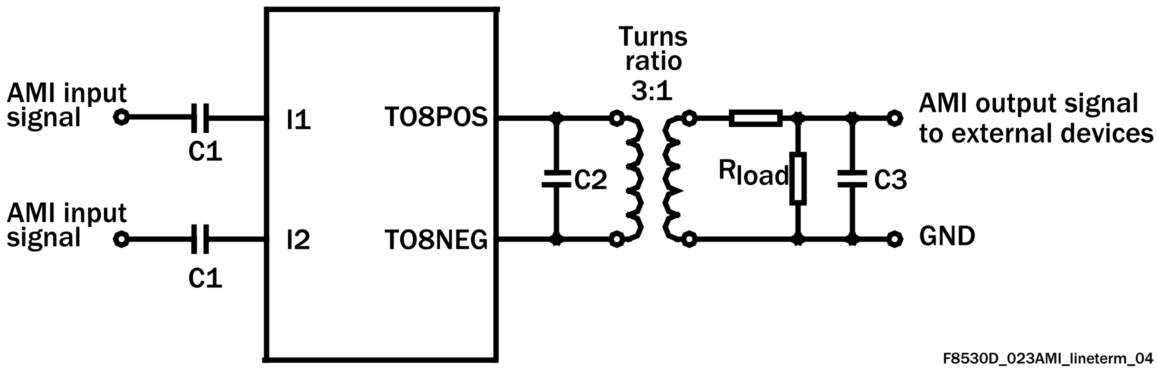


Figure 16 Recommended Line Termination for AMI Output/Output Ports



Note...The AMI inputs I1 and I2 should be connected to the external AMI clock source by 470 nF coupling capacitor C1.

The AMI differential output T_{08}POS/T_{08}NEG should be coupled to a line transformer with a turns ratio of 3:1. Components C2 = 470 pF and C3 = 2 nF. If a transformer with a turns ratio of 1:1 is used, a 3:1 ratio potential divider R_{load} must be used to achieve the required 1 V p-p voltage level for the positive and negative pulses.

Jitter Performance

Table 25 DC Characteristics: Output Jitter Generation (Test Definition G.813)

Across all operating conditions unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI_{p-p} max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

Test Definition	Filter used	UI Spec	UI Measurement on ACS8510 Rev2.1
G813[11] for 155 MHz option 1	500 Hz to 1.3 MHz	UI_{p-p} = 0.5	0.058 (Note (ii))
G813[11] for 155 MHz option 1	65 kHz to 1.3 MHz	UI_{p-p} = 0.1	0.048 (Note (iii)) 0.048 (Note (ii))
G813[11] for 155 MHz option 2	12 kHz to 1.3 MHz	UI_{p-p} = 0.1	0.053 (Note (iv)) 0.053 (Note (v))
			0.058 (Note (vi)) 0.053 (Note (vii))
			0.053 (Note (ii)) 0.058 (Note (iii))
			0.057 (Note (viii)) 0.055 (Note (ix))
			0.057 (Note (x)) 0.057 (Note (xi))
			0.057 (Note (xii)) 0.053 (Note (xiii))
G813[11] and G812[10] for 2.048 MHz option 1	20 Hz to 100 kHz	UI_{p-p} = 0.5	0.046 (Note (xiv))

Table 26 DC Characteristics: Output Jitter Generation (Test Definition G812)

Across all operating conditions unless otherwise stated
Output jitter generation measured over 60 seconds interval, UI_{p-p} max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

Test Definition	Filter used	UI Spec	UI Measurement on ACS8510 Rev2.1
G812[10] for 1.544 MHz	10 Hz to 40 kHz	UI_{p-p} = 0.05	0.036 (Note (xiv))
G812[10] for 155.52 MHz electrical	500 Hz to 1.3 MHz	UI_{p-p} = 0.5	0.058 (Note (xv))
G812[10] for 2.048 MHz	65 Hz to 1.3 MHz	UI_{p-p} = 0.075	0.036 (Note (xv))

Table 27 DC Characteristics: Output Jitter Generation (Test Definition ETS-300-462-3)

Across all operating conditions unless otherwise stated
Output jitter generation measured over 60 seconds interval, UI_{p-p} max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

Test Definition	Filter used	UI Spec	UI Measurement on ACS8510 Rev2.1
ETS-300-462-3[3] for 2.048 MHz SEC	20 Hz to 100 kHz	UI_{p-p} = 0.5	0.046 (Note (xiv))
ETS-300-462-3[3] for 2.048 MHz SEC (Filter spec 49 Hz to 100 kHz)	20 Hz to 100 kHz	UI_{p-p} = 0.2	0.046 (Note (xiv))
ETS-300-462-3[3] for 2.048 MHz SSU	20 Hz to 100 kHz	UI_{p-p} = 0.05	0.046 (Note (xiv))
ETS-300-462-3[3] for 155.52 MHz	500 Hz to 1.3 MHz	UI_{p-p} = 0.5	0.058 (Note (xv))
ETS-300-462-3[3] for 155.52 MHz	65 kHz to 1.3 MHz	UI_{p-p} = 0.1	0.048 (Note (xv))

Table 28 DC Characteristics: Output Jitter Generation (Test Definition GR-253-CORE)

Across all operating conditions unless otherwise stated
Output jitter generation measured over 60 seconds interval, UI_{p-p} max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

Test Definition	Filter used	UI Spec	UI Measurement on ACS8510 Rev2.1
GR-253-CORE[17] net i/f, 51.84 MHz	100 Hz - 0.4 MHz	UI_{p-p} = 1.5	0.022 (Note (xv))
GR-253-CORE[17] net i/f, 51.84 MHz (Filter spec 20 kHz to 400 Hz)	18 kHz - 0.4 MHz	UI_{p-p} = 0.15	0.019 (Note (xv))
GR-253-CORE[17] net i/f, 155.52 MHz	500 Hz - 1.3 MHz	UI_{p-p} = 1.5	0.058 (Note (xv))
GR-253-CORE[17] net i/f, 155.52 MHz	65 kHz - 1.3 MHz	UI_{p-p} = 0.15	0.048 (Note (xv))
GR-253-CORE[17] cat II elect i/f, 155.52 MHz	12 kHz - 400 kHz	UI_{p-p} = 0.1	0.057 (Note (xv))
		UI_{rms}= 0.1	0.006 (Note (xv))
GR-253-CORE[17] cat II elect i/f, 51.84 MHz	12 kHz - 1.3 MHz	UI_{p-p} = 0.1	0.057 (Note (xv))
		UI_{rms}= 0.01	0.006 (Note (xv))
GR-253-CORE[17] DS1 i/f, 1.544 MHz	10_Hz - 40 kHz	UI_{p-p} = 0.1	0.036 (Note (xiv))
		UI_{rms}= 0.01	0.0055 (Note (xiv))

Table 29 DC Characteristics: Output Jitter Generation (Test Definition AT&T 62411)

Across all operating conditions unless otherwise stated
Output jitter generation measured over 60 seconds interval, UI_{p-p} max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

Test Definition	Filter used	UI Spec	UI Measurement on ACS8510 Rev2.1
AT&T 62411[2] for 1.544 MHz (Filter spec 10Hz to 8 kHz)	10 Hz to 40 kHz	UI_{rms} = 0.02	0.0055 (Note (xiv))
AT&T 62411[2] for 1.544 MHz	10 Hz to 40 kHz	UI_{rms} = 0.025	0.0055 (Note (xiv))
AT&T 62411[2] for 1.544 MHz	10 Hz to 40 kHz	UI_{rms} = 0.025	0.0055 (Note (xiv))
AT&T 62411[2] for 1.544 MHz	Broadband	UI_{rms} = 0.05	0.0055 (Note (xiv))

Table 30 DC Characteristics: Output Jitter Generation (Test Definition G.742)

Across all operating conditions unless otherwise stated
Output jitter generation measured over 60 seconds interval, UI_{p-p} max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

Test Definition	Filter used	UI Spec	UI Measurement on ACS8510 Rev2.1
G-742[8] for 2.048 MHz	DC to 100 kHz	UI_{p-p} = 0.25	0.047 (Note (xiv))
G-742[8] for 2.048 MHz (Filter spec 18 kHz to 100 kHz)	20 Hz to 100 kHz	UI_{p-p} = 0.05	0.046 (Note (xiv))
G-742[8] for 2.048 MHz	20 Hz to 100 kHz	UI_{p-p} = 0.05	0.046 (Note (xiv))

Table 31 DC Characteristics: Output Jitter Generation (Test Definition GR-499-CORE)

Across all operating conditions unless otherwise stated
Output jitter generation measured over 60 seconds interval, UI_{p-p} max measured using Vectron 6664 12.8 MHz TCXO on ICT Flexacom + 10 MHz reference from Wavetek 905.

Test Definition	Filter used	UI Spec	UI Measurement on ACS8510 Rev2.1
GR-499-CORE[18] & G824[14] for 1.544 MHz	10 Hz to 40 kHz	UI_{p-p} = 5.0	0.036 (Note (xiv))
GR-499-CORE[18] & G824[14] for 1.544 MHz (Filter spec 8 kHz to 40 kHz)	10 Hz to 40 kHz	UI_{p-p} = 0.1	0.036 (Note (xiv))
GR-499-CORE[18] for 1.544 MHz	>10 Hz	UI_{p-p} = 0.05	0.036 (Note (xiv))

Notes for Tables 25 to 31

Notes: (i) Filter used is that defined by test definition unless otherwise stated

(ii) 5 Hz bandwidth, 19.44 MHz direct lock

(iii) 5 Hz bandwidth, 8 kHz lock

(iv) 20 Hz bandwidth, 19.44 MHz direct lock

(v) 20 Hz bandwidth, 8 kHz lock

(vi) 10 Hz bandwidth, 19.44 MHz direct lock

(vii) 10 Hz bandwidth, 8 kHz lock

(viii) 2.5 Hz bandwidth, 19.44 MHz direct lock

(ix) 2.5 Hz bandwidth, 8 kHz lock

(x) 1.2 Hz bandwidth, 19.44 MHz direct lock

(xi) 1.2 Hz bandwidth, 8 kHz lock

(xii) 0.6 Hz bandwidth, 19.44 MHz direct lock

(xiii) 0.6 Hz bandwidth, 8 kHz lock

(xiv) 5 Hz bandwidth, 8 kHz lock, 2.048 MHz input

(xv) 5 Hz bandwidth, 8 kHz lock, 19.44 MHz input

Figure 17 JTAG Timing

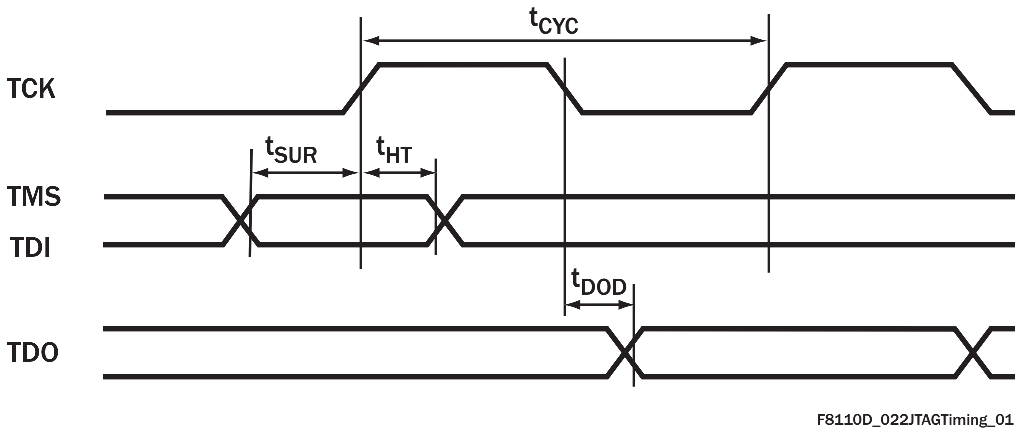
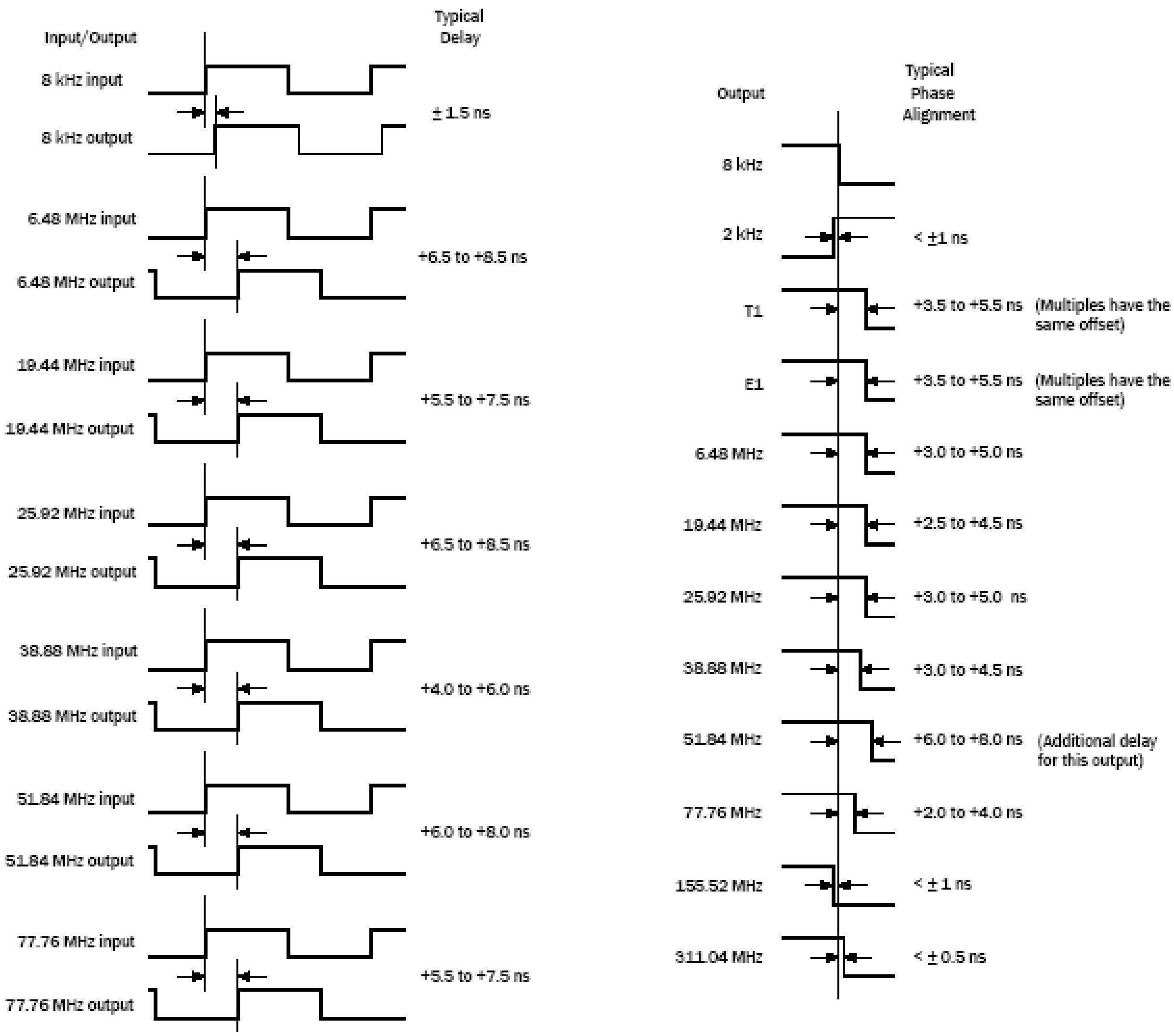


Table 32 JTAG Timing (for use with Figure 17)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Cycle Time	t_{CYC}	50	-	-	ns
TMS/TDI to TCK rising edge time	t_{SUR}	3	-	-	ns
TCK rising to TMS/TDI hold time	t_{HT}	23	-	-	ns
TCK falling to TDO valid	t_{DOD}	-	-	5	ns

Input/Output Timing

Figure 18 Input/Output Timing with Phase Build-out Off



Motorola Mode

In MOTOROLA mode, the device is configured to interface with a microprocessor using a 680x0 type bus as parallel data + address. Figure 19 and Figure 20 show the timing diagrams of read and write accesses for this mode.

Figure 19 Read Access Timing in MOTOROLA Mode

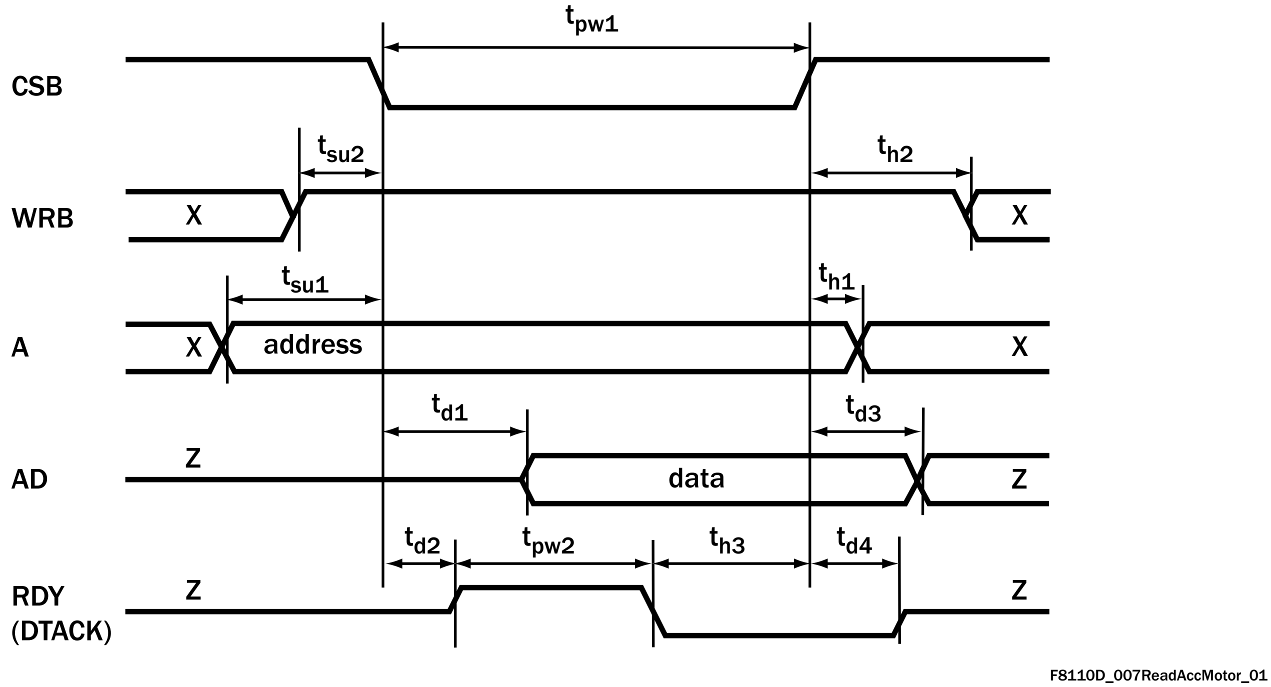


Table 33 Read Access Timing in MOTOROLA Mode (for use with Figure 19)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{su2}	Setup WRB valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $CSB_{falling\ edge}$ to AD valid	-	-	177 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to $DTACK_{rising\ edge}$	-	-	13 ns
t_{d3}	Delay $CSB_{rising\ edge}$ to AD high-Z	-	-	0 ns
t_{d4}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	CSB *Low* time	485 ns(i)	-	-
t_{pw2}	RDY *High* time	310 ns	-	472 ns
t_{h1}	Hold A valid after $CSB_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold WRB valid after $CSB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB *Low* after $RDY_{falling\ edge}$	0 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	320 ns	-	-

Note: (i) Timing with RDY. If RDY not used, t_{pw1} becomes 178 ns.

Figure 20 Write Access Timing in MOTOROLA Mode

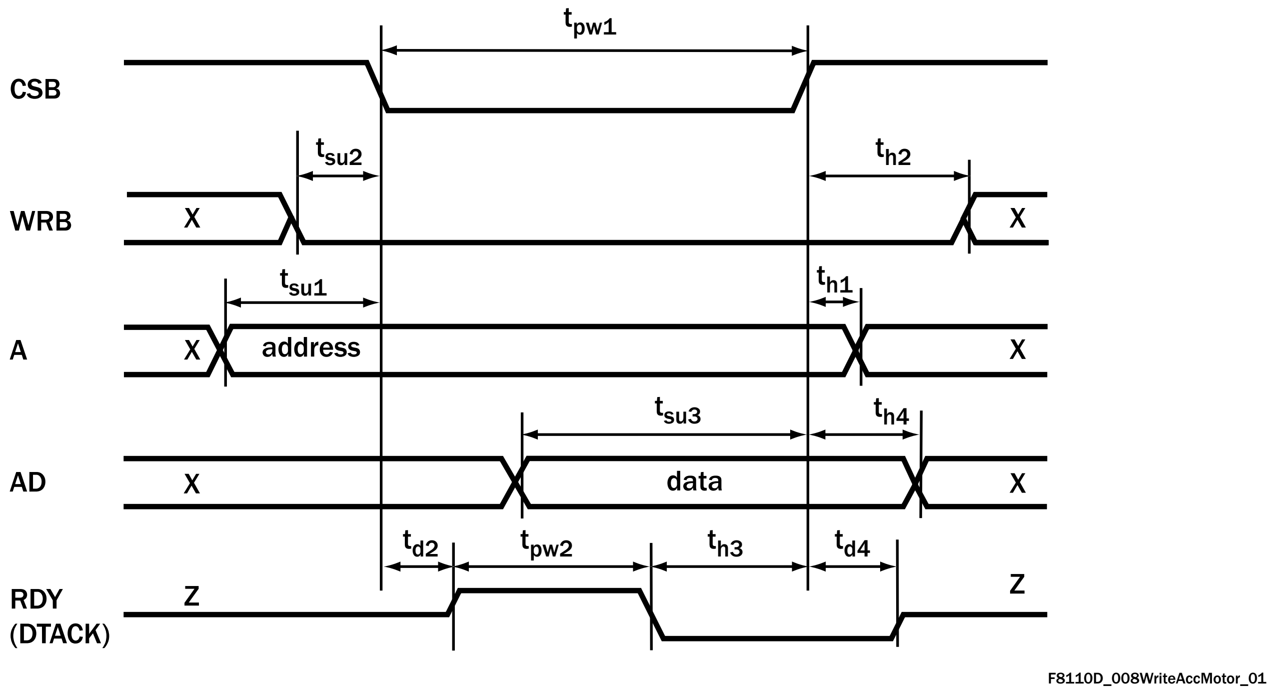


Table 34 Write Access Timing in MOTOROLA Mode (for use with Figure 20)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{su2}	Setup WRB valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before $CSB_{rising\ edge}$	3 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to $RDY_{rising\ edge}$	-	-	13 ns
t_{d4}	Delay $CSB_{rising\ edge}$ to RDY *High-Z*	-	-	7 ns
t_{pw1}	CSB *Low* time	485 ns(i)	-	-
t_{pw2}	RDY *High* time	310 ns	-	472 ns
t_{h1}	Hold A valid after $CSB_{rising\ edge}$	3 ns	-	-
t_{h2}	Hold WRB *Low* after $CSB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold CSB *Low* after $RDY_{falling\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after $CSB_{rising\ edge}$	4 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	320 ns	-	-

Note: (i) Timing with RDY. If RDY not used, t_{pw1} becomes 178 ns.

Intel Mode

In Intel mode, the device is configured to interface with a microprocessor using a 80x86 type bus as parallel data + address. Figure 21 and Figure 22 show the timing diagrams of read and write accesses for this mode.

Figure 21 Read Access Timing in INTEL Mode

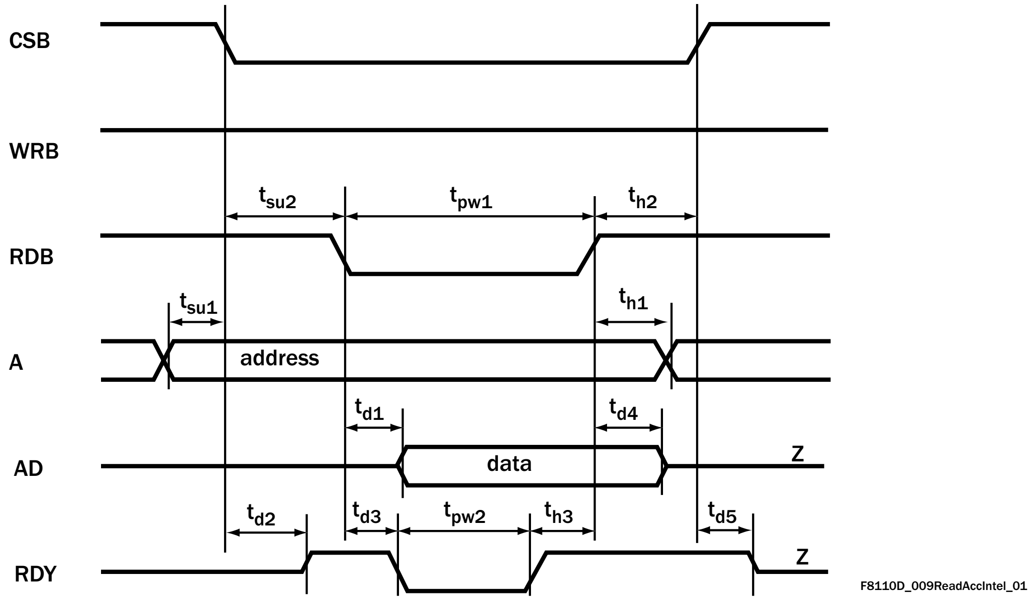


Table 35 Read Access Timing in INTEL Mode (for use with Figure 21)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $RDB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $RDB_{falling\ edge}$ to AD valid	-	-	177 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $RDB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	14 ns
t_{d4}	Delay $RDB_{rising\ edge}$ to AD high-Z	-	-	10 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	RDB *Low* time	486 ns(i)	-	-
t_{pw2}	RDY *Low* time	310 ns	-	472 ns
t_{h1}	Hold A valid after $RDB_{rising\ edge}$	0 ns	-	-
t_{h2}	Hold CSB *Low* after $RDB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB *Low* after $RDY_{rising\ edge}$	0 ns	-	-
t_p	Time between consecutive accesses ($RDB_{rising\ edge}$ to $RDB_{falling\ edge}$, or $RDB_{rising\ edge}$ to $WRB_{falling\ edge}$)	320 ns	-	-

Note: (i) Timing with RDY. If RDY not used, t_{pw1} becomes 180 ns.

Figure 22 Write Access Timing in INTEL Mode

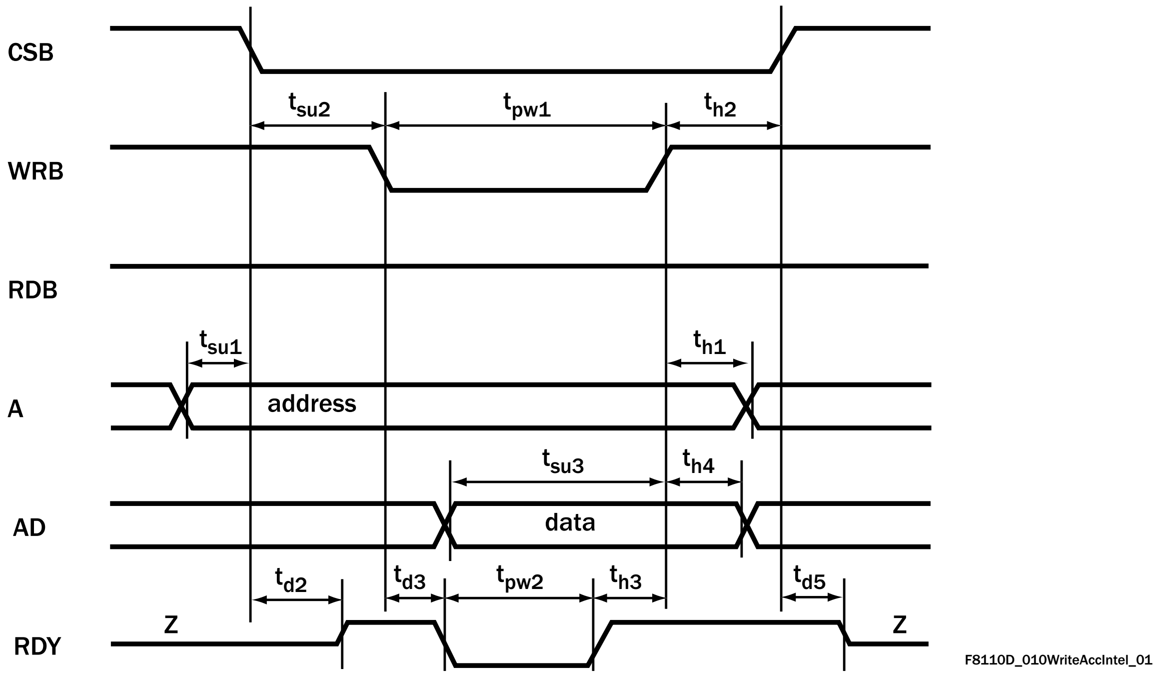


Table 36 Write Access Timing in INTEL Mode (for use with Figure 22)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup A valid to $CSB_{falling\ edge}$	0 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $WRB_{falling\ edge}$	0 ns	-	-
t_{su3}	Setup AD valid before $WRB_{rising\ edge}$	3 ns	-	-
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $WRB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	14 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	9 ns
t_{pw1}	WRB *Low* time	486 ns(i)	-	-
t_{pw2}	RDY *Low* time	310 ns	-	472 ns
t_{h1}	Hold A valid after $WRB_{rising\ edge}$	170 ns(ii)	-	-
t_{h2}	Hold CSB *Low* after $WRB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold WRB *Low* after $RDY_{rising\ edge}$	0 ns	-	-
t_{h4}	Hold AD valid after $WRB_{rising\ edge}$	4 ns	-	-
t_p	Time between consecutive accesses ($WRB_{rising\ edge}$ to $WRB_{falling\ edge}$, or $WRB_{rising\ edge}$ to $RDB_{falling\ edge}$)	320 ns	-	-

Notes: (i) Timing with RDY. If RDY not used, t_{pw1} becomes 180 ns.

(ii) Timing if t_{h2} is greater than 170 ns, otherwise 5 ns after CSB rising edge.

Multiplexed Mode

In MULTIPLEXED mode, the device is configured to interface with a microprocessor using a multiplexed address/data bus. Figures 23 and 24 show the timing diagrams of read and write accesses.

Figure 23 Read Access Timing in MULTIPLEXED Mode

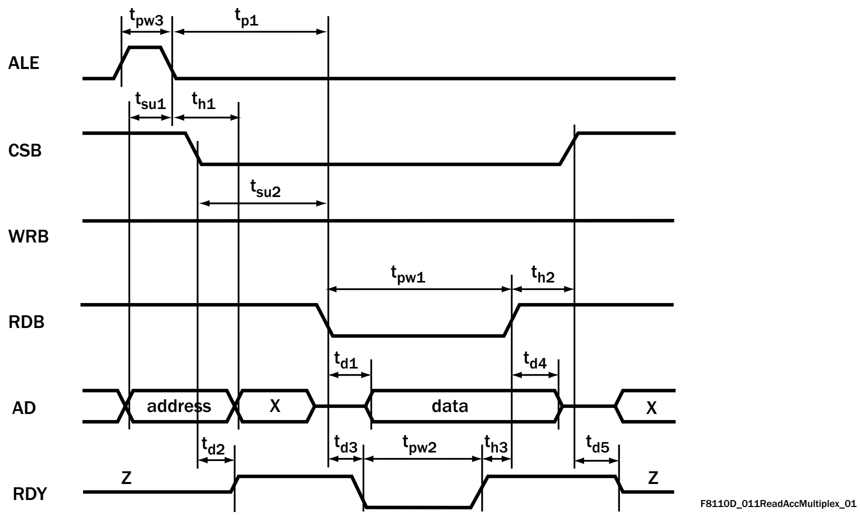


Table 37 Read Access Timing in MULTIPLEXED Mode (for use with Figure 23)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup AD address valid to $ALE_{falling\ edge}$	2 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $RDB_{falling\ edge}$	0 ns	-	-
t_{d1}	Delay $RDB_{falling\ edge}$ to AD data valid	-	-	177 ns
t_{d2}	Delay $CSB_{falling\ edge}$ to RDY active	-	-	13 ns
t_{d3}	Delay $RDB_{falling\ edge}$ to $RDY_{falling\ edge}$	-	-	15 ns
t_{d4}	Delay $RDB_{rising\ edge}$ to AD data high-Z	-	-	9 ns
t_{d5}	Delay $CSB_{rising\ edge}$ to RDY high-Z	-	-	10 ns
t_{pw1}	RDB *Low* time	487 ns(i)	-	-
t_{pw2}	RDY *Low* time	310 ns	-	472 ns
t_{pw3}	ALE *High* time	2 ns	-	-
t_{h1}	Hold AD address valid after $ALE_{falling\ edge}$	3 ns	-	-
t_{h2}	Hold CSB *Low* after $RDB_{rising\ edge}$	0 ns	-	-
t_{h3}	Hold RDB *Low* after $RDY_{rising\ edge}$	0 ns	-	-
t_{p1}	Time between $ALE_{falling\ edge}$ and $RDB_{falling\ edge}$	0 ns	-	-
t_{p2}	Time between consecutive accesses ($RDB_{rising\ edge}$ to $ALE_{rising\ edge}$)	320 ns	-	-

Note: (i) Timing with RDY. If RDY not used, t_{pw1} becomes 180 ns.

Figure 24 Write Access Timing in MULTIPLEXED Mode

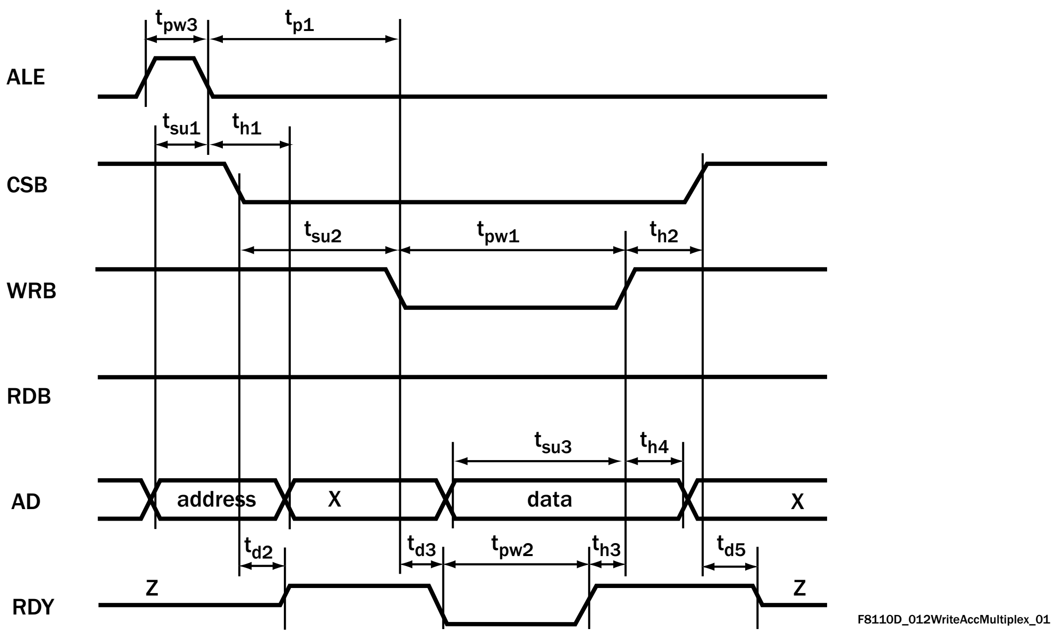


Table 38 Write Access Timing in MULTIPLEXED Mode (For use with Figure 24)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Set up AD address valid to ALE$_{\text{falling edge}}$	2 ns	-	-
t_{su2}	Set up CSB$_{\text{falling edge}}$ to WRB$_{\text{falling edge}}$	0 ns	-	-
t_{su3}	Set up AD data valid to WRB$_{\text{rising edge}}$	3 ns	-	-
t_{d2}	Delay CSB$_{\text{falling edge}}$ to RDY active	-	-	13 ns
t_{d3}	Delay WRB$_{\text{falling edge}}$ to RDY$_{\text{falling edge}}$	-	-	15 ns
t_{d5}	Delay CSB$_{\text{rising edge}}$ to RDY high-Z	-	-	9 ns
t_{pw1}	WRB *Low* time	487 ns$^{(i)}$	-	-
t_{pw2}	RDY *Low* time	310 ns	-	472 ns
t_{pw3}	ALE *High* time	2 ns	-	-
t_{h1}	Hold AD address valid after ALE$_{\text{falling edge}}$	3 ns	-	-
t_{h2}	Hold CSB *Low* after WRB$_{\text{rising edge}}$	0 ns	-	-
t_{h3}	Hold WRB *Low* after RDY$_{\text{rising edge}}$	0 ns	-	-
t_{h4}	AD data hold valid after WRB$_{\text{rising edge}}$	4 ns	-	-
t_{p1}	Time between ALE$_{\text{falling edge}}$ and WRB$_{\text{falling edge}}$	0 ns	-	-
t_{p2}	Time between consecutive accesses (WRB$_{\text{rising edge}}$ to ALE$_{\text{rising edge}}$)	320 ns	-	-

Note: (i) Timing with RDY. If RDY not used, t_{pw1} becomes 180 ns.

Serial Mode

In Serial mode, the device is configured to interface with a serial microprocessor bus. The combined minimum High and Low times for SCLK define the maximum clock rate.

For Write access this is 2.77 MHz (360 ns). For Read access the maximum SCLK rate is slightly slower and is affected by the setting of CLKE, being either 2.0 MHz (500 ns) or 1 MHz (1 us).

This mismatch in rates is caused by the sampling technique used to detect the end of the address field in Read mode. It takes up to 3 cycles of an internal 6.40 MHz clock to start the Read process following receipt of the final address bit. This is 468 ns. The Read data is then decoded and clocked out onto SDO directly using SCLK. With CLKE=1, the falling edge of SCLK is used to clock out the SDO. With CLKE=0, the rising edge of SCLK is used to clock out the SDO.

A minimum period of 500 ns (468 capture plus 32 decode) is required between the final address bit and clocking it out onto SDO. This means that to guarantee the correct operation of the Serial interface, with CLKE=0, SCLK has a maximum clock rate of 2 MHz. With CLKE=1, SCLK has a maximum clock rate of 1 MHz.

SCLK is not required to run between accesses (i.e., when CSB = 1). The following Figures show the timing diagrams for Write and Read access for this mode.

Figure 25 Read Access Timing in SERIAL Mode

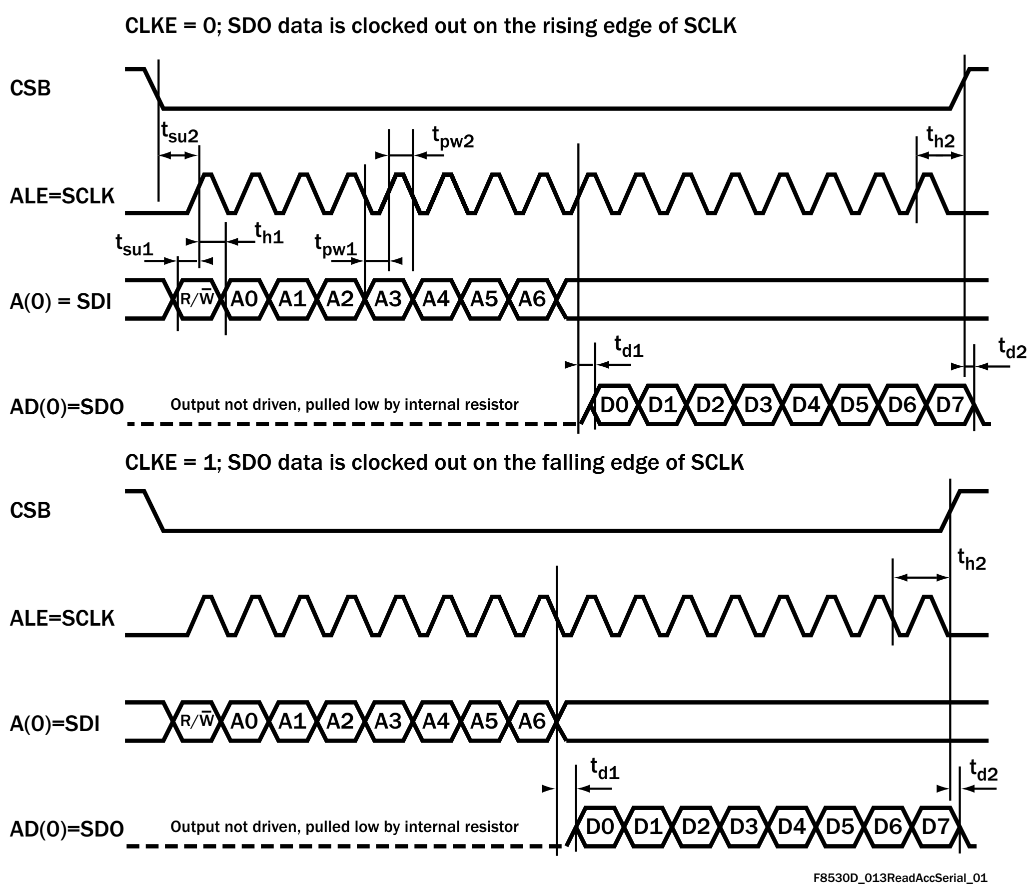


Table 39 Read Access Timing in SERIAL Mode (For use with Figure 25)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	0 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	160 ns	-	-
t_{d1}	Delay $SCLK_{rising\ edge}$ ($SCLK_{falling\ edge}$ for CLKE = 1) to SDO valid	-	-	17 ns
t_{d2}	Delay $CSB_{rising\ edge}$ to SDO high-Z	-	-	10 ns
t_{pw1}	SCLK *Low* time CLKE = 0 CLKE = 1	 250 ns 500 ns	-	-
t_{pw2}	SCLK *High* time CLKE = 0 CLKE = 1	 250 ns 500 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	170 ns	-	-
t_{h2}	Hold CSB *Low* after $SCLK_{rising\ edge}$, for CLKE = 0 Hold CSB *Low* after $SCLK_{falling\ edge}$, for CLKE = 1	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

Figure 26 Write Access Timing in SERIAL Mode

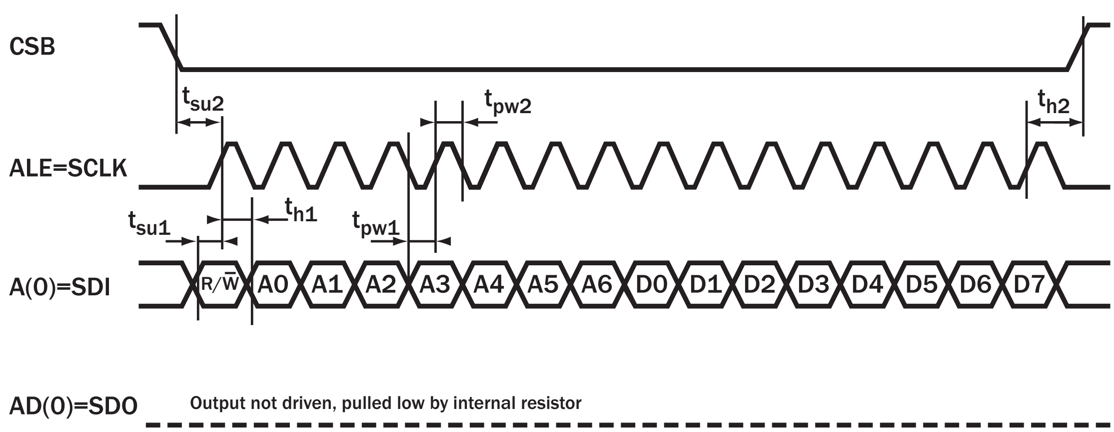


Table 40 Write Access Timing in SERIAL Mode (For use with Figure 26)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	0 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	160 ns	-	-
t_{pw1}	SCLK *Low* time	180 ns	-	-
t_{pw2}	SCLK *High* time	180 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	170 ns	-	-
t_{h2}	Hold CSB *Low* after $SCLK_{rising\ edge}$	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

EPROM Mode

This mode is suitable for use with an EPROM, in which configuration data is stored (one-way communication - status information will not be accessible). A state machine internal to the ACS8510 Rev2.1 device will perform numerous EPROM read operations to read the data out of the EPROM. In EPROM Mode, the ACS8510 Rev2.1 takes control of the bus as Master and reads the device set-up from an AMD AM27C64 type EPROM at lowest speed (250ns) after device set-up (system reset). The EPROM access state machine in the up interface sequences the accesses. Figure 27 shows the access timing of the device in EPROM mode.

Further information can be found in the AMD AM27C64 datasheet.

Figure 27 Access Timing in EPROM mode

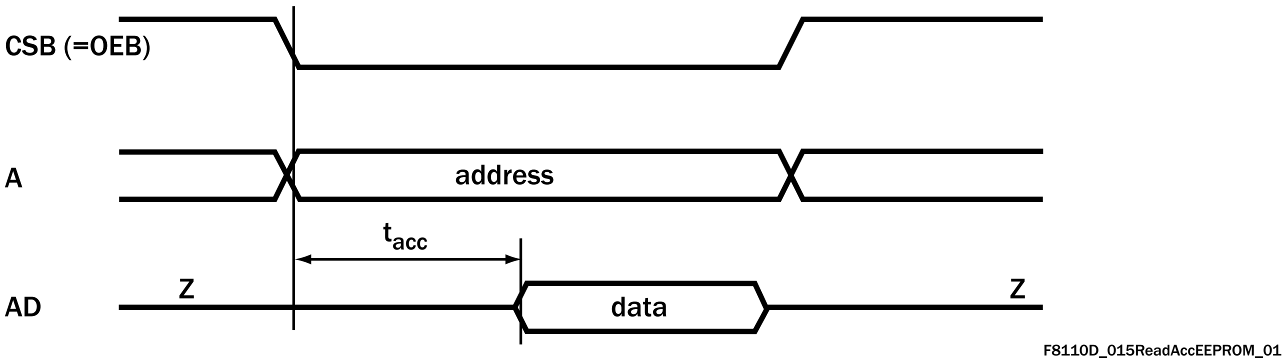
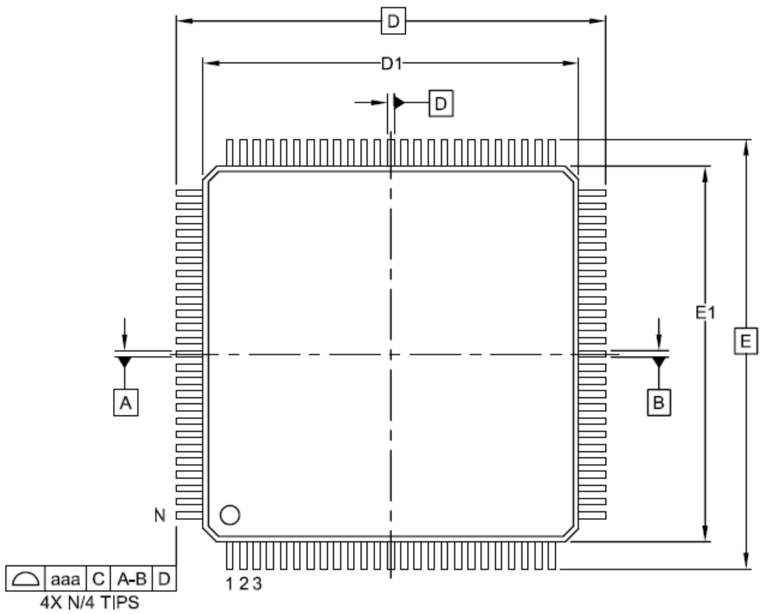


Table 41 Access Timing in EPROM mode (For use with Figure 27)

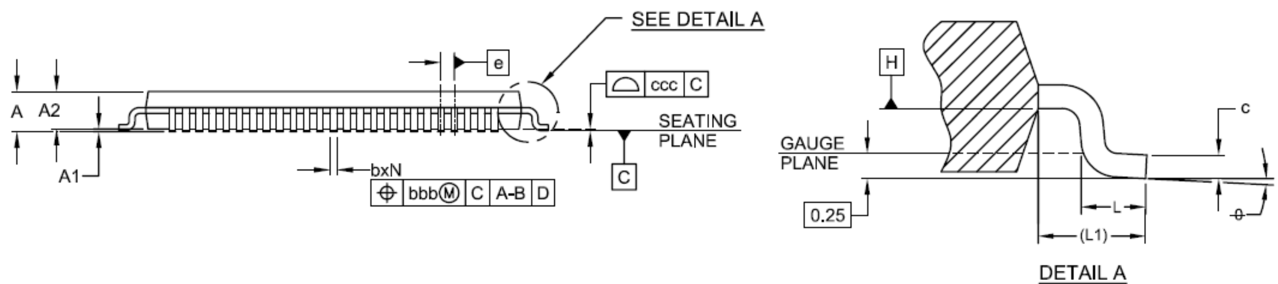
Symbol	Parameter	MIN	TYP	MAX
t_{acc}	Delay $CSB_{falling\ edge}$ or A change to AD valid	-	-	920 ns

Package Information

Figure 28 LQFP Package



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.055	-	.063	1.40	-	1.60
A1	.002	-	.006	0.05	-	0.15
A2	.053	.055	.057	1.35	1.40	1.45
b	.007	.009	.011	0.17	-	0.27
c	.004	-	.008	0.09	-	0.20
D	.630 BSC			16.00 BSC		
D1	.547	.551	.559	13.90	14.00	14.10
E	.630 BSC			16.00 BSC		
E1	.547	.551	.559	13.90	14.00	14.10
e	.020 BSC			0.50 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.00)		
N	100			100		
θ1	0°	-	7°	0°	-	7°
aaa	.008			0.20		
bbb	.003			0.08		
ccc	.003			0.08		



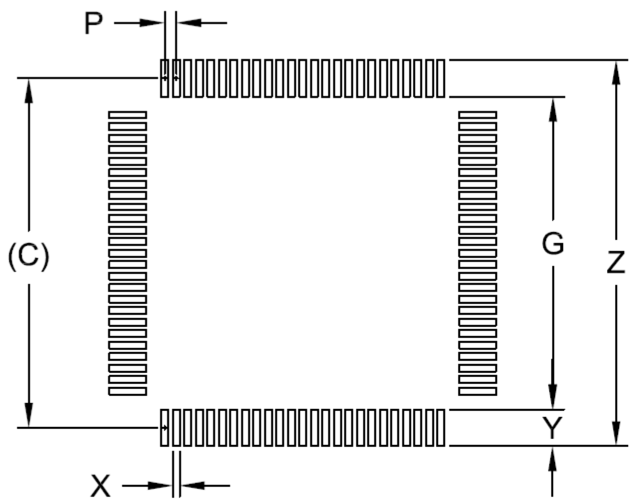
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
3. DIMENSIONS "E1" AND "D1" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-026, VARIATION BED.

Thermal Conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

Figure 29 Typical 100 Pin LQFP Footprint



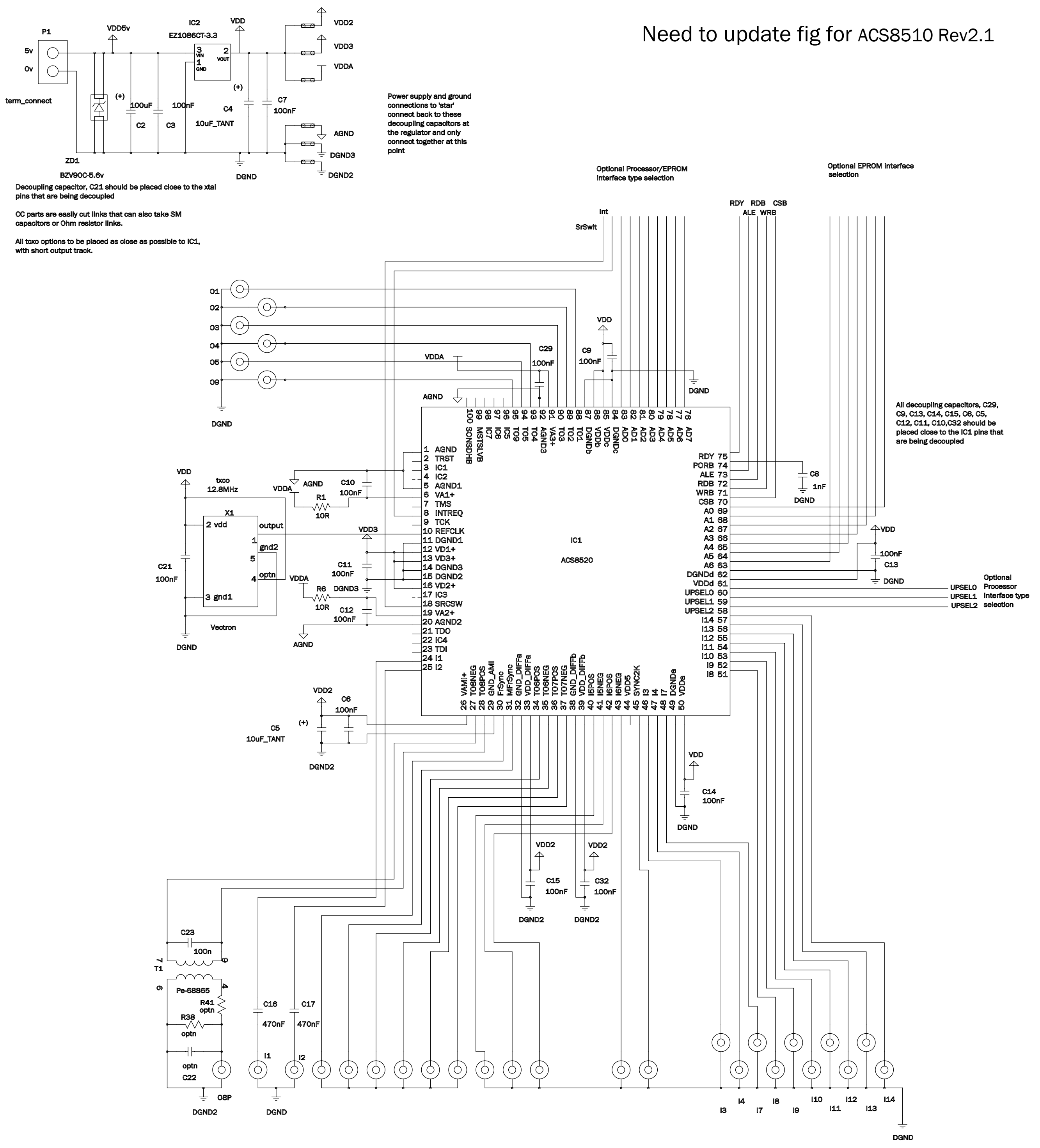
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.598)	(15.20)
G	.535	13.60
P	.020	0.50
X	.012	0.30
Y	.063	1.60
Z	.661	16.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.
3. REFERENCE IPC-SM-782A, RLP NO. 592A.

Figure 30 Simplified Application Schematic

Need to update fig for ACS8510 Rev2.1



Abbreviations

AMI	Alternate Mark Inversion
APLL	Analogue Phase Locked Loop
BITS	Building Integrated Timing Supply
DFS	Digital Frequency Synthesis
DPLL	Digital Phase Locked Loop
DS1	1544 kb/s interface rate
DTO	Discrete Time Oscillator
E1	2048 kb/s interface rate
I/O	Input - Output
LOF	Loss of Frame Alignment
LOS	Loss Of Signal
LQFP	Low profile Quad Flat Pack
LVDS	Low Voltage Differential Signal
MTIE	Maximum Time Interval Error
NE	Network Element
OCXO	Oven Controlled Crystal Oscillator
PBO	Phase Build-out
PDH	Plesiochronous Digital Hierarchy
PECL	Positive Emitter Coupled Logic
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
POR	Power-On Reset
ppb	parts per billion
ppm	parts per million
p-p	peak-to-peak
R/W	Read/Write
rms	root-mean-square
RO	Read Only
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
SSF	Synchronization Signal Failure
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
TDEV	Time Deviation
TCXO	Temperature Compensated Crystal Oscillator
UI	Unit Interval
WEEE	Waste Electrical and Electronic Equipment (directive)

References

[1] ANSI T1.101-1999 (1999)
Synchronization Interface Standard

[2] AT & T 62411 (12/1990)
ACCUNET® T1.5 Service description and Interface Specification

[3] ETSI ETS 300 462-3, (01/1997)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3: The control of jitter and wander within synchronization networks

[4] ETSI ETS 300 462-5 (09/1996)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment

[5] IEEE 1149.1 (1990)
Standard Test Access Port and Boundary-Scan Architecture

[6] ITU-T G.703 (10/1998)
Physical/electrical characteristics of hierarchical digital interfaces

[7] ITU-T G.736 (03/1993)
Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s

[8] ITU-T G.742 (1988)
Second order digital multiplex equipment operating at 8448 kbit/s, and using positive justification

[9] ITU-T G.783 (10/2000)
Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks

[10] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[11] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[12] ITU-T G.822 (11/1988)
Controlled slip rate objectives on an international digital connection

[13] ITU-T G.823 (03/2000)
The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

[14] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[15] ITU-T G.825 (03/2000)
The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH)

[16] ITU-T K.41 (05/1998)
Resistibility of internal interfaces of telecommunication centres to surge overvoltages

[17] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[18] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements

[19] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria

Trademark Acknowledgements

Revision Status/History

The Revision Status of the datasheet, as shown in the center of the datasheet header bar, may be DRAFT, PRELIMINARY, or FINAL, and refers to the status of the Device (not the datasheet) within the design cycle. DRAFT status is used when the design is being realized but is not yet physically available, and the datasheet content reflects the intention of the design. The datasheet is raised to PRELIMINARY status when initial prototype devices are physically available, and the datasheet content more accurately represents the realization of the design. The datasheet is only raised to FINAL status after the device has been fully characterized, and the datasheet content updated with measured, rather than simulated parameter values.

This is a FINAL release (Revision 2.02) of the ACS8510 Rev2.1 datasheet. Changes made for this document revision are given in Table 42, together with a brief summary of previous revisions. For specific changes between earlier revisions, refer (where available) to those earlier revisions. Always use the current version of the datasheet.

Table 42 Revision History

Revision	Reference	Description of changes
1.06 to 2.00 September 2003	Non-revertive Mode p36-37	Updated description of Non-Revertive Mode
2.01 September 2004	All pages	Document reformatted, no technical changes.
2.02 June 2006	Front page, back page and “Abbreviations” on page 72	Updated to reflect availability of lead (Pb)-free packaged part.
	Trademark Acknowledgements and Revision Status/History	Sections updated.
	Back page	Former US mailing address removed. (Mail now delivered to main address).
	Figure 28 and Figure 29	Updated Package and Footprint drawings.
	Back page	Taiwan address updated.

Notes

Ordering Information

Table 43 Parts List

Part Number	Description
ACS8510 Rev2.1	SETS Synchronous Equipment Timing Source for SONET or SDH Network Elements
ACS8510 Rev2.1T	Lead (Pb)-free packaged version of ACS8510 Rev2.1; RoHS and WEEE compliant.

Disclaimers

Life support- This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications, and is not authorized or warranted for such use.

Right to change- Changes may be made to this product without notice. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards- Operation of this device is subject to the User's implementation and design practices. It is the responsibility of the User to ensure equipment using this device is compliant to any relevant standards.

Contact Information for Semtech International AG

Taiwan Branch	Tel: 886-2-2748-3380 Fax: 886-2-2748-3390	Semtech Switzerland GmbH Japan Branch	Tel: 81-3-6408-0950 Fax: 81-3-6408-0951
Korea Branch	Tel: 82-2-527-4377 Fax: 82-2-527-4376	Semtech Limited (U.K.)	Tel: 44-(0)1794-527-600 Fax: 44-(0)1794-527-601
Shanghai Office	Tel: 86-21-6391-0830 Fax: 86-21-6391-0831	Semtech France SARL	Tel: 33-(0)169-28-22-00 Fax: 33-(0)169-28-12-98
Semtech International AG is a wholly-owned subsidiary of Semtech Corporation, which has its headquarters in the U.S.A.		Semtech Germany GmbH	Tel: 49-(0)8161-140-123 Fax: 49-(0)8161-140-124

ISO9001
CERTIFIED