

# A8519 and A8519-1

## Wide Input Voltage Range, High-Efficiency, Fault-Tolerant LED Driver

### FEATURES AND BENEFITS (CONTINUED)

- Excellent input voltage transient response at lowest PWM duty cycle
- Gate driver for optional P-channel MOSFET input disconnect switch
- LED current accuracy 0.7%
- LED string current-matching accuracy 0.8%
- Protection against:
  - Shorted boost switch, inductor or output capacitor
  - Shorted FSET or ISET resistor
  - Open or shorted LED pins and LED strings
  - Open boost diode
  - Overtemperature

### DESCRIPTION (CONTINUED)

The A8519 has a synchronization pin that allows boost switching frequencies to be synchronized in the range of 320 kHz to 2.3 MHz. The high switching frequency allows the converter to operate above the AM radio band. The IC contains a clock output pin that allows other converters to be synchronized to the A8519's boost switching frequency.

The A8519 employs hysteresis control to help regulate the LED current at extremely short PWM on-time. The A8519-1 is identical to the A8519, except that it uses a smaller hysteresis window to reduce output voltage ripple during PWM dimming.

### SELECTION GUIDE

Part Number	Operating Ambient Temperature Range $T_A$ (°C)	Hysteresis Window	Package	Packaging [1]	Leadframe Plating
A8519KLPTTR-T	–40 to 125	350 mV	20-pin TSSOP with exposed thermal pad	4000 pieces per reel	100% matte tin
A8519KETTR-R	–40 to 125	350 mV	28-pin 5 × 5 mm QFN with exposed thermal pad and sidewall plated	1500 pieces per reel	100% matte tin
A8519KLPTTR-T-1	–40 to 125	150 mV	20-pin TSSOP with exposed thermal pad	4000 pieces per reel	100% matte tin
A8519KETTR-R-1	–40 to 125	150 mV	28-pin 5 × 5 mm QFN with exposed thermal pad and sidewall plated	1500 pieces per reel	100% matte tin

[1] Contact Allegro for additional packing options.



### ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
LEDx Pins	$V_{LEDx}$	x = 1, 2, 3, or 4	–0.3 to 40	V
OVP Pin	$V_{OVP}$		–0.3 to 40	V
VIN, VOUT Pins	$V_{IN}, V_{OUT}$		–0.3 to 40	V
VSENSE, GATE Pins	$V_{SENSE}, V_{GATE}$		$V_{IN} - 7.4$ to $V_{IN} + 0.4$	V
SW Pin [3]	$V_{SW}$	Continuous	–0.6 to 42	V
		t < 50 ns	–1 to 48	V
FAULT Pin	$V_{FAULT}$		–0.3 to 40	V
APWM, PWM, CLKOUT, COMP, FSET, ISET, VDD Pins			–0.3 to 5.5	V
Operating Ambient Temperature	$T_A$	K temperature range	–40 to 125	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	$T_{stg}$		–55 to 150	°C

[2] Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the electrical characteristics table is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

[3] SW DMOS is self-protecting and will conduct when  $V_{SW}$  exceeds 48 V.

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**THERMAL CHARACTERISTICS:** May require derating at maximum conditions; see application information.

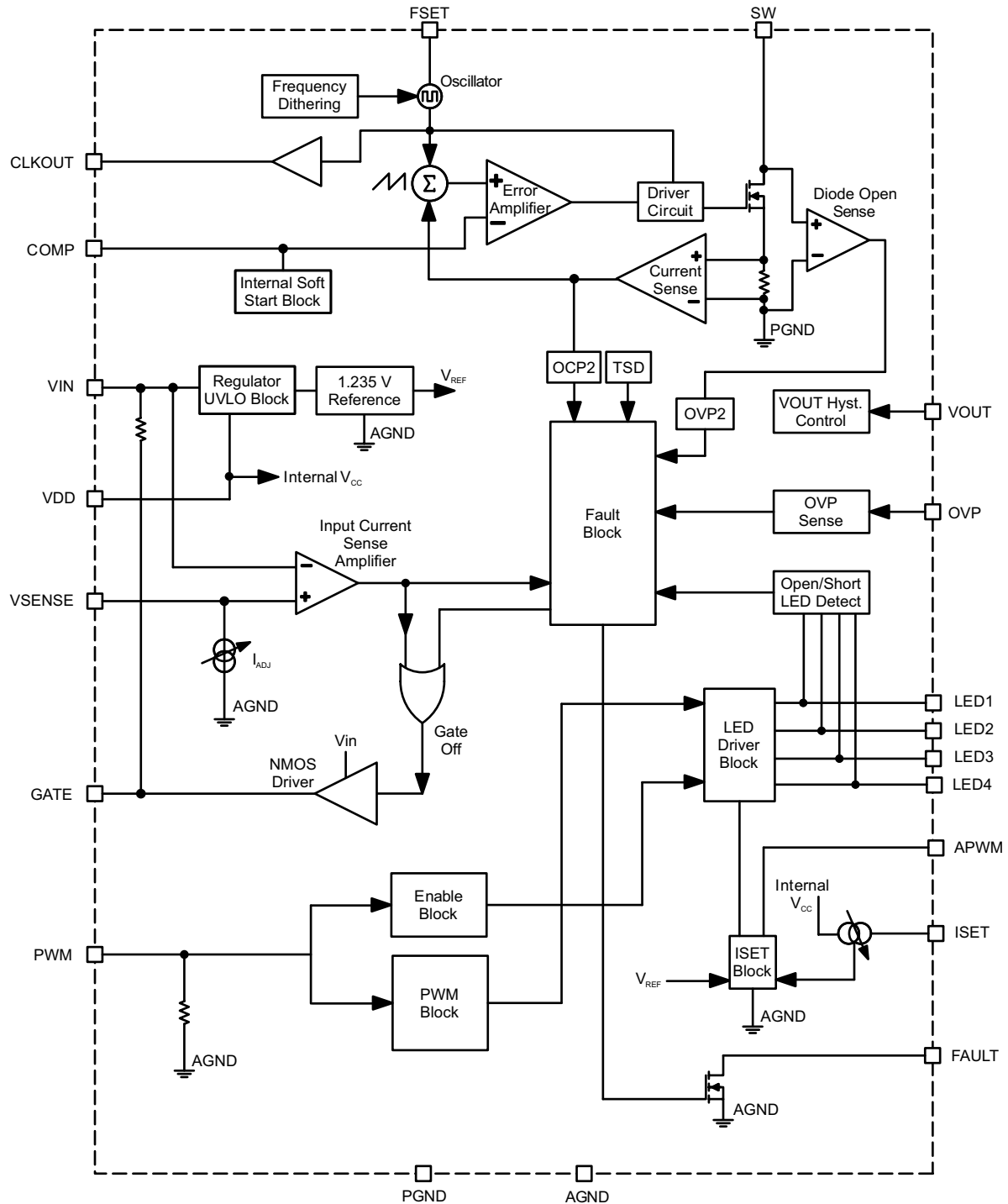
Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LP Package on 2-layer 3 in <sup>2</sup> PCB	40	°C/W
		ET Package on 2-layer 3 in <sup>2</sup> PCB	Contact factory	°C/W
		LP Package on 4-layer PCB Based on JEDEC Standards	29	°C/W
		ET Package on 4-layer PCB Based on JEDEC Standards	32	°C/W

[1] Additional thermal information available on the Allegro website.

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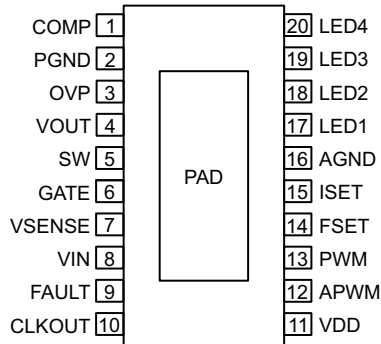
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### Functional Block Diagram

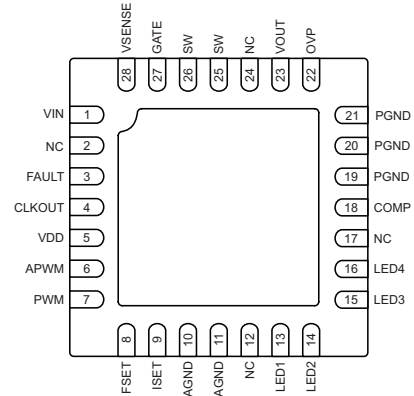


### PINOUT DIAGRAMS

20-Pin TSSOP with Exposed Thermal Pad (suffix LP)



28-Pin QFN with Exposed Thermal Pad (suffix ET)



Terminal List Table

Pin Number		Name	Function
LP	ET		
1	18	COMP	Output of the error amplifier and compensation node. Connect an R <sub>z</sub> -C <sub>z</sub> -C <sub>p</sub> network from this pin to GND for control loop compensation.
2	19, 20, 21	PGND	Power ground for internal N-channel MOSFET switching device. Connect to PCB ground plane.
3	22	OVP	Overvoltage protection. Connect external resistor from VOUT to this pin to adjust the overvoltage protection level.
4	23	VOUT	Connect directly to boost output voltage.
5	25, 26	SW	The drain of the internal N-channel MOSFET switching device of the boost converter.
6	27	GATE	Output gate driver pin for external P-channel MOSFET control.
7	28	VSENSE	Connect this pin to the negative sense side of the current sense resistor R <sub>sc</sub> . The threshold voltage is measured as V <sub>IN</sub> -V <sub>SENSE</sub> . There is also fixed current sink to allow for trip threshold adjustment.
8	1	VIN	Input power to the IC as well as the positive input used for current sense resistor.
9	3	FAULT	The pin is an open-drain type configuration that will be pulled low when a fault occurs. Connect a 100 kΩ resistor between this pin and desired logic level voltage.
10	4	CLKOUT	Logic output representing the switching frequency of internal boost oscillator. This allows other converters to be synchronized to the same frequency (with the same frequency dithering, if applicable)
11	5	VDD	Output of internal LDO (bias regulator). Connect a 1 μF decoupling capacitor between this pin and GND.
12	6	APWM	Analog trimming option or dimming. Applying a digital PWM signal to this pin adjusts the internal I <sub>SET</sub> current.
13	7	PWM	Enables the IC when this pin is pulled high. Also serves to control the LED intensity by using pulse-width modulation. Typical PWM dimming frequency is in the range of 100 to 400 Hz.
14	8	FSET	Frequency/synchronization pin. A resistor R <sub>FSET</sub> from this pin to GND sets the switching frequency (with dithering superimposed). It can also be used to synchronize two or more converters in the system to an external frequency between 320 kHz and 2.3 MHz (dithering is disabled in this case).
15	9	ISET	Connect R <sub>ISET</sub> resistor between this pin and GND to set the desired LED current setting.
16	10, 11	AGND	LED current ground. Connect to PCB ground plane.
17, 18, 19, 20	13, 14, 15, 16	LED 1-4	LED current sinks #1 to 4. Connect the cathode of each LED string to associated pin. Unused LED pin must be terminated to GND through a 3.09 kΩ resistor.
–	2, 12, 17, 24	NC	No connect. Leave open or connect to GND.
–	–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 8 vias, directly in the pad.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>INPUT VOLTAGE</b>						
Input Voltage Range [3]	$V_{IN}$		• 4.5	–	40	V
UVLO Start Threshold	$V_{UVLOrise}$	$V_{IN}$ rising	• –	–	4.35	V
UVLO Stop Threshold	$V_{UVLOfall}$	$V_{IN}$ falling	• –	–	3.9	V
UVLO Hysteresis	$V_{UVLOHYS}$		300	450	600	mV
<b>INPUT SUPPLY CURRENT</b>						
Input Quiescent Current	$I_Q$	$V_{PWM} = V_{IH}$ , $f_{SW} = 2\text{ MHz}$	• –	8	15	mA
Input Sleep Supply Current	$I_{SLEEP}$	$V_{IN} = 16\text{ V}$ , $V_{PWM} = V_{SYNC} = 0\text{ V}$	• –	2.0	10	$\mu\text{A}$
<b>INPUT LOGIC LEVELS (PWM, APWM)</b>						
Input Logic Level Low	$V_{IL}$		• –	–	0.4	V
Input Logic Level High	$V_{IH}$		• 1.5	–	–	V
PWM Input Pull-Down Resistor	$R_{EN}$	$V_{PWM} = 5\text{ V}$	60	100	140	k $\Omega$
APWM Input Pull-Down Resistor	$R_{APWM}$	$V_{PWM} = V_{IH}$	60	100	140	k $\Omega$
<b>APWM</b>						
APWM Frequency [2]	$f_{APWM}$		• 40	–	1000	kHz
<b>OUTPUT LOGIC LEVELS (CLKOUT)</b>						
Output Logic Level Low	$V_{OL}$	$5\text{ V} < V_{IN} < 40\text{ V}$	• –	–	0.3	V
Output Logic Level High	$V_{OH}$	$5\text{ V} < V_{IN} < 40\text{ V}$	• 1.8	–	–	V
<b>ERROR AMPLIFIER</b>						
Source Current	$I_{EA(source)}$	$V_{COMP} = 1.5\text{ V}$	–	–600	–	$\mu\text{A}$
Sink Current	$I_{EA(sink)}$	$V_{COMP} = 1.5\text{ V}$	–	+600	–	$\mu\text{A}$
COMP Pin Pull-Down Resistance	$R_{COMP}$	$FAULT = 0$ , $V_{COMP} = 1.5\text{ V}$	–	1.4	–	k $\Omega$
<b>OVERVOLTAGE PROTECTION</b>						
OVP Pin Voltage Threshold	$V_{OVP(th)}$	OVP pin connected to $V_{OUT}$	• 7	8.3	9.5	V
OVP Pin Sense Current Threshold	$I_{OVP(th)}$	Current into OVP pin	• 190	200	210	$\mu\text{A}$
OVP Pin Leakage Current	$I_{OVP(LKG)}$	$V_{IN} = 16\text{ V}$ , $PWM = L$	• –	0.1	1	$\mu\text{A}$
OVP Accuracy			–	–	5	%
Undervoltage Protection Threshold	$V_{UVP(th)}$	Measured at $V_{OUT}$ pin when $R_{OVP} = 160\text{ k}\Omega$ [2]	–	3	–	V
		Measured at $V_{OUT}$ pin when $R_{OVP} = 0$	–	0.55	0.7	V
Secondary Overvoltage Protection	$V_{OVP(sec)}$	Measured at SW pin	• 42	45	48	V

Continued on the next page...

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.

[3] Minimum  $V_{IN} = 4.5\text{ V}$  is only required at startup. After startup is completed, IC can continue to operate down to  $V_{IN} = 3.9\text{ V}$

[4] LED current is trimmed to cancel variations in both Gain and ISET voltage

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
BOOST SWITCH							
Switch On-Resistance	R <sub>SW</sub>	I <sub>SW</sub> = 0.75 A, V <sub>IN</sub> = 16 V	●	100	250	500	mΩ
Switch Leakage Current	I <sub>SW(LKG)</sub>	V <sub>SW</sub> = 16 V, V <sub>PWM</sub> = V <sub>IL</sub>	●	–	0.1	1	μA
Switch Current Limit	I <sub>SW(LIM)</sub>		●	3	3.65	4.5	A
Secondary Switch Current Limit [2]	I <sub>SW(LIM2)</sub>	Higher than max I <sub>SW(LIM)</sub> under all conditions part latches when detected		–	4.9	–	A
Minimum Switch On-Time	t <sub>SW(on)</sub>		●	45	65	85	ns
Minimum Switch Off-Time	t <sub>SW(off)</sub>		●	–	65	85	ns
OSCILLATOR FREQUENCY							
Oscillator Frequency [5]	f <sub>SW</sub>	R <sub>FSET</sub> = 10 kΩ	●	1.95	2.15	2.35	MHz
		R <sub>FSET</sub> = 21.5 kΩ	●	0.9	1	1.1	MHz
		R <sub>FSET</sub> = 110 kΩ		–	200	–	kHz
Oscillator Frequency Dithering Range	f <sub>SW_DITH</sub>	R <sub>FSET</sub> = 10 kΩ		–	±5	–	%
Dithering Modulation Frequency	f <sub>SW_MOD</sub>	R <sub>FSET</sub> = 10 kΩ		–	12.5	–	kHz
FSET Pin Voltage	V <sub>FSET</sub>	A8519, R <sub>FSET</sub> = 10 kΩ		–	1.02	–	V
		A8519-1, R <sub>FSET</sub> = 10 kΩ		–	1.07	–	V
SYNCHRONIZATION							
Sync Input Logic Level	V <sub>SYNCL</sub>	FSET pin logic Low	●	–	–	0.4	V
	V <sub>SYNCH</sub>	FSET pin logic High	●	2	–	–	V
Synchronized Switching Frequency	f <sub>SW(sync)</sub>		●	320	–	2300	kHz
Synchronization Input Min. Off-Time	t <sub>SYNC(off)</sub>		●	150	–	–	ns
Synchronization Input Min. On-Time	t <sub>SYNC(on)</sub>		●	150	–	–	ns
LED CURRENT SINKS							
LEDx Accuracy [4]	Err <sub>LED</sub>	R <sub>ISET</sub> = 8.33 kΩ	●	–	0.7	3	%
LEDx Matching	Δ <sub>LEDx</sub>	I <sub>ISET</sub> = 120 μA	●	–	0.8	2	%
LEDx Regulation Voltage	V <sub>LEDx</sub>	V <sub>LED1</sub> = V <sub>LED2</sub> = V <sub>LED3</sub> = V <sub>LED4</sub> , I <sub>ISET</sub> = 120 μA	●	750	850	975	mV
ISET to I <sub>LEDx</sub> Current Gain	A <sub>ISET</sub>	I <sub>ISET</sub> = 120 μA	●	696	710	727	A/A
ISET Pin Voltage	V <sub>ISET</sub>			0.987	1.017	1.047	V
Allowable ISET Current	I <sub>ISET</sub>		●	20	–	144	μA
V <sub>LEDx</sub> Short Detect	V <sub>LEDx(SC)</sub>	While LED sinks are in regulation; sensed from V <sub>LEDx</sub> to AGND	●	4.7	5.2	7.0	V
LED Startup Ramp Time [2]	t <sub>SS</sub>	Time duration before all LED channels come into regulation, or OVP is tripped		–	20	–	ms

Continued on the next page...

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[2] Ensured by design and characterization, not production tested.

[3] Minimum  $V_{IN} = 4.5\text{ V}$  is only required at startup. After startup is completed, IC can continue to operate down to  $V_{IN} = 3.9\text{ V}$

[4] LED current is trimmed to cancel variations in both Gain and ISET voltage

[5]  $f_{SW}$  measurements were taken with dithering function is disabled.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>PWM DIMMING</b>						
Maximum PWM Dimming Until Off-Time [2]	$t_{PWML}$	Measured while PWM = low, during dimming control and internal references are powered on (exceeding $t_{PWML}$ results in shutdown)	–	32750	–	$f_{sw}$ cycles
Minimum PWM On-Time	$t_{PWMH(min1)}$	First cycle when powering up IC ( $V_{PWM} = 0$ to $3.3\text{ V}$ )	•	–	0.75	$\mu\text{s}$
	$t_{PWMH(min)}$	Subsequent PWM pulses	•	–	0.5	$\mu\text{s}$
PWM High to LED On Delay	$t_{d(PWMon)}$	Time between PWM going high and when LED current reaches 90% of maximum ( $V_{PWM} = 0$ to $3.3\text{ V}$ )	•	–	0.2	$\mu\text{s}$
PWM Low to LED Off Delay	$t_{d(PWMOff)}$	Time between PWM going low and when LED current reaches 10% of maximum ( $V_{PWM} = 3.3$ to $0\text{ V}$ )	•	–	0.36	$\mu\text{s}$
<b>HYSTERESIS CONTROL</b>						
Hysteresis Window (A8519)	$V_{HYST}$	Measured at VOUT pin when PWM = H to L	–	0.35	–	V
Hysteresis Window (A8519-1)	$V_{HYST1}$	Measured at VOUT pin when PWM = H to L	–	0.15	–	V
<b>GATE PIN</b>						
Gate Pin Sink Current	$I_{G(sink)}$	$V_{GATE} = V_{IN}$ , no input OCP fault	–	–113	–	$\mu\text{A}$
Gate Pin Source Current	$I_{G(source)}$	$V_{GATE} = V_{IN} - 6\text{ V}$ , input OCP fault tripped	–	6	–	mA
Gate Shutdown Delay When Overcurrent Fault Is Tripped [2]	$t_{FAULT}$	$V_{IN} - V_{SENSE} = 200\text{ mV}$ , monitored at FAULT pin	–	–	3	$\mu\text{s}$
Gate Voltage	$V_{GATE}$	Measured between GATE and VIN when gate is on	–	–6.7	–	V
<b>VSENSE PIN</b>						
VSENSE Pin Sink Current	$I_{VSENSE}$		•	17.2	21.5	$\mu\text{A}$
VSENSE Trip Point	$V_{SENSE(trip)}$	Measured between VIN and VSENSE, $R_{adj} = 0$	•	95	110	mV
<b>FAULT PIN</b>						
FAULT Pull-Down Voltage	$V_{FAULT}$	$I_{FAULT} = 1\text{ mA}$	–	–	0.5	V
FAULT Pin Leakage Current	$I_{FAULT(1kg)}$	$V_{FAULT} = 5\text{ V}$	–	–	1	$\mu\text{A}$
<b>THERMAL PROTECTION (TSD)</b>						
Thermal Shutdown Threshold [2]	$T_{SD}$	Temperature rising	155	170	–	$^\circ\text{C}$
Thermal Shutdown Hysteresis [2]	$T_{SD(hys)}$		–	20	–	$^\circ\text{C}$

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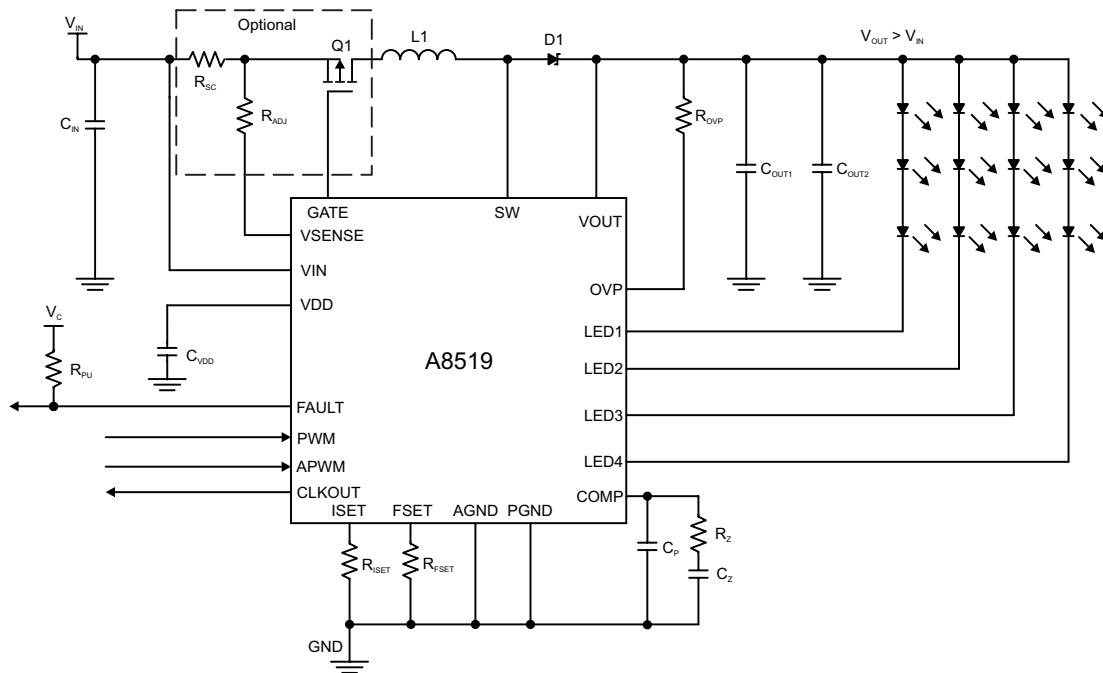
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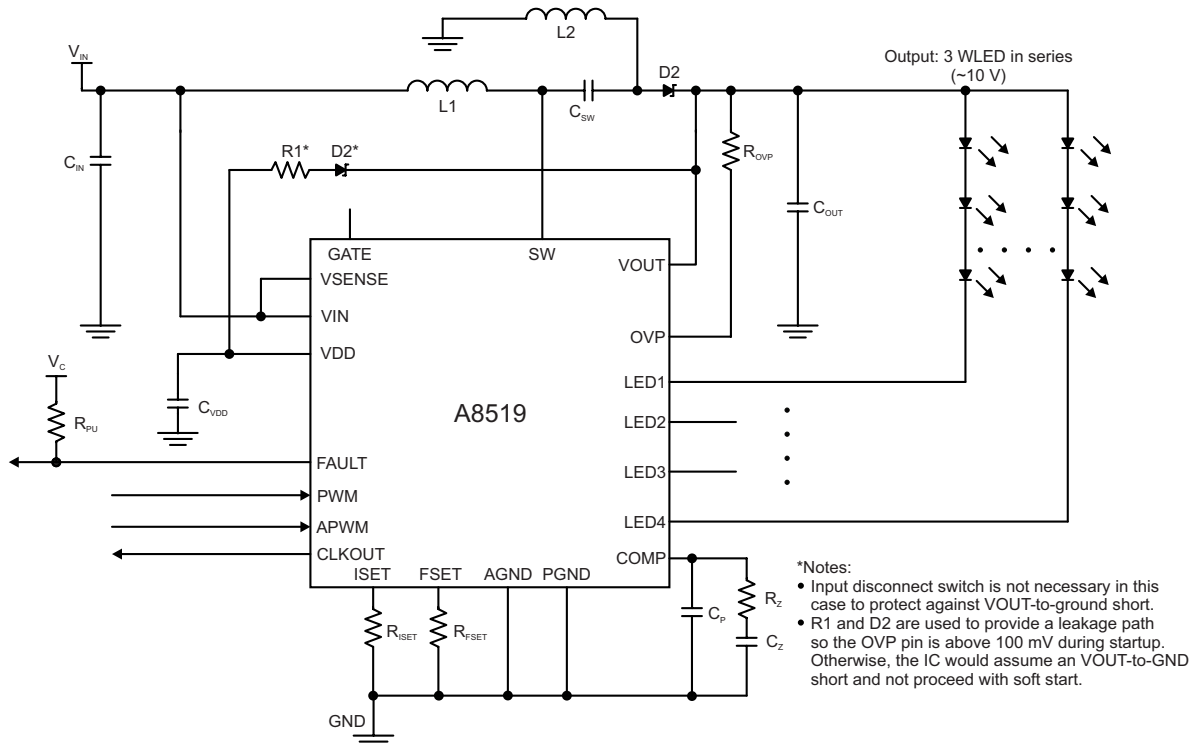
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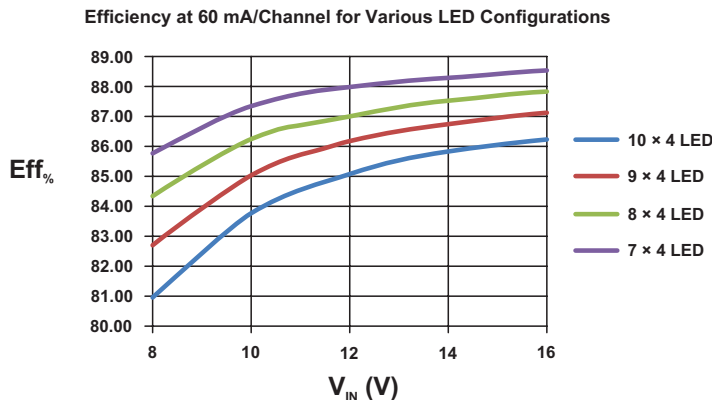
Typical Application Showing Boost Configuration with Input Disconnect Switch to Protect Against VOUT-to-Ground Short



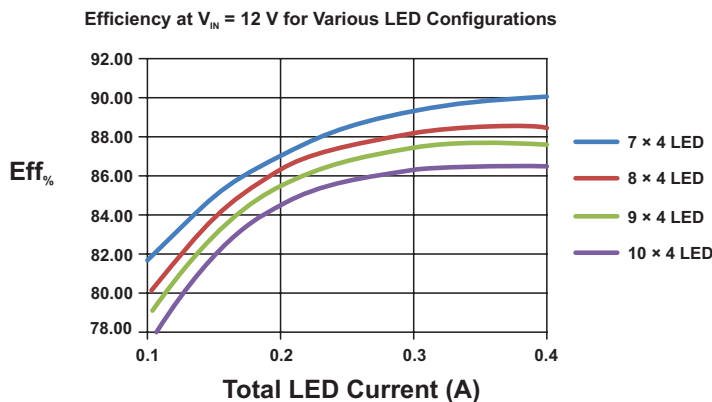
Typical Application Showing SEPIC Configuration for Flexible Input/Output Voltage Ratio

### CHARACTERISTIC PERFORMANCE

#### Efficiency Measurement



A8519 Evaluation Board Efficiency versus Input Voltage while Disconnect Switch and Snubber Circuit are Used

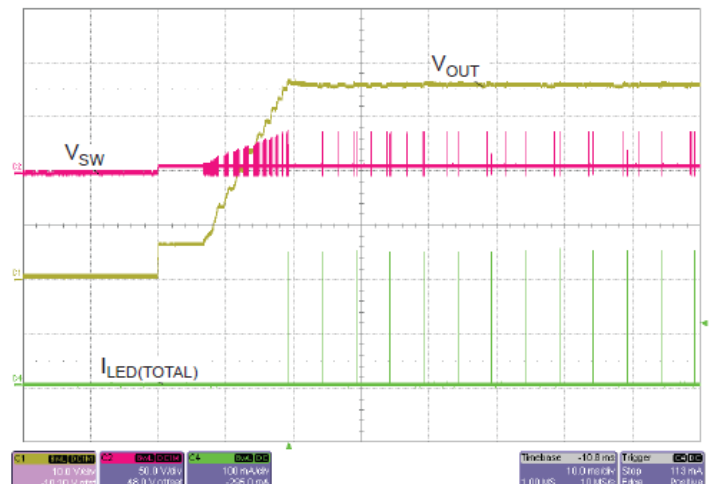
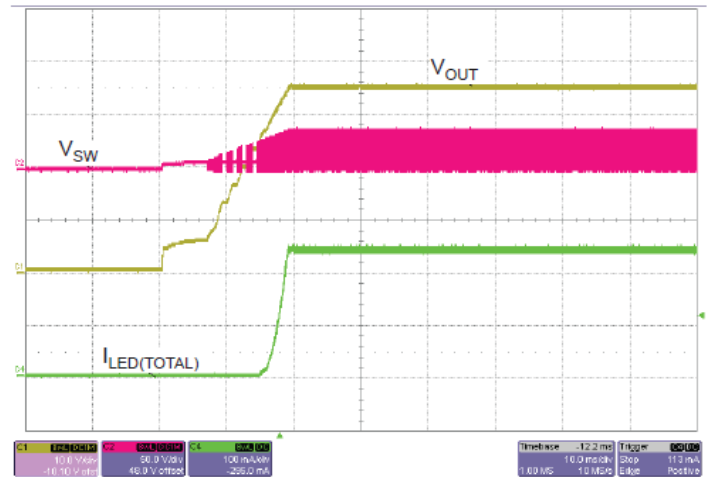


A8519 Evaluation Board Efficiency versus Total LED Current while Disconnect Switch and Snubber Circuit are Used

Higher efficiency can be achieved by:

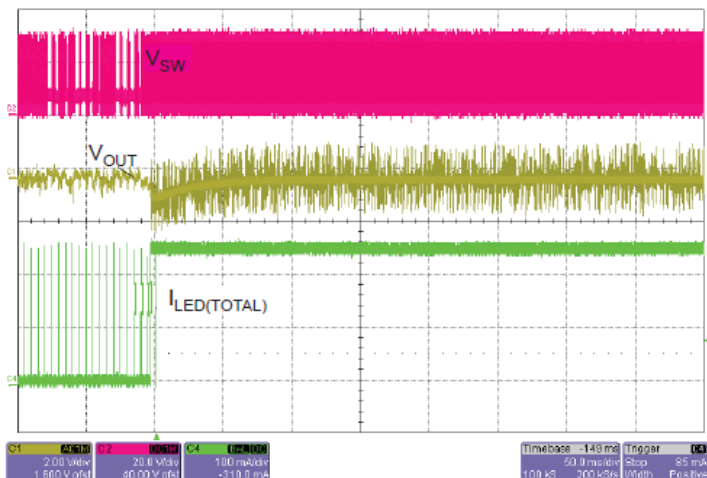
- Using an inductor with low DCR.
- Using lower forward voltage drop and smaller junction capacitance Schottky diode.
- Removing the snubber circuit; however, this might compromise the EMI performance.
- Shorting out the disconnect switch and the input current sense resistor; however, this will eliminate the output short-to-GND protection feature.
- Lowering switching frequency. This will significantly improve the efficiency; however, to avoid the EMI AM band limits, careful switching frequency selection is required. In addition, a larger inductor will be needed.

#### Startup Waveforms



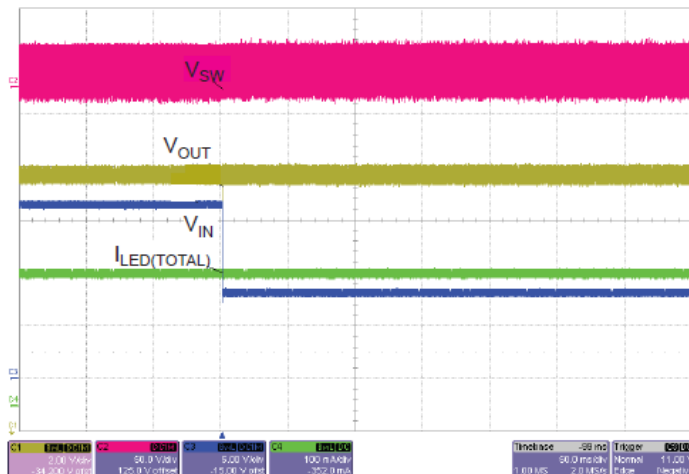
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### Transient Response to Step Change in PWM Dimming

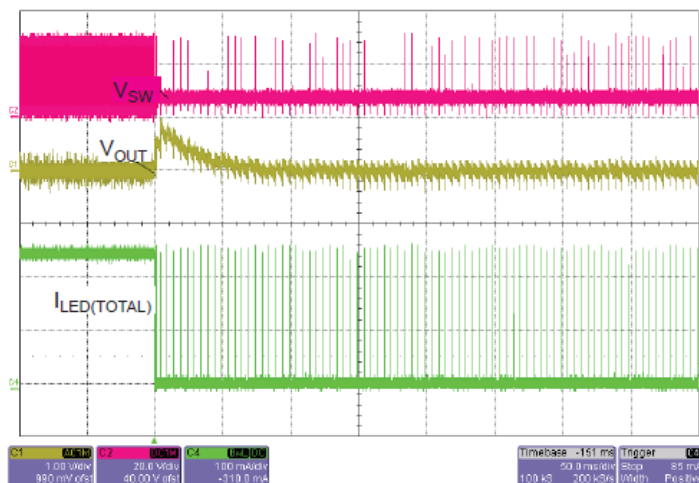


From PWM = 0.1% to PWM = 100% at 4 Channels,  
60 mA/Channel,  $V_{IN} = 12\text{ V}$ ; Time base = 50 ms/Div

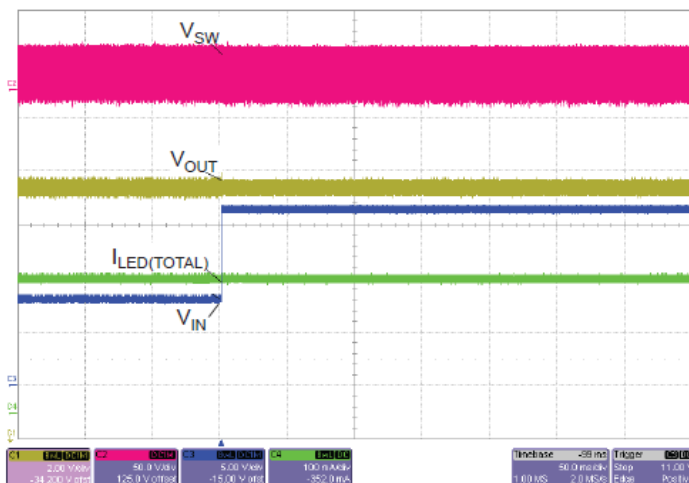
### Transient Response to Step Change in $V_{IN}$ Voltage



From  $V_{IN} = 16\text{ V}$  to  $V_{IN} = 5.5\text{ V}$ , 4 Channels, 60 mA/Channel,  
PWM = 100%; Time base = 50 ms/Div



From PWM = 100% to PWM = 0.1% at 4 Channels,  
60 mA/Channel,  $V_{IN} = 12\text{ V}$ ; Time base = 50 ms/Div



From  $V_{IN} = 5.5\text{ V}$  to  $V_{IN} = 16\text{ V}$ , 4 Channels, 60 mA/Channel,  
PWM = 100%; Time base = 50 ms/Div

FUNCTIONAL DESCRIPTION

Enabling the IC

The IC turns on when a logic high signal is applied on the PWM pin with a minimum duration of  $t_{pPWMH}$  for the first clock cycle, and the input voltage present on the VIN pin is greater than 4.35 V to clear the UVLO threshold. Before the LEDs are enabled, the A8519 driver goes through a system check to see if there are any possible fault conditions that might prevent the system from functioning correctly. Also if the FSET pin is pulled low the IC will not power up. More information on the FSET pin can be found in the Synchronization section of the datasheet.

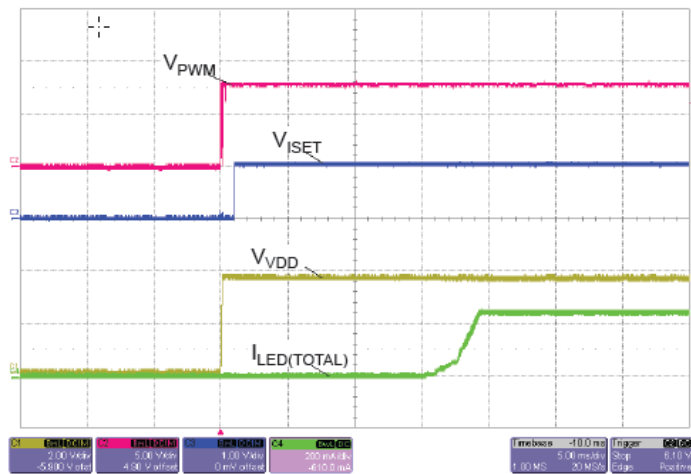


Figure 1: Power Up Diagram Showing PWM, ISET, and VDD Voltages and Total LED Current

Once the IC is enabled, there are only two ways to shut down the IC into low-power mode:

- 1. Pull PWM pin to low for at least 32,750 clock cycles (approximately 16 ms at 2 MHz).
- 2. Cut off the supply and allow VIN to drop below UVLO falling threshold (less than 3.9 V).

Powering Up: LED Pin Check

Once VIN pin goes above UVLO and a high signal is present on the PWM pin, the IC proceeds to power up. The A8519 then enables the disconnect switch (GATE) and checks to see if the LED pins are shorted to ground and/or are not used. The LED detect phase starts when the GATE voltage of the disconnect switch is equal to  $V_{IN} - 3.3\text{ V}$ .

Figure 2 shows the relation of LEDx pins with respect to the gate voltage of the disconnect switch (if used) during LED detect phase, as well as the duration of the LED detect for a switching frequency of 2 MHz.

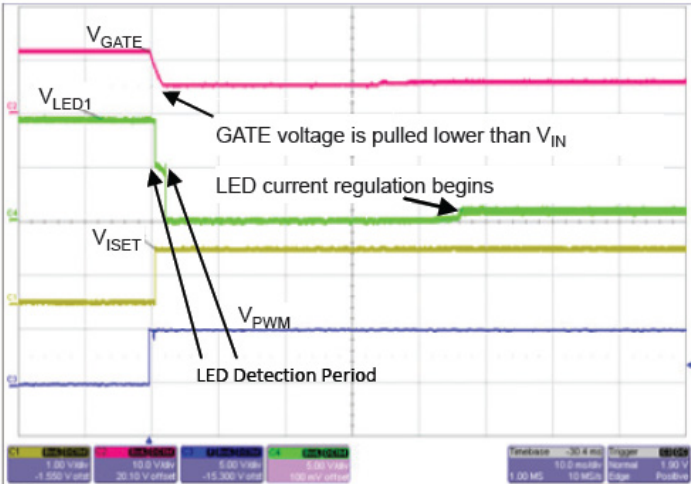


Figure 2: Power Up Diagram Showing Disconnect  $V_{GATE}$ ,  $V_{LED1}$ ,  $V_{ISET}$ , and  $V_{PWM}$  During LED Pins Detect and Regulation Period

When the voltage threshold on VLEDx pins exceeds 120 mV, a delay between 3000 and 4000 clock cycles (1.5 to 2 ms) is used to determine the status of the pins.

Table 1: LED Detection Duration for Given Switching Frequency

Switching Frequency	Detection Time
2 MHz	1.5 to 2 ms
1 MHz	3 to 4 ms
800 kHz	3.75 to 5 ms
600 kHz	5 to 6.7 ms

All unused LED pins should be connected with a 3.09 kΩ resistor to GND. The unused pin, with the pull-down resistor, will be taken out of regulation at this point and will not contribute to the boost regulation loop.

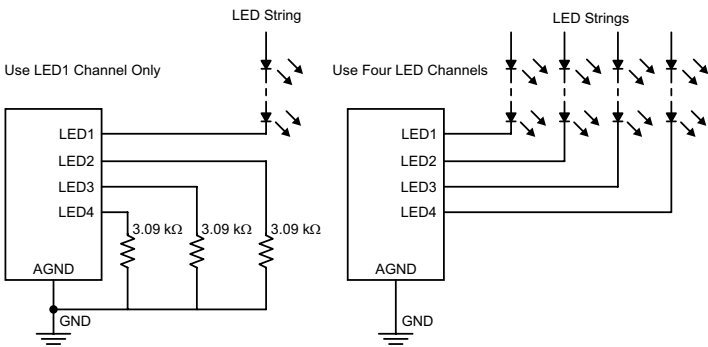


Figure 3: Channel Select Setup

Table 2: LED Detection Voltage Thresholds

LED Pin Voltage Level	LED Pin	Action
Less than 70 mV	Indicates a short to PCB GND	A8519 will not proceed with power up.
150 mV	Not used	LED string connected with the unused LED pin is removed from operation
325 mV	LED pin in use	None

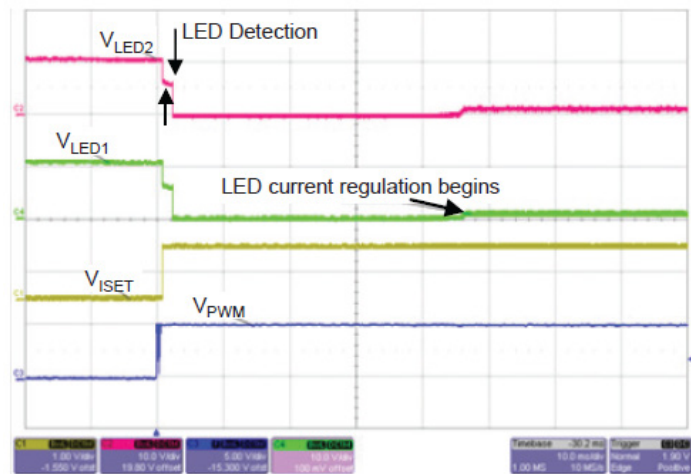


Figure 4: LED String Detect Occurs when All LED Strings are Selected to be Used

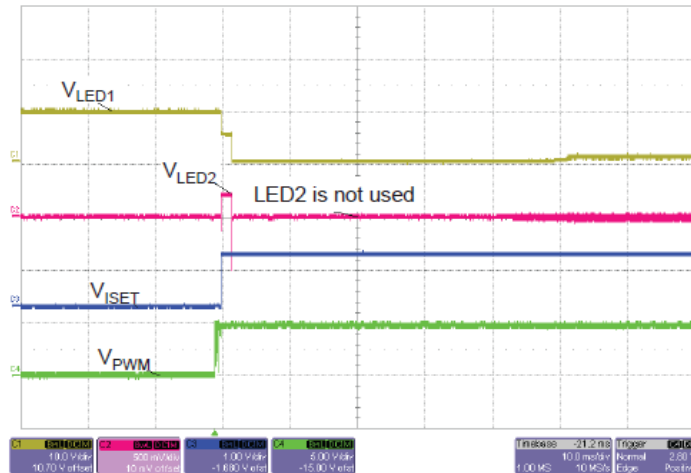


Figure 5: Detect Voltage is about 150 mV when LED Pin 2 is not Used

If an LED pin is shorted to ground, the A8519 will not proceed with soft-start until the short is removed from the LED pin. This prevents the A8519 from powering up and putting an uncontrolled amount of current through the LEDs.

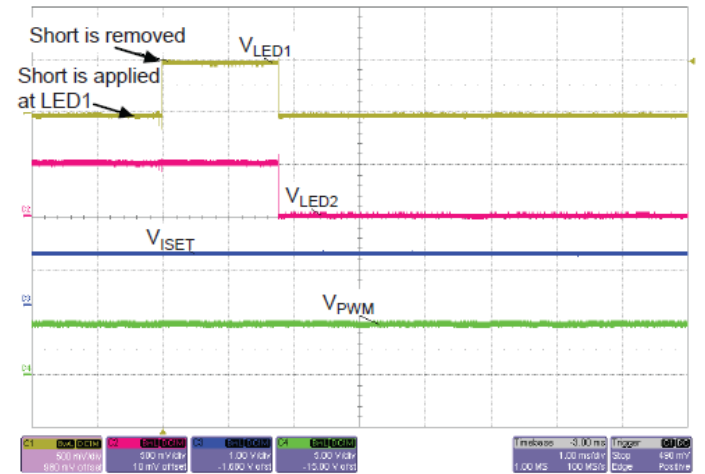


Figure 6: One LED Pin is Shorted to GND. The IC will not proceed with power up until LED pin is released, at which point the LED pin is checked to see if it is used.

Powering Up: Boost Output Undervoltage Protection

During startup, after the input disconnect switch has been enabled, the output voltage is checked through the OVP pin. If the sensed voltage does not rise above  $V_{UVP(th)}$ , the output is assumed to be at fault and the IC will not proceed with soft-start.

Undervoltage protection may be caused by one of the following faults:

- Output capacitor shorted to GND
- Boost inductor or diode open
- OVP sense resistor open

After an Output UVP fault has been detected, the A8519 immediately shuts down but does not latch off. It will retry as soon as the UVP fault is removed.

In case of output capacitor shorted to GND fault, however, the high inrush current will also trip the Input OCP fault. This causes the IC to shut down and latch off. To enable the IC again, the PWM pin must be pulled low for at least 32,750 clock cycles (about 16 ms at 2 MHz), then pulled high again.

### Soft-Start Function

During startup, the A8519 ramps up its boost output voltage following a fixed ramp function. This technique limits the input inrush current and ensures the same startup time regardless of the PWM duty cycle.

The soft-start process is completed when any one of the following conditions is met:

1. All LED currents have reached their regulation targets,
2. Output voltage has reached 93% of its OVP threshold, or
3. Soft-start ramp time ( $t_{SS}$ ) has expired.

### Frequency Selection

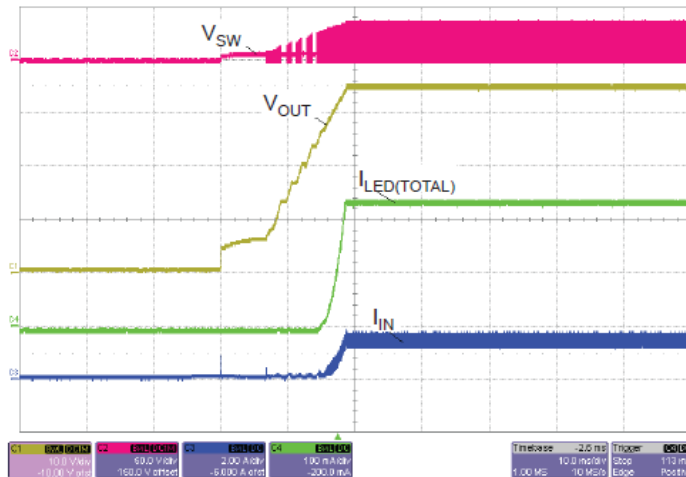


Figure 7: Startup Diagram Showing the Input Current, Output Voltage, Total LED Current, and Switch Node Voltage

The switching frequency on the boost regulator is set by a single resistor connected to the FSET pin. The switching frequency can be anywhere from 200 kHz to 2.15 MHz. Figure 8 shows typical switching frequency in MHz for a given resistor value (in kΩ). The following equation can also be used to determine typical switching frequency from FSET resistance:

$$f_{SW} = 21.4/R_{FSET} + 0.008$$

where  $f_{SW}$  is in MHz,  $R_{FSET}$  is in kΩ.

If a fault occurs during operation that will increase the switching frequency, the FSET pin is clamped to a maximum switching frequency of no more than 3.5 MHz. If the FSET pin is shorted to GND, the part will shut down. For more details, see the Fault Mode table on page 25.

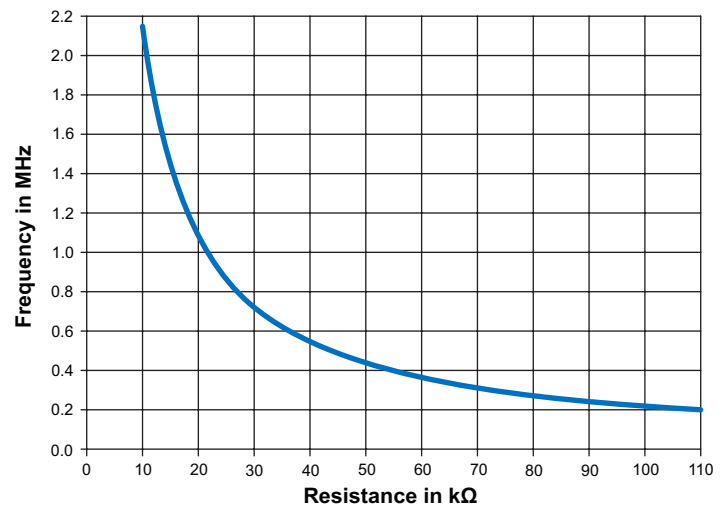


Figure 8: Switching Frequency versus  $R_{FSET}$  Resistor

### Synchronization

The A8519 can also be synchronized using an external clock. At power-up, if the FSET pin is held low, the IC will not power-up. Only when the FSET pin is tri-stated to allow for the pin to rise to about 1 V, or when a sync clock is detected, the A8519 will try to power up. The basic requirement of the sync signal is 150 ns minimum on-time and 150 ns minimum off-time as dictated by the requirements of pulse-width on- and off-times.

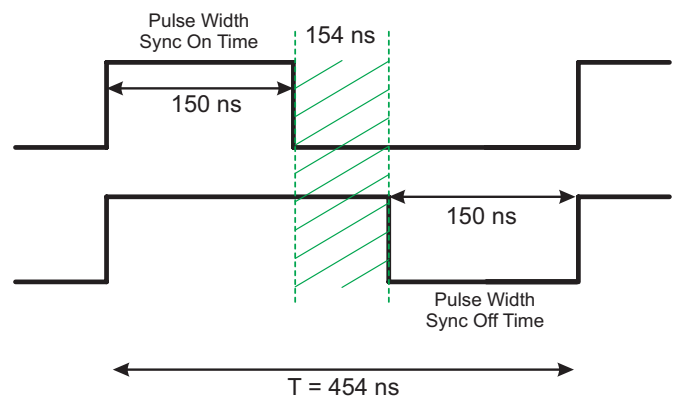


Figure 9: Sync Pulse On- and Off-Time Requirements

Figure 9 shows timing for a synchronization clock into the A8519 at 2.2 MHz.

Any pulse with a duty cycle of 33% to 66% at 2.2 MHz can be used to synchronize the IC. Table 3 summarizes the duty cycle range at various synchronization frequencies.

Table 3: Sync Pulse Duty Cycle Range for Selected Switching Frequencies.

Sync Pulse Frequency	Duty Cycle Range
2.2 MHz	33% to 66%
2 MHz	30% to 70%
1 MHz	15% to 85%
600 kHz	9% to 91%
300 kHz	4.5% to 95.5%

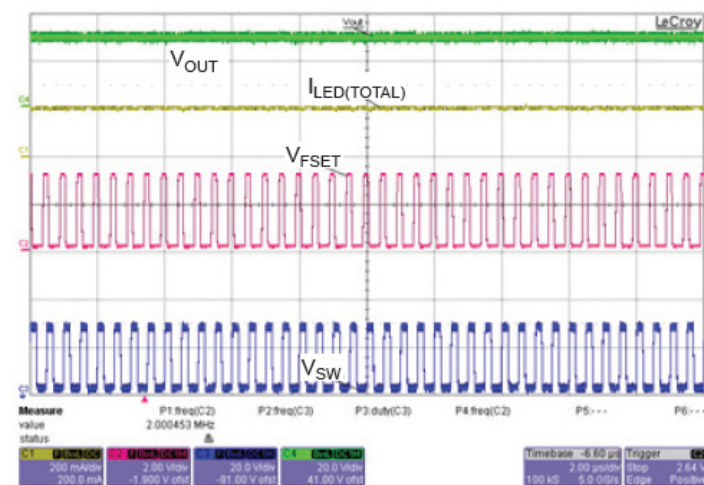


Figure 10: Synchronized FSET Pin and Switch Node SW Voltage.

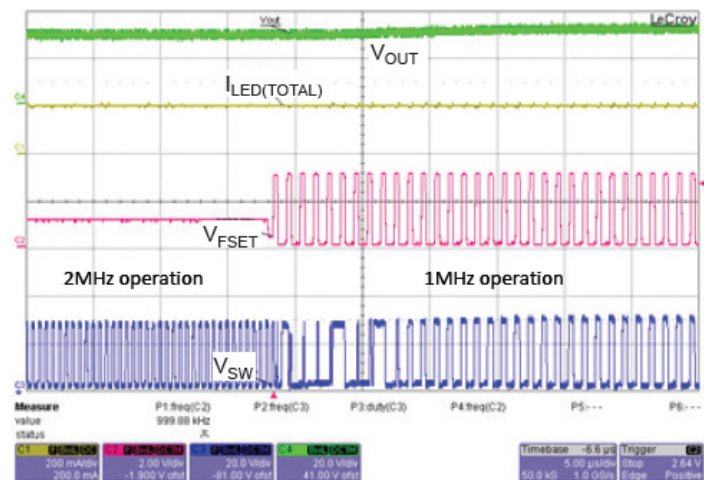


Figure 11: Transition of the Switch Wave Form when the Sync Pulse is Detected. The A8519 is switching at 2 MHz, and the applied sync pulse is 1 MHz. The LED current does not show any variation while the frequency changeover occurs.

Suppose the A8519 is started up with a valid external SYNC signal, but the SYNC signal is lost during normal operation. In that case, one of the following happens:

- If the external SYNC signal is high impedance (open), the A8519 continues normal operation after approximately 5 µs, at the switching frequency set by  $R_{FSET}$ . No FAULT flag is generated.
- If the external SYNC signal is stuck low (shorted to ground), the A8519 will detect an FSET-short-to-GND fault. The FAULT pin is pulled low after approximately 10 µs, and switching is disabled. Once the FSET pin is released or SYNC signal is detected again, the A8519 will proceed to soft-start.

To prevent generating a fault when the external SYNC signal is stuck at low, the circuit shown in Figure 12 can be used. When the external SYNC signal goes low, the A8519 will continue to operate normally at the switching frequency set by the  $R_{FSET}$ . No FAULT flag is generated.

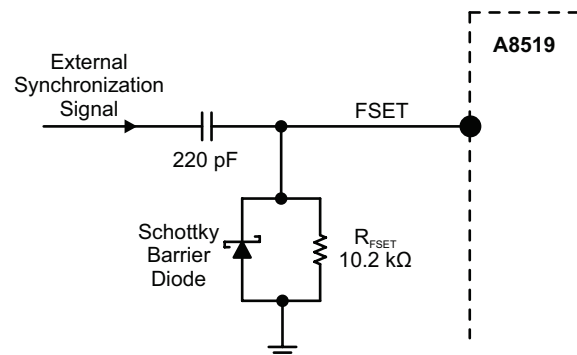
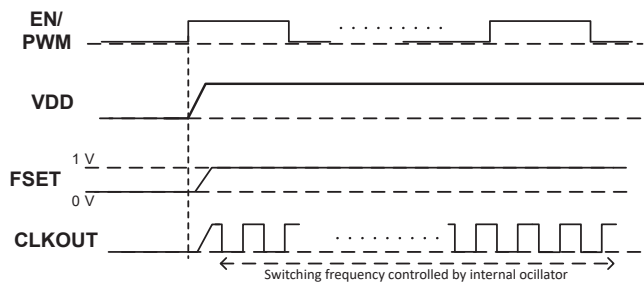


Figure 12: Countermeasure to Prevent External Sync Signal Stuck-at-Low Fault.

The following timing diagrams (not to scale) illustrate how the switching frequency of A8519 may be programmed.

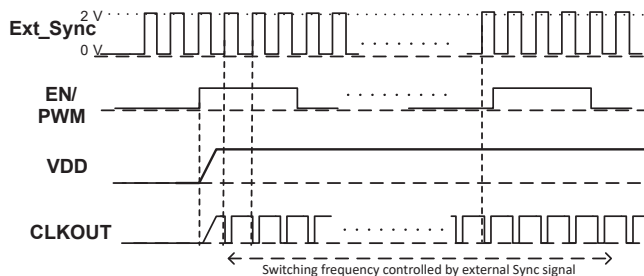
### Case 1: Startup with internal oscillator (RFSET connected to FSET pin)



#### Remarks:

- After the IC powers up, CLKOUT signal is generated by internal oscillator based on FSET pin current.
- Duty cycle of CLKOUT is approximately 50%.
- When boost switching is enable, it has the same frequency as CLKOUT but different duty cycle.

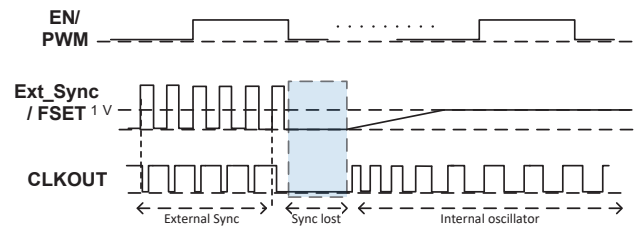
### Case 2: Startup with External Sync clock signal applied to FSET pin



#### Remarks:

- Ext\_Sync clock signal should be applied before EN/PWM pin goes High.
- After the IC powers up, CLKOUT signal is controlled by Ext\_Sync.
- CLKOUT generates a fixed negative pulse of 200 ns following each rising edge of Ext\_Sync. Its duty cycle varies with external frequency.

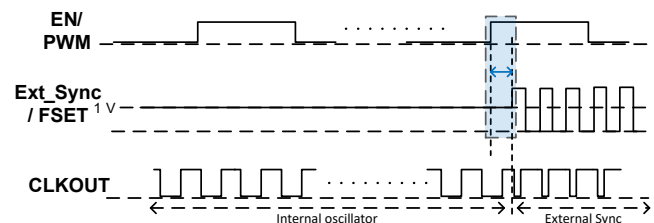
### Case 3: Operating with External Sync initially, then switches over to internal oscillator



#### Remarks:

- If the next rising edge of Ext\_Sync failed to arrive within approximately 5  $\mu$ s, the IC switches over to internal oscillator mode.
- This transition could happen during fault condition when Ext\_Sync line is broken. It is not recommended as part of the normal operation.
- DC-blocking capacitor is required (see Figure 12) to prevent Stuck-at-Low fault at FSET pin.

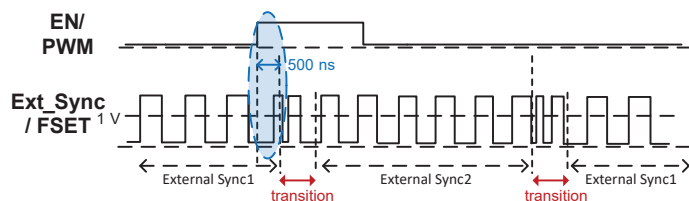
### Case 4: Operating with internal oscillator initially, then switches over to External Sync



#### Remarks:

- This transition could happen during fault condition when Ext\_Sync line is intermittent. It is not recommended as part of the normal operation.
- DC-blocking capacitor is required (see Figure 12) to prevent Stuck-at-Low fault at FSET pin.
- Make sure the first Ext\_Sync rising edge and the PWM rising edge do not coincide within a 500 ns window.

### Case 5: Operating with Ext\_Sync1 initially, then switches over to Ext\_Sync2



#### Remarks:

- Irregular clock pulses may occur during transition between two external sync frequencies.
- Ensure the transition takes place at least 500 ns after the previous PWM = H rising edge.
- Alternatively, execute the switchover during PWM = L only.

A8519 and  
A8519-1

Wide Input Voltage Range, High-Efficiency, Fault-Tolerant LED Driver

LED Current Setting and LED Dimming

The maximum LED current can be up to 100 mA per channel, and is set through the ISET pin. Connect a resistor, R<sub>ISET</sub>, between this pin and GND. To set I<sub>LED</sub> calculate R<sub>ISET</sub> as follows:

$$I_{LED} = I_{SET} \times A_{ISET}$$
$$I_{SET} = \frac{V_{ISET}}{R_{ISET}}$$
$$R_{ISET} = \frac{(V_{ISET} \times A_{ISET})}{I_{LED}}$$

where I<sub>LED</sub> current is in A and R<sub>ISET</sub> is in Ω.

This sets the maximum current through the LEDs, referred to as the 100% current.

Table 4: LED Current Setting Resistors (Values Rounded to the Nearest Standard Resistor Value)

Standard Closest R <sub>ISET</sub> Resistor Values	LED Current I <sub>LED</sub>
7.15 kΩ	100 mA per LED
8.87 kΩ	80 mA per LED
11.8 kΩ	60 mA per LED
14.3 kΩ	50 mA per LED
17.8 kΩ	40 mA per LED

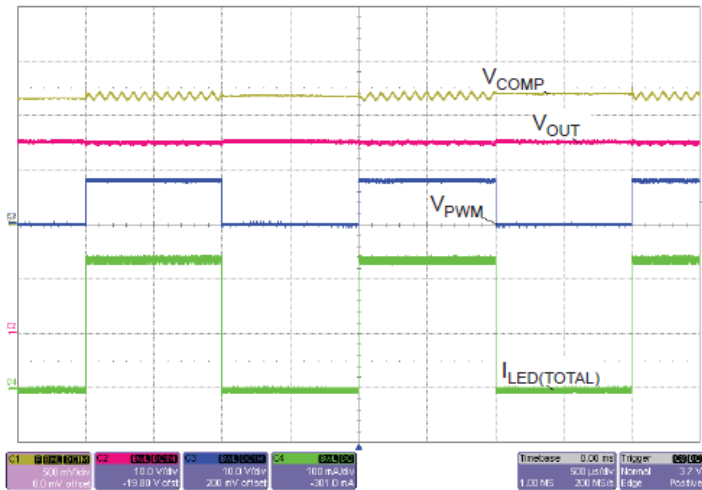


Figure 13: Typical PWM Diagram Showing V<sub>OUT</sub>, I<sub>LED</sub> and COMP Pin, as well as the PWM Signal. (PWM dimming Frequency is 500 Hz 50% duty cyle.)

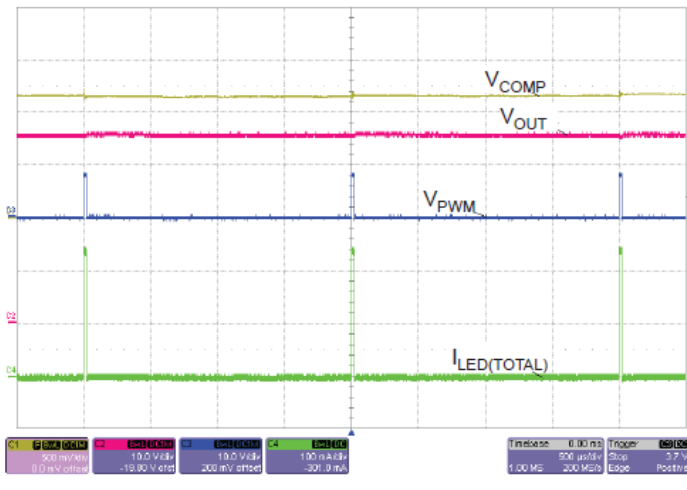


Figure 14: Typical PWM Diagram Showing V<sub>OUT</sub>, I<sub>LED</sub>, and COMP Pin, as well as the PWM Signal. (PWM dimming frequency is 500 Hz 1% duty cycle.)

### PWM Dimming

The LED current can be reduced from the 100% current level by PWM dimming using the PWM pin. When the PWM pin is pulled high, the A8519 turns on and all enabled LEDs sink 100% current. When PWM is pulled low, the boost converter and LED sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active. The typical PWM dimming frequencies fall between 200 Hz and 1 kHz.

The A8519 is designed to deliver a maximum dimming ratio of 10,000:1 at PWM frequency of 100 Hz. That means a minimum PWM duty cycle of 0.01%, or an on-time of just 1  $\mu$ s out of a period of 10 ms.

High-PWM dimming ratio is achieved by regulating the output voltage during PWM off-time. The VOUT pin samples the output

voltage during PWM on-time and regulates it during off-time. A hysteresis control loop brings VOUT higher by approximately 350 mV (150 mV for A8519-1) whenever it drops below the target voltage. In a highly noisy switching environment, it is necessary to insert an RC filter at the VOUT pin. A typical value of  $R = 10 \text{ k}\Omega$  and  $C = 47 \text{ pF}$  is recommended.

Another important feature of the A8519 is the PWM signal to LED current delay. This delay is typically less than 500 ns, which allows for greater LED current accuracy at low-PWM dimming duty cycles.

The error introduced by LED turn-on delay is partially offset by LED turn-off delay. Therefore, a PWM pulse width of under 1  $\mu$ s is still feasible, but the percentage error of LED current will increase with narrower pulse width.

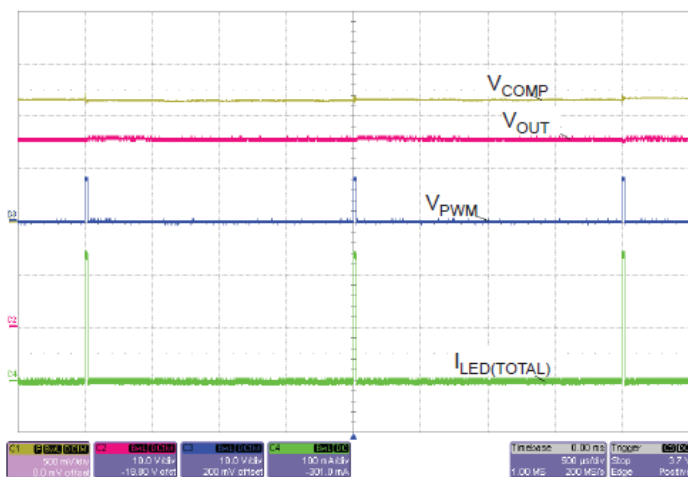


Figure 15: Rising Edge PWM Signal to Total LED Current  
 $I_{LED(TOTAL)}$  Turn-On Delay; Time base = 100 ns

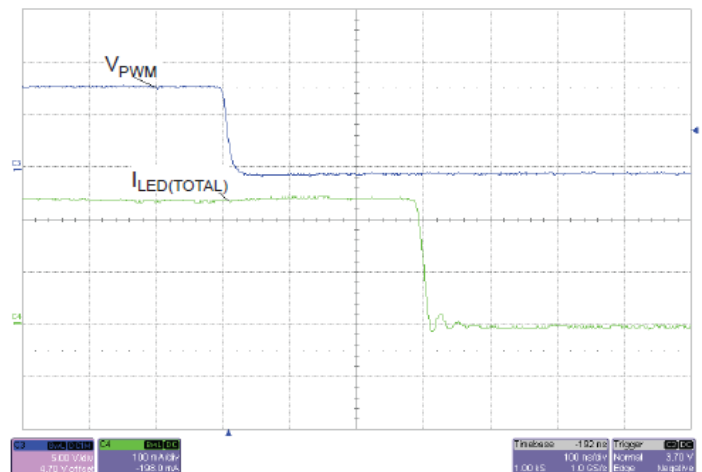


Figure 16: Falling Edge PWM Signal to Total LED Current  
 $I_{LED(TOTAL)}$  Turn-Off Delay; Time base = 100 ns

### APWM Pin

The APWM pin is used in conjunction with the ISET pin (see Figure 17). This is a digital signal pin that internally adjusts the  $I_{\text{ISET}}$  current. The typical input signal frequency is between 40 kHz and 1 MHz. The duty cycle of this signal is inversely proportional to the percentage of current that is delivered to the LED (see Figure 18). As an example, a system that delivers  $I_{\text{LED(TOTAL)}} = 240 \text{ mA}$  would deliver  $I_{\text{LED(TOTAL)}} = 180 \text{ mA}$  when an APWM signal with a duty cycle of 25% is applied. When this pin is not used it should be tied to AGND.

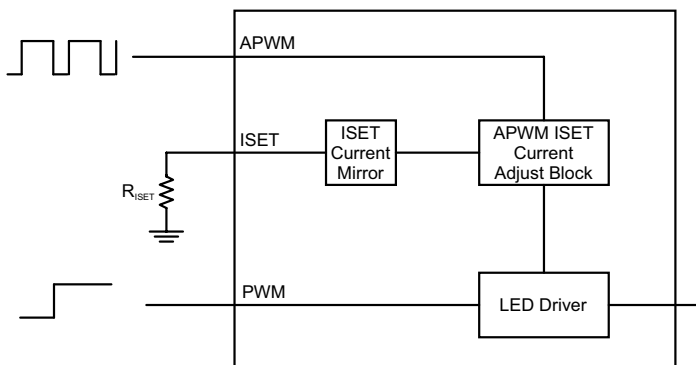


Figure 17: Simplified Block Diagram of APWM ISET Block

To use the APWM pin as a trim function, the user should set the maximum output current to a value higher than the desired current by at least 5%. The LED  $I_{\text{ISET}}$  current is then trimmed down to the appropriate desired value. Another consideration is the limitation of the APWM signal's duty cycle. In some cases, it might be more desirable to set the maximum  $I_{\text{ISET}}$  current to be 25% to 50% higher, thus allowing the APWM signal to have duty cycles that are between 25% and 50%.

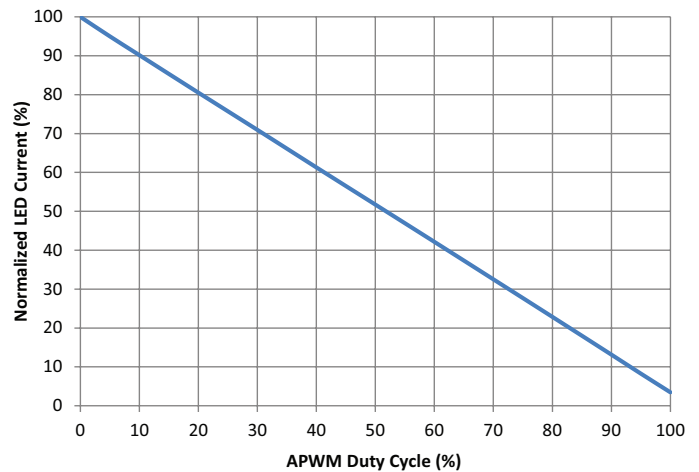


Figure 18: Normalized LED Current vs. APWM Duty Cycle  
 $V_{\text{IN}} = 9 \text{ V}$ ,  $V_{\text{OUT}} = \sim 22 \text{ V}$ ,  $R_{\text{ISET}} = 24 \text{ k}\Omega$ , APWM = 200 kHz

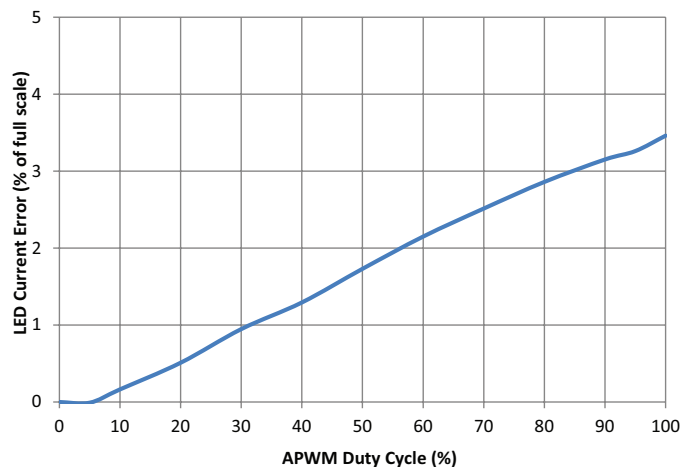


Figure 19: Error in LED Current vs. APWM Duty Cycle  
 $V_{\text{IN}} = 9 \text{ V}$ ,  $V_{\text{OUT}} = \sim 22 \text{ V}$ ,  $R_{\text{ISET}} = 24 \text{ k}\Omega$ , APWM = 200 kHz

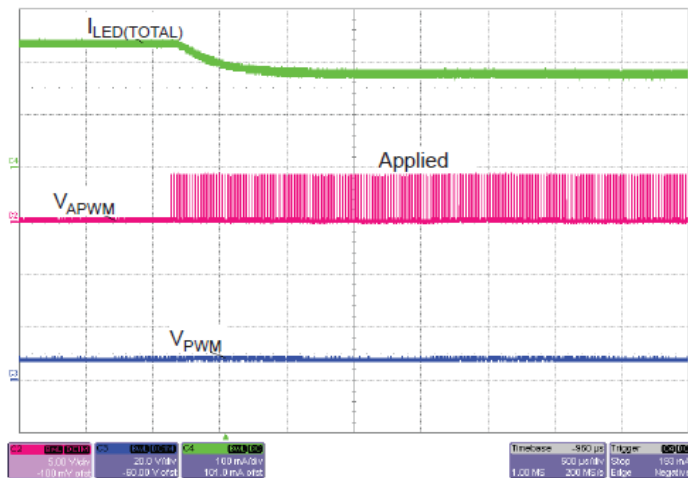


Figure 20: Transition of Total LED Current from 240 mA to 180 mA, when a 25% APWM signal is applied to the APWM pin. (Dimming PWM = 100%)

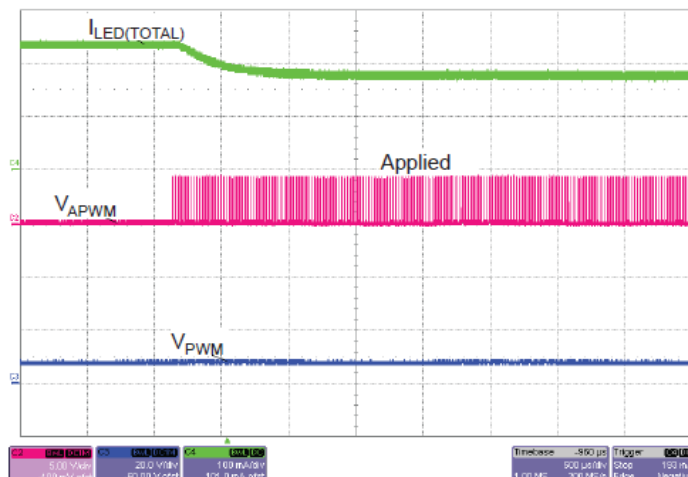


Figure 21: Transition of Total LED Current from 180 mA to 240 mA, when a 25% APWM stops being applied to the APWM pin. (Dimming PWM = 100%)

Although the APWM dimming function has a wide frequency range, if used strictly as an analog dimming function, it is recommended to use frequency ranges between 50 and 500 kHz for best accuracy. The frequency range needs to be considered only if the user is not using APWM as a closed-loop trim function. It takes about 1 millisecond to change the actual LED current due to propagation delay between the APWM signal and the  $I_{LED(TOTAL)}$ .

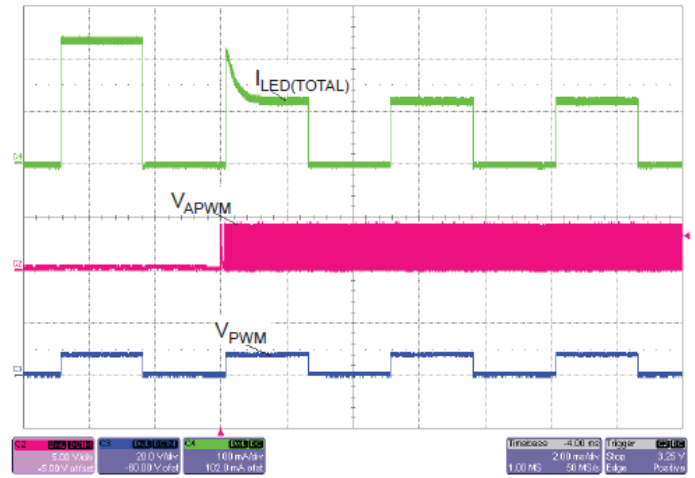


Figure 22: Transition of output current level when a 50% duty cycle APWM signal is applied to the APWM pin, in conjunction with 50% duty cycle applied to the PWM pin.

### Extending LED Dimming Ratio

The dynamic range of LED brightness can be further extended by using a combination of PWM duty cycle, APWM duty cycle, and analog dimming method.

For example, the following approach can be used to achieve a 50,000:1 dimming ratio at 200 Hz PWM frequency:

- Vary PWM duty cycle from 100% down to 0.02% to give 5,000:1 dimming.
- With PWM duty cycle at 0.02%, vary APWM duty from 0% to 90% to reduce LED current down to 10%. This gives a net effect of 50,000:1 dimming.

### Analog Dimming

Besides using APWM signal, the LED current can also be reduced by using an external DAC or another voltage source. Connect  $R_{ISET}$  between the DAC output and the ISET pin. The limit of this type of dimming is dependent of the range of the ISET pin. In the case of the A8519, the limit is 20 to 144  $\mu A$ .

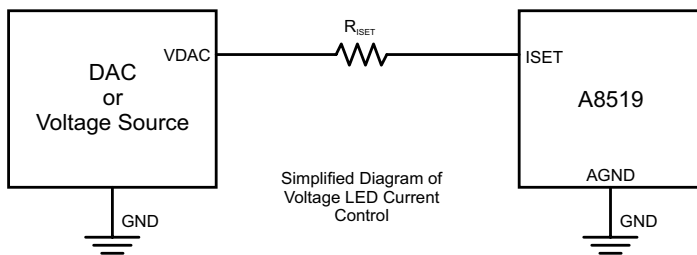


Figure 23: Typical Application Circuit Using a DAC to Control the LED Current in the A8519

The ISET current is controlled by the following formula:

$$I_{ISET} = \frac{V_{ISET} - V_{DAC}}{R_{ISET}}$$

where  $V_{ISET}$  is the ISET pin voltage and  $V_{DAC}$  is the DAC output voltage.

When the DAC voltage is 0 V, the LED current will be at its maximum. To keep the internal gain amplifier stable, do not decrease the current through the  $R_{ISET}$  resistor to less than 20  $\mu$ A.

Below is a typical application circuit using a DAC to control the LED current using a two-resistor configuration. The advantage of this circuit is that the DAC voltage can be higher or lower, thus adjusting the LED current to a higher or lower value of the preset LED current set by the  $R_{ISET}$  resistor.

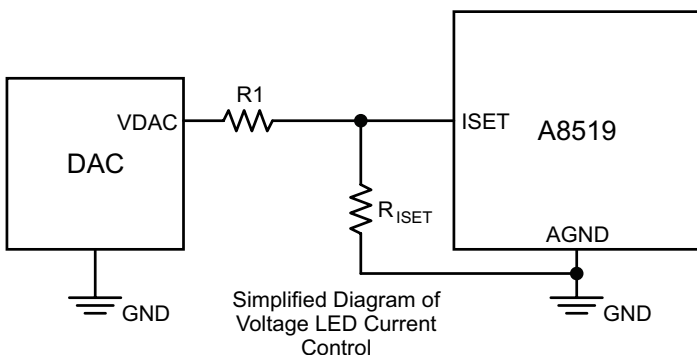


Figure 24: Typical Application Circuit Using a DAC and  $R_{ISET}$  Resistor to Control the LED Current in the A8519

The LED current can be adjusted using the following formula:

$$I_{ISET} = \frac{V_{ISET}}{R_{ISET}} - \left[ \frac{V_{DAC} - V_{ISET}}{RI} \right]$$

where  $V_{ISET}$  is the ISET pin voltage and  $V_{DAC}$  is the DAC output voltage.

When  $V_{DAC}$  is equal to 1 V, the output is strictly controlled by the  $R_{ISET}$  resistor. When  $V_{DAC}$  is higher than 1 V, the LED current is reduced. When  $V_{DAC}$  is lower than 1 V, the LED current is increased.

### LED String Short Detect

All LEDx pins are capable of handling the maximum  $V_{OUT}$  that the converter can deliver, thus allowing for LEDx pin to  $V_{OUT}$  protection in case of a connector short.

In case some of the LEDs in an LED string are shorted, the voltage at the corresponding LEDx pin will increase. Any LEDx pin that has a voltage exceeding  $V_{LEDx(SC)}$  will be removed from operation. This will prevent the IC from dissipating too much power by having a large voltage present on an LEDx pin.

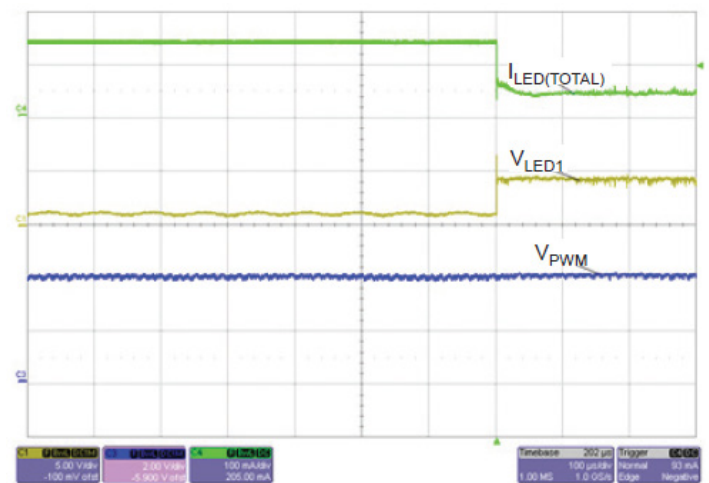


Figure 25: Disabling of LED1 String when the LED1 Pin Voltage is Increased Above 4.6 V

While the IC is being PWM dimmed, the IC will recheck the disabled LED every time the PWM signal goes high to prevent false tripping of LED short. This also allows for some self-correction if an intermittent LED pin short-to-VOUT is present.

At least one LED must be in regulation for the LED string short-detect protection to activate. In case all of the LED pins are above regulation voltage (this could happen when the input voltage rises too high for the LED strings), they will continue to operate normally.

### Overvoltage Protection

The A8519 has output overvoltage protection (OVP) and open Schottky diode protection (secondary OVP). The OVP pin has a threshold level of 8.3 V typical. A resistor can be used to set the output overvoltage protection threshold up to 40 V approximately. This is sufficient for driving 11 white LED in series.

The formula for calculating the OVP resistor is shown below:

$$R_{OVP} = \frac{(V_{OVP} - V_{OVP(th)})}{I_{OVP(th)}}$$

where  $V_{OVP(th)} = 8.3 \text{ V}$  typical and  $I_{OVP(th)} = 200 \mu\text{A}$  typical.

The OVP function is not a latched fault. If the OVP condition occurs during a load dump, the IC will stop switching but not shut down.

There are several possibilities why an OVP condition is encountered during operation, the two most common being an open LED string and a disconnected output condition.

Figure 26 illustrates when the output of the A8519 is disconnected from load during normal operation. The output voltage instantly increases up to OVP voltage level, and then the boost stops switching to prevent damage to the IC. When the output voltage decreases to a low value, the boost converter will begin switching. If the condition that caused the OV event still exists, OVP will be triggered again.

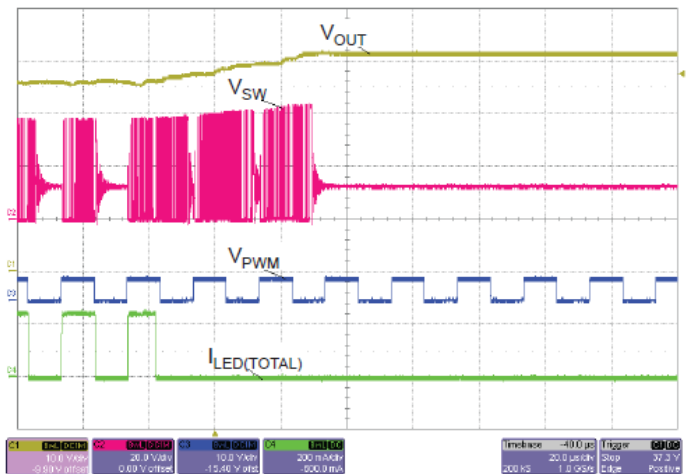


Figure 26: Output of A8519 when Disconnected from Load During Normal Operation

Figure 27 illustrates a typical OVP condition caused by an open LED string. Once OVP is detected, the boost stops switching, and the open LED string is removed from operation. Afterwards, VOUT is allowed to fall, the boost will resume switching, and the A8519 will resume normal operation.

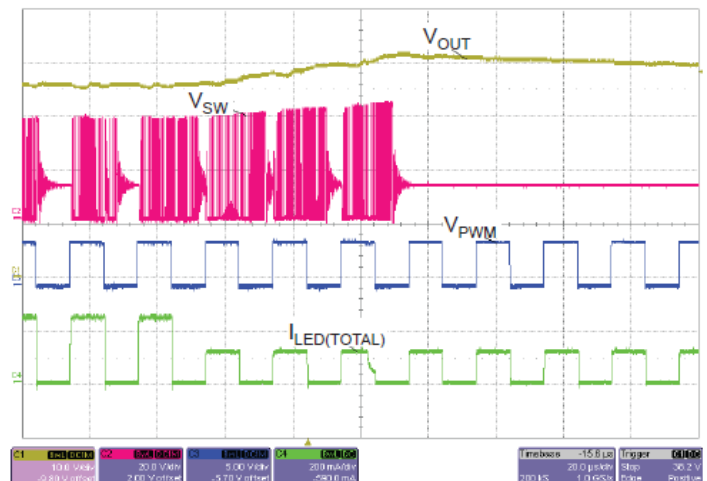


Figure 27: Typical OVP Condition Caused by an Open LED String

The A8519 also has built-in secondary overvoltage protection to protect the internal switch in the event of an open-diode condition. Open Schottky diode detection is implemented by detecting overvoltage on the SW pin of the device. If voltage on the SW pin exceeds the device's safe operating voltage rating, the A8519 disables and remains latched. To clear this fault, the IC must be shut down by either using the PWM signal or by going below the UVLO threshold on the VIN pin.

Figure 28 illustrates open Schottky diode protection while the IC is in normal operation. As soon as the switch node voltage ( $V_{SW}$ ) exceeds 48 V, the IC will shut down. Due to small delays in the detection circuit, as well as there being no load present, the switch node voltage ( $V_{SW}$ ) will rise above the trip point voltage.

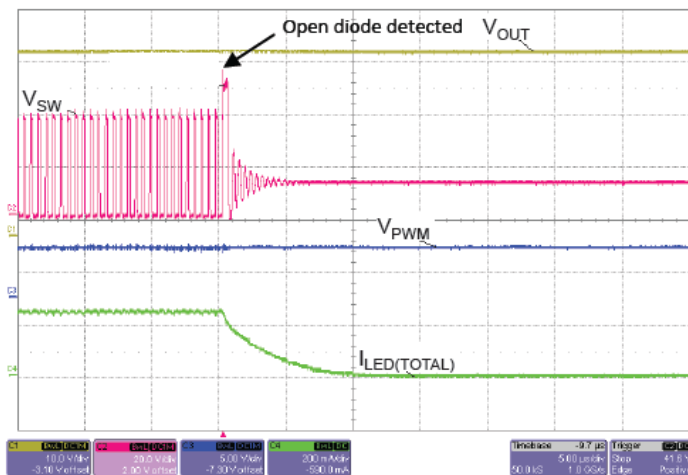


Figure 28: Open Schottky Diode Protection

When enabling the A8519 into an open-diode condition, the IC will first go through all of its initial LED detection and will then check the boost output voltage. At that point, the open diode is detected.

### Boost Switch Overcurrent Protection

The boost switch is protected with cycle-by-cycle current limiting set at a minimum of 3 A. Figure 29 illustrates the normal operation of the switch node ( $V_{SW}$ ), inductor current, and output voltage ( $V_{OUT}$ ) for a 11×4 LED configuration.

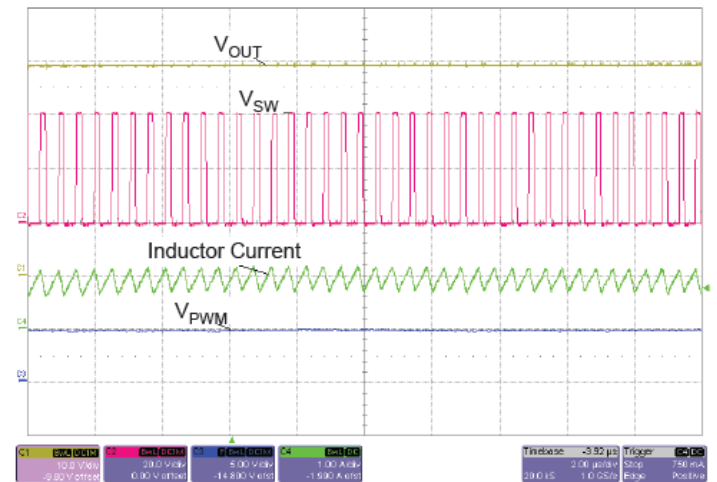


Figure 29: Normal Operation of Switch Node ( $V_{SW}$ ), Inductor Current, and Output Voltage ( $V_{OUT}$ )

Figure 30 shows the cycle-by-cycle current limit showing inductor current as a green trace. Note the inductor current is truncated and as a result the output voltage is reduced as compared to normal operation shown for the 11×4 LED configuration.

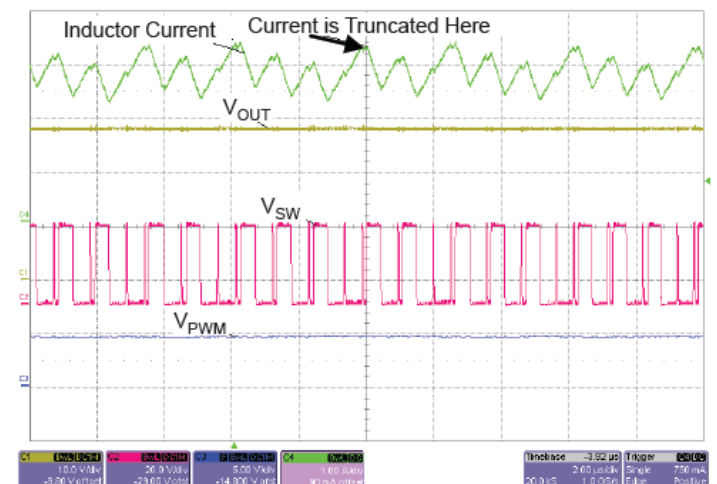


Figure 30: Cycle-by-Cycle Current Limit

There is also a secondary current limit ( $I_{SW(LIM2)}$ ) that is sensed through the boost switch. This current limit, once detected, immediately shuts down the A8519. The level of this current limit is set above the cycle-by-cycle current limit to protect the switch from destructive currents when boost inductor is shorted. Figure 31 shows the secondary boost switch OCP. Once this limit is reached, the A8519 will immediately shut down.

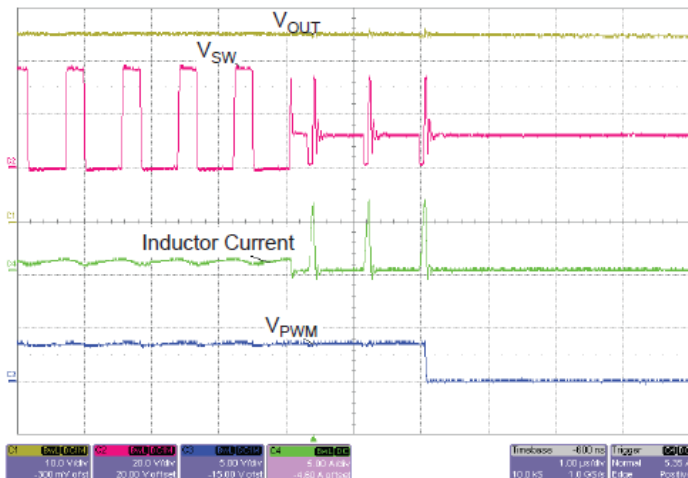


Figure 31: Secondary Boost Switch OCP

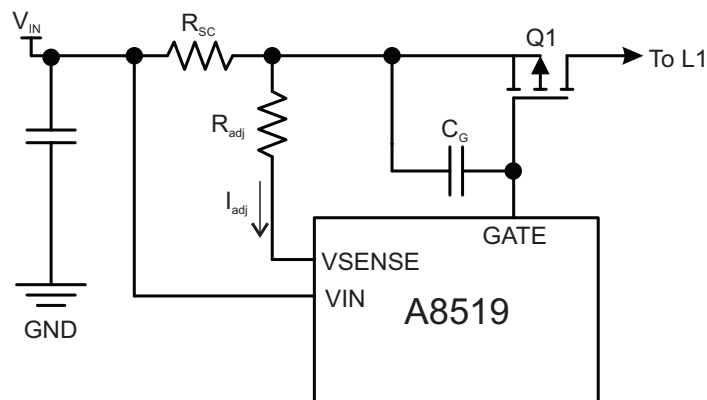


Figure 32: Typical Circuit Showing Implementation of Input Disconnect Feature

### Input Overcurrent Protection and Disconnect Switch

The primary function of the input disconnect switch is to protect the system and the device from catastrophic input currents during a fault condition.

If the input current level goes above the preset current limit threshold, the part will be shut down in less than 3  $\mu$ s—this is a latched condition. The fault flag is also set low to indicate a fault. This protection feature prevents catastrophic failure in the system due to a short of the inductor, inductor short to GND, or short at the output GND. Figure 33 illustrates the typical input overcurrent fault condition. As soon as input OCP limit is reached, the part disables the gate of the disconnect switch Q1.

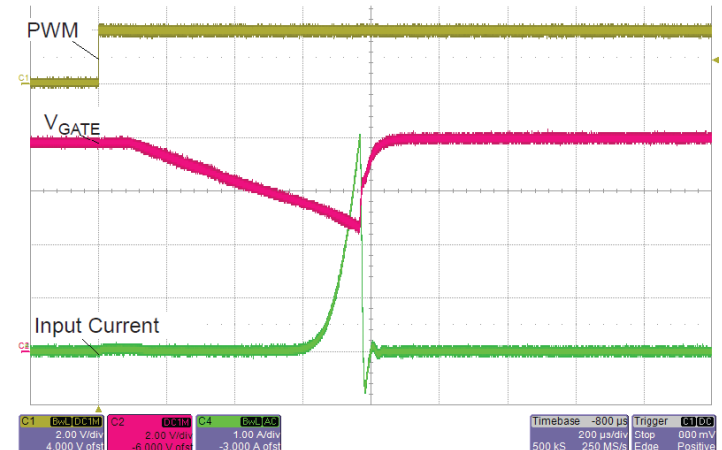


Figure 33: Startup into Output Shorted to GND fault. Input OCP tripped at 4 A ( $R_{SC} = 0.024$  W,  $R_{adj} = 383$   $\Omega$ )

During startup when Q1 first turns on, an inrush current flows through Q1 into the output capacitance. If Q1 turns on too fast (due to its low gate capacitance), the inrush current may trip input OCP limit. In this case, an external gate capacitance  $C_G$  is added to slow down the turn-on transition. Typical value for  $C_G$  is around 4.7 to 22 nF. Do not make  $C_G$  too large, since it also slows down the turn-off transient during a real input OCP fault.

### Setting the Current Sense Resistor

As shown in Figure 32:

$$V_{IN} - V_{SENSE} = V_{SC} + I_{adj} \times R_{adj}$$

$$I_{SC} = ((V_{IN} - V_{SENSE}) - I_{adj} \times R_{adj}) / R_{SC}$$

where  $V_{SC}$  = the voltage drop across  $R_{SC}$ . The typical threshold for the current sense is  $V_{IN} - V_{SENSE} = 110$  mV when  $R_{adj}$  is  $0 \Omega$ . The A8519 can have this voltage trimmed using the  $R_{adj}$  resistor. It is recommended to set trip point to be above 3.65 A to avoid conflicts with the cycle-by-cycle current limit typical threshold. A sample calculation is done below for 4.25 A of input current.

Calculated max value of sense resistor  $R_{SC} = 0.11 \text{ V} / 4.25 \text{ A} = 0.0259 \Omega$ .

The  $R_{SC}$  chosen is  $0.024 \Omega$ , a standard value. Therefore, the voltage drop across  $R_{SC}$  is:

$$V_{SC} = 4.25 \text{ A} \times 0.024 \Omega = 0.102 \text{ V}$$

$$R_{adj} = \frac{V_{SENSE(trip)} - V_{SC}}{I_{adj}}$$

$$R_{adj} = \frac{0.11 \text{ V} - 0.102 \text{ V}}{21.5 \mu\text{A}} = 372 \Omega$$

### Input UVLO

When  $V_{IN}$  and  $V_{SENSE}$  rise above  $V_{UVLOrise}$  threshold, the A8519 is enabled. The A8519 is disabled when  $V_{IN}$  falls below  $V_{UVLOfall}$  threshold for more than 50  $\mu\text{s}$ . This small delay is used to avoid shutting down because of momentary glitches in the input power supply.

Figure 34 illustrates a shutdown due to a falling input voltage ( $V_{IN}$ ). When  $V_{IN}$  falls below 3.90 V, the IC will shut down.

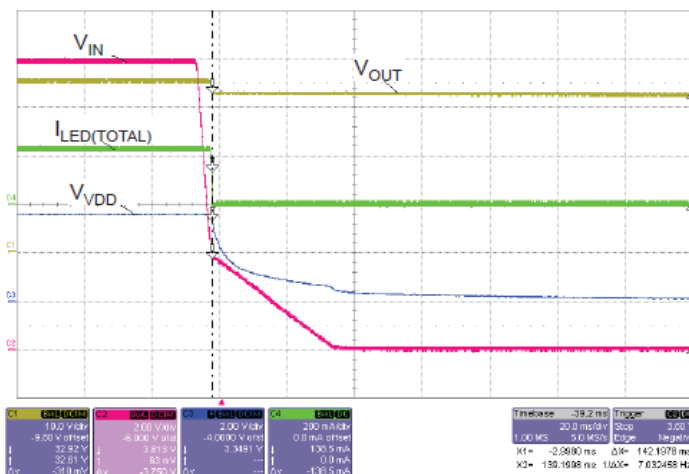


Figure 34: Shutdown with Falling Input Voltage

### VDD

The VDD pin provides regulated bias supply for internal circuits. Connect a capacitor with a value of 1  $\mu\text{F}$  or greater to this pin. The internal LDO can deliver no more than 2 mA of current with a typical VDD voltage of about 3.5 V, enabling this pin to serve as the pull-up voltage for the fault pin.

### Shutdown

If PWM pin is pulled low for more than  $t_{PWML}$  (32,750 clock cycles), the device enters shutdown mode and clears all internal fault registers. As an example, at 2 MHz clock frequency, it will take approximately 16.3 ms to shut down the IC into the low power mode. When shut down, the IC will disable all current sources and wait until the PWM goes high to re-enable the IC.

Figure 35 depicts the shutdown using the PWM enable, showing the 16.3 ms delay between PWM signal and when the VDD and GATE of disconnect switch turn off.

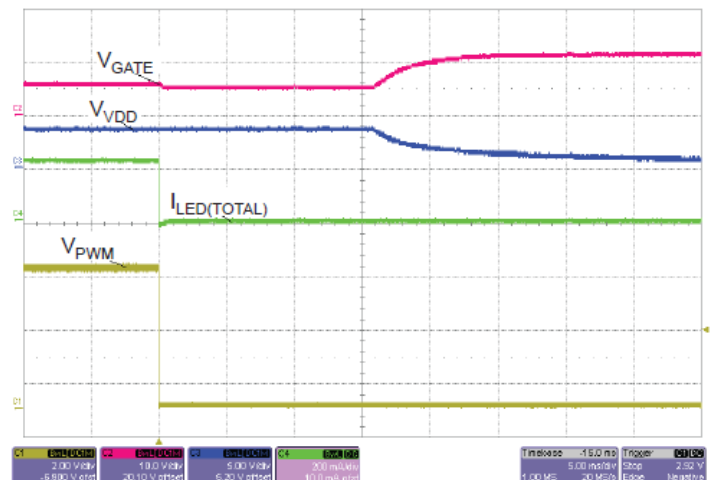


Figure 35: Shutdown Using the PWM Enable

### Dithering Feature

To minimize the switching frequency harmonics, a dithering feature is implemented in A8519. This feature simplifies the input filters needed to meet the automotive CISPR 25 conducted and radiated emission limits. The dithering sweep is internally set at  $\pm 5\%$ . The switching frequency will ramp from 0.95 times the programmed frequency to 1.05 times the programmed frequency. The rate or modulation at which the frequency sweeps is governed by an internal 12.5 kHz triangle pattern.

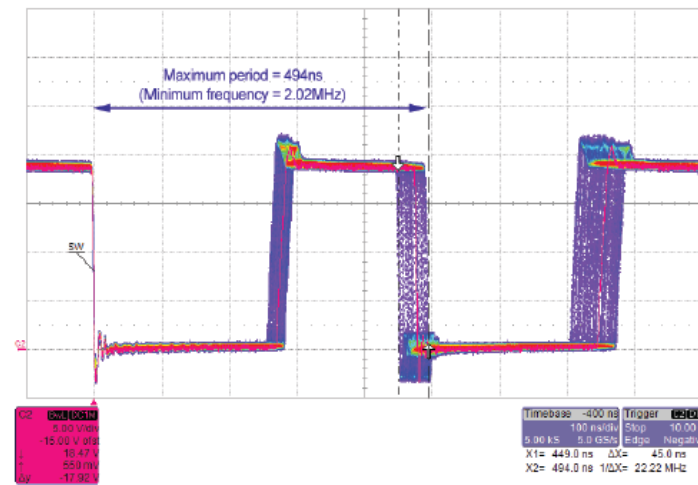


Figure 36: Minimum Dithering Switching Frequency = 2.02 MHz at  $V_{IN} = 12$  V, and PWM Ratio = 100%

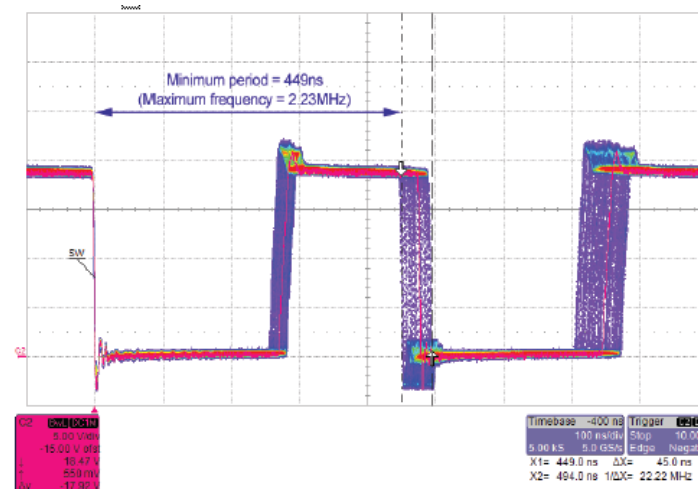


Figure 37: Maximum Dithering Switching Frequency = 2.23 MHz at  $V_{IN} = 12$  V, and PWM Ratio = 100%

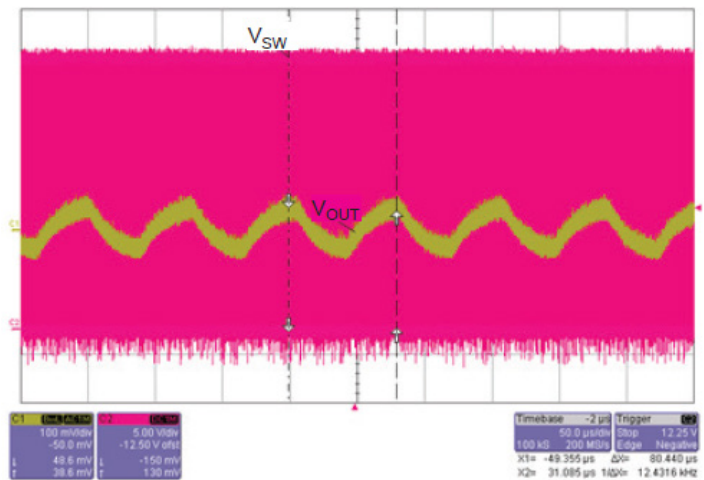


Figure 38: Output Voltage Ripple Frequency Due to Dithering = 12.4 kHz at  $V_{IN} = 12$  V, and PWM Ratio = 100%

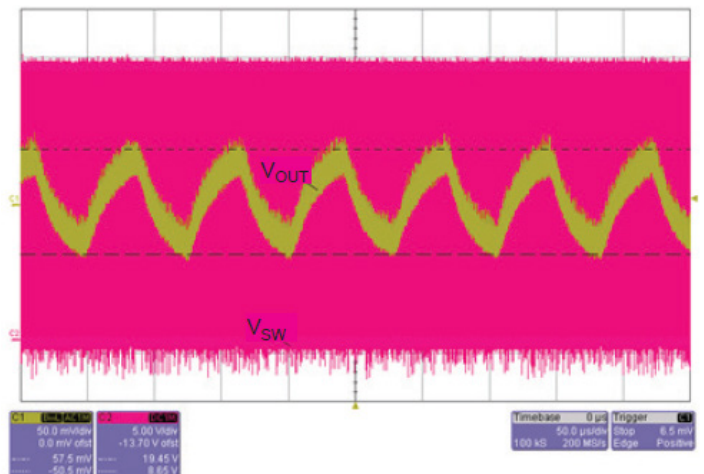


Figure 39: Output Voltage Ripple Amplitude Due to Dithering = 100 mV at  $V_{IN} = 12$  V, and PWM Ratio = 100%

### Fault Protection During Operation

The A8519 series devices constantly monitor the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in the table below. There are several points at which the A8519 monitors for faults during operation. The locations are input current, switch current, output voltage, switch voltage, and LED pins. (Note: Some protection features might not be active during startup to prevent false triggering of fault conditions.)

The detectable fault conditions are:

- Open LED pin
- Shorted LED pin to GND
- Open or shorted inductor
- Open or shorted boost diode
- Shorted inductor
- $V_{OUT}$  short to GND
- SW pin shorted to GND
- ISET pin shorted to GND
- Input disconnect switch source shorted to GND

Note: Some faults will not be protected if the input disconnect switch is not used. An example of this is  $V_{OUT}$  short to GND.

Table 5: Fault Mode Table

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Disconnect Switch	LED Sink Drivers
Primary Switch Overcurrent Protection (cycle-by-cycle current limit)	Auto-restart	Always	NO	This fault condition is triggered when the SW current exceeds the cycle-by-cycle current limit, $I_{SW(LIM)}$ . The present SW on-time is truncated immediately to limit the current. Next switching cycle starts normally.	Off for a single cycle	ON	ON
Secondary Switch Current Limit	Latched	Always	YES	When current through boost switch exceeds secondary SW current limit ( $I_{SW(LIM2)}$ ), the device immediately shuts down the disconnect switch, LED drivers, and boost. The Fault flag is set. To re-enable the part, the PWM pin needs to be pulled low for 32,750 clock cycles.	OFF	OFF	OFF
Input Disconnect Current Limit	Latched	Always	YES	The device is immediately shut off if the voltage across the input sense resistor is above the $V_{VSENSE(trip)}$ threshold. To re-enable the device, the PWM pin must be pulled low for 32,750 clock cycles.	OFF	OFF	OFF
Secondary OVP	Latched	Always	YES	Secondary overvoltage protection is used for open-diode detection. When diode D1 opens, the SW pin voltage will increase until $V_{OVP(sec)}$ is reached. This fault latches the IC. The input disconnect switch is disabled as well as the LED drivers. To re-enable the part, the PWM pin needs to be pulled low for 32,750 clock cycles.	OFF	OFF	OFF
LEDx Pin Short Protection	Auto-restart	Startup	NO	This fault prevents the part from starting up if any of the LED pins are shorted. The part stops soft-start from starting while any of the LED pins are determined to be shorted. Once the short is removed, soft-start is allowed to start.	OFF	ON	OFF
LEDx Pin Open	Auto-restart	Normal operation	NO	When an LED pin is open, the device will determine which LED pin is open by increasing the output voltage until OVP is reached. Any LED string not in regulation will be turned OFF. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level.	ON	ON	OFF for open pins, ON for all others
ISET Short Protection	Auto-restart	Always	NO	Fault occurs when the $I_{ISET}$ current goes above 150% of max current. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to regulate to the preset LED current.	OFF	ON	OFF
FSET Short Protection	Auto-restart	Always	YES	Fault occurs when the FSET current goes above 150% of max current. The boost will stop switching, Disconnect switch will turn off, and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to restart with soft-start.	OFF	OFF	OFF
Overvoltage Protection	Auto-restart	Always	NO	Fault occurs when OVP pin exceeds $V_{OVP(th)}$ threshold. The IC will immediately stop switching to try to reduce the output voltage. If the output voltage decreases, then the IC will restart switching to regulate the output voltage.	STOP during OVP event	ON	ON

# A8519 and A8519-1

## Wide Input Voltage Range, High-Efficiency, Fault-Tolerant LED Driver

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Disconnect Switch	LED Sink Drivers
Undervoltage Protection	Auto-restart	Always	YES	Device immediately shuts off boost and current sinks if the voltage at OVP pin is below $V_{UVLP(th)}$ . It will auto-restart once the fault is removed.	OFF	ON	OFF
LED String Short Detection	Auto-restart	Always	NO	Fault occurs when the LED pin voltage exceeds 5.2 V. Once the LED string short fault is detected, the LED string above the threshold will be removed from operation.	ON	ON	OFF for shorted pins, ON for all others
Overtemperature Protection	Auto-restart	Always	YES	Fault occurs when the die temperature exceeds the overtemperature threshold, typically 170°C.	OFF	OFF	OFF
$V_{IN}$ UVLO	Auto-restart	Always	NO	Fault occurs when $V_{IN}$ drops below $V_{UVLOfall}$ , typically below 3.9 V. This fault resets all latched faults.	OFF	OFF	OFF

### APPLICATION INFORMATION

#### Design Example

This section provides a method for selecting component values when designing an application using the A8519.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- $V_{IN}$ : 10 to 14 V
- Quantity of LED channels, #CHANNELS: 4
- Quantity of series LEDs per channel, #SERIESLEDS: 10
- LED current per channel,  $I_{LED}$ : 60 mA
- LED  $V_f$  at 60 mA: 3.2 V
- $f_{SW}$ : 2 MHz
- PWM dimming frequency 200 Hz, 1% duty cycle

**Step 1:** Connect LED strings to pins LED1, LED2, LED3, and LED4.

**Step 2:** Determine the LED current set resistor  $R_{ISET}$

$$R_{ISET} = \frac{(V_{ISET} \times A_{ISET})}{I_{LED}}$$

$$R_{ISET} = \frac{(1.017 \times 710)}{0.06 A} = 12 k\Omega$$

$$R_{ISET} = 11.8 k\Omega$$

An 11.8 k $\Omega$  resistor was chosen.

**Step 3a:** Determining the OVP resistor.

The OVP resistor is connected between the OVP pin and the output voltage of the converter. The first step is to determine the maximum voltage based on the LED requirements. The regulation voltage for an LED pin ( $V_{LEDx}$ ) of the A8519 is 850 mV. A 5 V headroom is added to give margin to the design due to noise and output voltage ripple.

$$V_{OUT(ovp)} = \#SERIESLEDS \times V_f + V_{LED} + 5 V$$

$$V_{OUT(ovp)} = 10 \times 3.2 V + 0.850 V + 5 V$$

$$V_{OUT(ovp)} = 37.85 V$$

The OVP resistor is:

$$R_{OVP} = \frac{(V_{OUT(ovp)} - V_{OVP(th)})}{I_{OVP(th)}}$$

Where both  $I_{OVP(th)}$  and  $V_{OVP(th)}$  values are from the datasheet's Electrical Characteristics table.

$$R_{OVP} = \frac{37.85 - 8.3}{0.2}$$

$$R_{OVP} = 147.75 k\Omega$$

Choose a value of resistor that is higher value than the calculated  $R_{OVP}$ . In this case, a value of 158 k $\Omega$  was selected. Below is the actual value of the minimum OVP trip level with the selected resistor.

$$V_{OUT(ovp)} = 158 k\Omega \times 0.2 mA + 8.3 V$$

$$V_{OUT(ovp)} = 39.9 V$$

**Step 3b:** At this point, a quick check needs to be done to see if the conversion ratio is adequate for the selected frequency. Where  $V_D$  is the boost diode forward voltage, minimum off-time ( $t_{SW(off)}$ ) is found in the datasheet:

$$D_{MAX(boost)} = 1 - t_{SW(off)} \times f_{SW(max)}$$

$$D_{MAX(boost)} = 1 - (85 ns \times 2.2 MHz) = 0.813$$

$$Theoretical Max V_{OUT} = \left[ \frac{V_{IN(min)}}{1 - D_{MAX(boost)}} \right] - V_D$$

$V_D$  is the voltage drop of the boost diode.

$$Theoretical Max V_{OUT} = \left[ \frac{10 V}{1 - 0.813} \right] - 0.4 = 53.1 V$$

Theoretical Max  $V_{OUT}$  value needs to be greater than the value  $V_{OUT(ovp)}$ . If this is not the case, the switching frequency of the boost converter is going to have to be reduced to meet the maximum duty cycle requirements.

**Step 4:** Inductor selection.

The inductor needs to be chosen such that it can handle the necessary input current. In most applications, due to stringent EMI requirements, the system needs to operate in continuous conduction mode throughout the whole input voltage range.

**Step 4a:** Determine the Duty Cycle.

$$D_{MAX} = 1 - \left[ \frac{V_{IN(min)}}{(V_{OUT(ovp)} + V_D)} \right]$$

$$D_{MAX} = 1 - \left[ \frac{10}{(39.9 + 0.4)} \right] = 0.75$$

**Step 4b:** Determine the maximum and minimum input current to the system. The minimum input current will dictate the inductor value. The maximum current rating will dictate the current rating of the inductor.

$$I_{IN(max)} = \frac{V_{OUT(ovp)} \times I_{OUT}}{V_{IN(min)} \times \eta}$$

$$I_{OUT} = \#Channels \times I_{LED}$$

$$I_{OUT} = 4 \times 0.060 A = 0.240 A$$

A good approximation of efficiency  $\eta$  can be taken from the efficiency curves located on page 10. A value of 90% is a good starting approximation.

$$I_{IN(max)} = \frac{39.9 V \times 240 mA}{10 V \times 0.90} = 1.06 A$$

$$I_{IN(max)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN(max)} \times \eta}$$

$$V_{OUT} = 10 \times 3.2 V + 0.85 V = 32.85 V$$

$$I_{IN(min)} = \frac{32.85 V \times 240 mA}{14 V \times 0.90} = 0.625 A$$

**Step 4c:** Determining the inductor value. To ensure that the inductor operates in continuous conduction mode, the value of the inductor needs to be set such that the  $\frac{1}{2}$  inductor ripple current is not greater than the average minimum input current. A first pass calculation for  $K_{ripple}$  should be 30% of the maximum inductor current.

$$\Delta I_L = I_{IN(max)} \times K_{ripple}$$

$$\Delta I_L = 1.06 A \times 0.3 = 0.318 A$$

$$L = \frac{(V_{IN(min)} \times D_{MAX})}{(\Delta I_L \times f_{SW})}$$

$$L = \frac{10 V}{0.318 A \times 2 MHz} \times 0.75 = 11.79 \mu H$$

Double-check to make sure that  $\frac{1}{2}$  current ripple is less than  $I_{IN(min)}$ .

$$I_{IN(min)} > \frac{1}{2} \Delta I_L$$

$$0.625 A > 0.159 A$$

A good inductor value to use would be 10  $\mu H$ .

**Step 4d:** This step is used to verify that there is sufficient slope compensation for the inductor chosen. 6 A/ $\mu s$  slope compensation value is applied inside the IC at 2 MHz switching frequency. The slope compensation at any switching frequency can be determined by the following formula:

$$Slope\ Comp = \frac{6 A/\mu s \times f_{SW}}{2 \times 10^6}$$

Next, insert the inductor value used in the design:

$$\Delta I_{L(used)} = \frac{V_{IN(min)} \times D_{MAX}}{L(used) \times f_{SW}}$$

$$\Delta I_{L(used)} = \frac{10 V \times 0.75}{10 \mu H \times 2 MHz} = 0.375 A$$

$$Required\ Min\ Slope = \frac{\Delta I_{L(used)} \times \Delta S \times 10^{-6}}{\frac{1}{f_{SW}} \times (1 - D_{MAX})}$$

where  $\Delta S$  is taken from the following formula:

$$\Delta S = 1 - \frac{0.18}{D_{MAX}}$$

$$\Delta S = 0.76$$

$$Required\ Min\ Slope = \frac{0.375 \times 0.76 \times 10^{-6}}{\frac{1}{2 MHz} \times (1 - 0.75)} = 2.28 A/\mu s$$

If the required minimum slope is larger than the calculated slope compensation, the inductor value needs to be increased. Note that the slope compensation value is in A/μs the  $1 \times 10^{-6}$  is constant multiplier.

**Step 4e:** Determining the inductor current rating.

$$I_{L(min)} = I_{IN(max)} + (1/2) \times \Delta I_L$$

$$I_{L(min)} = 1.06 \text{ A} + \frac{0.375 \text{ A}}{2} = 1.25 \text{ A}$$

**Step 5:** To determine the resistor value for a switching frequency refer to the graph in Figure 8. A 10 kΩ resistor will result in a 2 MHz switching frequency.

**Step 6:** Choosing the proper output Schottky diode. The diode needs to be chosen for three characteristics when it is used in LED lighting circuitry. The most obvious two are the current rating of the diode and the reverse voltage rating. The reverse voltage rating should be larger than the maximum output  $V_{OVP}$ . The peak current through the diode is:

$$I_{D(pk)} = I_{IN(max)} + \frac{\Delta I_{L(used)}}{2}$$

$$I_{D(pk)} = 1.06 + \frac{0.375 \text{ A}}{2} = 1.25 \text{ A}$$

The other major factor in deciding the switching diode is the reverse current characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time, the boost converter is not switching. This results in a slow bleeding off of the output voltage due to leakage currents.  $I_R$  or reverse current can be a large contributor especially at high temperatures. The reverse current of the selected diode varies between 1 and 100 μA. For higher efficiency, use a small forward voltage drop diode. For lower high-frequency noise, choose a small junction capacitor diode.

**Step 7:** Choosing the output capacitors. The output capacitors need to be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. The biggest factor that contributes to the size of the output capacitor is PWM dimming frequency and the PWM duty cycle. Another major contributor is leakage current ( $I_{LK}$ ). This current is the combination of the OVP current sense as well as the reverse current of the boost diode. In this design, the PWM dimming frequency is

200 Hz; the minimum duty cycle is 0.02%. Typically, the voltage variation on the output during PWM dimming needs to be less than 250 mV ( $V_{COUT}$ ) so there is no audible hum.

$$C_{OUT} = I_{LK} \times \frac{(1 - \text{minimum dimming duty cycles})}{\text{PWM dimming frequency} \times V_{COUT}}$$

The selected diode leakage current at a 150°C junction temperature and 30 V output is 100 μA, and the maximum leakage current through OVP pin is 1 μA. The total leakage current can be calculated as follows:

$$I_{LK} = I_{LKG(diode)} + I_{LKG(ovp)}$$

$$= 100 \mu\text{A} + 1 \mu\text{A}$$

$$= 101 \mu\text{A}$$

$$C_{OUT} = 101 \mu\text{A} \times \frac{(1 - 0.02)}{200 \text{ Hz} \times 0.250 \text{ V}} = 2 \mu\text{F}$$

A capacitor larger than 2 μF should be selected. Due to degradation of capacitance at dc voltages, a 4.7 μF / 50 V capacitor is a good choice.

Vendor	Value	Part Number
Murata	4.7 μF / 50 V	GRM21BC18H475KE11K

It is also necessary to note that if a high dimming ratio of 5000:1 must be maintained at lower input voltages, then larger output capacitors will be needed.  $4 \times 4.7 \mu\text{F} / 50 \text{ V} / \text{X6S} / 0805$  capacitors are chosen; 0805 size is selected to minimize possible audible noise.

The RMS current through the capacitor is given by:

$$C_{OUT(rms)} = I_{OUT} \times \sqrt{\frac{D_{MAX} + \frac{\Delta I_{L(used)}}{I_{IN(max)} \times 12}}{1 - D_{MAX}}}$$

$$C_{OUT(rms)} = 0.240 \times \sqrt{\frac{0.75 + \frac{0.375}{1.06 \times 12}}{1 - 0.75}} = 0.424 \text{ A}$$

The output capacitor needs to have a current rating of at least 0.424 A. The capacitors selected in this design,  $4 \times 4.7 \mu\text{F} / 50 \text{ V} / \text{X6S} / 0805$ , have a combined current rating of more than 3 A current rating.

**Step 8:** Selection of input capacitor. The input capacitor needs to be selected such that it provides good filtering of the input voltage waveform. A good rule of thumb is to set the input voltage ripple  $\Delta V_{IN}$  to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows:

$$C_{IN} = \frac{\Delta I_{L(used)}}{8 \times f_{SW} \times \Delta V_{IN}}$$

$$C_{IN} = \frac{0.375 A}{8 \times 2 MHz \times 0.1 V} = 0.234 \mu F$$

$$C_{IN(rms)} = \frac{I_{OUT} \times \frac{\Delta I_{L(used)}}{I_{IN(max)}}}{(1 - D_{MAX}) \times \sqrt{12}} = 0.1 A$$

$$C_{IN(rms)} = \frac{0.240 A \times \frac{0.375 A}{1.06 A}}{(1 - 0.75) \times \sqrt{12}} = 0.1 A$$

A good ceramic input capacitor with ratings of 50 V / 2.2  $\mu F$  or 50 V / 4.7  $\mu F$  will suffice for this application.

Vendor	Value	Part Number
Murata	4.7 $\mu F$ / 50 V	GRM32ER71H475KA88L
Murata	2.2 $\mu F$ / 50 V	GRM31CR71H225KA88L

If long wires are used for the input, it is necessary to use a much

larger input capacitor. A larger input capacitor is also required to have stable input voltage during line transients. Combinations of aluminum electrolytic and ceramic capacitors can be used.

**Step 9:** Choosing the input disconnect switch components.

Set the input disconnect current limit to 4.25 A.

$$R_{SC} = \frac{0.11 V}{4.25 A} = 0.0259 \Omega$$

The  $R_{SC}$  chosen is 0.024 ohms. Therefore, the voltage drop across  $R_{SC}$  is:

$$V_{SC} = 4.25 A \times 0.024 \Omega = 0.102 V$$

$$R_{adj} = \frac{V_{VSENSE(trip)} - V_{SC}}{I_{adj}}$$

$$R_{adj} = \frac{0.11 V - 0.102 V}{21.5 \mu A} = 372 \Omega$$

A value of 383  $\Omega$  was chosen for this design. The disconnect switch Q1 works as on or off. Therefore, the  $R_{adj}$  value is not really critical.

For the input disconnect switch, an AO4421 6.2 A / 60 V P-channel MOSFET is selected.

To achieve proper operation at low dimming ratios, connect an RC filter to the VOUT pin. Use R = 10 k $\Omega$  and C = 47 pF.

## Wide Input Voltage Range, High-Efficiency, Fault-Tolerant LED Driver



### PACKAGE OUTLINE DRAWINGS

#### For Reference Only – Not for Tooling Use

(Reference MO-153 ACT)

Dimensions in millimeters – NOT TO SCALE

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

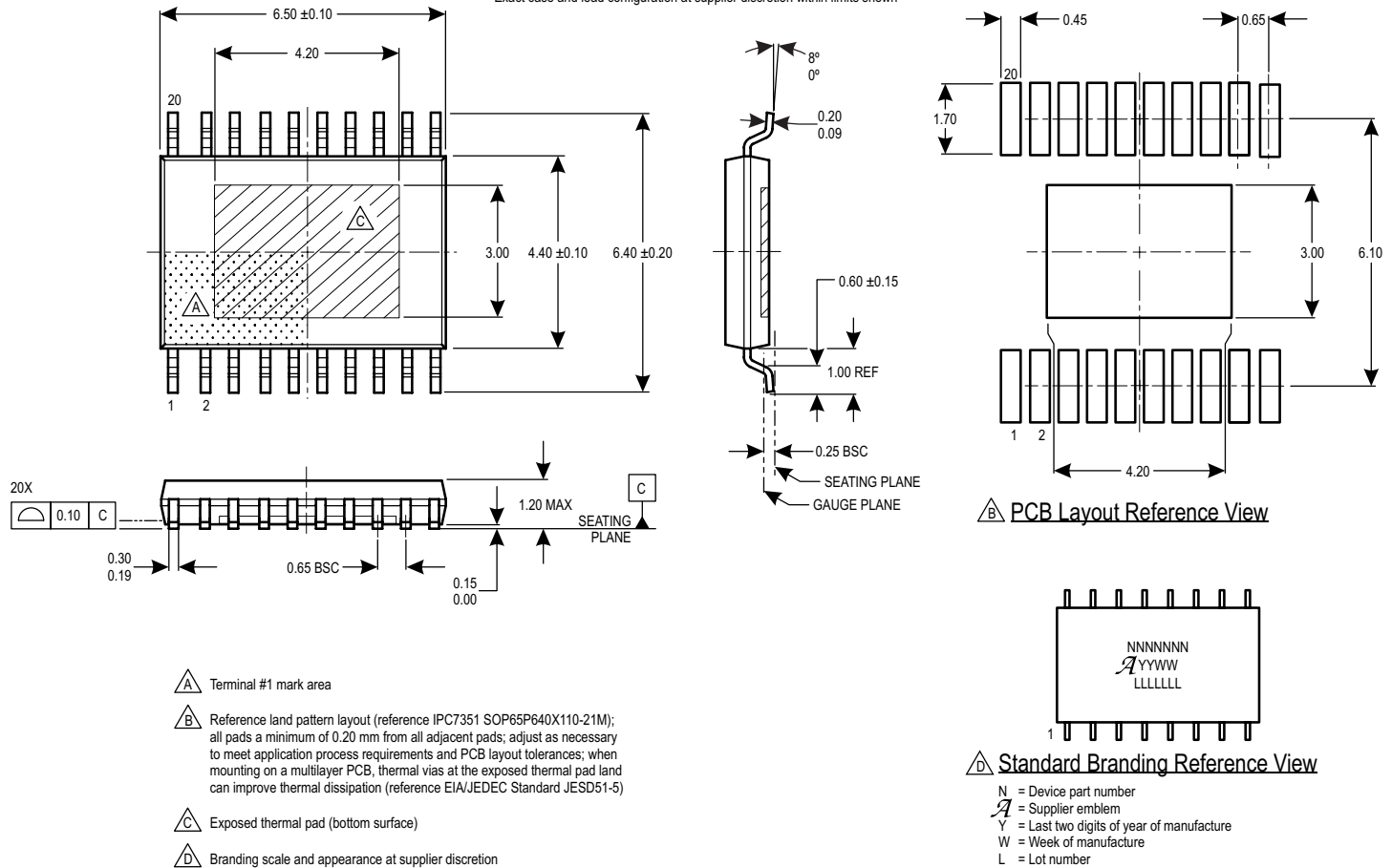
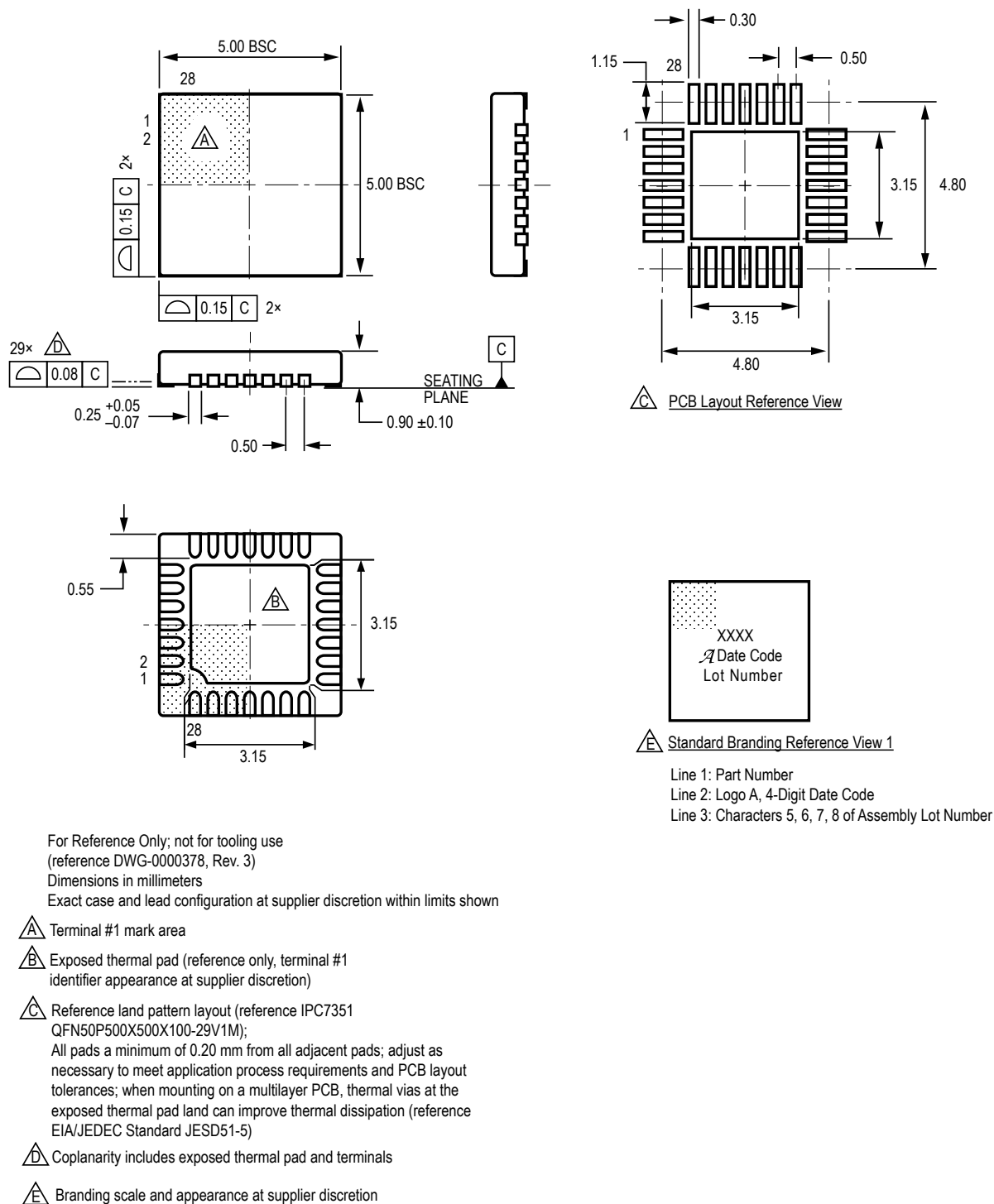


Figure 41: Package LP: 20-Pin, 0.65 mm Pin Pitch TSSOP with Exposed Thermal Pad



**Figure 42: Package ET: 28-Pin QFN with Exposed Thermal Pad**

# A8519 and A8519-1

## Wide Input Voltage Range, High-Efficiency, Fault-Tolerant LED Driver

### Revision History

Number	Date	Description
–	September 10, 2014	Initial Release
1	October 24, 2014	Lowered minimum $f_{SW}$ (when using $R_{FSET}$ ) to 200 kHz and SYNC down to 260 kHz.
2	March 18, 2015	Revised OVP Thresholds and Oscillator Frequencies.
3	May 19, 2015	Added A8519-1 variant.
4	June 10, 2015	Fixed typo on page 2; revised FSET pin voltage typical spec.
5	November 4, 2015	Amended “Enabling the IC” (page 12) and “Synchronization” (page 15) of Functional Description; inserted Figures 18 and 19; updated Selection Guide table (page 2); corrected 2nd Typical Application Drawing (page 9)
6	January 8, 2016	Amended “Powering Up: Boost Output Undervoltage Protection” (page 13)
7	October 24, 2016	Updated Input Overcurrent Protection and Disconnect Switch section (page 22)
8	December 21, 2018	Increased minimum external SYNC frequency to 320 kHz
9	January 23, 2019	Added timing diagrams to illustrate all possible cases to program the switching frequency (page 16); Corrected Fault table for FAULT flag behavior during Overtemperature Protection (page 29)
10	March 14, 2019	Added Case 5 to Synchronization section (page 17)
11	September 22, 2021	Updated $V_{LEDx}$ Short Detect maximum value (page 7) and ET-28 package drawing (page 38)

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