

**Description (continued)**

The A2550 also includes power-on reset circuitry (NPOR) as well as an integrated watchdog circuit. Combined, they service the monitoring and reset requirements of a system microprocessor.

The A2550 is supplied in a 16-pin TSSOP package with exposed thermal pad (package LP). The package is lead (Pb) free, with 100% matte tin leadframe plating.

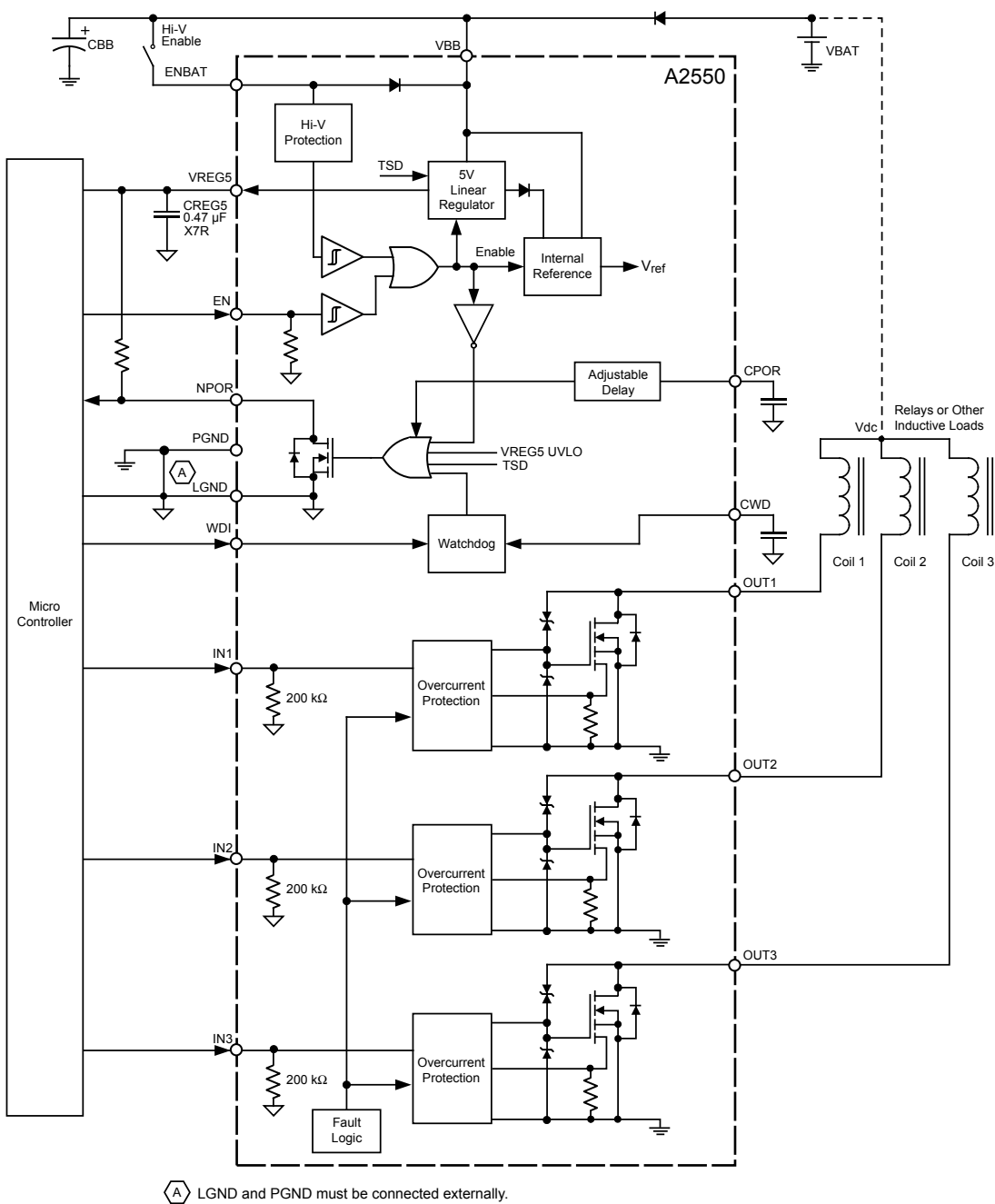
**Selection Guide**

Part Number	Packing
A2550KLPT-R	13-in. reel, 4000 pieces/reel

**Absolute Maximum Ratings**

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	$V_{BB}$		–0.3 to 60	V
High Voltage Enable	$V_{ENBAT}$		–0.3 to 60	V
Output Driver	$V_{OUT}$	Continuous rating; outputs off	–1.4 to 48	V
Output Load Clamp	$V_{OUT(CL)}$	Transient rating	60	V
Maximum Energy at Outputs	$E_{OUT}$	Single Pulse, $T_J(\text{initial}) = 125^\circ\text{C}$	100	mJ
Peak Power Dissipation at Outputs	$P_{PK}$	Single pulse, $T_J(\text{initial}) = 125^\circ\text{C}$ , $\Delta t = 1 \text{ ms}$ ; see figure 2 for different durations and $T_J(\text{initial})$	1.7	W
All other pins			–0.3 to 7	V
ESD Rating – Human Body Model		AEC-Q100-002; all pins	2.5	kV
ESD Rating – Charged Device Model		AEC-Q100-011; all pins	1050	V
Operating Ambient Temperature	$T_A$	Range K	–40 to 125	$^\circ\text{C}$
Maximum Junction Temperature	$T_{J(\text{max})}$		150	$^\circ\text{C}$
Storage Temperature	$T_{\text{stg}}$		–55 to 150	$^\circ\text{C}$

Functional Block Diagram



Component Selection Table

Name	Suitable Characteristics	Representative Device
CBB	33 $\mu$ F, 63 V electrolytic	United Chemi-Con EGXE630E--330MH12D
CREG5	0.47 $\mu$ F, 25 V, X7R ceramic	
CWD, CPOR	0.22 $\mu$ F, 16 V, X7R ceramic	

ELECTRICAL CHARACTERISTICS,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $V_{BB}$  within operating limits, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply						
VBB Operating Voltage <sup>1</sup>	V <sub>BB</sub>		7	–	40	V
VBB Supply Current	I <sub>BBQ</sub>	All OUTx Off; EN = 5 V, V <sub>BB</sub> = ENBAT = 14 V	–	–	4	mA
	I <sub>BB</sub>	All OUTx On; EN = 5 V, V <sub>BB</sub> = ENBAT= 14 V	–	–	5	mA
	I <sub>BBS</sub>	Sleep mode, EN = ENBAT = 0	–	–	10	μA
Logic Inputs						
ENBAT Input Voltage <sup>2</sup>	V <sub>ENBAT</sub>	HIGH input level	3.5	–	V <sub>BB</sub>	V
		LOW input level	0	–	1.5	V
EN, WDI, and INx Input Voltage	V <sub>IH</sub>	HIGH input level	3.5	–	5.5	V
	V <sub>IL</sub>	LOW input level	0	–	1.5	V
ENBAT, EN, WDI, INx Input Voltage Hysteresis	V <sub>Ihys</sub>		200	–	–	mV
ENBAT Input Current <sup>2,3</sup>	I <sub>ENBAT</sub>	HIGH input level, V <sub>BB</sub> = V <sub>BB(max)</sub>	–	–	400	μA
		HIGH input level, V <sub>BB</sub> = 14 V	–	–	70	μA
		LOW input level	–50	–	10	μA
EN Input Current <sup>2</sup>	I <sub>EN</sub>	HIGH input level	–	–	50	μA
		LOW input level	–50	–	10	μA
WDI Input Current <sup>2</sup>	I <sub>WDI</sub>	HIGH input level	–	–	50	μA
		LOW input level	–10	–	10	μA
INx Input Current <sup>2</sup>	I <sub>INx</sub>	HIGH input level	–	–	50	μA
		LOW input level	–10	–	10	μA
Drivers						
Propagation Delays	t <sub>p(ON)</sub>	INx change to unloaded output change	–	1	2	μs
	t <sub>p(OFF)</sub>	INx change to unloaded output change	–	0.5	1	μs
Driver On-Resistance	R <sub>DS(on)</sub>	I <sub>OUTx</sub> = 250 mA, V <sub>BB</sub> = 14 V	–	–	5	Ω
		I <sub>OUTx</sub> = 250 mA, V <sub>BB</sub> = 9 V	–	–	5.5	Ω
		I <sub>OUTx</sub> = 250 mA, V <sub>BB</sub> = 7 V	–	–	6	Ω
Driver Leakage Current	I <sub>DSS</sub>	V <sub>OUTx</sub> = 40 V	–	–	10	μA
Diode Forward Voltage	V <sub>F</sub>	I <sub>OUTx</sub> = –250 mA	–	–1.3	–1.4	V
Output Clamp Voltage	V <sub>CL</sub>	I <sub>OUTx</sub> = 100 μA	50	–	60	V
Low-Side Driver Overcurrent (O.C.) Threshold	I <sub>OUT(OC)</sub>		275	–	500	mA
Blanking Time Before Overcurrent Detect	t <sub>BLANK</sub>	I <sub>OUT</sub> = 500 mA	2	–	20	μs
Regulator						
Voltage Regulator Output Voltage	V <sub>REG5</sub>	C <sub>REG5</sub> ≥ 0.47 μF (X7R Ceramic, ESR ≤ 0. 5Ω), 1 mA ≤ I <sub>REG5</sub> ≤ 40 mA	4.9	5.0	5.1	V
Pass Transistor On-Resistance <sup>1</sup>	R <sub>REG5</sub>	I <sub>REG5</sub> = 40 mA	–	–	55	Ω
Line Regulation Voltage	V <sub>LNR</sub>	I <sub>REG5</sub> = 1 mA	–	–	20	mV
Load Regulation Voltage	V <sub>LDR</sub>	1 mA ≤ I <sub>REG5</sub> ≤ 40 mA, V <sub>BB</sub> = 7 V	–	–	100	mV
		1 mA ≤ I <sub>REG5</sub> ≤ 40 mA, V <sub>BB</sub> ≥ 9 V	–	–	40	mV
Current Limit Level <sup>4</sup>	I <sub>REG5Lim</sub>	V <sub>REG5</sub> = 4.63 V, V <sub>BB</sub> = 7 V	40	–	150	mA
		V <sub>REG5</sub> = 4.63 V, V <sub>BB</sub> ≥ 9 V	65	–	200	mA
		V <sub>REG5</sub> = 0 V	65	–	200	mA
Under Voltage Lockout Threshold	V <sub>UVREG5</sub>	V <sub>REG5</sub> falling	4.25	4.38	4.63	V
		V <sub>REG5</sub> rising	4.36	4.50	4.75	V
Under Voltage Lockout Hysteresis	V <sub>UVREG5hys</sub>		–	0.12	–	V

Continued on the next page...

ELECTRICAL CHARACTERISTICS, continued  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $V_{BB}$  within operating limits, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Watchdog and Power-On Reset						
NPOR Active Voltage	V <sub>NPOR</sub>	I <sub>NPOR</sub> = 1 mA; V <sub>REG5</sub> = 1.5 V; 1.5 V ≤ V <sub>BB</sub> ≤ 40 V	–	–	400	mV
NPOR Inactive Leakage Current	I <sub>NPOR(Off)</sub>	V <sub>NPOR</sub> = 5 V	–	–	10	μA
CWD and CPOR Trip Voltage	V <sub>TRIP(H)</sub>	V <sub>TRIP(H)</sub> = V <sub>REF</sub>	–	1.2	–	V
	V <sub>TRIP(L)</sub>		–	0.2	–	V
CPOR Charge Current	I <sub>POR</sub>		2.5	5	7.5	μA
Power-On Reset Cycle Time <sup>5</sup>	t <sub>POR</sub>	C <sub>POR</sub> = 0.22 μF	–	44	–	ms
CWD Charge Current	I <sub>CWD</sub>	Charging	2.5	5	7.5	μA
		Discharging	–	70	–	μA
Thermal Protection						
Thermal Shut Down Threshold	T <sub>TSD</sub>		150	175	–	°C
Thermal Shut Down Hysteresis	T <sub>TSDhys</sub>		–	15	–	°C

<sup>1</sup>See Applications Information section for operation with  $V_{BB} < 7\text{ V}$ . For  $V_{BB} > 24\text{ V}$ , thermal constraints limit regulator current.

<sup>2</sup>For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

<sup>3</sup>When  $V_{ENBAT}$  exceeds  $V_{BB}$  it is clamped with a diode. ( $V_{ENBAT} - V_{BB}$ )  $\leq 1.2\text{ V}$  at 40 mA.

<sup>4</sup>Defined as the maximum current level allowed during excessive load condition.

<sup>5</sup>See Applications Information section for calculations. Values guaranteed by design, and depend on capacitor tolerances.

## THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Thermal Resistance, Junction to Pad	$R_{\theta JP}$		2	$^{\circ}\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	34	$^{\circ}\text{C/W}$
		2-layer PCB with 2 in. <sup>2</sup> copper both sides	44	$^{\circ}\text{C/W}$
Maximum Allowable Power Dissipation	$P_D$	$R_{\theta JA} = 44\text{ }^{\circ}\text{C/W}$ (estimated), 2-layer PCB with 2.0 in. <sup>2</sup> of 2 oz. copper, $T_A = 125^{\circ}\text{C}$	0.57	W
		$R_{\theta JA} = 44\text{ }^{\circ}\text{C/W}$ (estimated), 2-layer PCB with 2.0 in. <sup>2</sup> of 2 oz. copper, $T_A = 85^{\circ}\text{C}$	1.48	W

\*Additional thermal data available on the Allegro Web site.

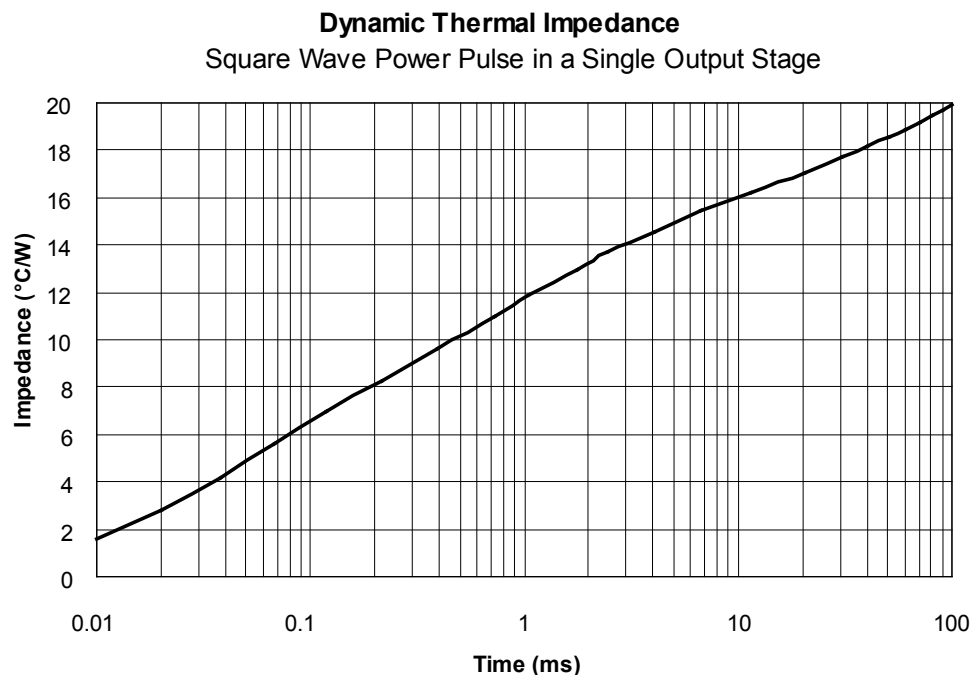


Figure 1. Dynamic thermal impedance of an individual output stage during active clamp of an inductive load (mounted on a 4-layer PCB based on JEDEC standard).

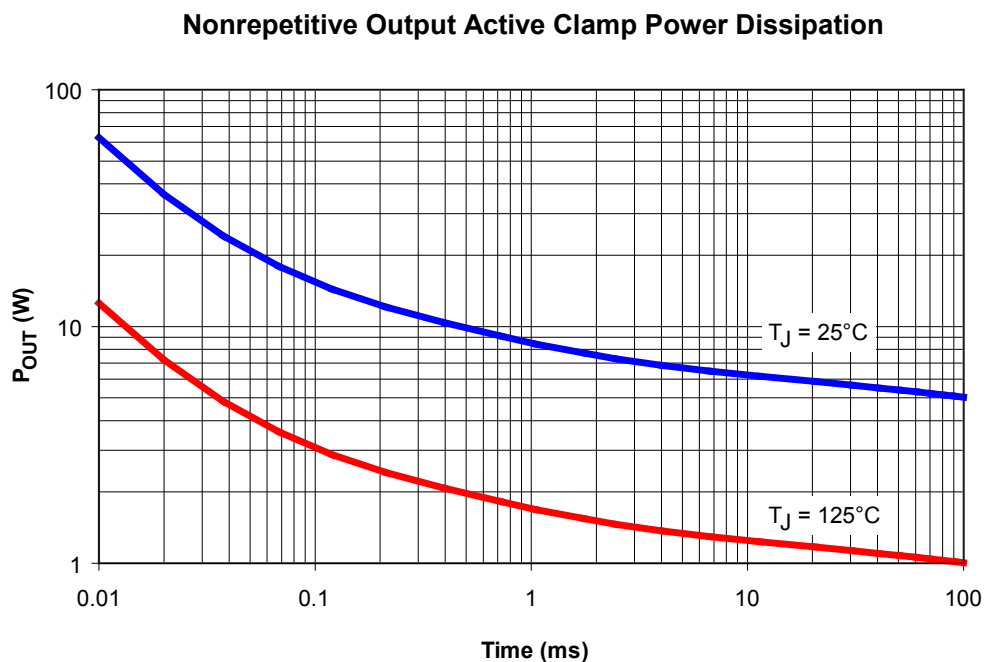


Figure 2. Peak power dissipation curves for nonrepetitive clamped outputs. Output voltage is clamped during turn-off of inductive loads while current decays.

## Functional Description

## Pin Descriptions

**EN** Enable pin; logical OR with ENBAT. This logic-level input enables the A2550. If there are no faults, the regulator is live and outputs can be switched. When both the EN and ENBAT pins are held low, the A2550 enters Sleep mode.

**ENBAT** Enable pin; logical OR with EN. Same as EN, except that this pin is high-voltage protected, and specified up to  $V_{BB}$  so it can be tied to the battery or power source. Not to exceed  $V_{BB}$  because the ESD structure places a diode between the ENBAT and VBB pins.

**WDI** Watchdog Input. Monitors the microcontroller to detect when it stops functioning. This pin is connected to an edge trigger. To avoid a fault, the latter must be triggered before CWD times-out. When not used, WDI is defeated by tying it to NPOR and shorting CWD.

**CWD** Watchdog timer capacitor terminal. Used with WDI. A current source charges the external capacitor tied to this pin. A reverse current source discharges the capacitor when either WDI transitions or the high Trip Voltage,  $V_{TRIP(H)}$ , is reached (see specification table for values). The charge-up time defines the maximum period allowed WDI to toggle before a fault is issued; the charge-down time defines the width of NPOR pulses issued to wake-up the microcontroller.

**NPOR** NOT Power On Reset. This active-low pin indicates a fault. Except for watchdog faults, NPOR is held low during the fault state. Refer to the Fault Logic table to determine

which faults are latched. Watchdog faults generate a train of pulses to “wake up” the microcontroller.

**CPOR** Power-On Reset timer capacitor terminal. Whenever VREG5 first charges up (at start-up or when a fault is cleared) a “fault” condition remains in effect until the onboard current source drives CPOR to the high Trip Voltage,  $V_{TRIP(H)}$ . This allows external circuits, such as a microcontroller, to be initialized before activating the outputs. CPOR is defeated by pulling it high to VREG5 with a 50 k $\Omega$  resistor.

**INx** Input pin. Active-high CMOS input. Internally tied to 200 k $\Omega$  pull-down resistors.

**OUTx** Output pin. Open drain DMOS. Clamps to a voltage greater than  $V_{BB}$  when an inductive load is switched off. Includes current mirror for overcurrent protection.

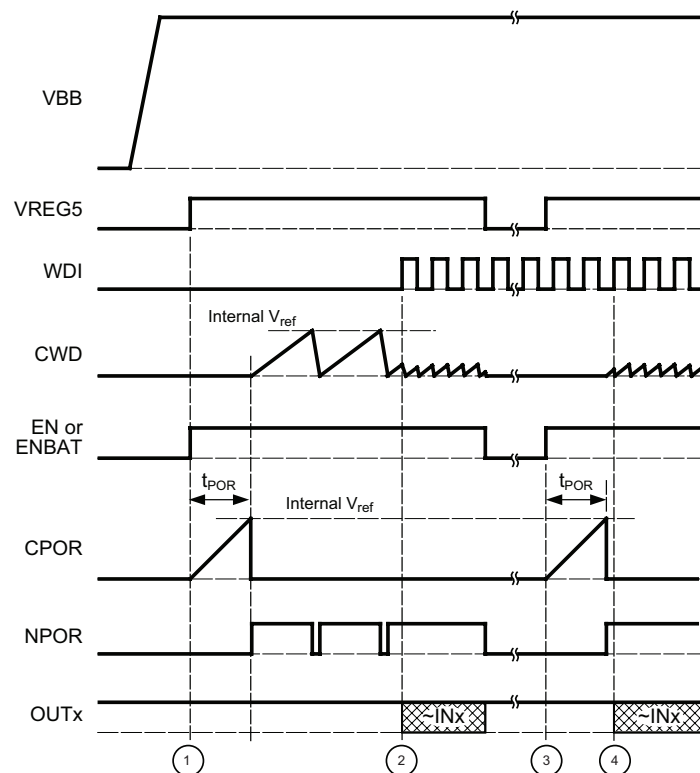
**VBB** Power pin, or “battery.” Specified for automotive voltages.

**VREG5** 5 V Regulator output. Clamped at the Current Limit Level ( $I_{REG5Lim}$ ) for excessive loads. As load resistance decreases, VREG5 is pulled below the UVLO level. In that case, a fault is generated (NPOR low).

**LGND** Logic Ground. The reference pin for the logic circuits. Must be connected to PGND externally.

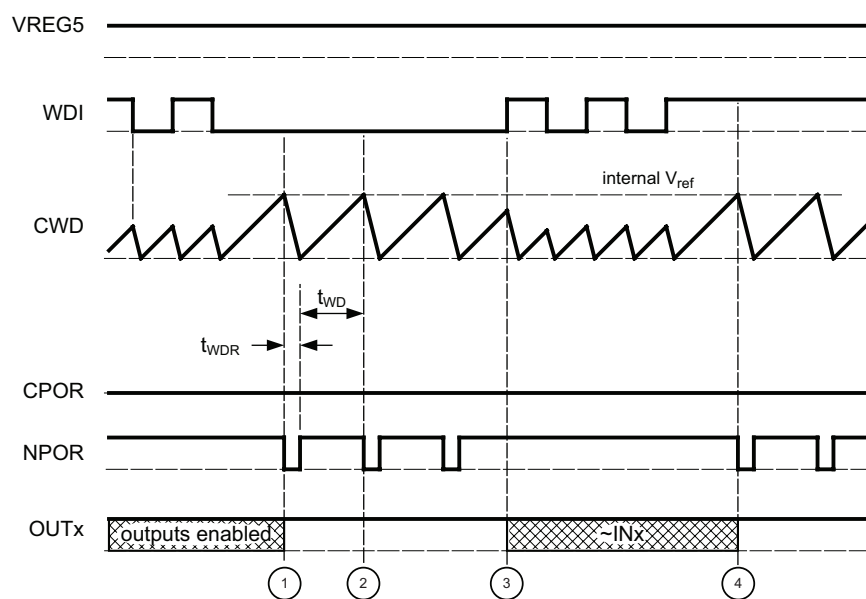
**PGND** Power Ground. The reference pin for the outputs (OUTx). Must be connected to LGND externally.

Timing Diagram: Initial Start-up and Exiting Sleep Mode



1. 5 V signal to wake up microcontroller.
2. OUTx enabled with first watchdog pulse.
3. Power ramp-up sequence with watchdog active.
4. NPOR inactive, but outputs not enabled until watchdog detected.

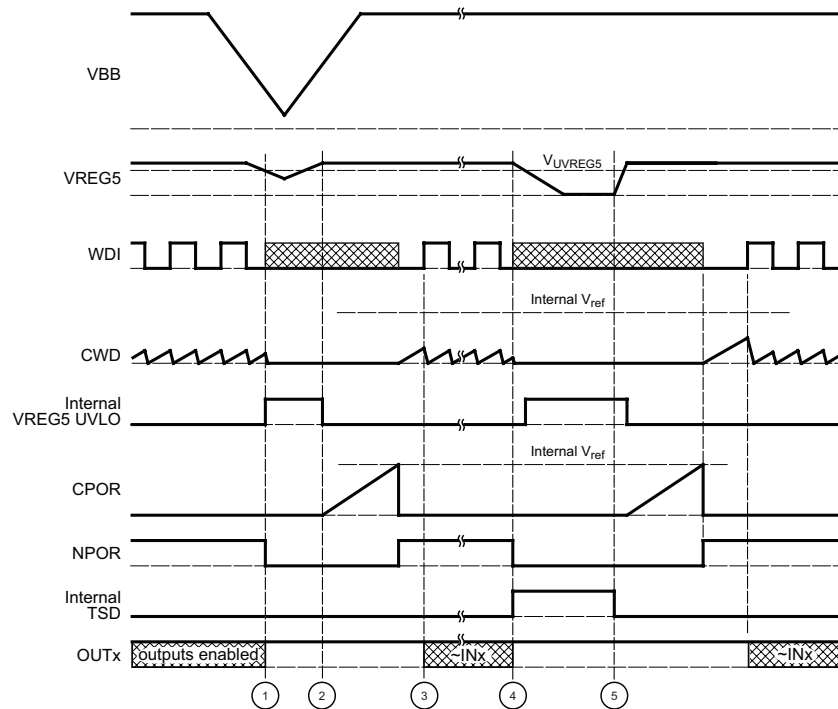
Timing Diagram: Watchdog Monitoring



1. Missing watchdog detected (WDI low).
2. NPOR pulses generated periodically.
3. NPOR inactive, but outputs not enabled until watchdog detected.
4. Missing watchdog detected (WDI low, steps 2 and 3 repeat).



Timing Diagram: VREG5 UVLO and TSD Monitoring



1. VREG5 undervoltage detected.
2. VREG5 recovers, and after it rises above  $V_{UVREG5} + V_{UVREG5(Hys)}$ , UVLO flag is deactivated and CPOR recharges.
3. NPOR inactive, but outputs not enabled until watchdog detected.
4. TSD event detected and NPOR is activated. When  $V_{REG5} \leq V_{UVREG5}$ , VREG5 shuts down.
5. TSD flag deactivated (VREG5 allowed to rise; steps 2 and 3 repeat)

## Applications Information

## Dropout Voltage

For operation with  $V_{BB}$  below the specified range of operating voltages, use the Pass Transistor On-Resistance  $R_{REG5}$  to determine the maximum allowed regulator current,  $I_{REG5(max)}$ . This current is limited by the difference between  $V_{BB}$  and  $V_{REG5}$ , according to the following equation:

$$I_{REG5} < \frac{V_{BB} - V_{REG5}}{R_{REG5}} \quad (1)$$

Figure 3 shows the results of this condition combined with the rated regulator current, in normal operation.

Note that, although the regulator is specified for normal operation with  $V_{BB}$  well above normal automotive voltages, in general thermal constraints will limit maximum operational  $V_{BB}$ .

## Fault Logic

The A2550 offers several protection and fault detection features. The operation of thermal shutdown, watchdog monitoring of the microcontroller, and regulated voltage undervoltage lockout are described in the Timing Diagrams section. The fault logic is described in table 1.

## NPOR

The following faults generate a RESET state:

- watchdog alarm
- VREG5 falls below the UVLO level

In addition, the following conditions cause a low NPOR signal *if* the NPOR pin is pulled up by VREG5 (because these conditions disable VREG5):

- overtemperature (Thermal Shut Down)
- no ENABLE signal ( $EN = ENBAT = 0$ )



Figure 3. Current Capability of the 5 V Regulator (VREG5)

Table 1. Fault Logic<sup>a</sup>

Inputs					Outputs				Mode of Operation
EN OR ENBAT <sup>b</sup>	TSD	UVLO	Watchdog alarm	OCx	Internal 5V	VREG5	NPOR	OUTx	
1	0	0	0	0	1	1	1	INx	Normal Operation: OUTx active for INx active.
1	0	0	0	1	1	1	1	Z	OCx disables OUTx only. OUTx latched OFF until INx removed and reapplied.
1	0	0	1	X	1	1	Pulse	Z	NPOR periodically pulses to attempt RESET of microcontroller.
1	0	1	X	X	1	1	0	Z	NPOR remains active after UVLO recovers until POR delay expires.
1	1	X	X	X	1	0	0	Z	
0	X	X	X	X	0	0	Off	Z	Sleep mode. NPOR = 0 when pulled up by VREG5 because VREG5 = 0.

<sup>a</sup>X indicates "don't care," Z indicates high impedance.

<sup>b</sup>This entry is a logical OR of the EN and ENBAT pins.

## Applications Information

NPOR is pulsed for a watchdog fault. For the remaining faults, NPOR is held low for the duration of the fault. After the fault condition is removed, NPOR remains low during the  $t_{\text{POR}}$  period. The latter is set by the value of the external capacitor fed by a current source at the CPOR pin, according to the following formula:

$$t_{\text{POR}} = \left( 200 \frac{\text{ms}}{\mu\text{F}} \right) \times C_{\text{POR}} \quad (2)$$

The scaling factor is simply derived from the specifications using the typical value of  $I_{\text{POR}}$ :

$$\frac{t_{\text{POR}}}{C_{\text{POR}}} = \frac{V_{\text{REF}} - V_{\text{TRIP(L)}}}{I_{\text{POR}}} \quad (3)$$

**Watchdog**

The watchdog monitors the microcontroller to detect if it locks up. To do so, the watchdog checks for pulses on the Watchdog Input pin (WDI), and if they are absent for longer than the timeout period,  $t_{\text{WD}}$ , the watchdog activates NPOR, which pulses periodically.  $t_{\text{WD}}$  is proportional to the external capacitor fed by a current source at the CWD pin. The voltage change is 1 V, so using the typical value of  $I_{\text{CWD}}$ (charging) we have:

$$t_{\text{WD}} = \left( 200 \frac{\text{ms}}{\mu\text{F}} \right) \times C_{\text{WD}} \quad (4)$$

The pulse width for NPOR active,  $t_{\text{WDR}}$ , also scales proportionally to the value of the external capacitor at the CWD pin. Using the typical value of  $I_{\text{CWD}}$ (discharging) we have:

$$t_{\text{WDR}} = \left( 14 \frac{\text{ms}}{\mu\text{F}} \right) \times C_{\text{WD}} \quad (5)$$

See the specification tables for tolerances.

When not used, disable watchdog by tying WDI to NPOR and tying CWD low. Table 2 shows watchdog timing for the nominal capacitances listed.

**Table 2. Timing Set by Capacitors**

C ( $\mu\text{F}$ )	$t_{\text{POR}}$ (ms)	$t_{\text{WD}}$ (ms)	$t_{\text{WDR}}$ (ms)
0.1	20	20	1
0.22	44	44	3
0.47	94	94	7
1	200	200	14

**Output Overcurrent**

When the OC (overcurrent) protection is triggered in a driver, that driver is disabled for self-protection. No other functions are affected; NPOR and VREG5 operate normally. A disabled output driver remains shut down until the respective INx is brought low, then high again; at which time OUTx turns on. OUTx will switch on again the next time INx is applied. If a short-to-battery still exists, the overcurrent will trip each time INx is reapplied.

**Sleep**

The A2550 is put to sleep by holding both EN and ENBAT low. In sleep mode all functions are shut down, including VREG5. If the VREG5 regulator is required at all times, disable sleep mode by tying ENBAT to VBB.

**Power Limits**

Power dissipation,  $P_D$ , is limited by thermal constraints. The maximum allowed power dissipation,  $P_{D(\text{max})}$ , is found from the formula:

$$T_J = (P_{D(\text{max})} \times R_{\theta JA} + T_A) \leq T_{J(\text{max})} \quad (6)$$

The maximum junction temperature,  $T_{J(\text{max})}$ , and the thermal resistance,  $R_{\theta JA}$ , are given in the specification tables.

The three main contributors to power dissipation are:

- $P_{\text{BIAS}}$  from the supply bias current
- $P_{\text{REG}}$  from the linear regulator voltage drop
- $P_{\text{LS}}$  from low-side driver conduction

For example, to determine if  $T_J$  is in an acceptable range, given:

$R_{\theta JA} = 55^\circ\text{C/W}$ , and

$T_A = 125^\circ\text{C}$ ; and

$$P_{\text{BIAS}} = V_{\text{BB}} \times I_{\text{BBQ}} \quad (7)$$

$$= 14 \text{ V} \times 3 \text{ mA} = 42 \text{ mW}, \text{ and}$$

$$P_{\text{REG}} = (V_{\text{BB}} - V_{\text{REG5(min)}}) \times I_{\text{REG5}} \quad (8)$$

$$= (14 \text{ V} - 4.9 \text{ V}) \times 20 \text{ mA} = 182 \text{ mW}, \text{ and}$$

$$P_{LS} = (R_{DS(on)} \times I_{LS1}^2) + (R_{DS(on)} \times I_{LS2}^2) + (R_{DS(on)} \times I_{LS3}^2) \quad (9)$$

Because  $I_{LS1} = I_{LS2} = I_{LS3} = 110 \text{ mA}$ , and given that  $R_{DS(on)} = 5 \Omega$ , then

$$P_{LS} = 3 (5 \Omega) \times (110 \text{ mA})^2 = 182 \text{ mW}.$$

Given also:

$$P_D = P_{BIAS} + P_{REG} + P_{LS} = 42 \text{ mW} + 182 \text{ mW} + 182 \text{ mW} = 406 \text{ mW}.$$

$T_J$  can be calculated by substitution into equation 6:

$$T_J = 0.406 \text{ W} \times 55^\circ\text{C/W} + 125^\circ\text{C} = 147^\circ\text{C}.$$

### Reverse Battery

The low-side driver outputs can withstand reverse battery when the load ( $R_{LOADx}$ ) is connected to limit current. Power dissipation ( $P_D = P_{LS(rvrs)}$ ) is limited by thermal constraints, according to the following formula:

$$P_{LS(rvrs)} = V_{F1} \times I_{F1} + V_{F2} \times I_{F2} + V_{F3} \times I_{F3}, \quad (11)$$

where:

$$I_{Fx} = \frac{V_{BB(rvrs)} - V_{Fx}}{R_{LOADx}}. \quad (12)$$

### Active Clamp on Outputs

The driver section includes an active clamp that prevents an overvoltage when an inductive load is switched off. Zener diodes are connected at the output pins. This removes the need for external freewheeling diodes across inductive loads.

The coil current,  $I_{COIL}$ , is quenched by allowing the output pin voltage,  $V_{OUTx}$ , to exceed the battery voltage at the load,  $V_{dc}$ . This applies a negative voltage drop across the load. Therefore the current gradient is driven negative, as shown in the following formula:

$$\frac{dI_{COIL}}{dt} = \frac{V_{dc} - V_{OUT} - I_{COIL} \times R_{COIL}}{L_{COIL}} < 0. \quad (13)$$

The output voltage is clamped to protect the driver. The active clamp works as follows. The voltage at the driver output is pushed high by the inductive current. Once the clamp voltage,  $V_{CL}$ , is reached, a Zener diode conducts current to the internal FET gate driver block. Therefore, the FET turns partially on, in order to limit any further increase in voltage at the output pin. The output is then held at this clamp voltage until the current decays to zero, as shown in figure 4.

Energy loss in the chip,  $E$ , may be calculated as follows. Load coil resistance,  $R_{COIL}$ , is usually a significant value, but a worst case scenario takes  $R_{COIL} = 0$  for simplicity. With active clamping at  $V_{CL}$ , the output current (with initial value  $I_{OUT0}$ ) is driven low and the upper limit on energy loss in the driver is calculated as:

$$E_{max} = \frac{1}{2} I_{OUT0} V_{CL} \Delta t. \quad (14)$$

From figure 4:

$$\Delta t = \frac{L_{COIL} I_{OUT0}}{V_{CL} - V_{dc}}, \quad (15)$$

and

$$E_{max} = \frac{1}{2} L_{COIL} I_{OUT0}^2 (1 - V_{dc}/V_{CL})^{-1}. \quad (16)$$

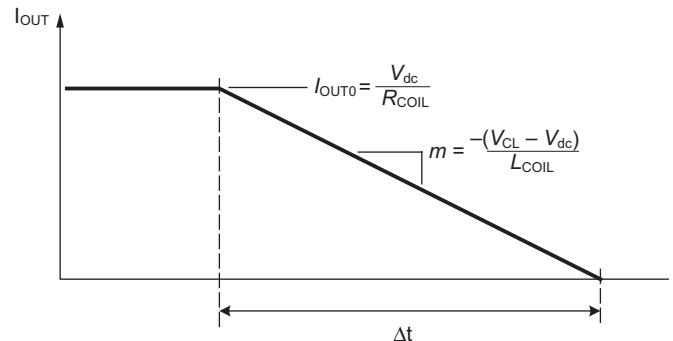


Figure 4. Output Voltage Clamping

A more rigorous derivation, including  $R_{\text{COIL}}$  during the exponential current decay results in:

$$i(t) = \frac{V_{\text{dc}}}{R_{\text{COIL}}} - \frac{V_{\text{CL}}}{R_{\text{COIL}}} \left[ 1 - \exp\left(-t \frac{R_{\text{COIL}}}{L_{\text{COIL}}}\right) \right], \quad (17)$$

and

$$\Delta t = \frac{L_{\text{COIL}}}{R_{\text{COIL}}} \ln(1 - V_{\text{dc}}/V_{\text{CL}})^{-1}. \quad (18)$$

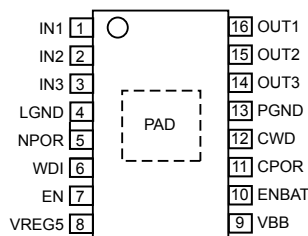
Energy loss in the driver is:

$$E = \frac{V_{\text{CL}} V_{\text{DC}} L_{\text{COIL}}}{R_{\text{COIL}}^2} [1 + (V_{\text{CL}}/V_{\text{dc}} - 1) \ln(1 - V_{\text{dc}}/V_{\text{CL}})]. \quad (19)$$

### Capacitive Loads

When capacitive loads are applied to the outputs, the constraint described below applies. Such is the case, for example, when capacitors are attached to the outputs to protect against ESD. Larger capacitors protect against larger ESD voltages. However, the upper limit on capacitance is determined by the blanking time. The latter allows for spurious current spikes and capacitor discharges to be completed before the overcurrent detection circuit senses the output current (see  $t_{\text{BLANK}}$  in the Electrical Characteristics table). The blanking time allows a 47 nF capacitor with 20% tolerance and nominal 12 V automotive voltages.

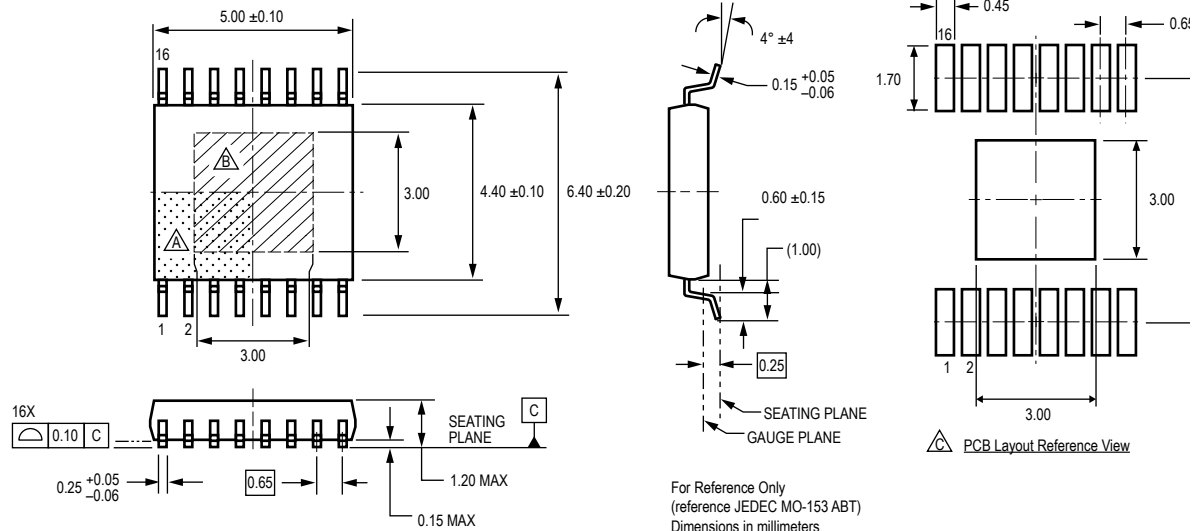
### Pin-out Diagram



Terminal List Table

No.	Name	Description
1	IN1	Activate driver 1
2	IN2	Activate driver 2
3	IN3	Activate driver 3
4	LGND	Logic ground; must be connected to PGND externally
5	NPOR	Not Power-On Reset
6	WDI	WatchDog Input
7	EN	Enable (low voltage)
8	VREG5	5V regulator
9	VBB	Supply voltage
10	ENBAT	Enable (high voltage)
11	CPOR	Capacitor terminal for Power-On Reset cycle time
12	CWD	Capacitor terminal for WatchDog timing
13	PGND	Power ground; must be connected to LGND externally
14	OUT3	Low side driver 3
15	OUT2	Low side driver 2
16	OUT1	Low side driver 1
–	PAD	Exposed pad for enhanced thermal performance

## 16-Pin TSSOP (Suffix LP) with Exposed Pad



For Reference Only  
(reference JEDEC MO-153 ABT)  
Dimensions in millimeters  
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

△ Terminal #1 mark area

△ Exposed thermal pad (bottom surface)

△ Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);  
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary  
to meet application process requirements and PCB layout tolerances; when  
mounting on a multilayer PCB, thermal vias at the exposed thermal pad land  
can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

### Revision History

Number	Date	Description
5	April 3, 2019	Minor editorial updates

Copyright 2019, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:  
[www.allegromicro.com](http://www.allegromicro.com)