

November 1988 Revised November 1999

# 74AC157 • 74ACT157 Quad 2-Input Multiplexer

### **General Description**

The AC/ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The AC/ACT157 can also be used as a function generator.

#### **Features**

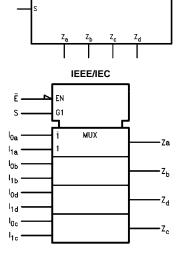
- $\blacksquare$   $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Outputs source/sink 24 mA
- ACT157 has TTL-compatible inputs

# **Ordering Code:**

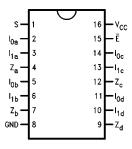
Order Number	Package Number	Package Description
74AC157SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74AC157SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC157MTC	MTC16	16 -Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC157PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT157SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT157SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT157MTC	MTC16	16 -Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT157PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

# **Logic Symbols**



# **Connection Diagram**



# **Pin Descriptions**

Pin Names	Description				
I <sub>0a</sub> –I <sub>0d</sub>	Source 0 Data Inputs				
I <sub>1a</sub> –I <sub>1d</sub>	Source 1 Data Inputs				
Ē	Enable Input				
S	Select Input				
Z <sub>a</sub> –Z <sub>d</sub>	Outputs				

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DS009929

# **Functional Description**

The AC/ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input  $(\overline{E})$  is active-LOW. When  $\overline{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The AC/ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{split} Z_a &= \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \\ Z_b &= \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S}) \\ Z_c &= \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \\ Z_d &= \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S}) \end{split}$$

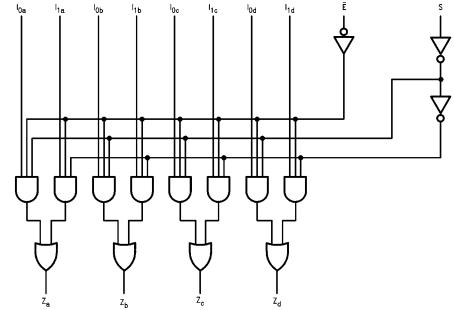
A common use of the AC/ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The AC/ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

## **Truth Table**

	Outputs			
E	S	I <sub>0</sub>	I <sub>1</sub>	Z
Н	Х	Х	Х	L
L	Н	Χ	L	L
L	Н	Χ	Н	Н
L	L	L	Χ	L
L	L	Н	X	Н

H = HIGH Voltage Level

# **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

L = LOW Voltage Level X = Immaterial

## **Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ ) -0.5V to +7.0V

DC Input Diode Current (I<sub>IK</sub>)

 $\begin{array}{ccc} \text{V}_{\text{I}} = -0.5 \text{V} & -20 \text{ mA} \\ \text{V}_{\text{I}} = \text{V}_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \\ \text{DC Input Voltage (V}_{\text{I}}) & -0.5 \text{V to V}_{\text{CC}} + 0.5 \text{V} \end{array}$ 

DC Output Diode Current (I<sub>OK</sub>)

 $V_{O} = -0.5V$  -20 mA  $V_{O} = V_{CC} + 0.5V$  +20 mA

DC Output Voltage ( $V_O$ ) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Source

or Sink Current (I<sub>O</sub>) ±50 mA

DC V<sub>CC</sub> or Ground Current

per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA Storage Temperature ( $T_{STG}$ )  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

Junction Temperature (T<sub>J</sub>)

PDIP 140°C

# Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>)

 $\begin{array}{ccc} AC & 2.0 V \text{ to } 6.0 V \\ ACT & 4.5 V \text{ to } 5.5 V \\ Input Voltage (V_I) & 0 V \text{ to } V_{CC} \\ Output Voltage (V_O) & 0 V \text{ to } V_{CC} \end{array}$ 

Operating Temperature ( $T_A$ )  $-40^{\circ}C$  to  $+85^{\circ}C$ 

Minimum Input Edge Rate (ΔV/Δt)

AC Devices

 $V_{\mbox{\scriptsize IN}}$  from 30% to 70% of  $V_{\mbox{\scriptsize CC}}$ 

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ( $\Delta V/\Delta t$ )

**ACT Devices** 

 $V_{\text{IN}}$  from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

#### **DC Electrical Characteristics for AC**

Symbol	Parameter	V <sub>CC</sub>	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
Symbol		(V)	Тур	Gu	aranteed Limits	Ullits	Conditions	
V <sub>IH</sub>	Minimum HIGH Level	3.0	1.5	2.1	2.1		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	3.15	3.15	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level	3.0	1.5	0.9	0.9		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	1.35	1.35	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level	3.0	2.99	2.9	2.9			
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		2.56	2.46		$I_{OH} = -12 \text{ mA}$	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 2)}$	
V <sub>OL</sub>	Maximum LOW Level	3.0	0.002	0.1	0.1			
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		0.36	0.44		I <sub>OL</sub> = 12 mA	
		4.5		0.36	0.44	V	I <sub>OL</sub> = 24 mA	
		5.5		0.36	0.44		I <sub>OL</sub> = 24 mA (Note 2)	
I <sub>IN</sub>	Maximum Input	5.5		±0.1	±1.0	μА	$V_1 = V_{CC}$ , GND	
(Note 4)	Leakage Current	3.3		±0.1	11.0	μΛ	VI = VCC, GIVD	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current (Note 3)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent	5.5		4.0	40.0	μА	$V_{IN} = V_{CC}$	
(Note 4)	Supply Current	3.3		4.0	40.0	μΛ	or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4:  $I_{\text{IN}}$  and  $I_{\text{CC}} @ 3.0 \text{V}$  are guaranteed to be less than or equal to the respective limit @ 5.5 V  $V_{\text{CC}}$ .

# 74AC157 • 74ACT157

#### **DC Characteristics for ACT** $T_A = +25^{\circ}C$ $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $v_{cc}$ Units Conditions Symbol (V) **Guaranteed Limits** Тур Minimum HIGH Level 4.5 1.5 2.0 $\overline{V_{OUT}} = 0.1V$ 5.5 1.5 2.0 or $V_{CC} - 0.1V$ $V_{\mathsf{IL}}$ Maximum LOW Level 4.5 1.5 8.0 0.8 $V_{OUT} = 0.1V$ ٧ Input Voltage 5.5 1.5 0.8 0.8 or $V_{CC} - 0.1 V$ Minimum HIGH Level 4.5 4.49 4.4 $V_{OH}$ 4.4 $I_{OUT} = -50~\mu\text{A}$ Output Voltage 5.5 5.49 5.4 5.4 $V_{IN} = V_{IL}$ or $V_{IH}$ 4.5 3.86 3.76 V $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 5)}$ 5.5 4.86 4.76 $V_{OL}$ Maximum LOW Level 4.5 0.1 0.1 $I_{OUT} = 50 \; \mu A$ Output Voltage 0.1 0.1 $V_{IN} = V_{IL}$ or $V_{IH}$ 4.5 0.44 ٧ $I_{OL} = 24 \text{ mA}$ 0.36 5.5 0.36 $I_{OL} = 24 \text{ mA (Note 5)}$ 0.44 Maximum Input $I_{IN}$ 5.5 ±0.1 ±1.0 $V_I = V_{CC}$ , GND μΑ Leakage Current I<sub>CCT</sub> Maximum 5.5 0.6 1.5 $V_I = V_{CC} - 2.1 V \,$ mΑ I<sub>CC</sub>/Input $\overline{V_{OLD}} = 1.65V \text{ Max}$ 75 Minimum Dynamic 5.5 mΑ $I_{\text{OLD}}$ V<sub>OHD</sub> = 3.85V Min Output Current (Note 6) 5.5 -75 $I_{OHD}$ mΑ Maximum Quiescent $V_{IN} = V_{CC}$ Icc 4.0 40.0 or GND Supply Current

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

#### **AC Electrical Characteristics for AC**

		V <sub>CC</sub>		$T_A = +25^{\circ}C$		T <sub>A</sub> = -40°	C to +85°C	
Symbol	Parameter	(V)	C <sub>L</sub> = 50 pF			$C_L = 50 \text{ pF}$		Units
		(Note 7)	Min	Тур	Max	Min	Max	•
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	7.0	11.5	1.5	13.0	ns
	S to Z <sub>n</sub>	5.0	1.5	5.5	9.0	1.5	10.0	115
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	6.5	11.0	1.5	12.0	ns
	S to Z <sub>n</sub>	5.0	1.5	5.0	8.5	1.0	9.5	
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	7.0	11.5	1.5	13.0	ns
	Ē to Z <sub>n</sub>	5.0	1.5	5.5	9.0	1.5	10.0	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	6.5	11.0	1.5	12.0	
	Ē to Z <sub>n</sub>	5.0	1.5	5.5	9.0	1.0	9.5	ns
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	5.0	8.5	1.0	9.0	ns
	$I_n$ to $Z_n$	5.0	1.5	4.0	6.5	1.0	7.0	115
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	5.0	8.0	1.0	9.0	ns
	$I_n$ to $Z_n$	5.0	1.5	4.0	6.5	1.0	7.0	113

Note 7: Voltage Range 3.3 is  $3.3V \pm 0.3V$ Voltage Range 5.0 is  $5.0V \pm 0.5V$ 

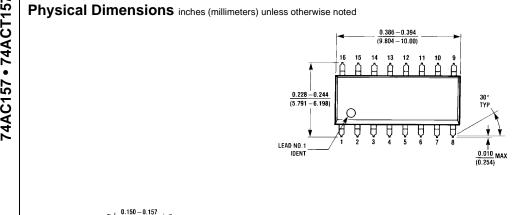
# **AC Electrical Characteristics for ACT**

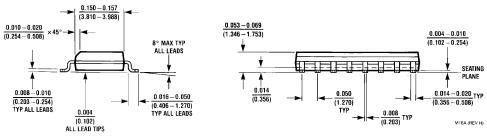
		V <sub>CC</sub>	$V_{CC}$ $T_A = +25^{\circ}C$			$T_A = -40^{\circ}C$ to $+85^{\circ}C$		
Symbol	Parameter	(V)	C <sub>L</sub> = 50 pF			C <sub>L</sub> = 50 pF		Units
		(Note 8)	Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	5.0	2.0	5.5	9.0	1.5	10.0	ns
	S to Z <sub>n</sub>	3.0		5.5	3.0			115
t <sub>PHL</sub>	Propagation Delay	5.0	2.0	5.5	9.5	2.0	10.5	ns
	S to Z <sub>n</sub>	3.0						
t <sub>PLH</sub>	Propagation Delay	5.0	1.5	6.0	10.0	1.5	11.5	ns
	E to Z <sub>n</sub>	5.0						
t <sub>PHL</sub>	Propagation Delay	5.0	1.5 5.0		0 8.5	1.0	9.0	ns
	E to Z <sub>n</sub>	5.0		5.0				
t <sub>PLH</sub>	Propagation Delay	5.0	1.5	4.0	7.0	1.0	8.5	ns
	I <sub>n</sub> to Z <sub>n</sub>	5.0			7.0			
t <sub>PHL</sub>	Propagation Delay	5.0	1.5	4.5	7.5	1.0	8.5	ns
	$I_n$ to $Z_n$	3.0	1.5	4.5			0.5	

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

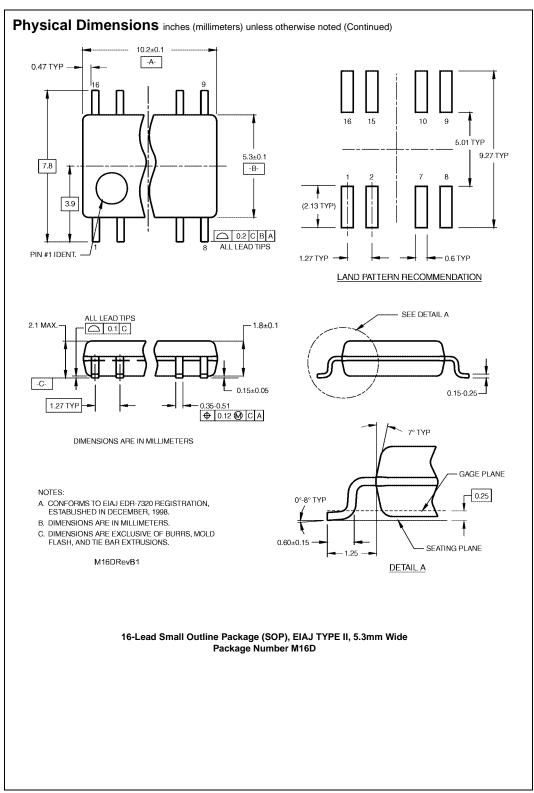
# Capacitance

Symbol	Parameter	Тур	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	50.0	pF	V <sub>CC</sub> = 5.0V

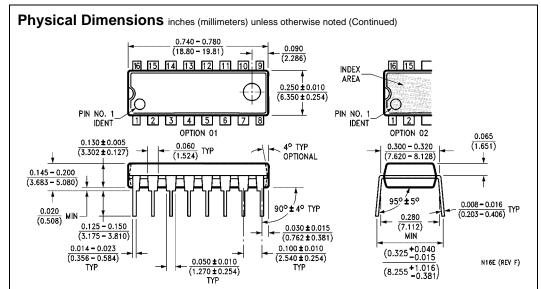




16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body Package Number M16A



# Physical Dimensions inches (millimeters) unless otherwise noted (Continued) DIMENSIONS METRIC ONLY 0.42 TYP LAND PATTERN RECOMMENDATION GAGE PLANE 6.4 0.25 4.4 ± 0.1 -B-3.2 SEATING PLANE 0.6 ± 0.1 DETAIL A TYPICAL, SCALE: 40X △ 0.2 C B A ALL LEAD TIPS SEE DETAIL A PIN #1 IDENT. (0.90) △ 0.1 C 0.09-0.20 TYP 0.10 ± 0.05 TYP 0.19 - 0.30 TYP 0.13 M B (S) c (S) Α MTC16 (REV C) 16- Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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