

ORDER NUMBER(S):**USB3280-AEZG FOR 36-PIN, QFN PACKAGE (LEAD-FREE ROHS COMPLIANT)****USB3280-AEZG-TR FOR 36-PIN, QFN LEAD-FREE ROHS COMPLIANT (TAPE AND REEL)**

Reel Size is 3000 pieces.



80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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General Description

The USB3280 provides the Physical Layer (PHY) interface to a USB 2.0 Device Controller. The IC is available in a 36-pin lead-free RoHS compliant QFN package.

The USB3280 is an industrial temperature USB 2.0 physical layer transceiver (PHY) integrated circuit. SMSC's proprietary technology results in low power dissipation, which is ideal for building a bus powered USB 2.0 peripheral. The PHY uses an 8-bit bidirectional parallel interface, which complies with the USB Transceiver Macrocell Interface (UTMI) specification. It supports 480Mbps transfer rate, while remaining backward compatible with USB 1.1 legacy protocol at 12Mbps.

All required termination and 5.25V short circuit protection of the DP/DM lines are internal to the chip. The USB3280 also has an integrated 1.8V regulator so that only a 3.3V supply is required.

While transmitting data, the PHY serializes data and generates SYNC and EOP fields. It also performs needed bit stuffing and NRZI encoding. Likewise, while receiving data, the PHY de-serializes incoming data, stripping SYNC and EOP fields and performs bit un-stuffing and NRZI decoding.

Block Diagram

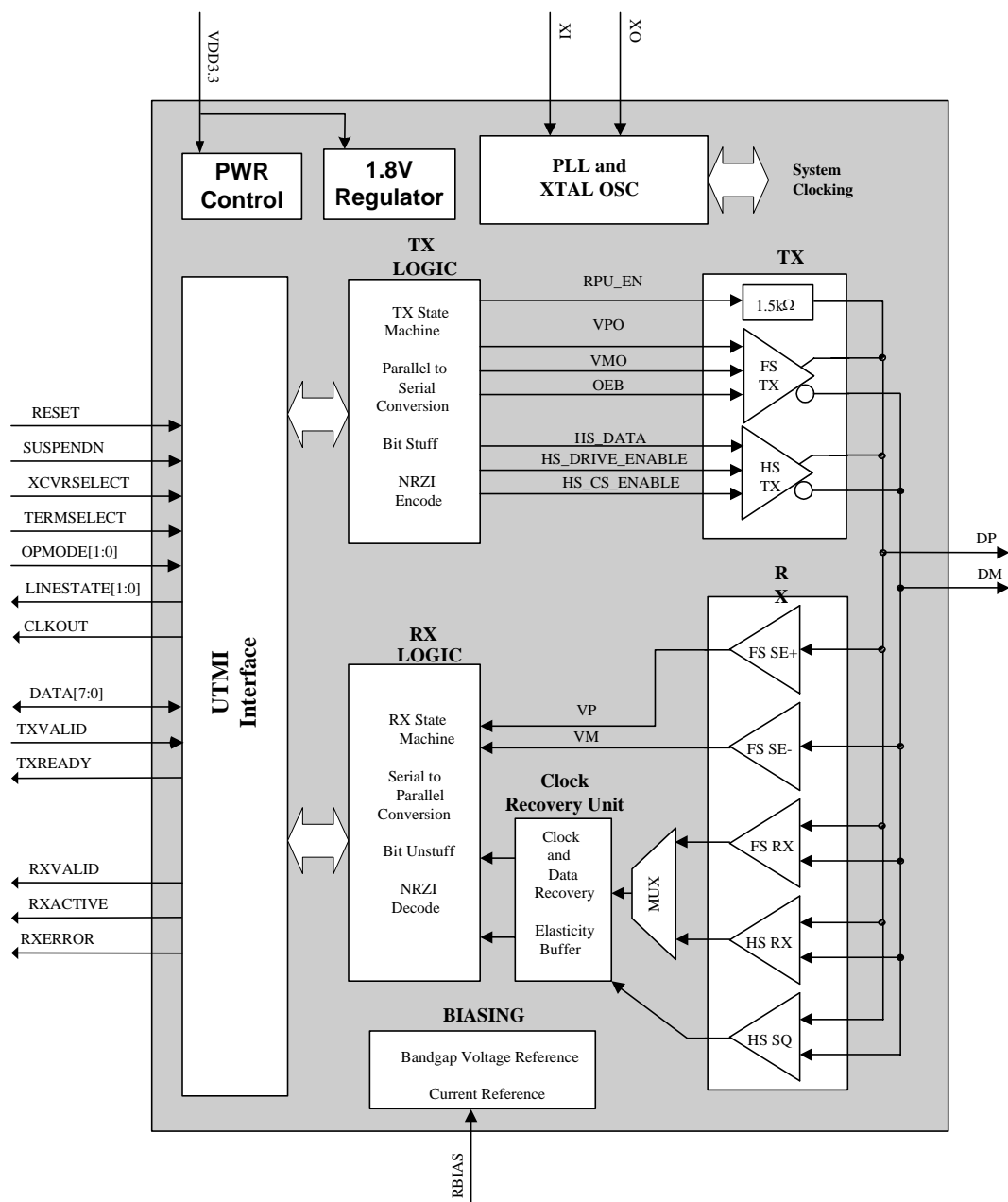


Figure 1 USB3280 Block Diagram

Package Outline

Revision 1.5 (11-15-07)

SMSC USB3280

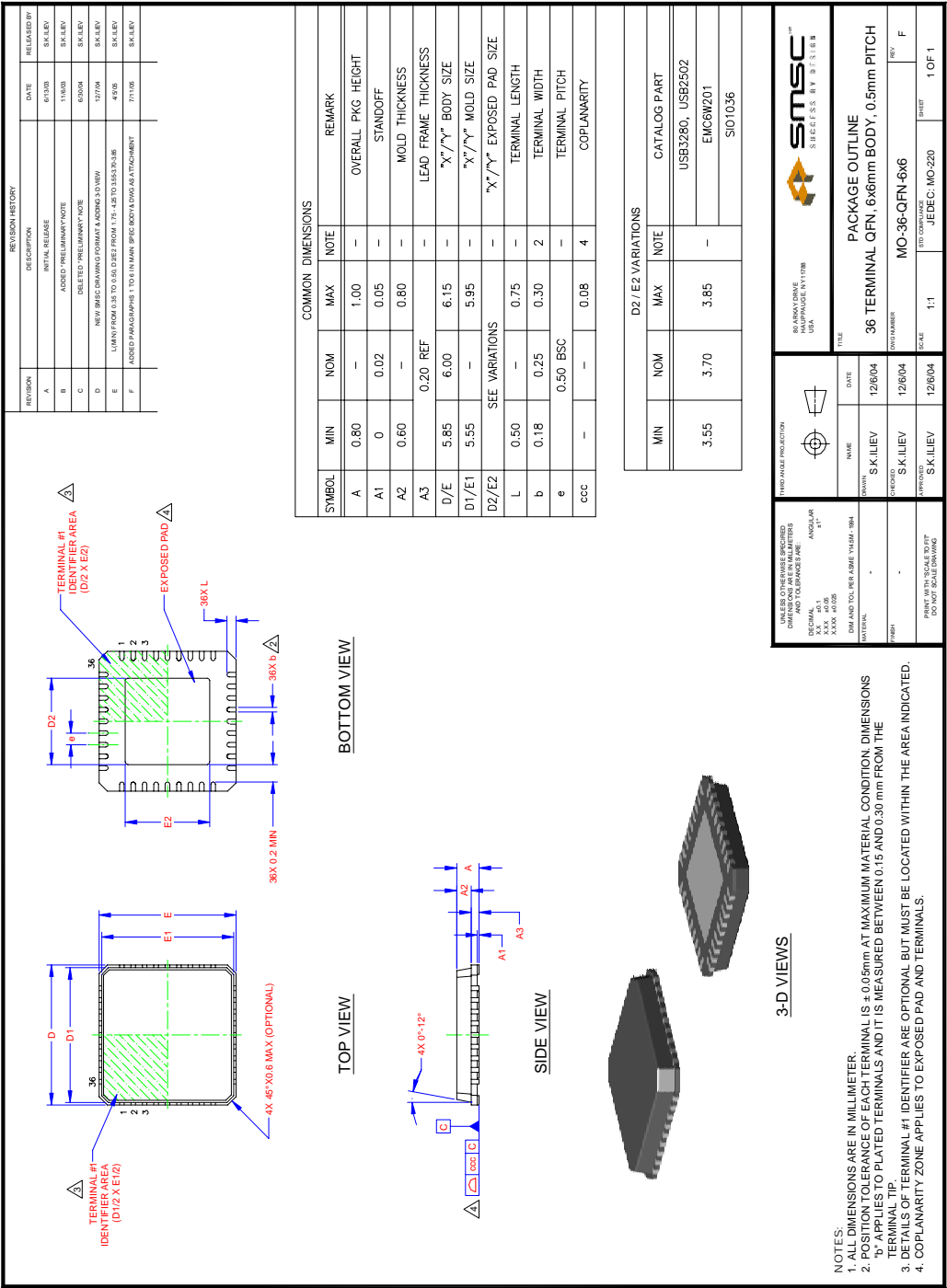


Figure 2 USB3280-AEZG 36-Pin QFN Package Outline and Parameters, 6 x 6 x 0.90 mm Body (Lead-Free RoHS Compliant)