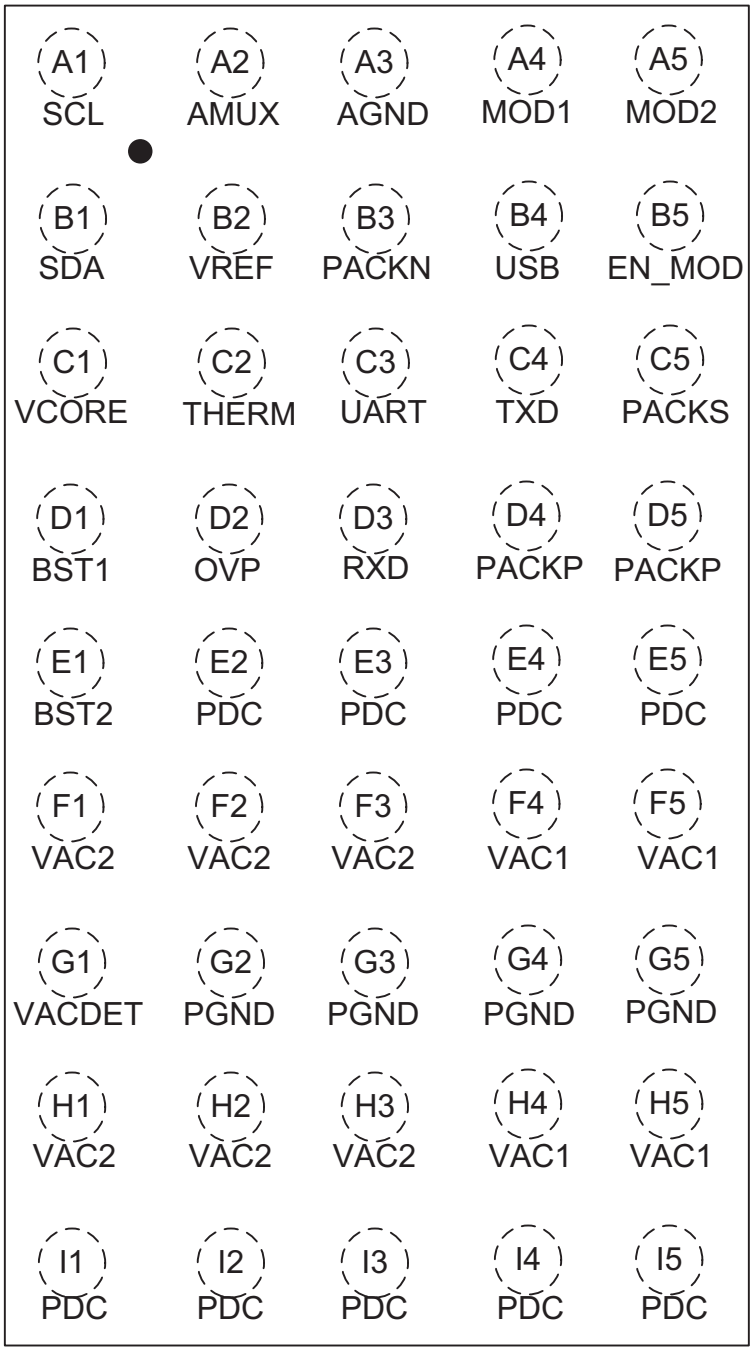
Pinout (WCSP)

(Top View)

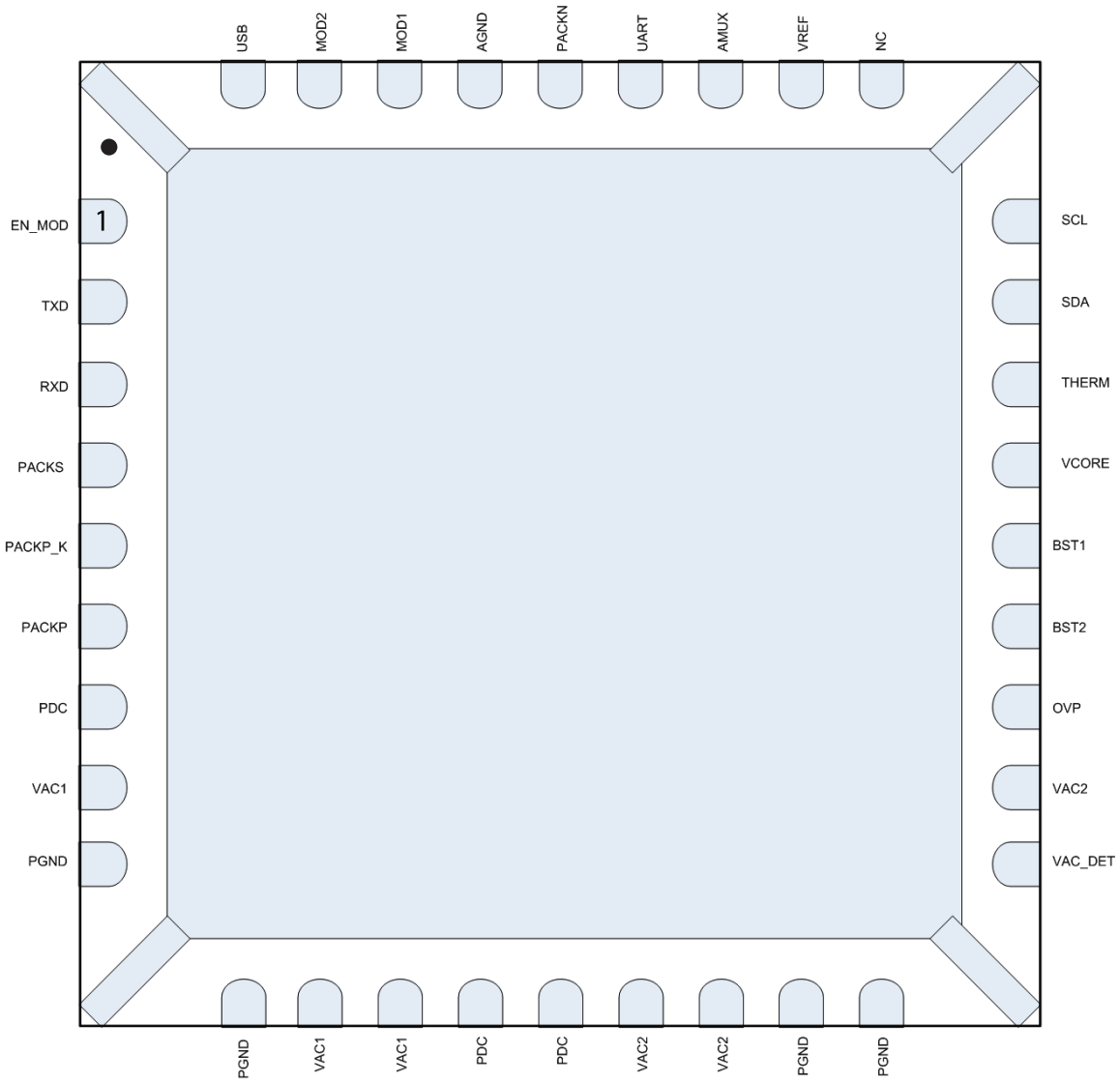


Pin Description (WCSP)

Pin #	Pin Name	Pin Function	Description
A1	SCL	I2C Clock	I2C clock
A2	AMUX	Analog Sense	Analog MUX output
A3	AGND	Analog Ground	Quiet ground connection
A4	MOD1	MOD cap connection	Pulldown for capacitive modulation
A5	MOD2	MOD cap connection	Pulldown for capacitive modulation
B1	SDA	I2C Data	I2C data
B2	VREF	Vref Output	ADC reference output
B3	PACKN	PACKN Sense	Battery negative terminal
B4	USB	USB Supply	USB supply and detection input
B5	EN_MOD	Enable Modulation	Enables modulation switches
C1	VCORE	VCORE LDO	LDO output
C2	THERM	Thermistor Drive	Thermistor drive
C3	UART	UART Bus	UART bus
C4	TXD	UART TX	UART Tx
C5	PACKS	Output Current Sense	Sense node for output current
D1	BST1	BST cap	Boost capacitor connection for HS FETs
D2	OVP	OV Clamp	Overvoltage pulldown clamp
D3	RXD	UART RX	UART Rx
D4, D5	PACKP	Battery Connection	Battery positive terminal
E1	BST2	BST cap	Boost capacitor connection for HS FETs
E2-5	PDC	Input power	Rectified input signal
F1-F3	VAC2	Coil input	AC power input from coil
F4, F5	VAC1	Coil input	AC power input from coil
G1	VACDET	VAC Detect	Indicates incoming power to external micro
G2-5	PGND	Power gnd	GND for synchronous rectifier and charging path
H1-H3	VAC2	Coil input	AC power input from coil
H4, H5	VAC1	Coil input	AC power input from coil
I1-5	PDC	Rectified voltage	Filter capacitor connection for rectified voltage

Pinout (QFN)

(Top View)



Pin Description (QFN)

Pin #	Pin Name	Pin Function	Description
1	EN_MOD	Enable Modulation	Enables modulation switches
2	TXD	UART TX	UART Tx
3	RXD	UART RX	UART Rx
4	PACKS	Output Current Sense	Sense node for output current
5	PACKP_K	PACKP Kelvin	PACKP Kelvin
6	PACKP	Battery Connection	Battery positive terminal
7, 13-14	PDC	Rectified voltage	Filter capacitor connection for rectified voltage
8, 11-12	VAC1	Coil input	AC power input from coil
9-10, 17-18	PGND	Power gnd	GND for synchronous rectifier and charging path
15-16, 20	VAC2	Coil input	AC power input from coil
19	VAC_DET	VAC Detect	Indicates incoming power to external micro
21	OVP	OV Clamp	Overvoltage pulldown clamp
22	BST2	BST cap	Boost capacitor connection for HS FETs
23	BST1	BST cap	Boost capacitor connection for HS FETs
24	VCORE	VCORE LDO	LDO output
25	THERM	Thermistor Drive	Thermistor drive
26	SDA	I2C Data	I2C data
27	SCL	I2C Clock	I2C clock
28	NC	No Connect	No Connect
29	VREF	Vref Output	ADC reference output
30	AMUX	Analog Sense	Analog MUX output
31	UART	UART Bus	UART bus
32	PACKN	PACKN Sense	Battery negative terminal
33	AGND	Analog Ground	Quiet ground connection
34	MOD1	MOD cap connection	Pulldown for capacitive modulation
35	MOD2	MOD cap connection	Pulldown for capacitive modulation
36	USB	USB Supply	USB supply and detection input

Functional Block Diagram

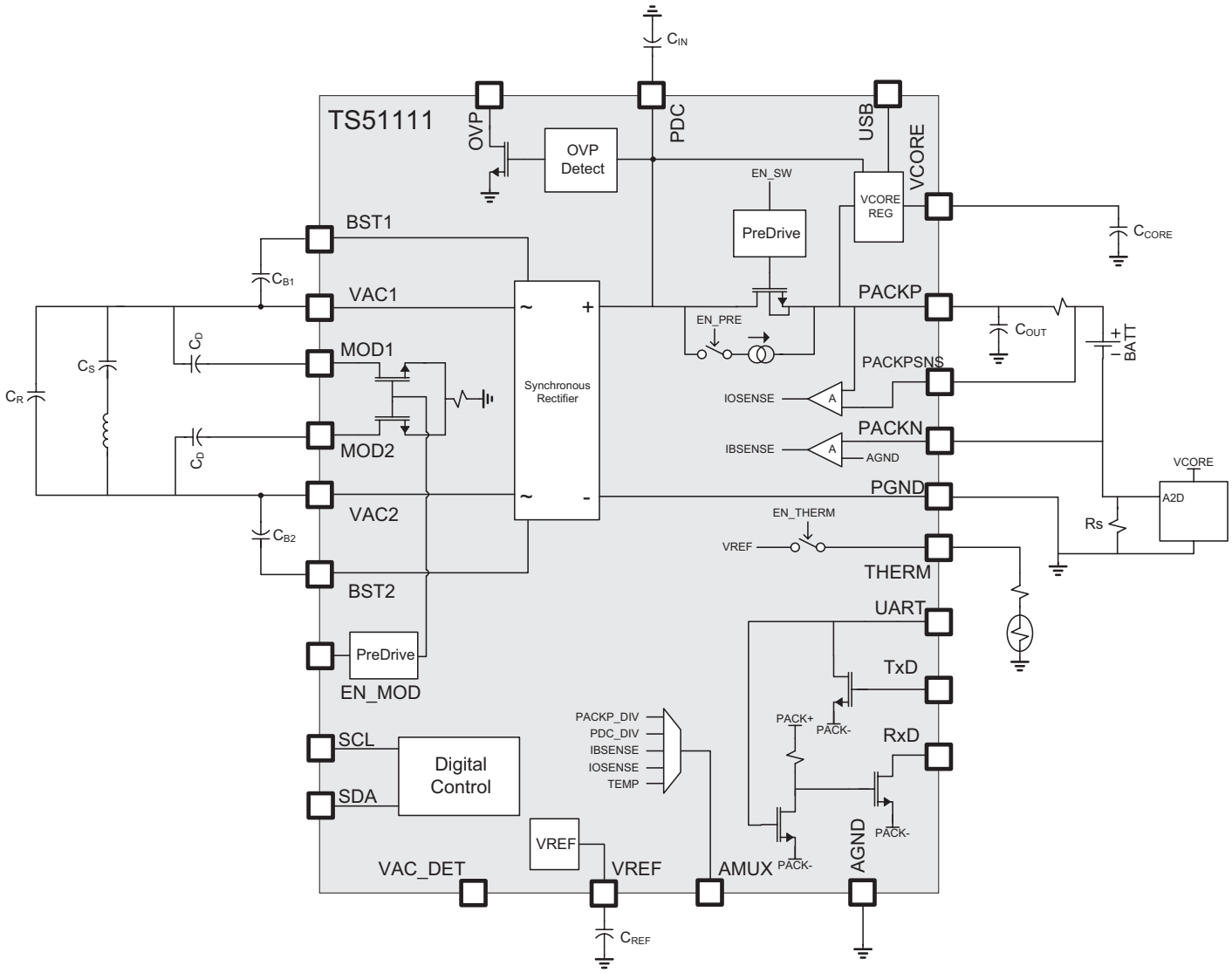


Figure 1: TS51111 Block Diagram

Absolute Maximum Rating

Over operating free–air temperature range unless otherwise noted[1, 2, 3]

Parameter	Value	Unit
VAC1, VAC2, PDC, MOD1, MOD2, OVP	-0.3 to 22	V
BST1, BST2	-0.3 to (VAC + 5.5)	V
VCORE, TX, RX, UART, PACKP, SCL, SDA, VAC_DET, VREF, AMUX, VCORE, USB	-0.3 to 5.5	V
Operating Junction Temperature Range, TJ	-40 to 125	°C
Storage Temperature Range, TSTG	-65 to 150	°C
Electrostatic Discharge – Human Body Model	±2k	V
Electrostatic Discharge – Machine Model	+/-200	V
Lead Temperature (soldering, 10 seconds)	260	°C

Notes:

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VAC_{PP}	Input Operating Voltage			20	V
F_{VAC}	Input Operating Frequency	100		210	kHz
PACKP	Battery input when externally driven	2.5		5.5	V
L_{IN}	Inductor (measured on charging mat)		14*		uH
C_R	Parallel resonant capacitor		1.8*		nF
C_S	Series resonant capacitor		183*		nF
C_O	Modulation capacitors		22		nF
C_{OUT}	Output capacitor	0.8	1		uF
C_{CORE}	LDO decoupling capacitor	8	10		uF
C_{B1}, C_{B2}	Rectifier boost capacitors	200	220	240	nF
C_{IN}	Synchronous rectifier / PDC decoupling capacitor	10	20		uF
C_{AMUX}	Analog mux decoupling capacitor	1	2		nF
C_{REF}	VREF decoupling capacitor	80	100	120	nF
T_A	Operating Free Air Temperature	-40		85	°C
T_J	Operating Junction Temperature	-40		125	°C

* Exact values of the resonant capacitors and inductor will depend on the specific system configuration.

Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	36QFN Thermal Resistance Junction to Air (Note 1)	32	°C/W

Note 1: Assumes 3.917 x 3.917 in2 area of 1 oz copper, 4 layer PCB, 4 thermal vias under PAD, and 25°C ambient temperature.

Characteristics

Electrical Characteristics, T_J = -40C to 85C, PDC = PACKP = 4.2V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_Q						
$I_{Q,Standby,LPM}$	Quiescent Current in Low Power Mode	Current from PACKP, ILDO = 0, EN_VREF = EN_SW = EN_PRE = 0		20	30	uA
$I_{Q,Disable}$	Quiescent Current in Disable (Direct Charge, Low Power Mode disabled)	Current from PACKP, ILDO = 0, EN_VREF = EN_SW = EN_PRE = 0		2		uA
UVLO						
$V_{UVLO-PACK\_P}$	PACKP UVLO	PACKP Rising		2.1		V
$HYST_{UVLO-PACK\_P}$	PACKP UVLO Hysteresis			400		mV
PDC-PACKP Pass Device						
T_{SW-ON}	Delay from EN_SW to switch ON			200		us
T_{SW-OFF}	Delay from EN_SW to switch OFF			100		ns
$I_{PRECHARGE}$	Precharge Current	Relative to set point T = 25C; PDC = 3.5V; PACKP = 2.7V	I_{NOM} -20%	I_{NOM}	I_{NOM} +20%	
$TC_{PRECHARGE}$	Precharge Current Temperature Coefficient	25C to 85C		-0.3		%/C
I_{LIMIT}	Current Limit	At 3.2 A setting	2.2	3.2		A
UART						
T_{RX}	Delay from UART to RX			0.7		us
T_{TX}	Delay from TX to UART			0.6		us
$V_{T,UART}$	UART threshold			0.8		V
$V_{T,TX}$	TX threshold			0.8		V
$R_{dson,RX}$	RX Switch Resistance			10		Ω
SDA / SCl / EN_MOD Digital Inputs						
V_{IH}	VCORE = 1.5V	Voltage Rising		0.875		V
V_{IL}	VCORE = 1.5V	Voltage Falling		0.465		V
V_{IH}	VCORE = 1.8V	Voltage Rising		1.01		V
V_{IL}	VCORE = 1.8V	Voltage Falling		0.525		V
V_{IH}	VCORE = 2.5V	Voltage Rising		1.25		V
V_{IL}	VCORE = 2.5V	Voltage Falling		0.665		V
V_{IH}	VCORE = 3.3V	Voltage Rising		1.47		V
V_{IL}	VCORE = 3.3V	Voltage Falling		0.825		V
R_{IN}	Pin input impedance	Resistance to GND		1M		Ω

Electrical Characteristics, T_j = -40C to 85C, PDC = PACKP = 4.2V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VAC Detect						
V_{OH}	Output high voltage	Totem-pole configuration only. 100uA load.		VCORE-100mV		V
V_{OL}	Output low voltage	Totem-pole or open-drain configurations. 100uA load.		100		mV
I_{OFF}	Output leakage	Output leakage in open-drain off-state.			0.1	uA
R_{dson,VAC_DETECT}	Switch Resistance	Output resistance to GND in open-drain on-state.		10		Ω
VREF						
CVREF	VREF decoupling capacitor		80	100	120	nF
VVREF	VREF voltage	T = 0 to 85 C, IOUT 0mA to 2mA	1.988	2.0	2.012	V
RPDC-DIV	PDC_DIV ratio	T = 0 to 85 C, PDC_DIV_SEL = 0	0.048	0.05	0.052	V/V
		T = 0 to 85 C, PDC_DIV_SEL = 1	0.198	0.2	0.202	V/V
RPACKP-DIV	PACKP_DIV ratio	T = 0 to 85 C	0.198	0.2	0.202	V/V
RUSB-DIV	USB_DIV ratio	T = 0 to 85 C	0.198	0.2	0.202	V/V
RTHERM-DIV	THERM_DIV ratio	T = 0 to 85 C	0.495	0.5	0.505	V/V
IQ,VREF	VREF quiescent current	PACKP current if VREF enabled		300		uA
TEN-VREF	VREF enable time	Delay from EN_VREF to VREF available		3.2		us
MOD						
T_{MOD-ON}	EN_MOD to switches ON delay			3		us
$T_{MOD-OFF}$	EN_MOD to switches OFF delay			0.7		us
$I_{Q,MOD}$	MOD block quiescent current	Current from PACKP when MOD switches closed. EN_MOD hi. EN_VREF = EN_SE = EN_PRE = lo		100		uA
$R_{dson,MOD}$	MOD Switch Resistance	MOD1 to MOD2		3		Ω
Low Power LDO						
$VCORE_{NOM}$	VCORE voltage	PACKP = 4.2V		3.3		V
$V_{Dropout}$	Dropout voltage	PACKP = 2.3V, IVCORE=1mA			100	mV
I_{out}	Output current	PACKP=4.2V, VCORE = 0.9*$VCORE_{NOM}$		10	50	mA
C_{CORE}	LDO Decoupling Capacitor		0.8	1	1.2	uF
OVP						
VOVP	OVP Threshold			21		V
Rdson,OVP	OVP Switch Resistance			2		Ω

Electrical Characteristics, T_J = -40C to 85C, PDC = PACKP = 4.2V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Temperature Sensing						
$T_{SHUTDOWN}$	Over-temperature shutdown threshold	Temperature rising		170		C
T_{HYST}	Over-temperature shutdown hysteresis			10		C
V_{TSENSE}	Temperature Sensor Voltage	25C	0.725	.75	0.775	V
TCV_{TSENSE}	Temperature Coefficient	0C to 85C		2.4		mV/C
Current Sensing						
IBSENSE GAIN	Battery current sense amp gain	PACKN - AGND 10mV to 20mV; Gain setting = 20	19.6	20	20.4	V/V
IOSENSE GAIN	Output current sense amp gain	PACKP - PACKS 10mV to 20mV Gain setting = 20; PACKP = 5V	19.6	20	20.4	V/V
IBSENSE V_{OFFSET}	Battery current sense amp offset	PACKN - AGND = 20mV; Gain setting = 20; 25C	-0.5	0	0.5	mV
IOSENSE V_{OFFSET}	Output current sense amp offset	PACKP - PACKS = 20mV Gain = 20; PACKP = 5V; 25C	-0.5	0	0.5	mV
$V_{IB,MAX}$	Full range amp output			750		mV
$V_{IO,MAX}$	Full range amp output			750		mV
VAC Detect						
V_{OH}	Output high voltage	Totem-pole configuration only. 100uA load.		VCORE-100mV		V
V_{OL}	Output low voltage	Totem-pole or open-drain configurations. 100uA load.		100		mV
I_{OFF}	Output leakage	Output leakage in open-drain off-state.			0.1	uA
R_{dson,VAC_DETECT}	Switch Resistance	Output resistance to GND in open-drain on-state.		10		Ω

Functional Description

Synchronous Rectifier

The bridge rectifier in the TS51111 has a synchronous controller which shunts the forward bias of the bridge diodes. This allows the TS51111 to provide currents of up to 3.2A to be efficiently transferred without significant power dissipation. The primary side of the bridge can stand-off up to 20V. On the secondary side, a capacitive load on the PDC pin can be used to help attenuate the voltage signal observed on both sides of the bridge rectifier. External boost capacitors CB1 and CB2 allow use of efficient high side nmos switches.

The rectifier is disabled by default and will remain in an asynchronous mode until incoming power is detected or EN_SW or EN_PRE are asserted. In asynchronous mode, the bridge FETs will not switch and voltage rectification will occur through the parasitic diodes of the FETs. In this mode, current draw in the IC is minimal.

The bridge can be forced into asynchronous (no FET switching) or half synchronous (LS FET only switching) operation at any time using the CNFG register using the ASYNC or HSYNC bits respectively. This can be used to improve efficiency at light loads where the switching losses of the bridge would exceed the conduction losses of the parasitic diodes.

Load Switch / Blocking FET

The integrated low impedance blocking switch provides a direct charging path to the battery and disconnects the output from the rectified signal until the system has been successfully configured. Control of the switch is achieved through the I2C interface. An integrated charge pump guarantees maximum drive strength is available for the FET when operated as a switch. When hard switched, gate drive is slewed slowly to limit inrush current from the PDC cap to the battery.

The load switch can be reconfigured to operate as a linear regulator (see Charge Termination section below). When enabled, the output will soft-start to limit inrush current. In linear regulation mode, the PDC voltage must be regulated close to the dropout voltage to limit power dissipation in the IC.

In linear regulation mode, a configurable, integrated current limit circuit provides fault protection to the system. At the maximum setting, current limit is disabled. If the output current hits the current limit threshold, the device will automatically limit the output current and set the FAULT register ILIM bit. In this condition, the PDC voltage will build up and must be managed through the system loop by reducing the transmitted power. If the transmitted power is not reduced, the TS51111 power dissipation will increase and eventually force a thermal shutdown of the part. Current limit in direct charge mode is not integrated but can be easily implemented by monitoring device output current using the integrated current sense amplifiers.

ILIMSET<3:0>	Current Limit Typical (mA)
0000	350
0001	600
0010	850
0011	1100
0100	1350
0101	1600
0110	1850
0111	2100
1000	2350
1001	2600
1010	2850
1011	3100
1100	3350
1101	3600
1110	3850
1111	Disable ILIM

Precharge

In low battery conditions, an integrated precharge current source can be used to slowly charge the battery with a controlled DC current source. The precharge current source is controlled using the I2C interface. The precharge current has a negative temperature coefficient to mitigate temperature rise of the TS51111 during pre-charge. The level of the Precharge current can be set according to the table below.

PRESET<2:0>	Precharge Current (mA)
000	30
001	40
010	50
011	60
100	70
101	80
110	90
111	100

Low Power Mode

The TS51111 supports a low-power mode when connected directly to a battery. In this mode, the ultra-low quiescent current LDO output is enabled to power an external microcontroller and the power consumption of the rest of the IC is minimized. In this mode, the TS51111 still supports UART level translation to the microcontroller. The part will automatically switch to normal operation when incoming power is detected.

Current Sense Amps

Two current sense amplifiers are included to allow for accurate battery charge current and received current measurements. The IBSENSE amplifier provides an output that is proportional to the sense voltage on the PACKN pin when a sense resistor is placed between PACKN and ground. The IOSENSE amplifier will measure the differential voltage across the sense resistor placed in series with the output current. This measurement is an indicator of the power received by the TS51111. The IOSENSE output is not valid when the device is in current limit. The system should check the FAULT register periodically to ensure the device is in a proper operating state without any faults. Both amplifiers have a configurable gain set by the ISET register. The gains are configurable from 10x to 80x.

USB

The TS51111 will automatically detect the presence of a voltage applied to the USB pin. If the USBCTRL bit is set low and a voltage is applied to the USB pin, the part will respond by disabling all charging paths to the battery and switching the LDO power input from the battery to the USB. If the USBCTRL bit is set hi, the part will not automatically disable charging or switch the LDO power input. The USBCTRL bit is programmed in Non-Volatile Memory (NVM) during manufacturing and is not user configurable. In either condition, the USBDET bit in the FAULT register will be set. When USB power is removed, the part will return to normal operation.

LDO

The TS51111 LDO supports a variety of system configurations. An on-chip ultra-low Iq LDO is provided for powering external system components when a battery or USB supply is available. The LDO is designed to operating with minimum quiescent but can still deliver high output current at low dropout voltage. Integrated current limit provides additional protection.

If an external USB power supply is available, the LDO will draw its input power from the USB pin instead of from the battery. In the event that neither an external USB supply nor an external battery is available, the LDO will automatically power-up of the rectified voltage when incoming power is detected and provide power to an external microcontroller.

To support multiple possible external microcontrollers, the internal LDO has a configurable output voltage. The voltage is set according to the following table. The LDOSET<1:0> bits are programmed in Non-Volatile Memory (NVM) during manufacturing and are not user configurable.

LDOSET<1:0>	VCORE (V)
00	1.5
01	1.8
10	2.5
11	3.3 (default)

VAC Detect

The presence of incoming power on the coils will be indicated by the TS51111 by asserting the VAC_DET output pin. The pin will be de-asserted when incoming power is removed. The VAC_DETECT output can be configured as open-drain with an external resistor pull-up or as a totem pole with a VCORE high level. This is set using the VAC_CNFG bit with hi for open-drain and low for totem-pole.

UART

UART level translators are included to facilitate communication between system components. The level shifters will translate voltage levels from VCORE for the system microprocessor to PACKP for a separate system.

VREF

An internal high-accuracy VREF circuit provides a precision reference for external analog-to-digital converters. Integrated voltage dividers provide sense voltages for external ADC measurement. The VREF circuit is enabled using the EN_VREF bit and will not draw any current when not active.

OVP

An on-board over-voltage sensor on the PDC signal is available if additional external over-voltage protection is needed. In an over-voltage condition, the OVP FET is active to provide a low impedance path to ground on the OVP pin. In addition, the OVP FET can be forced on using the register bit. This can be used to provide an additional load on PDC if required. In an OVP condition, the OVP bit of the FAULT register will be set hi.

Temperature Sensing

The die temperature of the TS51111 is measured using an onboard temperature sensor. The output of the temperature sensor is available on the AMUX pin.

If the temperature of the TS51111 exceeds the TSD threshold, all high current operations will be disabled until the die temperature reaches a safe level. Temperature hysteresis prevents rapid entering and exiting of the over-temperature state. In thermal shutdown, the load switch, precharge current, and synchronous rectifier are disabled. All other functions including OVP and MOD will still be available. When the TSD threshold is hit, the TSD bit in the FAULT register will be set.

Charge Termination

To allow for accurate charge termination in a charging application, the TS51111 load switch can be reconfigured to operate as a voltage regulator. In this mode, the switch source voltage will be regulated to the voltage set by the VOUTSET<6:0> bits. The switch is put into this mode by asserting the EN_TOP bit of the configuration register. Available voltage settings and the corresponding codes are shown. To support indirect charge applications, the EN_TOP and IND_SET bits must both be set hi. The output voltage will still be determined by the VOUTSET<6:0> bits. The VOUT setpoints are 3.0V to 5.54V in 20mV steps. In addition, VOUTSET<6:0>=0x64 will select a 5.0V setpoint.

AMUX

To reduce the number of connections required between the microprocessor and the TS51111, all analog outputs from the TS51111 are measured from the same analog pin and selectable via the AMUX register. Signals on the AMUX pin are buffered using an internal unity gain amplifier. When unselected, the AMUX pin will be high impedance.

AMUX<2:0>	Analog Signal
000	----
001	PDC_DIV
010	IOSENSE
011	IBSENSE
100	TEMP
101	PACKP_DIV
110	USB_DIV
111	THERM_DIV

Thermistor Driver

An integrated thermistor driver allows system temperature measurement. When enabled, the thermistor drive will drive the VREF voltage onto the THERM pin. When disabled, the THERM pin will be high impedance to allow external drive of the same thermistor. In the automatic mode, the thermistor driver is enabled whenever battery charging is enabled. This is whenever EN_SW or EN_PRE are active. The voltage on the THERM pin can be measured using the internal voltage divider and will be visible on the AMUX pin.

TCTRL<1:0>	Thermistor Operation
00	Disable
01	Enable
10	Auto
11	

Control Registers

REG	R/W	Description	
LSON	R/W	Forces on both LS FETs when hi. Allows normal synchronous rectifier operation when lo.	
VAC_CONFIG	R/W	Configures VAC_DET output pin behavior. Totem pole configuration when hi. Open-drain configuration when lo.	
HSYNC	R/W	Forces half-synchronous rectifier operation (LS FET only switching) when lo. Allows synchronous rectifier operation when hi. (ASYNC has priority when lo)	
ASYNC	R/W	Disables synchronous rectifier operation when lo. Allows synchronous rectifier operation when hi. (Has priority over HSYNC when lo)	
EN_VREF	R/W	Enables VREF reference for external analog-to-digital converters when hi. Disables VREF reference when lo.	
EN_TOP, EN_SW	R/W	EN_TOP = 0, EN_SW = 0	Load switch is disabled
		EN_TOP = 1, EN_SW = x	Load switch is enabled as an LDO
		EN_TOP = 0, EN_SW = 1	Load switch is enabled as a switch
EN_PRE	R/W	Enables the precharge current source when hi. Current source is disabled when lo.	
IND_SET	R/W	Configures part for indirect charge operation when hi. Configures part for topoff or direct charge operation when lo.	
PACKP_LD_EN	R/W	Enables an internal 500 Ohm resistive load on PACKP when hi. Load is disconnected when lo.	
OVP_ON	R/W	Forces the OVP FET to turn on as defined by the OVP_CS bit when hi. OVP is triggered only by high voltage on PDC when lo.	
EN_MOD	R/W	Turns on the MOD FETs when hi. Turns off the MOD FETs when lo.	
PRESET <2:0>	R/W	Sets the level of the pre-charge current	
AMUX <2:0>	R/W	Configures measurement point for AMUX pin	
PDC_DIV_SEL	R/W	Changes the ratio of the PDC divider	
ILIMSET <3:0>	R/W	Configures the indirect charging internal current limit	
TCTRL <1:0>	R/W	Configures the behavior of the Thermistor driver (THERM pin)	
DIS_VREF	R/W	Force the VREF output off	
OVP_CS	R/W	Configures the OVP FET as 30mA current source (hi) or a switch (lo)	
AMUX_10K_PLDN	R/W	Enable a 10K pull down load resistor on AMUX buffer	
VCORE_indset	R/W	Optimizes VCORE regulator for indirect charge mode.	
HI_R	R/W	Increases the Ron for HS switches in the synchronous rectifier	
IB <2:0>	R/W	Configures the gain of the IBSENSE amplifier (000=10X, 001=20X,…111=80X)	
IO <2:0>	R/W	Configures the gain of the IOSENSE amplifier (000=10X, 001=20X,…111=80X)	
VOUTSET <6:0>	R/W	Configures the VOUT voltage setting for charge termination	
PACKP_OVP	R	On-die over-voltage sensor status bit. Bit is hi during a PACKP over-voltage condition.	
OVP	R	On-die over-voltage sensor status bit. Bit is hi during a PDC over-voltage condition.	
TSD	R	On-die thermal sensor over-temperature status bit. Bit is hi during an over-temperature condition.	
USBDET	R	Status bit that indicates voltage applied to USB pin. Bit is hi when USB voltage is detected.	
ILIM	R	On-die current limit status bit. Bit is hi when current-limit is active.	

Register Map

REG	AD	R/W		B7	B6	B5	B4	B3	B2	B1	B0
CNFG	0x0	R/W	0x00		VAC_CNFG	HSYNC	ASYNC	EN_VREF	EN_TOP	EN_PRE	EN_SW
CNFG2	0x1	R/W	0x00					IND_SET	PACKP_LD_EN	OVP_ON	EN_MOD
PRESET	0x2	R/W	0x00						PRESET<2>	PRESET<1>	PRESET<0>
AMUX	0x3	R/W	0x00					PDC_DIV_SEL	AMUX<2>	AMUX<1>	AMUX<0>
	0x4	R/W	0x00					ILIMSET<3>	ILIMSET<2>	ILIMSET<1>	ILIMSET<0>
TCTRL	0x5	R/W	0x00	HI_R		VCORE_indset	AMUX_10K_PLDN	EN_OVP_CS	DIS_VREF	TCTRL<1>	TCTRL<0>
ISET	0x6	R/W	0x00			IB<2>	IB<1>	IB<0>	IO<2>	IO<1>	IO<0>
	0x7	R/W	0x00								
FAULT	0x8	R	--				PACKP_OVP	OVP	TSD	USBDET	ILIM

Device address is 0x48

I²C Interface Timing Requirements

Symbol	Parameter	Standard Mode		Fast Mode(1)		Unit
		Min	Max	Min	Max	
fscl	I²C clock frequency	0	100	0	400	kHz
tsch	I²C clock high time	4		0.6		µs
tscl	I²C clock low time	4.7		1.3		µs
tsp(2)	I²C tolerable spike time	0	50	0	50	ns
tsds	I²C serial data setup time	250		250		ns
tsdh	I²C serial data hold time	0		0		µs
ticr(2)	I²C input rise time		1000		300	ns
ticf(2)	I²C input fall time		300		300	ns
tocf(2)	I²C output fall time; 10 pF to 400 pF bus		300		300	ns
tbuf	I²C bus free time between Stop and Start	4.7		1.3		µs
tsts	I²C Start or repeated Start condition setup time	4.7		0.6		µs
tsth	I²C Start or repeated Start condition hold time	4		0.6		µs
tsps(2)	I²C Stop condition setup time	4		0.6		µs

(1) The I²C interface will operate in either standard or fast mode.
(2) Parameters not tested in production.

Application Schematic

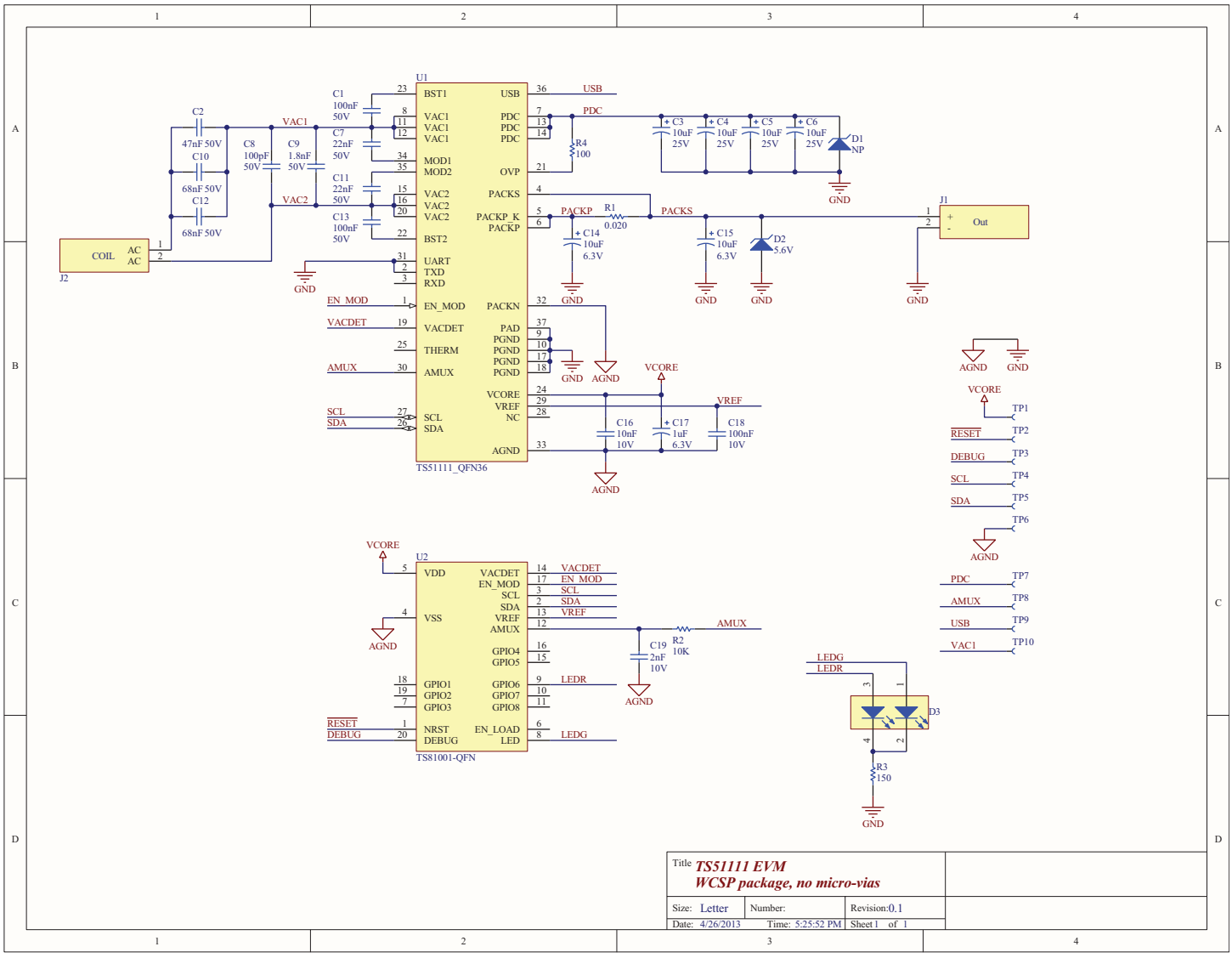
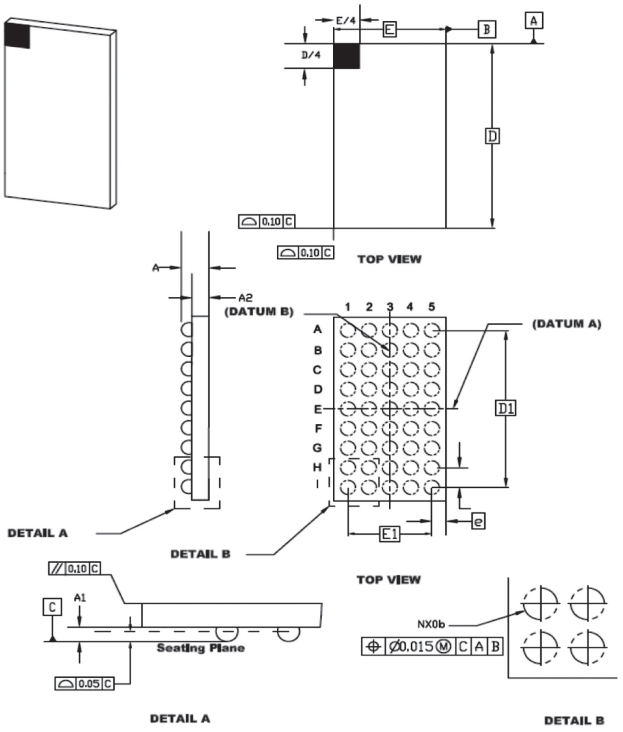


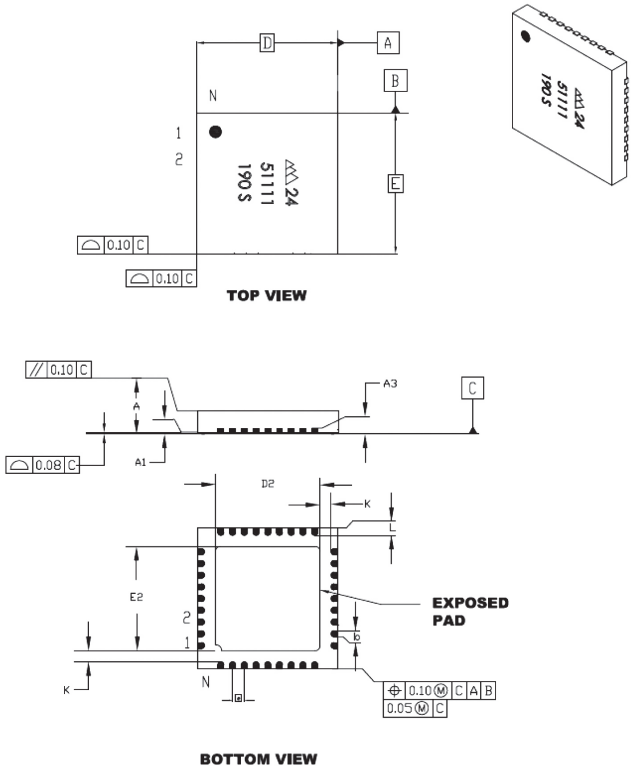
Figure 2: TS51111 Wireless Receiver Application

Package Drawing (WCSP)



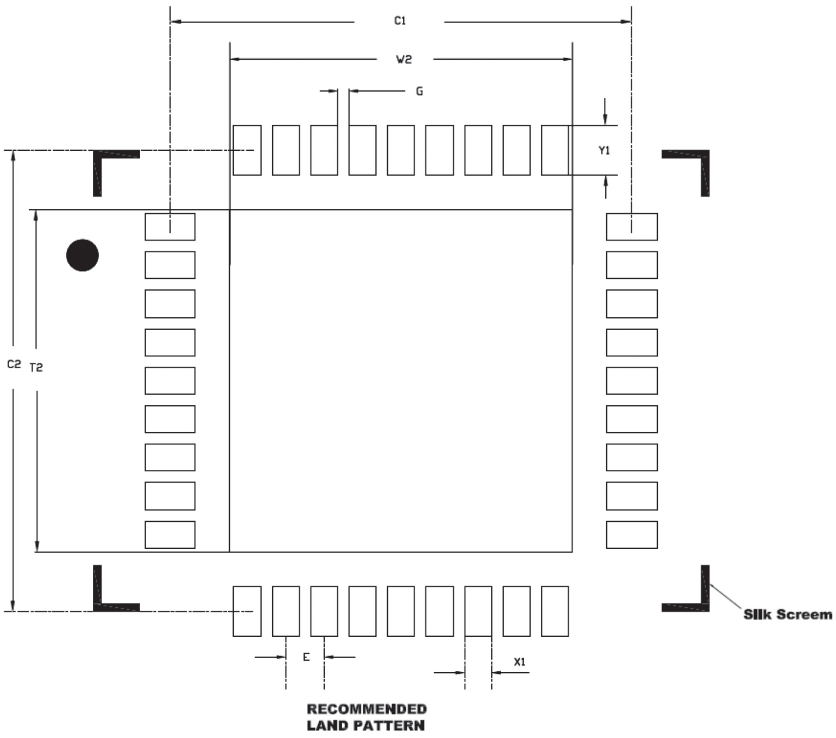
	Units	MILLIMETERS		
	Dimensions Limits	MIN	NOM	MAX
Number of Contacts	N		45	
Contact Pitch	e		0.40 BSC	
Overall Height	A	0.445	0.525	0.625
Standoff	A1	0.12	0.20	0.30
Moldel Package Tickeness	A2	-	-	0.325
Overall Width	E	2.195	-	2.200
Array Width	E1		1.60 BSC	
Overall Length	D	3.795	-	3.800
Array Length	D1		3.20 BSC	
Contact Diameter	b	0.250	0.265	0.280

Package Drawing (QFN)



	Units	MILLIMETERS		
	Dimensions Limits	MIN	NOM	MAX
Number of Pins	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Width	E2	4.30	4.45	4.55
Overall Width	E		6.00 BSC	
Exposed Pad Length	D2	4.30	4.45	4.55
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.45	0.55	0.65
Contact-to-Exposed Pad	K	0.20	-	-

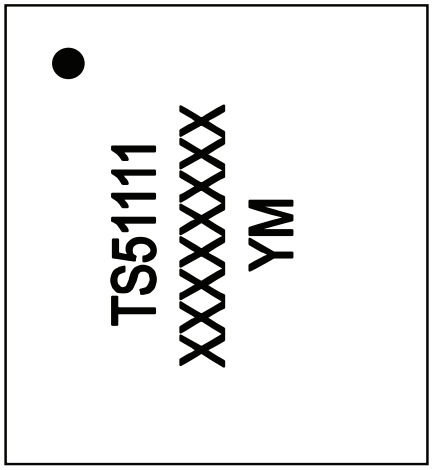
Package Drawing (QFN)



	Units	MILLIMETERS		
	Dimensions Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2	-	-	4.45
Optional tenter Pad Length	T2	-	-	4.45
Contact Pad Spacing	C1	-	6.00	-
Contact Pad Spacing	C2	-	6.00	-
Contact Pad Width (X36)	X1	-	-	0.35
Contact Pad Length (X36)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

Notes:
Dimensions and tolerancing per ASME Y14.5M
BSC: Basic Dimension, Theorically exact value shown with tolerances.
REF: Reference Dimension, usually with tolerance, for information only.

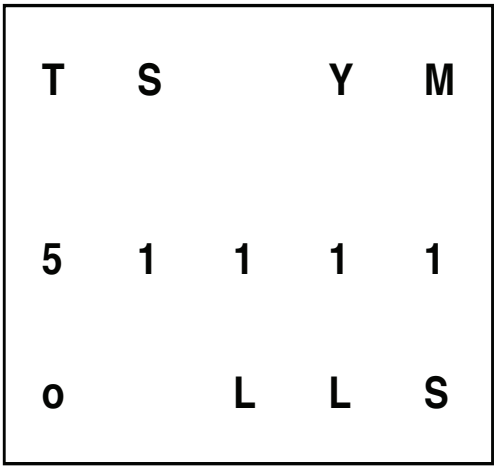
Package Marking (WCSP)



Legend:

	o	Pin 1 Identifier
Line 1 Marking:	TS51111	Device identification
Line 2 Marking:	XXXXXX	Lot number (2 - 9 digits)
Line 3 Marking:	Y	Y = last digit of year
	M	M = month (1=Jan, 2=Feb, 3=Mar … A=Oct, B=Nov, C=Dec)

Package Marking (QFN)



Legend:

Line 1 Marking:	TS	Triune Systems Logo
	Y	Y = last digit of year
	M	M = month (1=Jan, 2=Feb, 3=Mar … A=Oct, B=Nov, C=Dec)
Line 2 Marking:	51111	Device identification
Line 3 Marking:	o	Pin 1 Identifier
	LL	LL = Last two whole (non-fractional) digits of lot number
	S	Assembly Site Identifier

Ordering Information

Part Number	Description
TS51111-M22WCSR	High Efficiency Wireless Power Receiver, WCSP Package
TS51111-M22QFNR	High Efficiency Wireless Power Receiver, QFN Package

RoHS and Reach Compliance

Triune Systems is fully committed to environmental quality. All Triune Systems materials and suppliers are fully compliant with RoHS (European Union Directive 2011/65/EU), REACH SVHC Chemical Restrictions (EC 1907/2006), IPC-1752 Level 3 materials declarations, and their subsequent amendments. Triune Systems maintains certified laboratory reports for all product materials, from all suppliers, which show full compliance to restrictions on the following:

- Cadmium (Cd)
- Chlorofluorocarbons (CFCs)
- Chlorinate Hydrocarbons (CHCs)
- Halons (Halogen free)
- Hexavalent Chromium (CrVI)
- Hydrobromofluorocarbons (HBFCs)
- Hydrochlorofluorocarbons (HCFCs)
- Lead (Pb)
- Mercury (Hg)
- Perfluorocarbons (PFCs)
- Polybrominated biphenyls (PBB)
- Polybrominated Diphenyl Ethers (PBDEs)

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