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REVISION HISTORY

5/2019—Rev. 0 to Rev. A

Changes to Address: 0x04, Reset: 0xA1, Name: POWER_CTRL Section and Table 28 ... 40

4/2016—Revision 0: Initial Version

GENERAL DESCRIPTION

The SSM3582 is a fully integrated, high efficiency, digital input stereo Class-D audio amplifier. It can operate from a single supply, and requires only a few external components, significantly reducing the circuit bill of materials.

A proprietary, spread spectrum Σ-Δ modulation scheme enables direct connection to the speaker, and ensures state-of-the-art analog performance while lowering radiated emissions compared to other Class-D architectures. An optional ultralow electromagnetic interference (EMI) mode significantly reduces radiated emissions above 100 MHz, enabling longer speaker cable lengths. Audio is transmitted digitally to the amplifier, minimizing the possibility of signal corruption in digital environments. The amplifier provides outstanding analog performance, with an over 106 dB signal-to-noise ratio and a vanishingly low 0.004% THD + N.

The SSM3582 operates from a single 4.5 V to 16 V supply, and is capable of delivering 2 × 15 W rms continuously into 8 Ω and 4 Ω loads at <1% total harmonic distortion (THD). The efficient modulation scheme maintains excellent power efficiency over a wide range of impedances: 93% into an 8 Ω load and 90% into a 4 Ω load. Optimization of the output pulse maintains performance at impedances as low as 3 Ω/5 µH, enabling its use with extended bandwidth tweeters.

The pulse code modulation (PCM) audio serial port supports most common protocols, such as I^2S, left justified, and time division multiplexing (TDM), and can address up to 16 devices on a single interface, for up to 32 audio playback channels.

IC operation is controlled through a dedicated I^2C interface. The two ADDRx pins (2×, 5-level) define up to 16 individual addresses in I^2C and standalone modes, and automatically set the default TDM slots attribution.

A micropower shutdown mode is triggered by removing the digital audio interface clock, with a typical current of <1 µA. A software power-down mode is also available.

An automatic power-down feature shuts down the amplifier and the digital-to-analog converter (DAC) when no signal is present at the input, minimizing power consumption during digital silence. The device restarts when nonzero data is present at the input. Mute and unmute transitions are pop/click free.

The SSM3582 is specified over the commercial temperature range of −40°C to +85°C. The device has built-in thermal shutdown and output short-circuit protection, as well as an early thermal warning with programmable gain limiting to maintain operation.

The SSM3582 is available in a 40-lead, 6 mm × 6 mm lead frame chip scale package (LFCSP), with a thermal pad to improve heat dissipation.

SPECIFICATIONS

PV_{DD} = 12 V, AV_{DD} = 5 V (external), DV_{DD} = 1.8 V (external), R_L = 8 Ω + 33 µH, BCLK = 3.072 MHz, FSYNC = 48 kHz, T_A = −40°C to +85°C, unless otherwise noted. The measurements are taken with a 20 kHz AES17 low-pass filter. The other load impedances used are 4 Ω + 15 µH and 3 Ω + 10 µH. Measurements are taken with a 20 kHz AES17 low-pass filter, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power Per Channel	P_O					
Stereo Mode		f = 1 kHz, both channels driven				
		R_L = 8 Ω, THD + N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 16 V		14.4		W
		R_L = 8 Ω, THD + N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 12 V		8.1		W
		R_L = 8 Ω, THD + N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 7 V		2.76		W
		R_L = 8 Ω, THD + N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 5 V		1.41		W
		R_L = 8 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 16 V		18		W
		R_L = 8 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 12 V		10		W
		R_L = 8 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 7 V		3.43		W
		R_L = 8 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 5 V		1.75		W
		R_L = 4 Ω, THD + N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 16 V		25.6		W
		R_L = 4 Ω, THD + N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 12 V		14.67		W
		R_L = 4 Ω, THD + N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 7 V		5.06		W
		R_L = 4 Ω, THD +N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 5 V		2.6		W
		R_L = 4 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 16 V		31.76		W
		R_L = 4 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 12 V		18.31		W
		R_L = 4 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 7 V		6.3		W
		R_L = 4 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 5 V		3.21		W
Mono Mode		f = 1 kHz				
		R_L = 3 Ω, THD +N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 16 V		36.11		W
		R_L = 3 Ω, THD +N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 12 V		20.46		W
		R_L = 3 Ω, THD +N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 7 V		7		W
		R_L = 3 Ω, THD +N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 5 V		3.58		W
		R_L = 3 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 16 V		44.96		W
		R_L = 3 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 12 V		25.49		W
		R_L = 3 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 7 V		8.7		W
		R_L = 3 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 5 V		4.43		W
		R_L = 2 Ω, THD + N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 16 V		49.69		W
		R_L = 2 Ω, THD +N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 12 V		28.55		W
		R_L = 2 Ω, THD +N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 7 V		9.85		W
		R_L = 2 Ω, THD +N < 1%, f = 1 kHz, 20 kHz BW, PV_{DD} = 5 V		5		W
		R_L = 2 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 16 V		62.4		W
		R_L = 2 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 12 V		35.5		W
		R_L = 2 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 7 V		12.22		W
		R_L = 2 Ω, THD + N = 10%, f = 1 kHz, 20 kHz BW, PV_{DD} = 5 V		6.22		W
Minimal Load Inductance		Speaker inductance	5			µH
Efficiency	η					
Stereo Mode		Both channels driven				
		P_O = 10 W, R_L = 8 Ω, PV_{DD} = 12 V		94		%
		P_O = 10 W, R_L = 8 Ω, PV_{DD} = 12 V (low EMI mode)		93.8		%
		P_O = 18 W, R_L = 4 Ω, PV_{DD} = 12 V		90.6		%
		P_O = 15 W, R_L = 4 Ω, PV_{DD} = 12 V (low EMI mode)		89.5		%
Mono Mode						
		P_O = 25 W, R_L = 3 Ω, PV_{DD} = 12 V		92.3		%
		P_O = 25 W, R_L = 3 Ω, PV_{DD} = 12 V (low EMI mode)		92.1		%
		P_O = 35 W, R_L = 2 Ω, PV_{DD} = 12 V		89.9		%
		P_O = 35 W, R_L = 2 Ω, PV_{DD} = 12 V (low EMI mode)		89.7		%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise	THD + N	P_O = 5 W into 8 Ω, f = 1 kHz, PV_{DD} = 12 V		0.004		%
Output Stage On Resistance	R_{ON}			100		mΩ
Overcurrent Protection Trip Point	I_{OC}			6		A peak
Average Switching Frequency	f_{SW}			300		kHz
Differential Output Offset Voltage	V_{OOS}	A_V = 19 dB		1		mV
Crosstalk between Left and Right		Measured at 1 kHz with regards to full-scale output		100		dB
POWER SUPPLIES						
Supply Voltage Range	PV_{DD}		4.5		16	V
	AV_{DD}		4.5	5.0	5.5	V
	DV_{DD}		1.62	1.8	1.98	V
Power Supply Rejection Ratio	PSRR					
AC	$PSRR_{AC}$	V_{RIPPLE} =100 mV rms at 1 kHz		86		dB
		V_{RIPPLE} =1 V rms at 1 kHz		88		dB
ANALOG GAIN	A_V	Measured with 0 dBFS input at 1 kHz				
Gain = 00		PV_{DD} ≥ 6.3 V		6.2		V peak
Gain = 01		PV_{DD} ≥ 9 V		8.75		V peak
Gain = 10		PV_{DD} ≥ 12.6 V		12.5		V peak
Gain = 11		PV_{DD} = 16 V		15.5		V peak
SHUTDOWN CONTROL[1]						
Turn On Time, Volume Ramp Disabled	t_{WU}	Time from SPWDN = 0 to output switching, DAC_HV = 1 or DAC_MUTE_x = 1, t_{WU} = 4 FSYNC cycles to 7 FSYNC cycles + 7.68 ms				
f_S = 12 kHz			8.01		8.27	ms
f_S = 24 kHz			7.84		7.98	ms
f_S = 48 kHz			7.76		7.83	ms
f_S = 96 kHz			7.72		7.76	ms
f_S = 192 kHz			7.70		7.72	ms
Turn On Time, Volume Ramp Enabled	t_{WUR}	Time from SPWDN = 0 to full volume output switching, DAC_HV = 0 and DAC_MUTE_x = 0, VOL_x = 0x40				
f_S = 12 kHz		$t_{WUR} = t_{WU}$ + 15.83 ms	23.84		24.10	ms
f_S = 24 kHz		$t_{WUR} = t_{WU}$ + 15.83 ms	23.67		23.81	ms
f_S = 48 kHz		$t_{WUR} = t_{WU}$ + 15.83 ms	23.59		23.66	ms
f_S = 96 kHz		$t_{WUR} = t_{WU}$ + 7.92 ms	15.64		15.68	ms
f_S = 192 kHz		$t_{WUR} = t_{WU}$ + 0.99 ms	8.69		8.71	ms
Turn Off Time, Volume Ramp Disabled	t_{SD}	Time from SPWDN = 1 to full power-down, DAC_HV = 1 or DAC_MUTE_x = 1		100		µs
Turn Off Time, Volume Ramp Enabled	t_{SDR}	Time from SPWDN = 1 to full power-down, DAC_HV = 0 and DAC_MUTE_x = 0, VOL_x = 0x40				
f_S = 12 kHz		$t_{SDR} = t_{SD}$ + 15.83 ms		15.932		ms
f_S = 24 kHz		$t_{SDR} = t_{SD}$ + 15.83 ms		15.932		ms
f_S = 48 kHz		$t_{SDR} = t_{SD}$ + 15.83 ms		15.932		ms
f_S = 96 kHz		$t_{SDR} = t_{SD}$ + 7.92 ms		8.016		ms
f_S = 192 kHz		$t_{SDR} = t_{SD}$ + 0.99 ms		1.09		ms
Output Impedance	Z_{OUT}		100			kΩ

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE[2]		Stereo mode				
Output Voltage Noise	e_n	f = 20 Hz to 20 kHz, A weighted, PV_{DD} = 12 V, 8 Ω		37.8		μV rms
		f = 20 Hz to 20 kHz, A weighted, PV_{DD} = 16 V, 8 Ω		38.5		μV rms
		f = 20 Hz to 20 kHz, A weighted, PV_{DD} = 12 V, 4 Ω		36.8		μV rms
		f = 20 Hz to 20 kHz, A weighted, PV_{DD} = 16 V, 4 Ω		36.3		μV rms
Signal-to-Noise Ratio	SNR	P_O = 8.1 W, R_L = 8 Ω, A_V = 19 dB, PV_{DD} = 12 V, A weighted		106.5		dB
		P_O = 14.4 W, R_L = 8 Ω, A_V = 21 dB, PV_{DD} = 16 V, A weighted		108.9		dB
		P_O = 14.67 W, R_L = 4 Ω, A_V = 19 dB, PV_{DD} = 12 V, A weighted		106.3		dB
		P_O = 25.58 W, R_L = 4 Ω, A_V = 21 dB, PV_{DD} = 16 V, A weighted		108.9		dB
PV_{DD} ADC PERFORMANCE						
PV_{DD} Sense Full-Scale Range		PV_{DD} with full-scale ADC output	3.8		16.2	V
PV_{DD} Sense Absolute Accuracy		PV_{DD} = 15 V	−8		+8	LSB
		PV_{DD} = 5 V	−6		+6	LSB
Resolution		Unsigned 8-bit output with 3.8 V offset		8		Bits
Temperature Sense ADC						
Temperature Sense Range			−60		+160	°C
Temperature Sense Accuracy				±5		°C
DIE TEMPERATURE						
Overtemperature Warning				117		°C
Overtemperature Protection				145		°C
UNDERVOLTAGE FAULT						
AV_{DD}				3.6		V
PV_{DD}				3.6		V

[1] Guaranteed by design.
[2] Noise performance is based on the bench data for T_A = −40°C to +85°C.

Software master power-down indicates that the clocks are turned off. Automatic power-down indicates that there is no dither or zero input signal with clocks on; the device enters soft power-down after 2048 cycles of zero input values. Quiescent indicates triangular dither with zero input signal. All specifications are typical, with a 48 kHz sample rate, in stereo mode, unless otherwise noted.

Table 2. Power Supply Current Consumption, No Load[1]

Edge Rate Control Mode	Internal Regulator	Test Conditions	I_{PVDD}			I_{DVDD}	I_{AVDD}	Unit
			PV_{DD} = 5 V	PV_{DD} = 12 V	PV_{DD} = 16 V	PV_{DD} = 1.8 V	PV_{DD} = 5 V	
Normal	Disabled	Software master power-down	0.065	0.065	0.065	2.68	7.542	μA
		Automatic power-down	0.065	0.065	0.065	43.72	7.542	μA
		Quiescent	2.54	4.94	6.25	0.945	6.335	mA
	Enabled	Software master power-down	0.065	0.065	0.065	N/A	N/A	μA
		Automatic power-down	209	286	329	N/A	N/A	μA
		Quiescent	9.78	12.38	14.05	N/A	N/A	mA
Low EMI	Disabled	Software master power-down	0.065	0.065	0.065	2.68	7.542	μA
		Automatic power-down	0.065	0.065	0.065	43.72	7.542	μA
		Quiescent	2.56	5.01	6.31	0.945	6.171	mA
	Enabled	Software master power-down	0.065	0.065	0.065	N/A	N/A	μA
		Automatic power-down	209	286	329	N/A	N/A	μA
		Quiescent	9.69	12.09	13.74	N/A	N/A	mA

[1] N/A means not applicable.

Table 3. Power Supply Current Consumption, 4 Ω + 15 µH[1]

Edge Rate Control Mode	Internal Regulator	Test Conditions	I_{PVDD}			I_{DVDD}	I_{AVDD}	Unit
			PV_{DD} = 5 V	PV_{DD} = 12 V	PV_{DD} = 16 V	PV_{DD} = 1.8 V	PV_{DD} = 5 V	
Normal	Disabled	Software master power-down	0.065	0.065	0.065	2.68	7.542	µA
		Automatic power-down	0.065	0.065	0.065	43.72	7.542	µA
		Quiescent	2.6	4.93	6.25	0.945	6.477	mA
	Enabled	Software master power-down	0.065	0.065	0.065	N/A	N/A	µA
		Automatic power-down	209	286	329	N/A	N/A	µA
		Quiescent	9.83	12.34	13.58	N/A	N/A	mA
Low EMI	Disabled	Software master power-down	0.065	0.065	0.065	2.68	7.542	µA
		Automatic power-down	0.065	0.065	0.065	43.72	7.542	µA
		Quiescent	2.51	4.62	5.6	0.945	6.182	mA
	Enabled	Software master power-down	0.065	0.065	0.065	N/A	N/A	µA
		Automatic power-down	209	286	329	N/A	N/A	µA
		Quiescent	9.64	11.86	12.87	N/A	N/A	mA

[1] N/A means not applicable.

Table 4. Power Supply Current Consumption, 8 Ω + 33 µH[1]

Edge Rate Control Mode	Internal Regulator	Test Conditions	I_{PVDD}			I_{DVDD}	I_{AVDD}	Unit
			PV_{DD} = 5 V	PV_{DD} = 12 V	PV_{DD} = 16 V	PV_{DD} = 1.8 V	PV_{DD} = 5 V	
Normal	Disabled	Software master power-down	0.065	0.065	0.065	2.68	7.542	µA
		Automatic power-down	0.065	0.065	0.065	43.72	7.542	µA
		Quiescent	2.59	5.02	6.31	0.942	6.432	mA
	Enabled	Software master power-down	0.065	0.065	0.065	N/A	N/A	µA
		Automatic power-down	209	286	329	N/A	N/A	µA
		Quiescent	9.82	12.39	13.73	N/A	N/A	mA
Low EMI	Disabled	Software master power-down	0.065	0.065	0.065	2.68	7.542	µA
		Automatic power-down	0.065	0.065	0.065	43.72	7.542	µA
		Quiescent	2.57	4.86	6.02	0.942	6.232	mA
	Enabled	Software master power-down	0.065	0.065	0.065	N/A	N/A	µA
		Automatic power-down	209	286	329	N/A	N/A	µA
		Quiescent	9.65	12.02	13.18	N/A	N/A	mA

[1] N/A means not applicable.

Table 5. Power-Down Current

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN CURRENT		External AVDD = 5 V and DVDD = 1.8 V, software master power-down, no BCLK/FSYNC				
	I_{PVDD}	PV_{DD} = 5 V		65		nA
		PV_{DD} = 12 V		65		nA
		PV_{DD} = 16 V		65		nA
	I_{AVDD}	AVDD = 5 V external		7.542		µA
	I_{DVDD}	DVDD = 1.8 V external		2.7		µA

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT VOLTAGE[1]					
BCLK, FSYNC, SDATA, SCL, and SDA Pins					
High (V_{IH})	$0.7 \times DV_{DD}$		5.5	V	
Low (V_{IL})	−0.3		$+0.3 \times DV_{DD}$	V	
INPUT LEAKAGE					
BCLK, FSYNC, SDATA, ADDRx, SCL, and SDA Pins					
High (I_{IH})			1	µA	
Low (I_{IL})			1	µA	
INPUT CAPACITANCE			5	pF	
OUTPUT DRIVE STRENGTH[1]					
SDA	3		5	mA	
SAMPLE RATE (FSYNC FREQUENCY)	8		192	kHz	

[1] The pull-up resistor for SCL and SDA must be scaled according to the external pull-up voltage in the system. The typical value for a pull-up resistor for 1.8 V is 2.2 kΩ.

DIGITAL TIMING SPECIFICATIONS

All timing specifications are given for the default setting (I^2S mode) of the serial input port.

Table 7.

	Limit			
Parameter	Min	Max	Unit	Description
I^2C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.26		µs	SCL high
t_{SCLL}	0.5		µs	SCL low
t_{SCS}	0.26		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.26		µs	Hold time; after this period, the first clock is generated
t_{DS}	50		ns	Data setup time
t_{DH}	0.14		µs	Data hold time
t_{SCR}		120	ns	SCL rise time
t_{SCF}		120	ns	SCL fall time
t_{SDR}		120	ns	SDA rise time
t_{SDF}		120	ns	SDA fall time
t_{BFT}	0.5		µs	Bus free time (time between stop and start)

DIGITAL INPUT TIMING SPECIFICATIONS

Table 8.

	Limit			
Parameter	T_{MIN}	T_{MAX}	Unit	Description
SERIAL PORT				
t_{BIL}	10		ns	BCLK low pulse width
t_{BIH}	10		ns	BCLK high pulse width
t_{SIS}	4		ns	SDATA setup; time to BCLK rising
t_{SIH}	4		ns	SDATA hold; time from BCLK rising
t_{LIS}	5		ns	FSYNC setup time to BCLK rising
t_{LIH}	5		ns	FSYNC hold time to BCLK rising
t_{BP}	20		ns	Minimum BCLK period

Digital Timing Diagrams

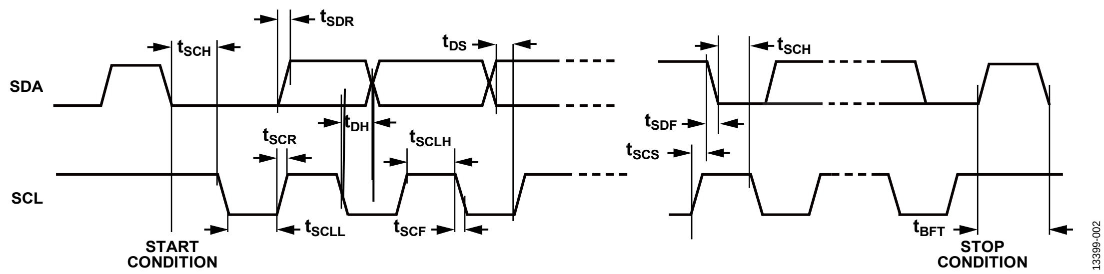


Figure 2. I²C Port Timing

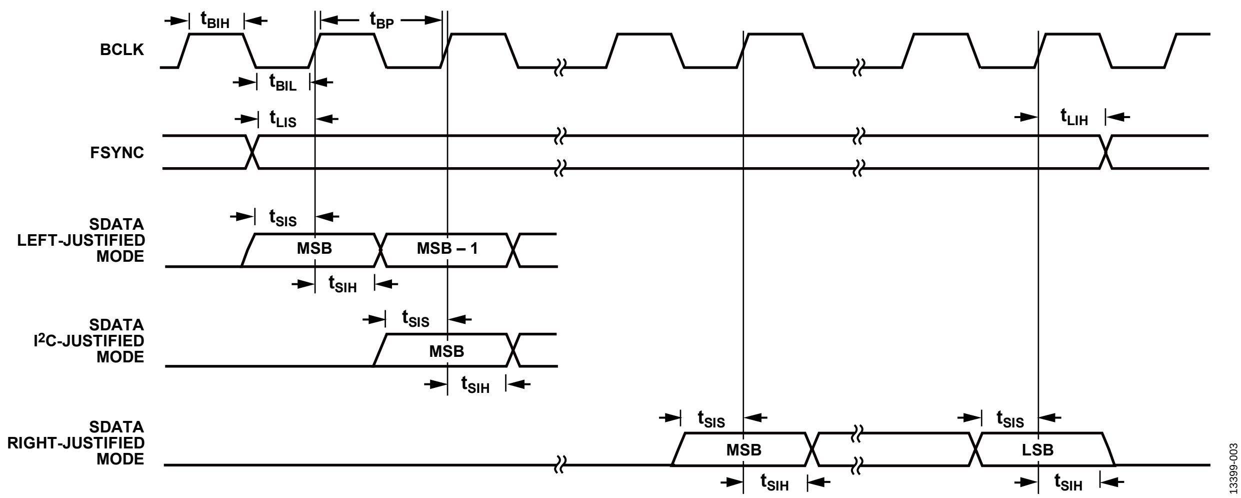


Figure 3. Serial Input Port Timing

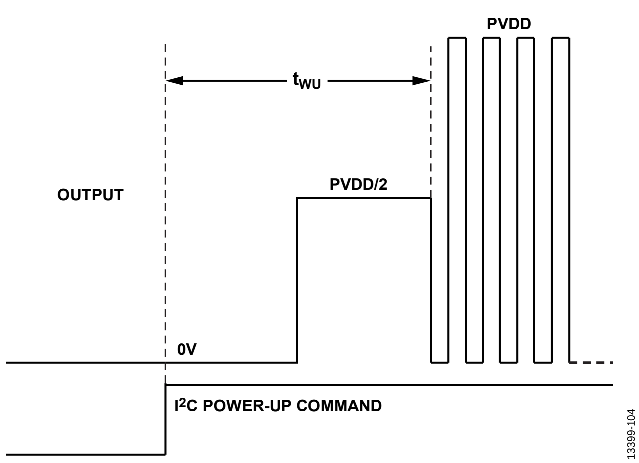


Figure 4. Turn On Time, Hard Volume

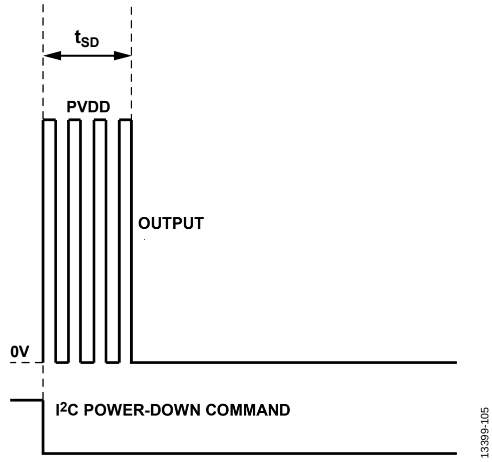


Figure 5. Turn Off Time, Hard Volume

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
PVDD Supply Voltage	−0.3 V to +17 V
DVDD Supply Voltage	−0.3 V to +1.98 V
AVDD Supply Voltage	−0.3 V to +5.5 V
PGND and AGND Differential	±0.3 V
Digital Input Pins	
FSYNC, BCLK, SDATA, SCL, SDA	−0.3 V to +5.5 V
Analog Input Pins	
ADDRx	−0.3 V to +1.98 V
AVDD_EN	−0.3 V to +17 V
DVDD_EN	−0.3 V to +5.5 V
ESD Susceptibility	
Human Body Model	2 kV
Charged Device Model	1 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

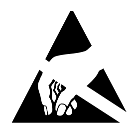
THERMAL RESISTANCE

θ_{JA} (junction to air) is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JA} and θ_{JB} are determined according to JESD51-9 on a 4-layer (2s2p) printed circuit board (PCB) with natural convection cooling.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead, 6 mm × 6 mm LFCSP	27	1.1	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

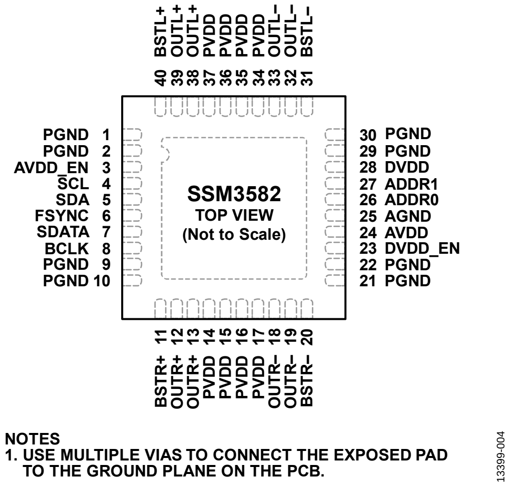


Figure 6. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	PGND	PWR	Left Channel Power Stage Ground.
2	PGND	PWR	Left Channel Power Stage Ground.
3	AVDD_EN	AIN	5 V AVDD Regulator Enable. Connect this pin to PVDD to enable the AVDD regulator or connect to AGND to disable the regulator. When this pin is connected to PVDD, the regulator is enabled. When this pin is connected to AGND, the regulator is disabled.
4	SCL	DIN	I^2C Clock Input.
5	SDA	DIO	I^2C Data.
6	FSYNC	DIN	I^2S/TDM Frame Sync (FSYNC) Input.
7	SDATA	DIN	I^2S/TDM Serial Data (SDATA) Input.
8	BCLK	DIN	I^2S/TDM Bit Clock (BCLK) Input.
9	PGND	PWR	Right Channel Power Stage Ground.
10	PGND	PWR	Right Channel Power Stage Ground.
11	BSTR+	AIN	Bootstrap Input, Right Channel Noninverting.
12	OUTR+	AOUT	Right Channel Noninverting Output.
13	OUTR+	AOUT	Right Channel Noninverting Output.
14	PVDD	PWR	Right Channel Power Stage Supply.
15	PVDD	PWR	Right Channel Power Stage Supply.
16	PVDD	PWR	Right Channel Power Stage Supply.
17	PVDD	PWR	Right Channel Power Stage Supply.
18	OUTR–	AOUT	Right Channel Inverting Output.
19	OUTR–	AOUT	Right Channel Inverting Output.
20	BSTR–	AIN	Bootstrap Input, Right Channel Inverting.
21	PGND	PWR	Right Channel Power Stage Ground.
22	PGND	PWR	Right Channel Power Stage Ground.
23	DVDD_EN	AIN	1.8 V DVDD Regulator Enable. Connect this pin to AVDD to enable the DVDD regulator or connect to AGND to disable the regulator. When this pin is connected to AVDD, the regulator is enabled. When this pin is connected to AGND, the regulator is disabled.
24	AVDD	PWR	Analog Supply 5 V Regulator Output/External 5 V Input.
25	AGND	PWR	Analog Ground.
26	ADDR0	AIN	Address Select 0 (See Table 14).
27	ADDR1	AIN	Address Select 1 (See Table 14).
28	DVDD	PWR	Digital Supply 1.8 V Regulator Output/External 1.8 V Input.
29	PGND	PWR	Left Channel Power Stage Ground.
30	PGND	PWR	Left Channel Power Stage Ground.
31	BSTL–	AIN	Bootstrap Input, Left Channel Inverting.

Pin No.	Mnemonic	Type[1]	Description
32	OUTL−	AOUT	Left Channel Inverting Output.
33	OUTL−	AOUT	Left Channel Inverting Output.
34	PVDD	PWR	Left Channel Power Stage Supply.
35	PVDD	PWR	Left Channel Power Stage Supply.
36	PVDD	PWR	Left Channel Power Stage Supply.
37	PVDD	PWR	Left Channel Power Stage Supply.
38	OUTL+	AOUT	Left Channel Noninverting Output.
39	OUTL+	AOUT	Left Channel Noninverting Output.
40	BSTL+	AIN	Bootstrap Input, Left Channel Noninverting.
	EPAD		Exposed Pad. Use multiple vias to connect the exposed pad to the ground plane on the PCB.

[1] PWR is power supply or ground pin, AIN is analog input, DIN is digital input, DIO is digital input/output, and AOUT is analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

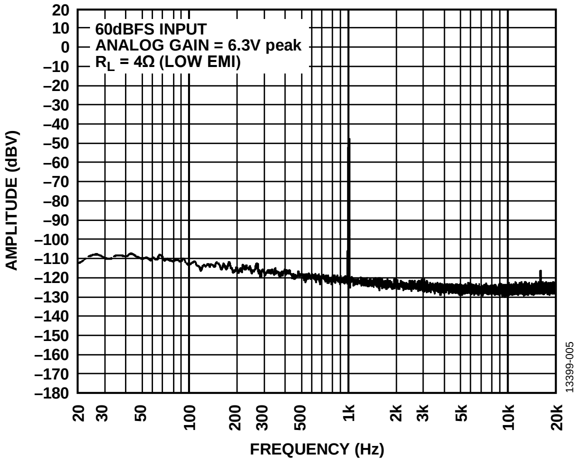


Figure 7. Amplitude vs. Frequency, 60 dBFS Input, Analog Gain = 6.3 V peak

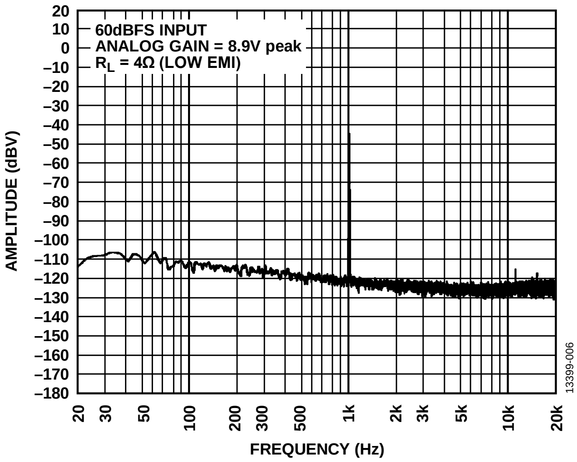


Figure 8. Amplitude vs. Frequency, 60 dBFS Input, Analog Gain = 8.9 V peak

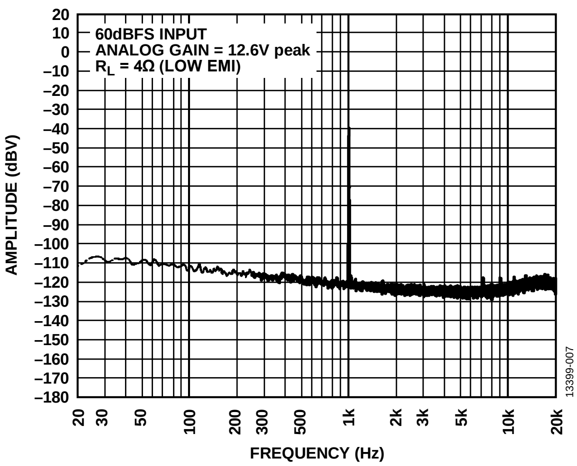


Figure 9. Amplitude vs. Frequency, 60 dBFS Input, Analog Gain = 12.6 V peak

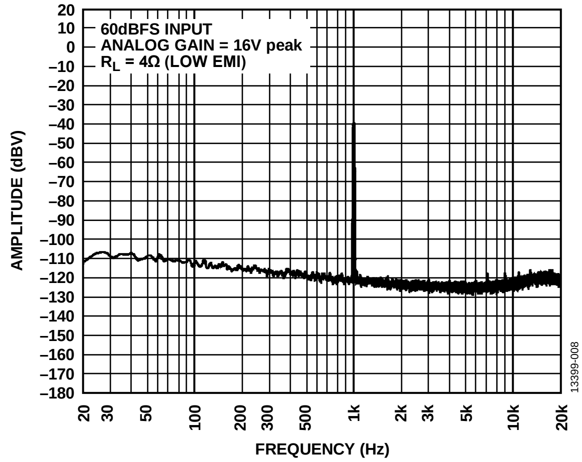


Figure 10. Amplitude vs. Frequency, 60 dBFS Input, Analog Gain = 16 V peak

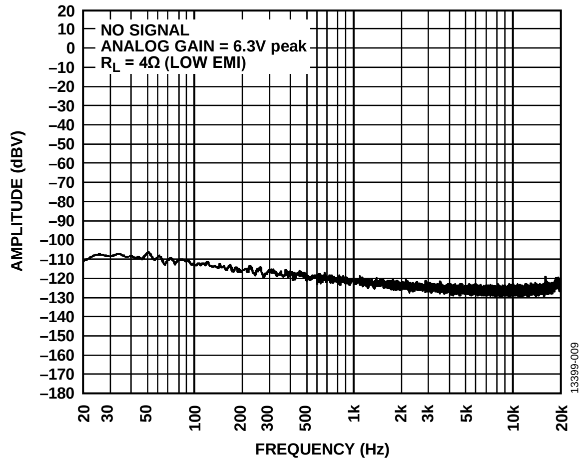


Figure 11. Amplitude vs. Frequency, No Signal, Analog Gain = 6.3 V peak

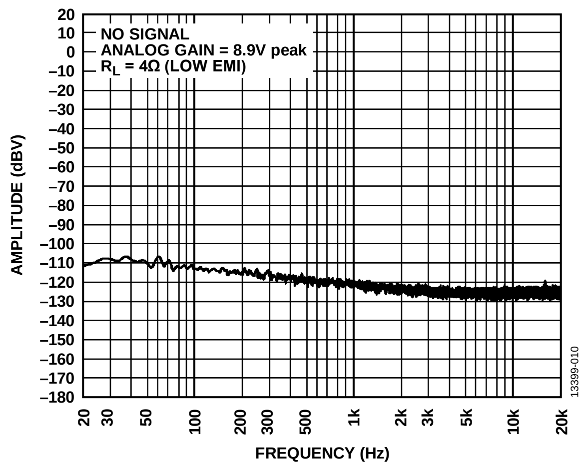


Figure 12. Amplitude vs. Frequency, No Signal, Analog Gain = 8.9 V peak

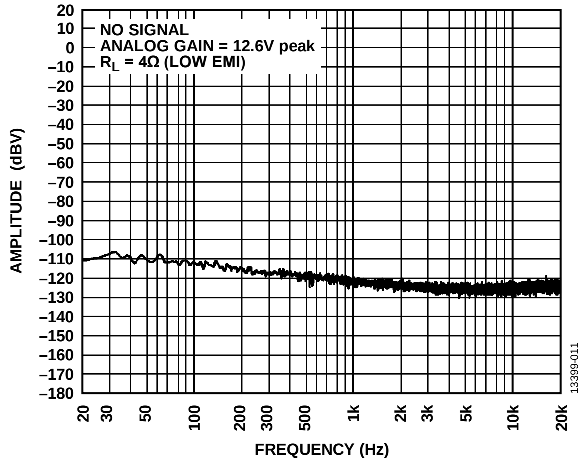


Figure 13. Amplitude vs. Frequency, No Signal, Analog Gain = 12.6 V peak

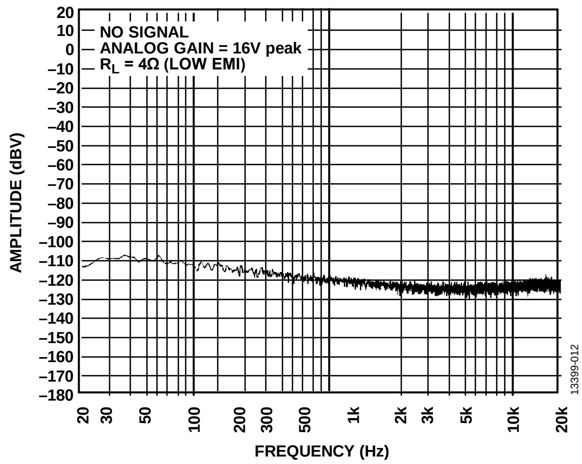


Figure 14. Amplitude vs. Frequency, No Signal, Analog Gain = 16 V peak

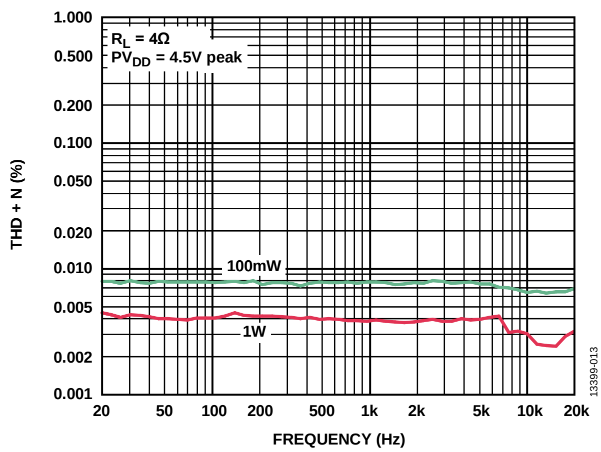


Figure 15. THD + N vs. Frequency, R_L = 4 Ω, PV_{DD} = 4.5 V peak

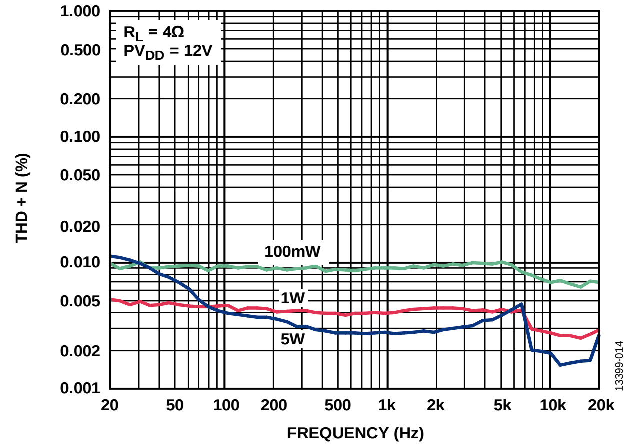


Figure 16. THD + N vs. Frequency, R_L = 4 Ω, PV_{DD} = 12 V

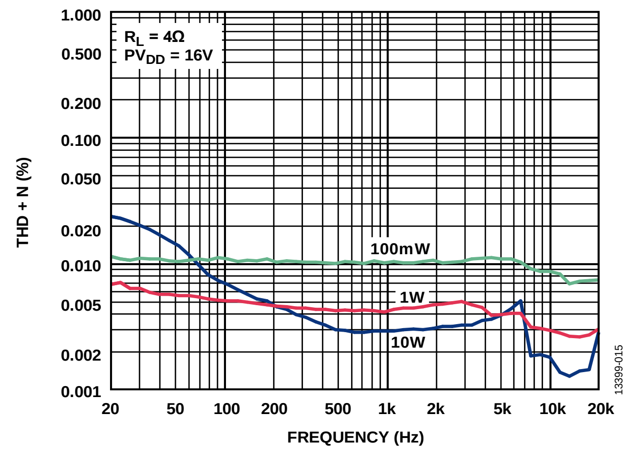


Figure 17. THD + N vs. Frequency, R_L = 4 Ω, PV_{DD} = 16 V

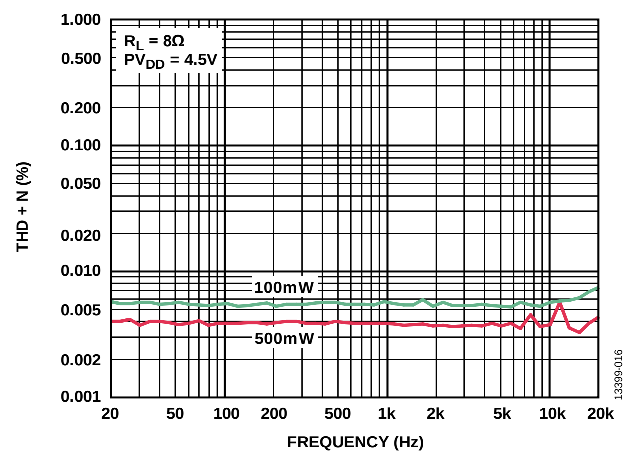


Figure 18. THD + N vs. Frequency, R_L = 8 Ω, PV_{DD} = 4.5 V

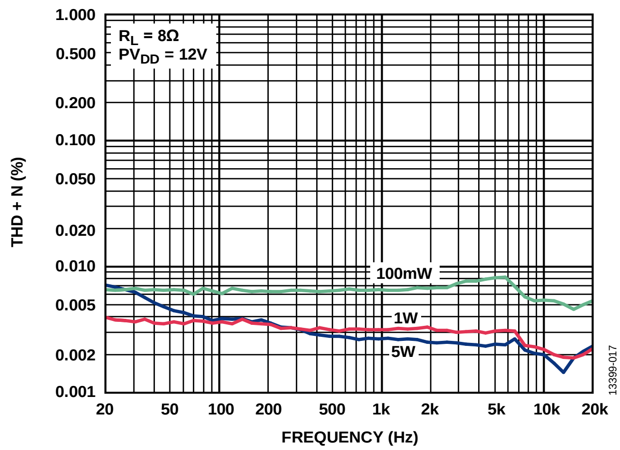


Figure 19. THD + N vs. Frequency, $R_L = 8\ \Omega$, $PV_{DD} = 12\ V$

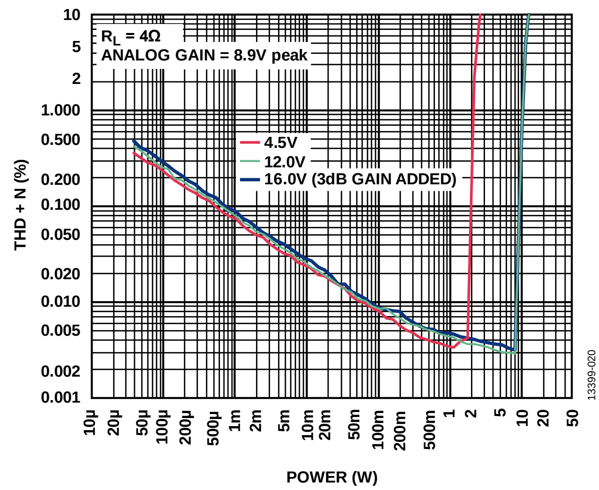


Figure 22. THD + N vs. Power, $R_L = 4\ \Omega$, Analog Gain = 8.9 V peak

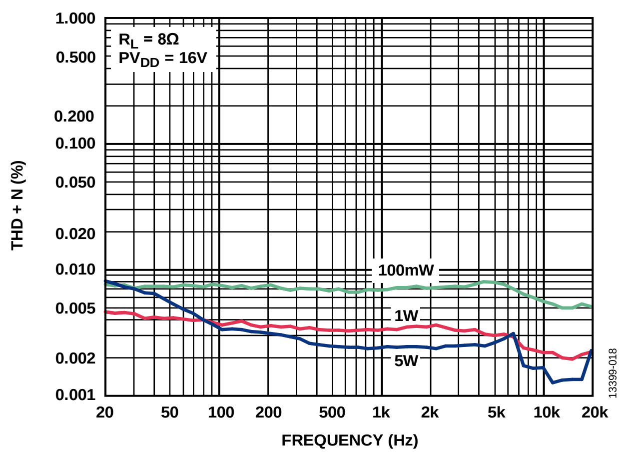


Figure 20. THD + N vs. Frequency, $R_L = 8\ \Omega$, $PV_{DD} = 16\ V$

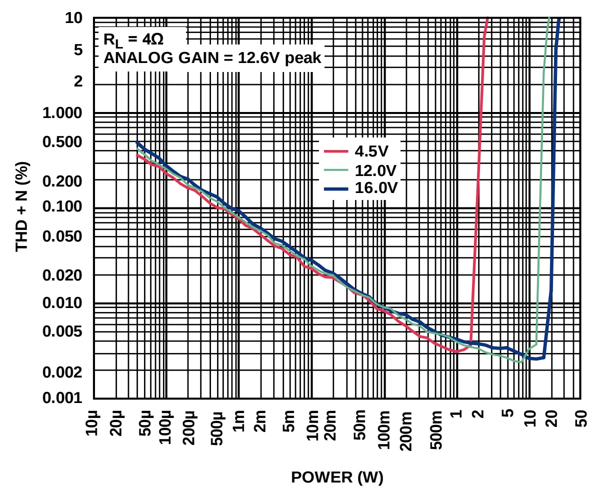


Figure 23. THD + N vs. Power, $R_L = 4\ \Omega$, Analog Gain = 12.6 V peak

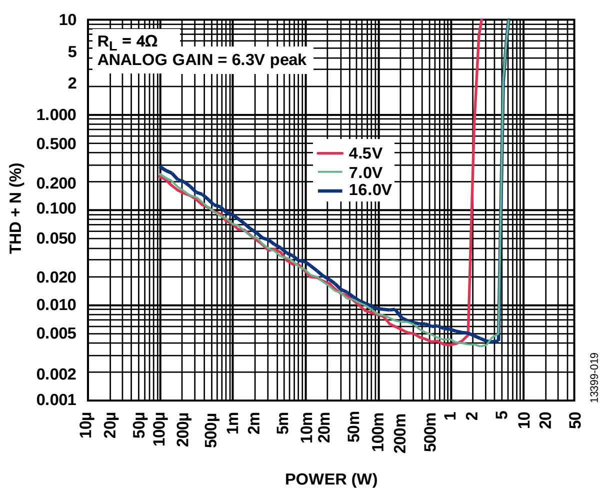


Figure 21. THD + N vs. Power, $R_L = 4\ \Omega$, Analog Gain = 6.3 V peak

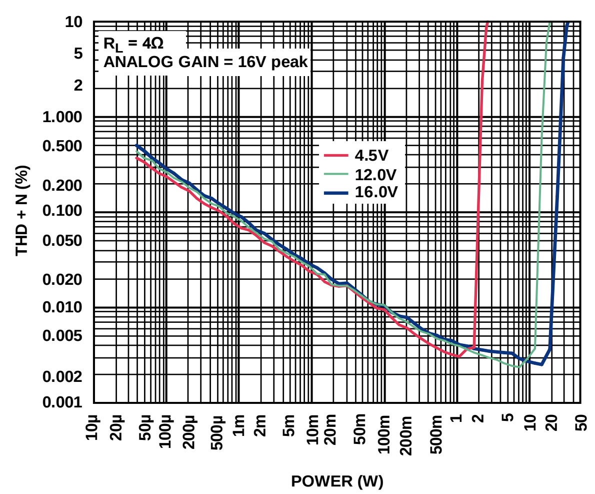


Figure 24. THD + N vs. Power, $R_L = 4\ \Omega$, Analog Gain = 16 V peak

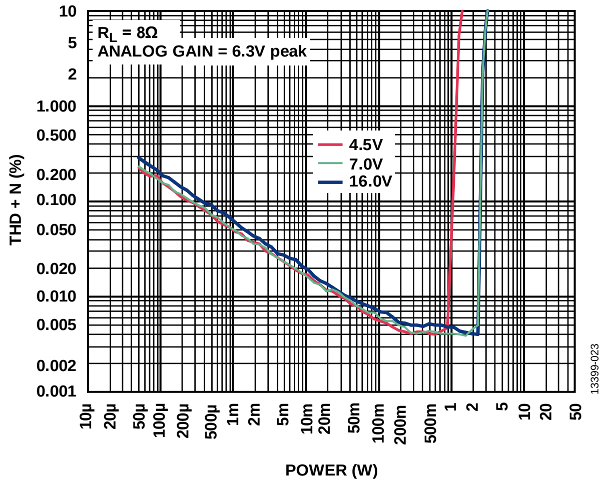


Figure 25. THD + N vs. Power, R_L = 8 Ω, Analog Gain = 6.3 V peak

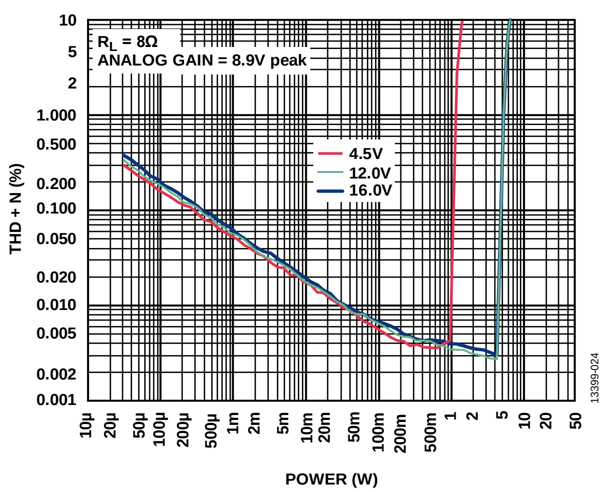


Figure 26. THD + N vs. Power, R_L = 8 Ω, Analog Gain = 8.9 V peak

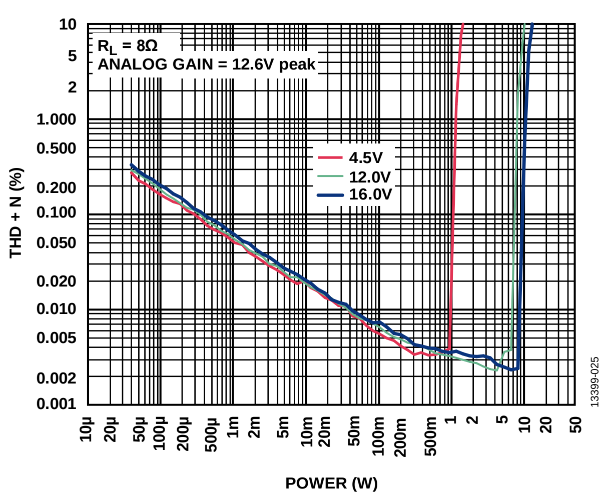


Figure 27. THD + N vs. Power, R_L = 8 Ω, Analog Gain = 12. 6 V peak

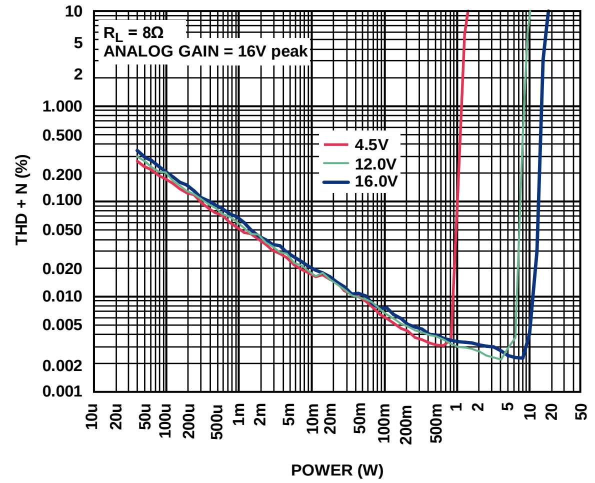


Figure 28. THD + N vs. Power, R_L = 8 Ω, Analog Gain = 16 V peak

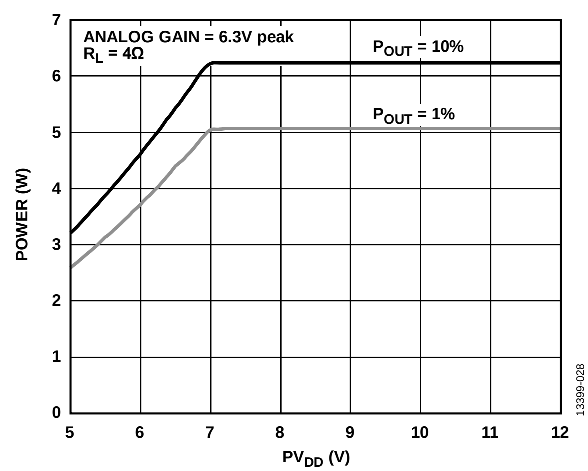


Figure 29. Power vs. PV_{DD}, R_L = 4 Ω, Analog Gain = 6.3 V peak

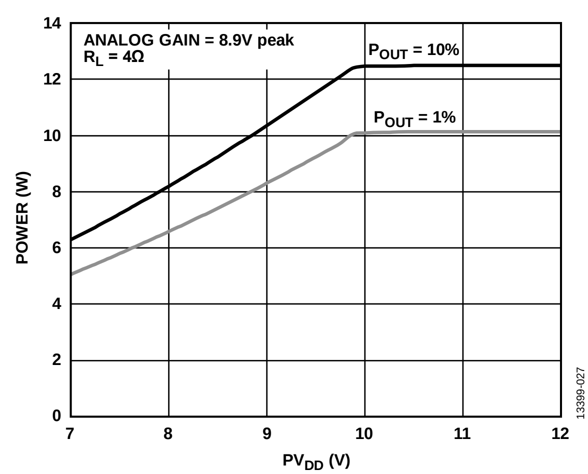


Figure 30. Power vs. PV_{DD}, R_L = 4 Ω, Analog Gain = 8.9 V peak

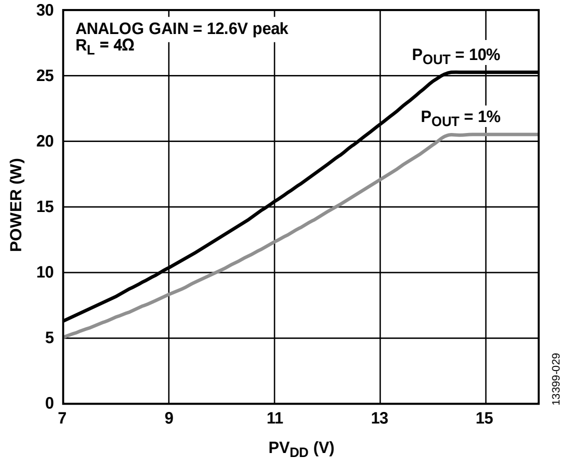


Figure 31. Power vs. PV_{DD}, R_L = 4 Ω, Analog Gain = 12.6 V peak

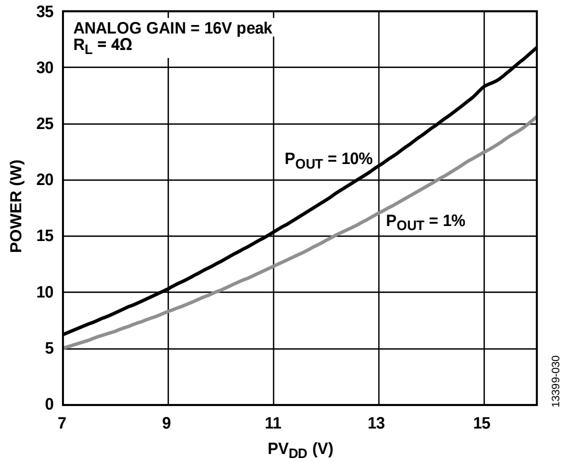


Figure 32. Power vs. PV_{DD}, R_L = 4 Ω, Analog Gain = 16 V peak

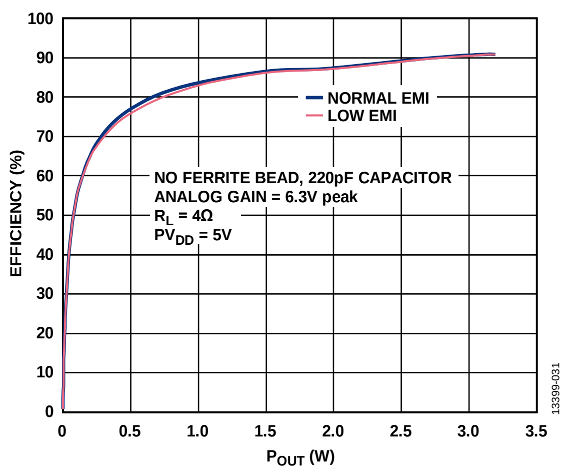


Figure 33. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 6.3 V peak, R_L = 4 Ω, PV_{DD} = 5 V

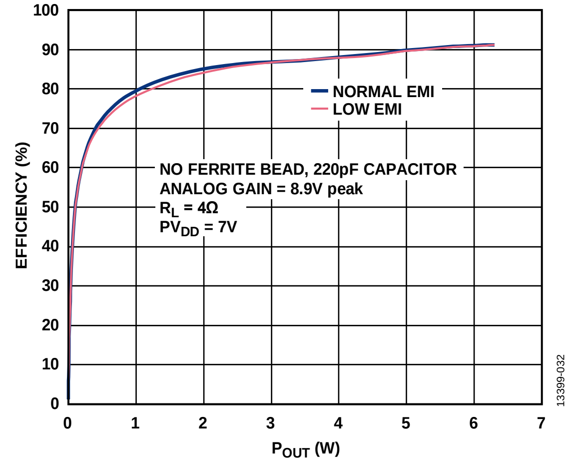


Figure 34. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 8.9 V peak, R_L = 4 Ω, PV_{DD} = 7 V

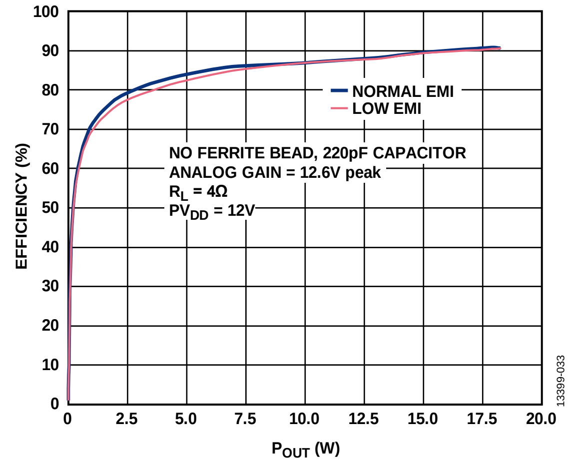


Figure 35. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 12.6 V peak, R_L = 4 Ω, PV_{DD} = 12 V

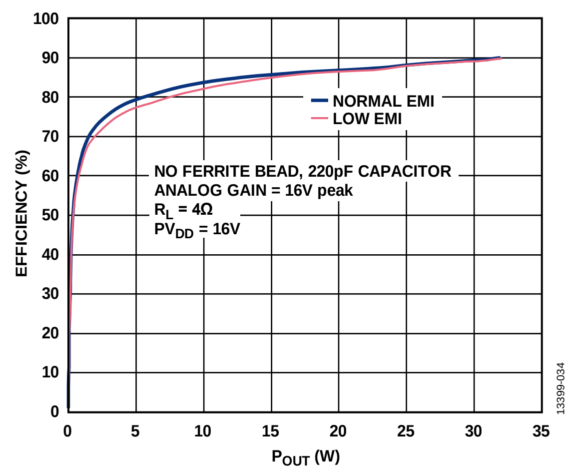


Figure 36. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 16 V peak, R_L = 4 Ω, PV_{DD} = 16 V

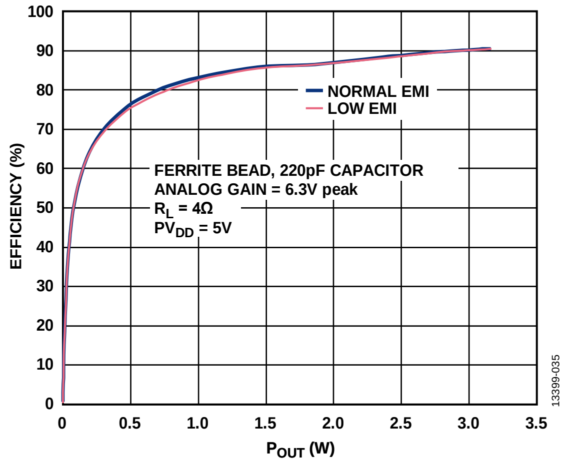


Figure 37. Efficiency vs. P_{OUT}, with Ferrite Bead, Analog Gain = 6.3 V peak, R_L = 4 Ω, PV_{DD} = 5 V

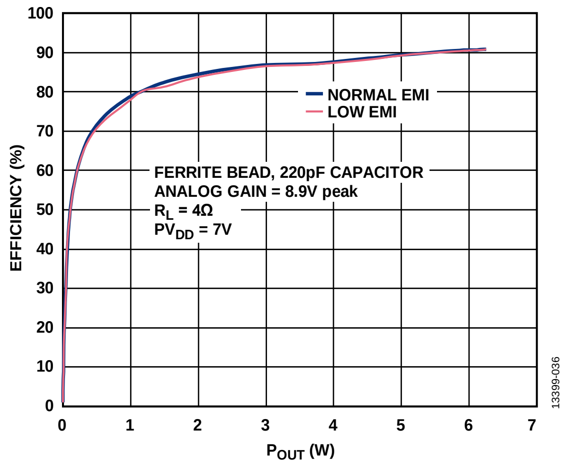


Figure 38. Efficiency vs. P_{OUT}, with Ferrite Bead, Analog Gain = 8.9 V peak, R_L = 4 Ω, PV_{DD} = 7 V

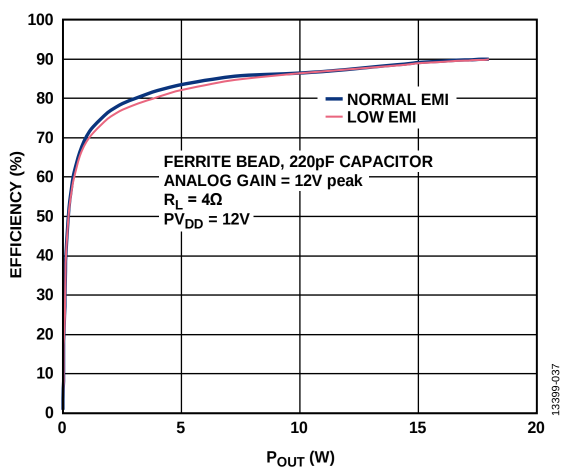


Figure 39. Efficiency vs. P_{OUT}, with Ferrite Bead, Analog Gain = 12 V peak, R_L = 4 Ω, PV_{DD} = 12 V

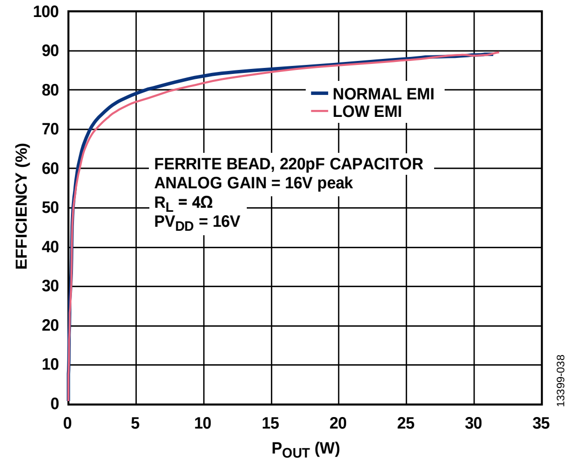


Figure 40. Efficiency vs. P_{OUT}, with Ferrite Bead, Analog Gain = 16 V peak, R_L = 4 Ω, PV_{DD} = 16 V

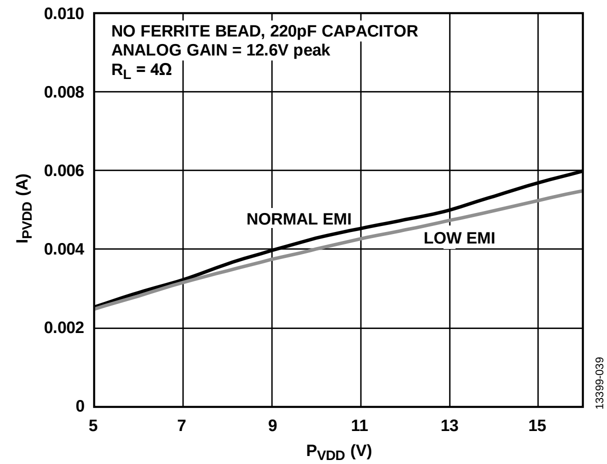


Figure 41. I_{PVDD} vs. PV_{DD}, No Ferrite Bead, Analog Gain = 12.6 V peak, R_L = 4 Ω

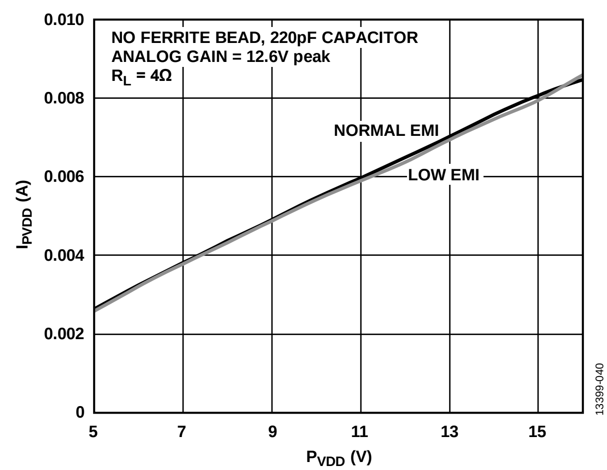


Figure 42. I_{PVDD} vs. PV_{DD}, No Ferrite Bead, Analog Gain = 12.6 V peak, R_L = 4 Ω

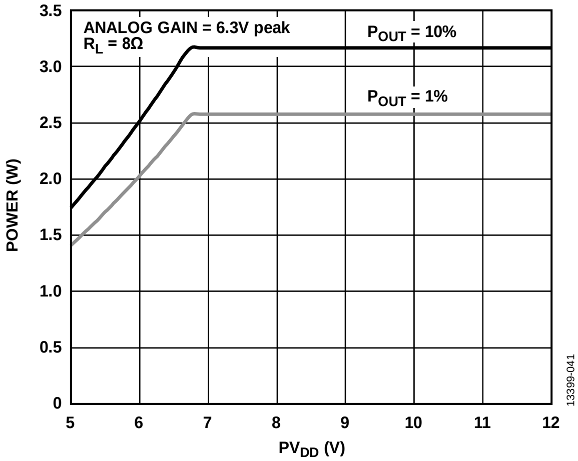


Figure 43. Power vs. PV_{DD}, Analog Gain = 6.3 V peak, R_L = 8 Ω

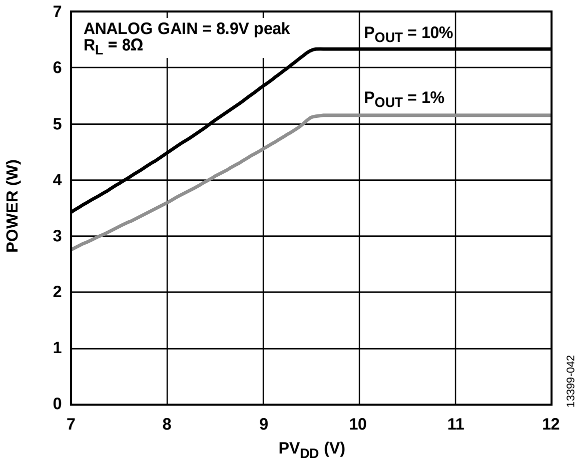


Figure 44. Power vs. PV_{DD}, Analog Gain = 8.9 V peak, R_L = 8 Ω

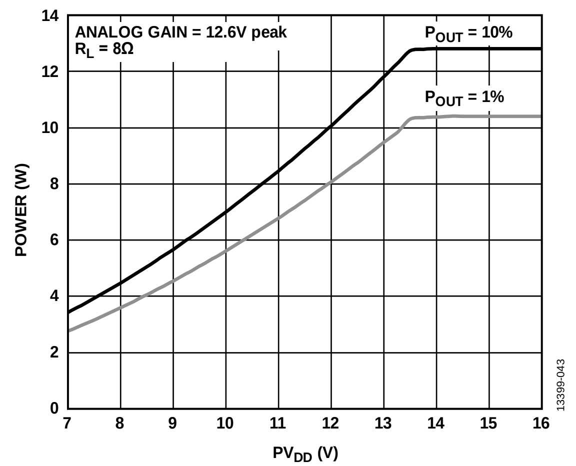


Figure 45. Power vs. PV_{DD}, Analog Gain = 12.6 V peak, R_L = 8 Ω

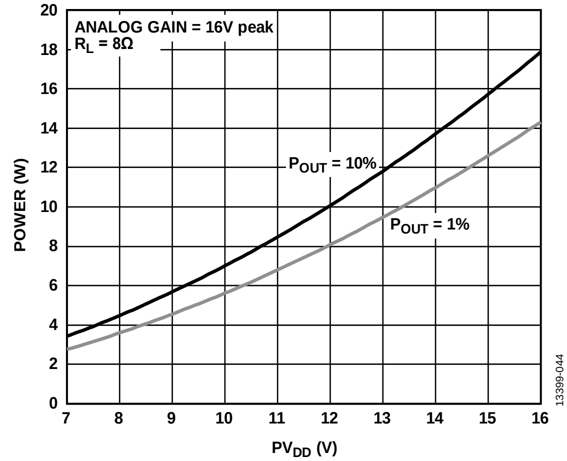


Figure 46. Power vs. PV_{DD}, Analog Gain = 16 V peak, R_L = 8 Ω

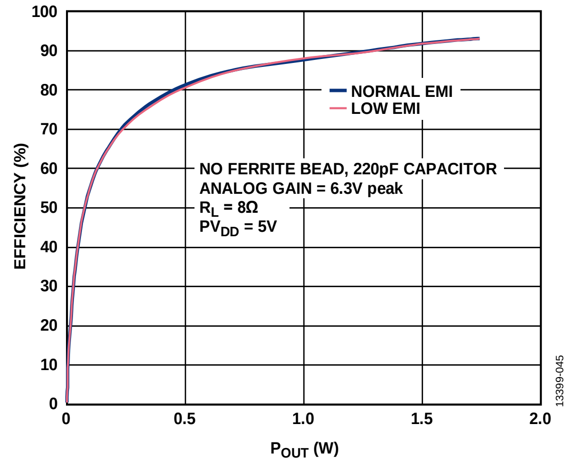


Figure 47. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 6.3 V peak, R_L = 8 Ω, PV_{DD} = 5 V

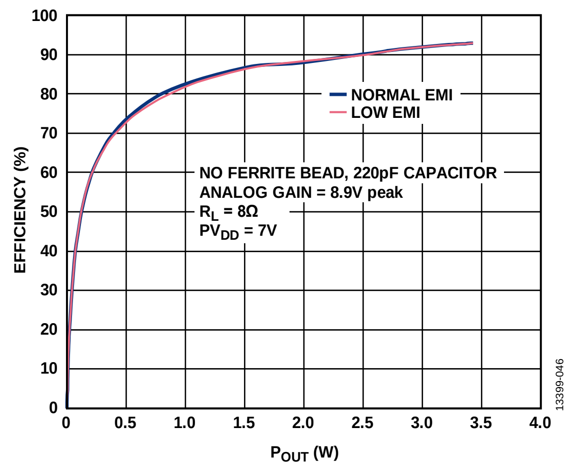


Figure 48. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 8.9 V peak, R_L = 8 Ω, PV_{DD} = 7 V

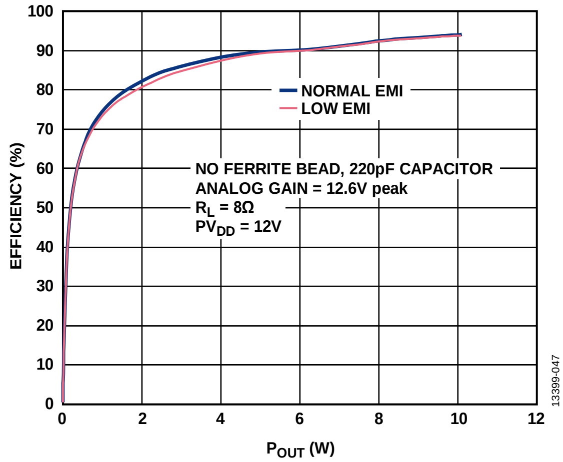


Figure 49. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 12.6 V peak, R_L = 8 Ω, PV_{DD} = 12 V

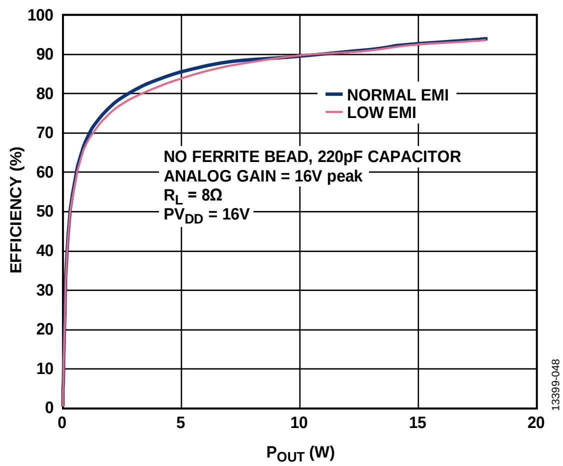


Figure 50. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 16 V peak, R_L = 8 Ω, PV_{DD} = 16 V

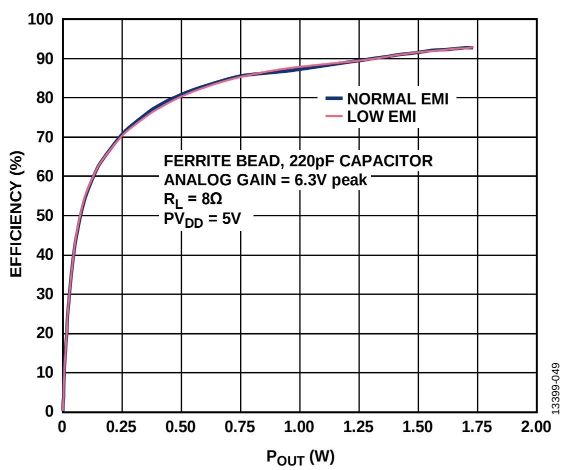


Figure 51. Efficiency vs. P_{OUT}, with Ferrite Bead, Analog Gain = 6.3 V peak, R_L = 8 Ω, PV_{DD} = 5 V

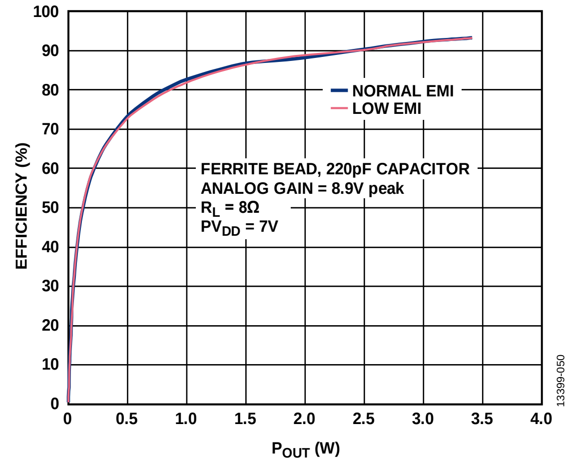


Figure 52. Efficiency vs. P_{OUT}, with Ferrite Bead, Analog Gain = 8.9 V peak, R_L = 8 Ω, PV_{DD} = 7 V

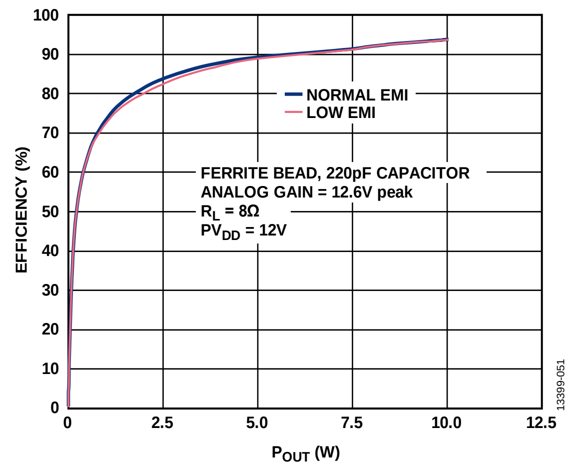


Figure 53. Efficiency vs. P_{OUT}, with Ferrite Bead, Analog Gain = 12.6 V peak, R_L = 8 Ω, PV_{DD} = 12 V

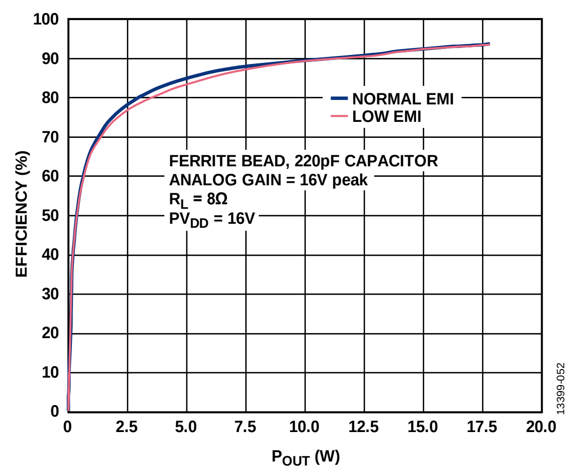


Figure 54. Efficiency vs. P_{OUT}, with Ferrite Bead, Analog Gain = 16 V peak, R_L = 8 Ω, PV_{DD} = 16 V

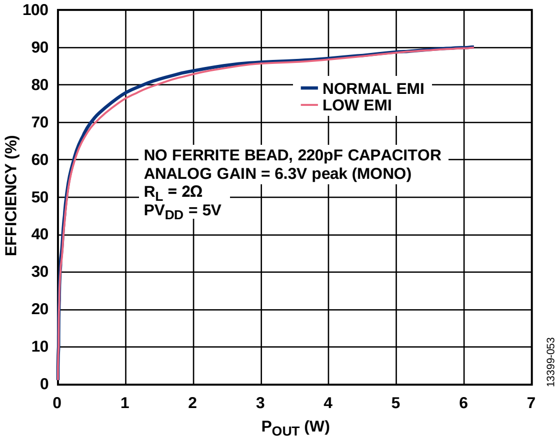


Figure 55. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 6.3 V peak, R_L = 2 Ω, PV_{DD} = 5 V

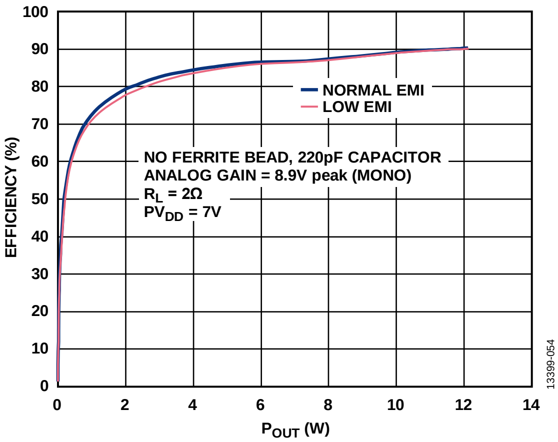


Figure 56. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 8.9 V peak, R_L = 2 Ω, PV_{DD} = 7 V

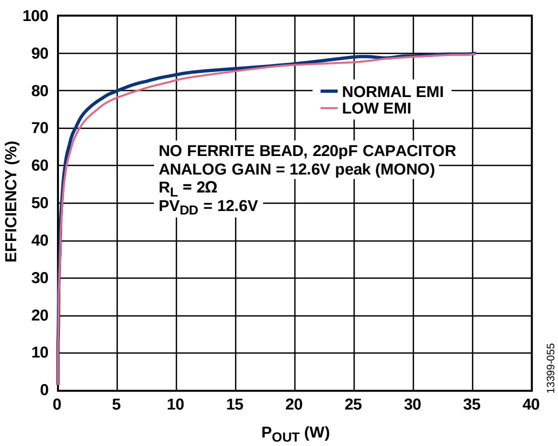


Figure 57. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 12.6 V peak, R_L = 2 Ω, PV_{DD} = 12.6 V

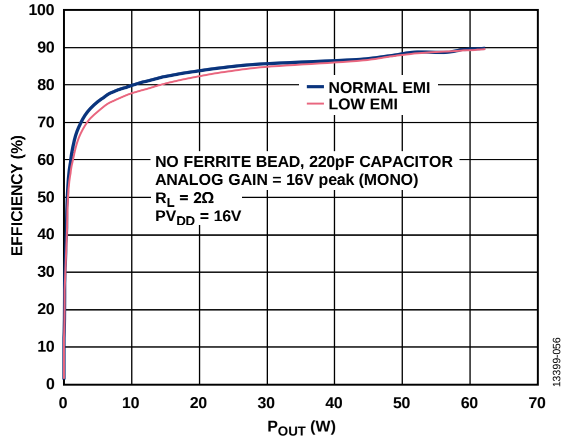


Figure 58. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 16 V peak, R_L = 2 Ω, PV_{DD} = 16 V

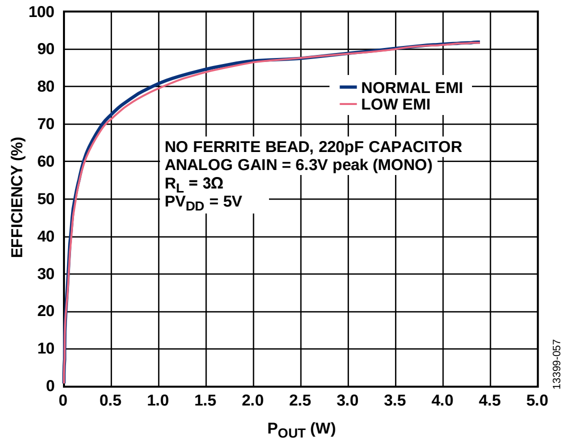


Figure 59. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 6.3 V peak, R_L = 3 Ω, PV_{DD} = 5 V

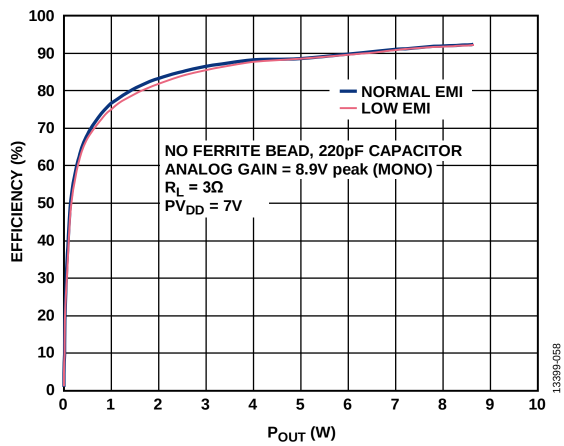


Figure 60. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 8.9 V peak, R_L = 3 Ω, PV_{DD} = 7 V

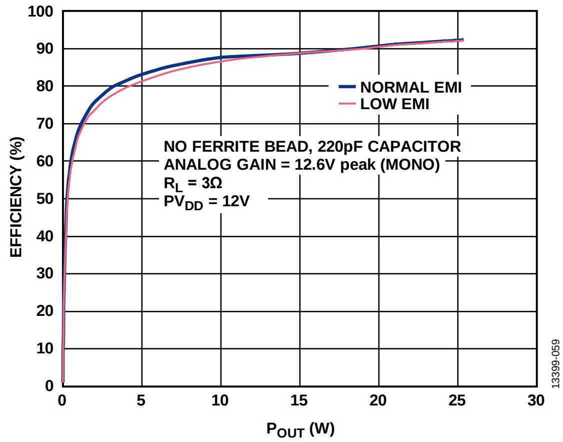


Figure 61. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 12.6 V peak, R_L = 3 Ω, PV_{DD} = 12 V

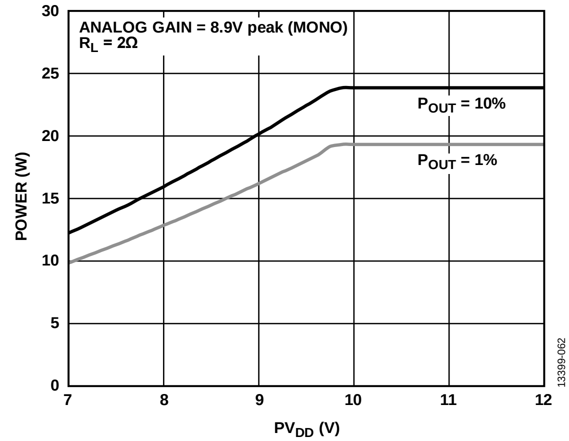


Figure 64. Power vs. PV_{DD}, Analog Gain = 8.9 V peak, R_L = 2 Ω

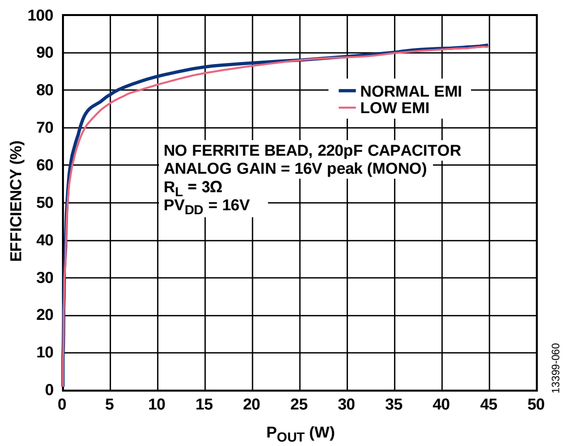


Figure 62. Efficiency vs. P_{OUT}, No Ferrite Bead, Analog Gain = 16 V peak, R_L = 3 Ω, PV_{DD} = 16 V

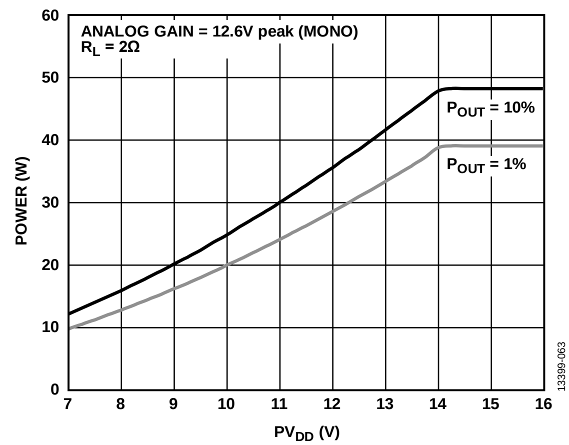


Figure 65. Power vs. PV_{DD}, Analog Gain = 12.6 V peak, R_L = 2 Ω

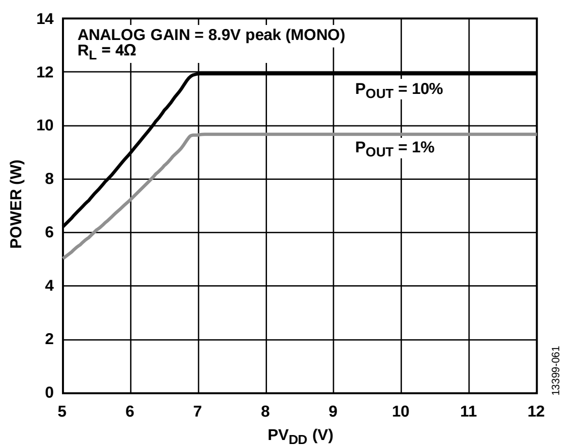


Figure 63. Power vs. PV_{DD}, Analog Gain = 8.9 V p-p, R_L = 4 Ω

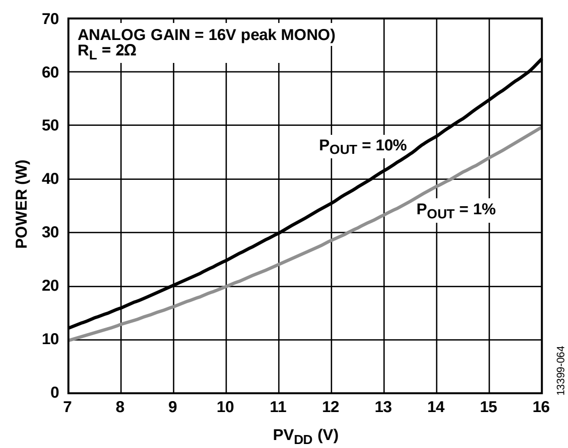


Figure 66. Power vs. PV_{DD}, Analog Gain = 16 V peak, R_L = 2 Ω

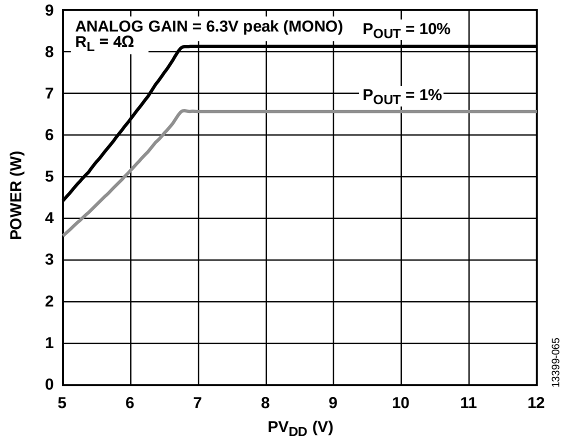


Figure 67. Power vs. PV_{DD}, Analog Gain = 6.3 V peak, R_L = 4 Ω

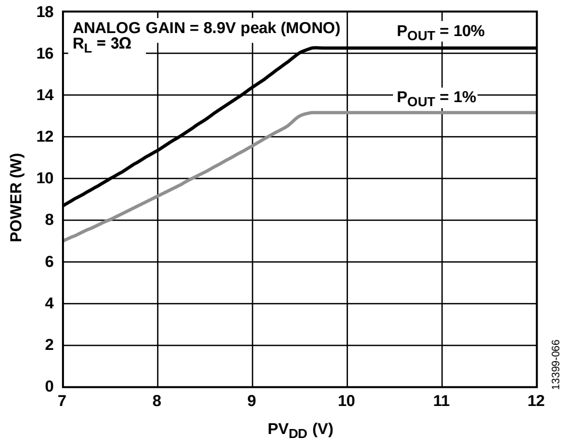


Figure 68. Power vs. PV_{DD}, Analog Gain = 8.9 V peak R_L = 3 Ω

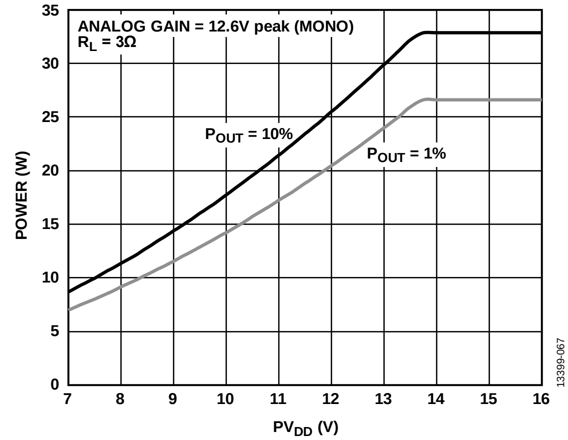


Figure 69. Power vs. PV_{DD}, Analog Gain = 12.6 V peak, R_L = 3 Ω

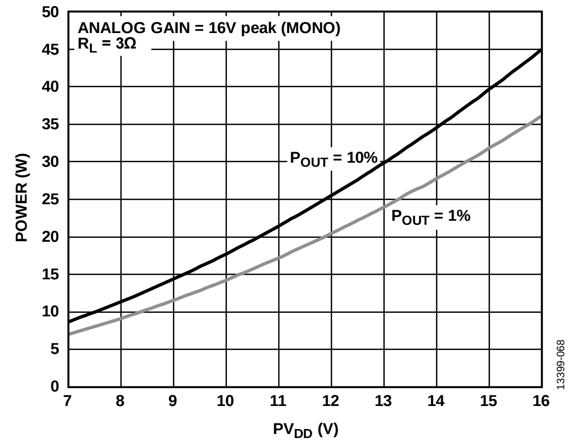


Figure 70. Power vs. PV_{DD}, Analog Gain = 16 V peak, R_L = 3 Ω

THEORY OF OPERATION

OVERVIEW

The SSM3582 is a stereo, Class-D audio amplifier with a filterless modulation scheme that greatly reduces external component count, conserving board space and reducing system cost. The SSM3582 does not require an output filter; it relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to recover the audio component of the square wave output. Most Class-D amplifiers use some variation of pulse-width modulation (PWM) to generate the output switching pattern, whereas the SSM3582 uses Σ-Δ modulation, resulting in important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM broadcast band, as pulse-width modulators often do. Σ-Δ modulation reduces the amplitude of spectral components at high frequencies, reducing EMI emission that may otherwise radiate from speakers and long cable traces. Due to the inherent spread spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM3582 amplifiers. The SSM3582 uses less power in quiescent conditions, which helps conserve the power drawn from the battery or power supply.

The SSM3582 integrates overcurrent and temperature protection and a thermal warning with optional programmable automatic gain reduction.

POWER SUPPLIES

PVDD

PVDD supplies the output power stages, as well as the low dropout (LDO) regulator for AVDD and DVDD.

AVDD

AVDD is the analog supply used for the modulator, power stage driver, and other analog blocks.

When the AVDD_EN pin = PVDD, the internal regulator generates 5 V and the AVDD pin is used for decoupling only.

When the AVDD_EN pin = AGND, 5 V must be provided to the AVDD pin from an external system source, minimizing power losses.

DVDD

DVDD supplies the digital circuitry. The current in this node is very low, below 1 mA.

When the DVDD_EN pin = AVDD, the internal regulator generates 1.8 V and the DVDD pin is used for decoupling only.

When the DVDD_EN pin = AGND, 1.8 V must be provided to the DVDD pin from an external system source, minimizing power losses.

Table 12 summarizes the power dissipation in various supply configurations, operating modes, and load characteristics.

Table 12. Typical Power Supply Current Consumption for f_S = 48 kHz[1]

						PVDD (V)					
						5		12		16	
AVDD_ EN Pin	Load	Test Conditions	AVDD Pin	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{PVDD} (mA)	Total Power (mW)	I_{PVDD} (mA)	Total Power (mW)	I_{PVDD} (mA)	Total Power (mW)
Low	No load	SPWDN = 1	External	0.007542	0.00268	0.000065	0.042859	0.000065	0.043314	0.000065	0.043574
		Automatic power-down	External	0.007542	0.04372	0.000065	0.116731	0.000065	0.117186	0.000065	0.117446
		Dither input	External	6.335	0.945	2.54	46.076	4.94	92.656	6.25	133.376
PVDD	No load	SPWDN = 1	Internal	N/A	N/A	0.000065	0.000325	0.000065	0.00078	0.000065	0.00104
		Automatic power-down	Internal	N/A	N/A	0.209	1.045	0.286	3.432	0.329	5.264
		Dither input	Internal	N/A	N/A	9.78	48.9	12.38	148.56	14.05	224.8
Low	8 Ω + 33 μH	SPWDN = 1	External	0.007542	0.00268	0.000065	0.042859	0.000065	0.043314	0.000065	0.043574
		Automatic power-down	External	0.007542	0.04372	0.000065	0.116731	0.000065	0.117186	0.000065	0.117446
		Dither input	External	6.432	0.942	2.59	46.8056	5.02	94.0956	6.31	134.8156
PVDD	8 Ω + 33 μH	SPWDN = 1	Internal	N/A	N/A	0.000065	0.000325	0.000065	0.00078	0.000065	0.00104
		Automatic power-down	Internal	N/A	N/A	0.209	1.045	0.286	3.432	0.329	5.264
		Dither input	Internal	N/A	N/A	9.82	49.1	12.39	148.68	13.73	219.68

[1] N/A means not applicable.

POWER-UP SEQUENCE

Using Only PVDD as a Source

When SSM3582 is used in single-supply mode, all internal rails are generated from PVDD. The internal AVDD (5 V) and DVDD (1.8 V) regulators can be enabled by pulling the AVDD_EN and DVDD_EN pins high. AVDD_EN is pulled to PVDD, and DVDD_EN is pulled to AVDD. The amplifier is operational and responds to I²C writes 10 ms after applying PVDD ≥ 5 V.

Using PVDD and External AVDD

Take care when an external 5 V is supplied to AVDD. The internal 5 V LDO must be disabled by pulling the AVDD_EN pin low. In this case, DVDD (1.8 V) is generated from PVDD. It is important to maintain PVDD > AVDD to prevent the back powering of PVDD.

Using PVDD and External AVDD and DVDD

If using an external AVDD and DVDD source, both the AVDD_EN and DVDD_EN pins must be pulled low. It is important to maintain PVDD > AVDD/DVDD to prevent back powering PVDD.

DVDD must be present for the device to respond to I²C commands. The device becomes operational ~10 ms after DVDD is present. PVDD must be at least 5 V for the output stage to turn on, and must be 6 V for optimal performance.

POWER-DOWN OPERATION

The SSM3582 offers several power-down options via the I²C. Register 0x04 provides multiple options for setting the various power-down modes.

When set to 1, the SPWDN bit fully powers down the device. In this case, only the I²C and 1.8 V regulator blocks, if enabled via the DVDD_EN pin, are kept active.

The SSM3582 monitors both the BCLK and FSYNC pins for clock presence. When no BCLK is present, the device automatically powers down all internal circuitry to its lowest power state. When BCLK returns, the device automatically powers up following its usual power sequence. To guarantee click/pop free shutdown, power down the device via the SPDWN control before clock removal.

If enabled, the APWDN_EN bit activates a low power state after 2048 consecutive zero input samples are received. Only the I²C and digital audio input blocks are kept active.

Individual channels can be powered down using Bits[3:2] in Register 0x04.

The temperature sense ADC can be powered down using Bit 5 in Register 0x04.

CLOCKING

A BCLK signal must be provided to the SSM3582 for proper operation. The BCLK signal must have a minimum frequency of 2.048 MHz. The BCLK rate is autodetected, but the sampling frequency must be indicated. The BCLK rates supported at 32 kHz to 48 kHz are 50, 64, 100, 128, 192, 200, 256, 384, 400, 512, 768, 800, and 1024 times the sample rate.

DIGITAL AUDIO SERIAL INTERFACE

The SSM3582 includes a standard serial audio interface that is slave only. The interface is capable of receiving I²S, left justified, PCM, or TDM formatted data.

The serial interfaces have three main operating modes. The stereo modes, typically I²S or left justified, are used when there is a single chip on the interface bus. TDM mode is more flexible and offers the ability to have multiple chips on the bus.

Stereo Operating Modes—I²S, Left Justified

Stereo modes use both edges of FSYNC to determine the placement of data. Stereo mode is enabled when SAI_MODE = 0, and the I²S or left justified format is determined by the SDATA_FMT register setting.

The I²S or left justified interface formats supports various BCLK/FSYNC ratios (see Table 13). Sample rates from 8 kHz to 192 kHz are accepted.

TDM Operating Mode

The TDM operating mode allows multiple chips to connect to a single serial interface.

The FSYNC signal operates at the desired sample rate. A rising edge of the FSYNC signal indicates the start of a new frame. For proper operation, this signal must be one BCLK cycle wide, transitioning on a falling BCLK edge. The MSB of data is present on the SDATA signal one BCLK cycle later. The SDATA signal is latched on a rising edge of BCLK.

Each chip on the TDM bus can occupy 16, 24, 32, 48, or 64 BCLK cycles, set via the TDM_BCLKS control bits. The maximum number of devices connected to a single TDM bus depends on the sample rate and number of bits per channel. The supported combinations of sample rates and bit depths are described in Table 13.

The maximum bit clock frequency is 49.152 MHz. Using the TDM16 format, up to eight devices (16 channels) can be connected to a single TDM interface, and can operate at up to a 96k sample rate and at 32 bits per channel. See Table 13 for the supported options at the 48 kHz, 96 kHz, and 192 kHz sample rates. Note that the interface is slave only, with the bit clock, frame sync, and data provided to the device.

ADDRx pin settings dictate the default TDM slots for each device, and can be modified using the TDM_SLOT control register.

Table 13. Supported BCLK Rates in MHz[1]

Sample Rate (kHz)	BCLK/FSYNC Ratio													
	50	64	100	128	192	200	256	384	512	768	800	1024	2048	4096
	BCLK (MHz)[2]													
8 to 12	N/A	N/A	N/A	N/A	N/A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
16 to 24	N/A	N/A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	N/A
32 to 48	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A
64 to 96	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	N/A
128 to 192	Yes	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A	N/A

[1] Yes means that the specified rate is supported and N/A means not applicable.
[2] BCLK = (BCLK/FSYNC ratio) × sample rate.

I²C Control

The SSM3582 supports an I²C-compatible, 2-wire serial bus, shared across multiple peripherals. Two signals, serial data (SDA) and serial clock (SCL), carry information between the SSM3582 and the system I²C master controller. The SSM3582 is always a slave on the bus, and cannot initiate a data transfer. Each slave device is identified by a unique address. The address byte format is shown in Table 14. The address resides in the first seven bits of the I²C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation and Logic Level 0 corresponds to a write operation. For device address settings, see Table 16.

Table 14. I²C Device Address Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
0	0	1	Bit 3	Bit 2	ADDR0	ADDR1	R/$\overline{\text{W}}$

Both SDA and SCL are open drain, and require pull-up resistors to the input/output voltage. The SSM3582 operates within the I²C voltage range of 1.6 V to 3.6 V.

Addressing

Initially, each device on the I²C bus is in an idle state, monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCL remains high. This start condition indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{\text{W}}$ bit), MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The device address for the SSM3582 is determined by the state of the ADDRx pins. See the Device Address Setting section for more details.

The R/$\overline{\text{W}}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means the master writes information to the peripheral, whereas a Logic 1 means the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. The timing for the I²C port is shown in Figure 71.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the SSM3582 immediately jumps to the idle condition. During a given SCL high period, issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued, the SSM3582 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in automatic-increment mode, one of two actions is taken.

In read mode, the SSM3582 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no acknowledge condition is a condition in which the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the SSM3582, and the device returns to the idle condition.

Device Address Setting

The device can be set at 16 different I²C addresses using the ADDR1 and ADDR0 pins, as well as 16 hardware modes.

ADDR1 and ADDR0 are sampled during the start-up procedure. These pins set the appropriate operating mode, the I²C address, and the default TDM slots. The ADDRx pins can be set to five different voltage levels, as defined in Table 15. The ADDRx pins are referenced to the DVDD rail of the device; connect pull-up resistors to the internally generated DVDD rail if the regulator is used.

Table 15. ADDRx Pin Input Level Mapping

ADDRx State	Level (V)
Connected to Ground	0
Connected to Ground Using a 47 kΩ Resistor	0.45
Left Floating	0.9
Connected to DVDD Using a 47 kΩ Resistor	1.35
Connected to DVDD	1.8

Table 16. ADDRx Pins to I²C Device Address and TDM Slot Mapping

ADDRx Pin State[1]			Default TDM Slot	
ADDR0	ADDR1	Device Address	MONO = 0	MONO = 1
0	0	0x10	1, 2	1
0	1	0x11	3, 4	2
1	0	0x12	5, 6	3
1	1	0x13	7, 8	4
0	Pull-down	0x14	9, 10	5
0	Pull-up	0x15	11, 12	6
1	Pull-down	0x16	13, 15	7
1	Pull-up	0x17	15, 16	8
Pull-down	0	0x18	17, 18	9
Pull-down	1	0x19	19, 20	10
Pull-up	0	0x1A	21, 22	11
Pull-up	1	0x1B	23, 24	12
Pull-down	Pull-down	0x1C	25, 26	13
Pull-down	Pull-up	0x1D	27, 28	14
Pull-up	Pull-down	0x1E	29, 30	15
Pull-up	Pull-up	0x1F	31, 32	16

[1] 0 = connect to ground, 1 = connect to DVDD. In the case of a pull-down state, connect to ground via a 47 kΩ resistor. In the case of a pull-up state, connect to DVDD via a 47 kΩ resistor.

I²C Read and Write Operations

Figure 72 shows the timing of a single-word write operation. Every ninth clock, the SSM3582 issues an acknowledge by pulling SDA low.

Figure 73 shows the timing of a burst mode write sequence. This figure shows an example where the target destination registers are two bytes. The SSM3582 knows to increment its subaddress register every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

The timing of a single-word read operation is shown in Figure 74. Note that the first R/$\overline{W}$ bit is 0, indicating a write operation, because the subaddress must still be written to set up the internal address. After the SSM3582 acknowledges the receipt of the subaddress, the master must issue a repeated start command, followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). This repeated command causes the SSM3582 SDA to reverse and to begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the SSM3582. Refer to Table 17 for a list of abbreviations in Figure 72 through Figure 75.

Table 17. Abbreviations for Figure 72 Through Figure 75

Symbol	Meaning
S	Start bit
P	Stop bit
A_M	Acknowledge (ACK used in Figure 72 through Figure 75) by master
A_S	Acknowledge (ACK used in Figure 72 through Figure 75) by slave

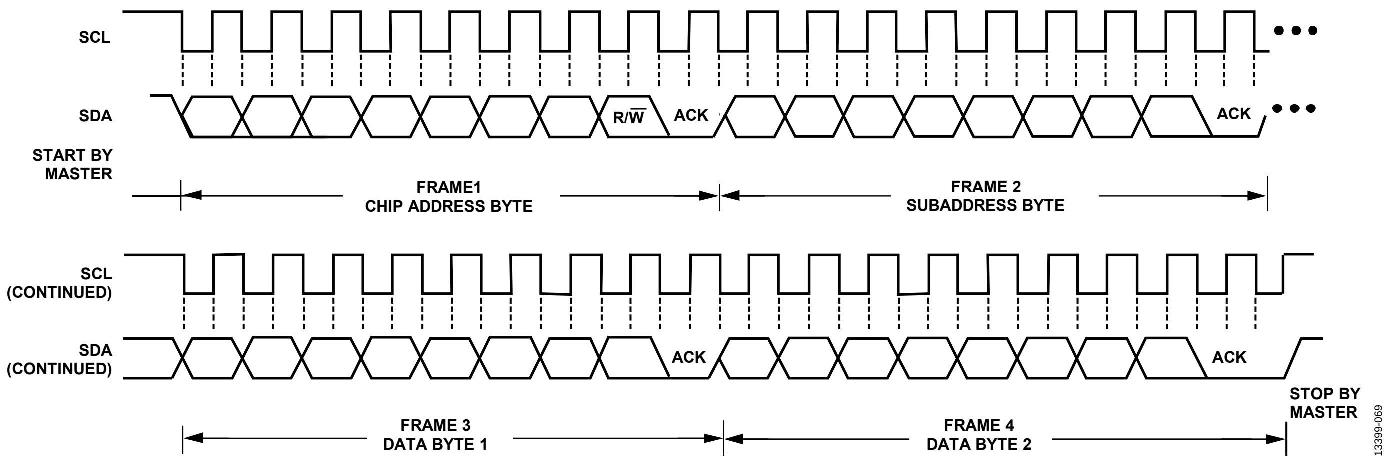


Figure 71. I²C Read/Write Timing

START BIT	IC ADDRESS (7 BITS)	R/$\overline{W}$ = 0	ACK BY SLAVE	SUBADDRESS (8 BITS)	ACK BY SLAVE	DATA BYTE 1 (8 BITS)	STOP BIT

Figure 72. Single-Word I²C Write Format

S	CHIP ADDRESS, R/$\overline{W}$ = 0	A_S	SUBADDRESS	A_S	DATA-WORD 1	A_S	DATA-WORD 2	A_S	...	P

Figure 73. Burst Mode I²C Write Format

S	CHIP ADDRESS, R/$\overline{W}$ = 0	A_S	SUBADDRESS	A_S	S	CHIP ADDRESS, R/$\overline{W}$ = 1	A_S	DATA BYTE 1	A_M	DATA BYTE N	P

Figure 74. Single-Word I²C Read Format

S	CHIP ADDRESS, R/$\overline{W}$ = 0	A_S	SUBADDRESS	A_S	S	CHIP ADDRESS, R/$\overline{W}$ = 1	A_S	DATA-WORD 1	A_M	...	P

Figure 75. Burst Mode I²C Read Format

STANDALONE OPERATION

The SSM3582 can be operated in a standalone hardware control mode without any I²C control. The same ADDRx pins used to set the I²C device address are used to set the functionality of the device. In standalone mode, the I²C pins (SCL and SDA) are inputs and are shorted to DVDD or AGND to set the TDM slot/sample rate of the device (see Table 18). In this case, the ANA_GAIN bits are set to 11 and SPWDN is set to 0 by default.

In standalone mode, TDM slot selection, mono mode operation, and sample rate are selected via different pin settings. The device looks at the FSYNC signal and, if it is a 50% duty cycle, uses I²S settings. If the FYSNC signal is a pulse, the device uses TDM settings.

Table 18. Standalone Mode Pin Settings and Functionality

	Pin States					
Sample Rate	**ADDR0**	**ADDR1**	**SDA**	**SCL**	**TDM Slot(s)**	**MONO**
32 kHz to 48 kHz	0	Open	0	0	1, 2	0
	1	Open	0	0	3, 4	0
	Pull-down	Open	0	0	5, 6	0
	Pull-up	Open	0	0	7, 8	0
	Open	0	0	0	9, 10	0
	Open	1	0	0	11, 12	0
	Open	Pull-down	0	0	13, 14	0
	Open	Pull-up	0	0	15, 16	0
8 kHz to 12 kHz	Open	Open	0	0	1, 2	0
32 kHz to 48 kHz	0	Open	0	1	1	1
	1	Open	0	1	2	1
	Pull-down	Open	0	1	3	1
	Pull-up	Open	0	1	4	1
	Open	0	0	1	5	1
	Open	1	0	1	6	1
	Open	Pull-down	0	1	7	1
	Open	Pull-up	0	1	8	1
8 kHz to 12 kHz	Open	Open	0	1	1, 2	1
64 kHz to 96 kHz	0	Open	1	0	1, 2	0
	1	Open	1	0	3, 4	0
	Pull-down	Open	1	0	5, 6	0
	Pull-up	Open	1	0	7, 8	0
	Open	0	1	0	9, 10	0
	Open	1	1	0	11, 12	0
	Open	Pull-down	1	0	13, 14	0
	Open	Pull-up	1	0	15, 16	0
16 kHz to 24 kHz	Open	Open	1	0	1, 2	0
64 kHz to 96 kHz	0	Open	1	1	1	1
	1	Open	1	1	2	1
	Pull-down	Open	1	1	3	1
	Pull-up	Open	1	1	4	1
	Open	0	1	1	5	1
	Open	1	1	1	6	1
	Open	Pull-down	1	1	7	1
	Open	Pull-up	1	1	8	1
128 kHz to 192 kHz	Open	Open	1	1	1, 2	0

MONO MODE

The SSM3582 can be operated in mono mode for driving low impedance loads. In mono mode, the left and right power stages can be connected in parallel, as shown in Figure 87. Use caution when setting up mono mode. For proper operation, any hardware changes are required along with setting the register. For mono mode operation, set MONO (Register 0x04, Bit 4) to 1. By default, this bit is set to 0 for stereo mode. After the bit is set for mono mode, only the left channel modulator is active and it feeds both the left and right channel power stages. The OUTL+ and OUTR+ pins are in phase. The OUTL− and OUTR− pins are also in phase. For mono mode, OUTL+ must be shorted to OUTR+; similarly, OUTL− must be shorted to OUTR−.

In standalone mode, the ADDR0, ADDR1, SCL, and SDA pins determine the TDM slot. See the Table 18 for the possible TDM slot configurations in mono mode.

ANALOG AND DIGITAL GAIN

Four different gain settings are available to optimize the dynamic range of the amplifier in relation to the PVDD supply voltage. In software mode, the initial 19 dB gain setting can be updated through the control interface. In standalone mode, the I²C interface pins set the gain of the device. Table 19 summarizes the gain settings and load drive characteristics of the amplifier.

The amplifier analog gain is set prior to enabling the device outputs and must not be changed during operation; a proper mute/unmute sequence is required to prevent audible transients between gain settings.

Finer level control is available in the digital domain, with a very flexible −70 dB to +24 dB, 0.375 dB/step ramp volume control and selectable nonaliasing clipping point. The digital volume control also includes a playback level limiter that can be set in tandem with the battery voltage monitor to prevent the amplifier from browning out the system when battery level is critically low.

Table 19. Analog Gain Settings and Drive Characteristics

ANA_GAIN[1:0]			V_{OUT}	
1	0	Gain, 1 V rms (dB)	RMS (V rms)	Peak-to-Peak (V)
0	0	13	4.47	6.32
0	1	16	6.31	8.92
1	0	19	8.91	12.60
1	1	21	11.20	15.87

POP AND CLICK SUPPRESSION

Pops and clicks are undesirable audible transients generated by the amplifier system that do not come from the system input signal. Voltage transients as small as 10 mV can be heard as an audible pop in the speaker. Voltage transients at the output of audio amplifiers often occur when shutdown is activated or deactivated. The SSM3582 has a pop and click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation. Set either mute or power-down before BCLK is removed to ensure a pop free experience.

TEMPERATURE SENSOR

The SSM3582 contains an 8-bit ADC that measures the die temperature of the device and is enabled via the TEMP_PWDN bit in Register 0x04. After the sensor is enabled, the temperature can be read via the I²C in the TEMP register, Register 0x1B. The temperature information is stored in Register 0x1B in an 8-bit, unsigned format. The ADC input range is fixed internally from −60°C to +195°C. To convert the hexadecimal value to the temperature (Celsius) value, use the following steps:

1. Convert the hexadecimal value to decimal and then subtract 60. For example, if the hexadecimal value is 0x54, the decimal value is 84.
2. Calculate the temperature using the following equation:

$$Temperature = Decimal\ Value - 60$$

With a decimal value of 84,

$$Temperature = 84 - 60 = 24°C$$

Table 20. Fault Reporting Registers

Fault Type	Flag Set Condition	Status Reported Register
PVDD Undervoltage (UV)	PVDD below <3.6 V	Register 0x18, Bit 7, UVLO_PVDD
5 V Regulator UV	5 V regulator voltage at AVDD < 3.6 V	Register 0x18, Bit 6, UVLO_VREG
Limiter/Gain Reduction Engage	Left channel limiter engaged	Register 0x19, Bit 3, LIM_EG_L
	Right channel limiter engaged	Register 0x19, Bit 7, LIM_EG_R
Clipping, Left Channel	Left channel DAC clipping	Register 0x19, Bit 2, CLIP_L
Clipping, Right Channel	Right channel DAC clipping	Register 0x19, Bit 6, CLIP_R
Output Overcurrent (OC)	Left channel output current > 6 A peak	Register 0x19, Bit 1, AMP_OC_L
	Right channel output current > 6 A peak	Register 0x19, Bit 5, AMP_OC_R
Die Overtemperature (OT)	Die temperature > 145°C	Register 0x18, Bit 1, OTF
Die Overtemperature Warning (OTW)	Die temperature > 117°C	Register 0x18, Bit 0, OTW
Battery Voltage > VBAT_INF_x	Battery voltage PV_{DD} > VBAT_INF_L	Register 0x19, Bit 0, BAT_WARN_L
	Battery voltage PV_{DD} > VBAT_INF_R	Register 0x19, Bit 4, BAT_WARN_R

FAULTS AND LIMITER STATUS REPORTING

The SSM3582 offers comprehensive protections against the faults at the outputs and reporting to help with system design. The faults listed in Table 20 are reported using the status registers.

The faults listed in Table 20 are reported in Register 0x18 and Register 0x19 and can be read via I²C by the microcontroller in the system.

In the event of a fault occurrence, use Register 0x0B to control how the device reacts to the faults.

Table 21. Register 0x16, Register 0x17, Fault Recovery

Fault Type	Flag Set Condition	Status Reported Register
OTW	The amount of gain reduction applied if there is an OTW for left channel	Register 0x16, Bits[1:0], OTW_GAIN_L
	The amount of gain reduction applied if there is an OTW for the right channel	Register 0x16, Bits[5:4], OTW_GAIN_R
Manual Recovery	Use to attempt manual recovery in case of a fault event	Register 0x17, Bit 7, MRCV
Autorecovery Attempts	When autorecovery from faults is used, set the number of attempts using this bit	Register 0x17, Bits[5:4], MAX_AR
UV	Recovery can be automatic or manual	Register 0x17, Bit 2, ARCV_UV
Die OT	Recovery can be automatic or manual	Register 0x17, Bit 1, ARCV_OT
OC	Recovery can be automatic or manual	Register 0x17, Bit 0, ARCV_OC

When the automatic recovery mode is set, the device attempts to recover itself after the fault event and, in case the fault persists, then the device sets the fault again. This process repeats until the fault is resolved.

When the manual recovery mode is used, the device shuts down and the recovery must be attempted using the system microcontroller.

VBAT (PV_{DD}) SENSING

The SSM3582 contains an 8-bit ADC that measures the voltage of the battery voltage (VBAT/PV_{DD}) supply. The battery voltage information is stored in Register 0x1A as an 8-bit unsigned format. The ADC input range is fixed internally at 3.8 V to 16.2 V. To convert the hexadecimal value to the voltage value, use the following steps:

Convert the hexadecimal value to decimal. For example, if the hexadecimal value is 0xA9, the decimal value is 169.

Calculate the voltage using the following equation:

$$Voltage = 3.8\text{ V} + 12.4\text{ V} \times Decimal\ Value/255$$

With a decimal value of 169,

$$Voltage = 3.8\text{ V} + 12.4\text{ V} \times 169/255 = 12.02\text{ V}$$

LIMITER AND BATTERY TRACKING THRESHOLD CONTROL

The SSM3582 contains an output limiter that can be used to limit the peak output voltage of the amplifier. The limiter works on the rms and peak value of the signal. The limiter threshold, slope, attack rate, and release rate are programmable using Register 0x0E, Register 0x0F, and Register 0x10 for the left channel and Register 0x11, Register 0x12, Register 0x13 for the right channel. The limiter can be enabled or disabled using LIM_EN_L, Bits[1:0] in Register 0x0E, Bits[1:0] for the left channel and the LIM_EN_R bits, Bits[1:0] in Register 0x11, for the right channel.

The threshold at which the output is limited is determined by the LIM_THRES_L bits setting, Bits[7:3] in Register 0x0F for the left channel, and the LIM_THRES_R bits setting, Bits[7:3] in Register 0x12 for the right channel. When the ouput signal level exceeds the set threshold level, the limiter activates and limits the signal level to the set limit. Below the set threshold, the output level is not affected.

The limiter threshold can be set above the maximum output voltage of the amplifier. In this case, the limiter allows maximum peak output; in other words, the output may clip depending on the power supply voltage and not the limiter.

The limiter threshold can be set as fixed or to vary with the battery voltage via the VBAT_TRACK_L bit (Register 0x0E, Bit 2) for the left channel and VBAT_TRACK_R bit (Register 0x11, Bit 2) for right channel. When set to fixed, the limiter threshold is fixed and does not vary with battery voltage. The threshold can be set from 2 V peak to 16 V peak using the LIM_THRES_x bit (see Figure 77).

When set to a variable threshold, the SSM3582 monitors the VBAT supply and automatically adjusts the limiter threshold based on the VBAT supply voltage.

The VBAT supply voltage at which the limiter begins to decrease the output level is determined by the VBAT inflection point (the VBAT_INF _L bits (Register 0x10, Bits[7:0]) for the left channel and VBAT_INF_R bits (Register 0x13, Bits[7:0]) for the right channel).

The VBAT_INF_x point is defined as the battery voltage at which the limiter either activates or deactivates depending on the LIM_EN_x mode (see Table 22). When the battery voltage is greater than VBAT_INF_x, the limiter is not active. When the battery voltage is less than VBAT_INF_X, the limiter is activated. The VBAT_INF_x bits can be set from 3.8 V to 16.2 V. The 8-bit value for the voltage can be calculated using the following equation:

$$Voltage = 3.8 + 12.4 \times Decimal\ Value/255$$

Convert the decimal value to an 8-bit hexadecimal value and use it to set the VBAT_INF_x bits.

The slope bits (Register 0x0F and Register 0x12, Bits[1:0]) determine the rate at which the limiter threshold is lowered relative to the amount of change in VBAT below the VBAT_INF_x point.

The slope is the ratio of the limiter threshold reduction to the VBAT voltage reduction.

$$Slope = \Delta Limiter\ Threshold/\Delta VBAT$$

The slope ratio can be set from 1:1 to 4:1. This function is useful to prevent early shutdown under low battery conditions. As the VBAT voltage falls, the limiter threshold is lowered. This lower threshold results in the lower output level and therefore helps to reduce the current drawn from the battery and in turn helps prevent early shutdown due to low VBAT.

The limiter offers various active modes that can be set using the LIM_EN_x bits (Register 0x0E and Register 0x11, Bits[1:0]) and the VBAT_TRACK_x bit, as shown in Table 22.

When LIM_EN_x = 01, the limiter is enabled. When LIM_EN_x = 10, the limiter mutes the output if VBAT falls below VBAT_INF_x. When LIM_EN_x = 11, the limiter engages only when the battery voltage is lower than VBAT_INF_x. When VBAT is greater than VBAT_INF_x, no limiting occurs. Note that there is hysteresis on VBAT_INF_x for the limiter disengaging.

The limiter, when active, reduces the gain of the amplifier. The rate of gain reduction or attack rate is determined by the LIM_ATR_x bits (Register 0x0E and Register 0x11, Bits[5:4]). Similarly, when the signal level drops below the limiter threshold, the gain is restored. The gain release rate is determined by the LIM_RRT bits (Register 0x0E and Register 0x11, Bits[7:6]).

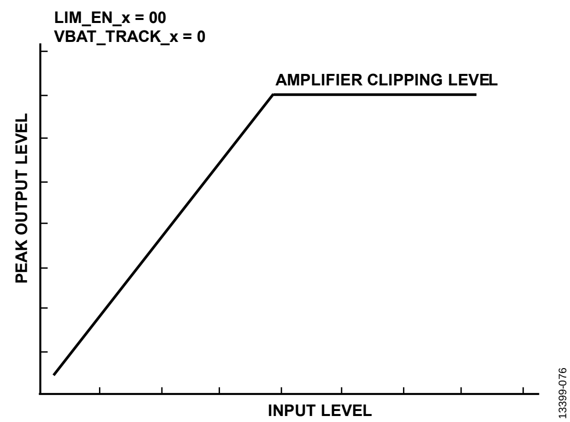


Figure 76. Limiter Example (LIM_EN_x = 0b0, VBAT_TRACK_x = 0bX)

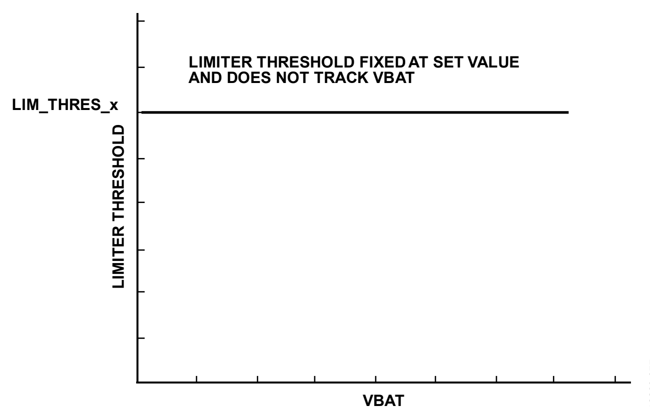


Figure 77. Limiter Fixed (LIM_EN_x = 0b01, VBAT_TRACK_x = 0b0)

Table 22. Limiter Modes

LIM_EN_x	VBAT_TRACK_x	Limiter	VBAT < VBAT_INF_x	VBAT > VBAT_INF_x	Comments
00	0 or 1	No	Not applicable	Not applicable	See Figure 76
01	0	Fixed	Use the set threshold	Use the set threshold	See Figure 77
01	1	Variable	Lowers the threshold	Use the set threshold	See Figure 78 and Figure 79
10	0 or 1	Fixed	Mutes the output	Use the set threshold	Not shown
11	0	Fixed	Use the set threshold	No limiting	See Figure 80 and Figure 81
11	1	Variable	Lowers the threshold	No limiting	See Figure 82 and Figure 83

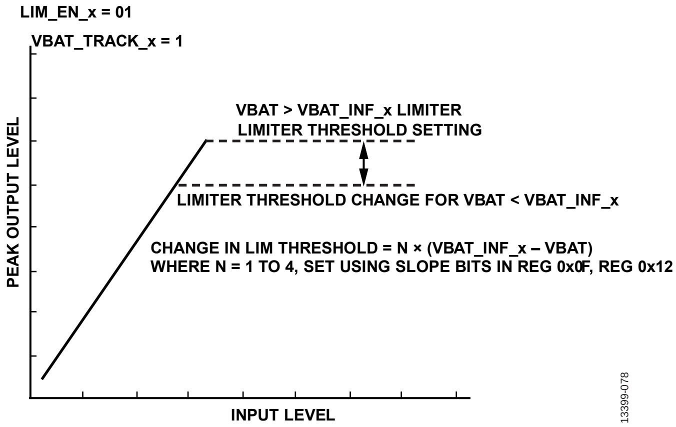


Figure 78. Limiter Fixed (LIM_EN_x = 0b01, VBAT_TRACK_x = 0b1)

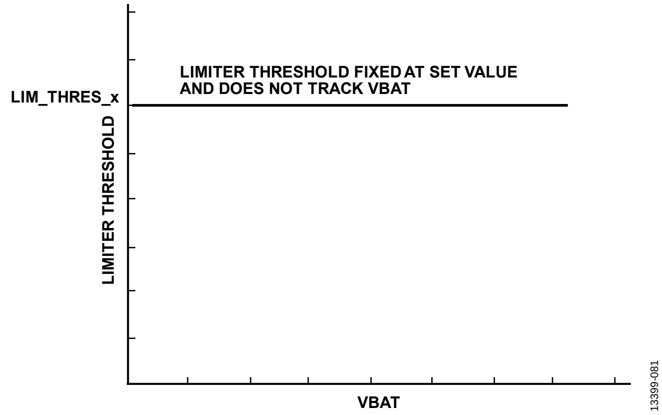


Figure 81. Limiter Fixed (LIM_EN_x = 0b11, VBAT_TRACK_x = 0b0)

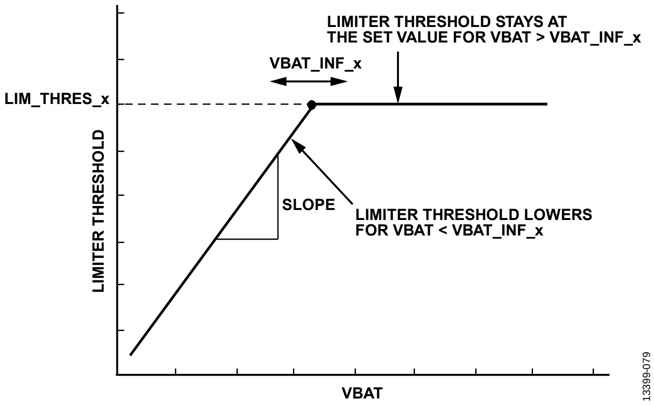


Figure 79. Output Level vs. VBAT in Limiter Tracking Mode (LIM_EN_x = 0b01, VBAT_TRACK_x = 0b1)

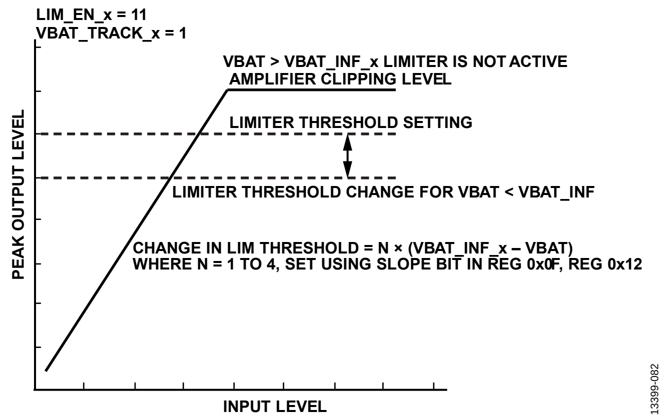


Figure 82. Limiter Example (LIM_EN_x = 0b11, VBAT_TRACK_x = 0b1)

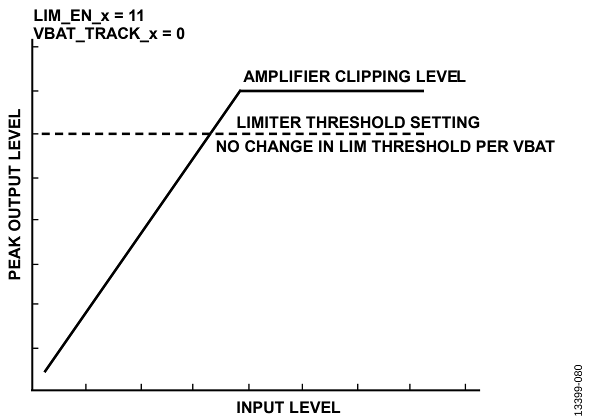


Figure 80. Limiter Example (LIM_EN_x = 0b11, VBAT_TRACK_x = 0)

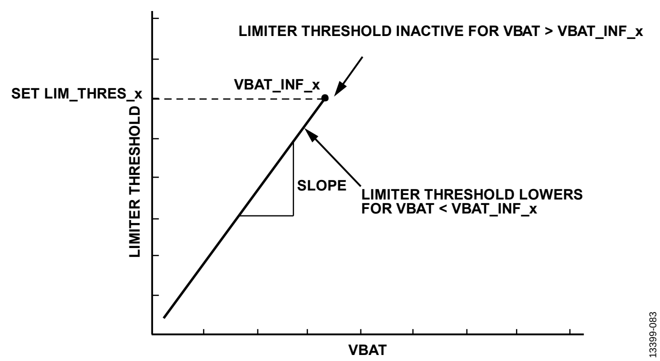


Figure 83. Output Level vs. VBAT in Limiter Tracking Mode (LIM_EN_x = 0b11, VBAT_TRACK_x = 0b1)

HIGH FREQUENCY CLIPPER

The high frequency clipper can be controlled via the DAC_CLIP_L bits (Register 0x14, Bits[7:0]) and the DACL_CLIP_R bits (Register 0x15, Bits[7:0]).

These bits determine the clipper threshold, relative to full scale. When enabled, the clipper digitally clips the signal after the DAC interpolation.

EMI NOISE

The SSM3582 uses a proprietary modulation and spread spectrum technology to minimize EMI emissions from the device. The SSM3582 passes FCC Class-B emissions testing with an unshielded 20 inch cable using ferrite bead-based filtering. For applications that have difficulty passing FCC Class-B emission tests, the SSM3582 includes an ultralow EMI emissions mode that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. Note that reducing the supply voltage greatly reduces radiated emissions.

OUTPUT MODULATION DESCRIPTION

The SSM3582 uses three level, Σ-Δ output modulation. Each output can swing from ground to PV_{DD}, and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, noise sources are always present.

Due to this constant presence of noise, a differential pulse is occasionally generated in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated. However, typically, the output differential voltage is 0 V. This feature ensures that the current flowing through the inductive load is small.

When the user sends an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 84 depicts three-level, Σ-Δ output modulation with and without input stimulus.

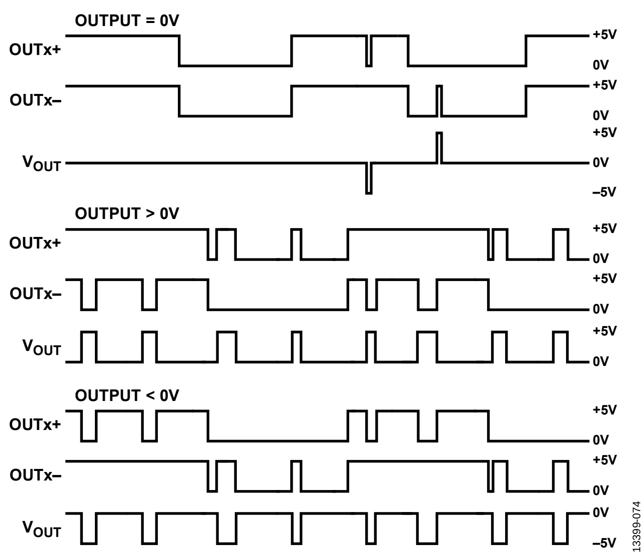


Figure 84. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

BOOTSTRAP CAPACITORS

The output stage of the SSM3582 uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate drive voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22 μF capacitors to connect the appropriate output pin (OUTx±) to the bootstrap pin (BSTx±). For example, connect a 0.22 μF capacitor between OUTL+ (a left channel, noninverting output) and BSTL+ for bootstrapping the left channel. Similarly, connect another 0.22 μF capacitor between the OUTL− and BSTL− pins for the left channel inverting output.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with a good quality, low ESL, low ESR bulk capacitor larger than 220 μF. This capacitor bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1 μF capacitors as close as possible to the PVDD pins of the device.

OUTPUT EMI FILTERING

Additional EMI filtering may be required when the speaker traces and cables are long and present a significant capacitive load that can create additional draw from the amplifier. Typical power ferrites present a significant magnetic hysteresis cycle that affects THD performance and are not recommended for high performance designs. The NFZ filter series from Murata, designed in close collaboration with Analog Devices, Inc., provides a closed hysteresis loop similar to an air coil with minimum impact on performance. Products are available at upwards of 4 A rms, well suited to this application. A small capacitor can be added between the output of the filter and ground to further attenuate very high frequencies. Take care to ensure the capacitor is properly sized so as not to affect idle power consumption or efficiency.

PCB PLACEMENT

Component selection and placement have great influence on system performance, both measured and subjective. Proper PVDD layout and decoupling is necessary to reach the specified level of performance, particularly at the highest power levels. The placement shown in Figure 85 ensures proper output stage decoupling for each channel, for minimum supply noise and maximum separation between channels. Additional bulk decoupling is necessary to reduce current ripple at low frequencies, and can be shared between several amplifiers in a multichannel solution.

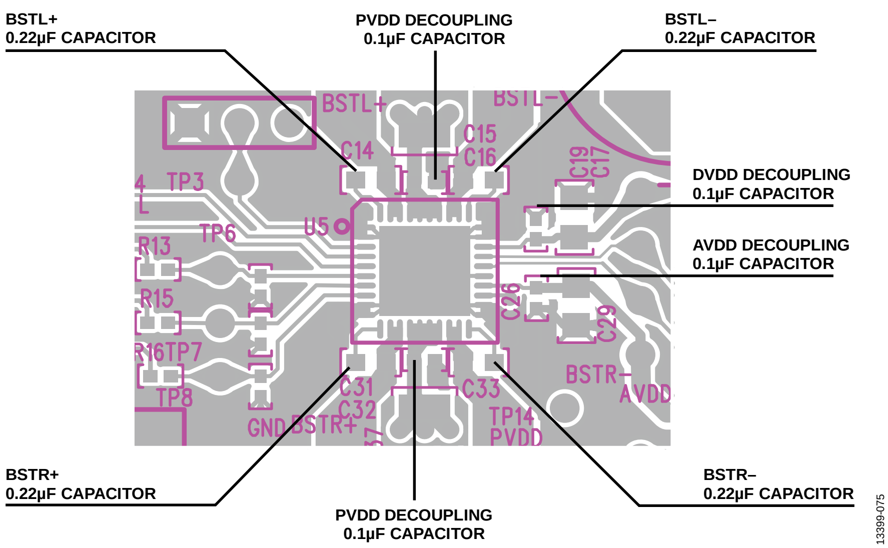


Figure 85. Recommended Component Placement

LAYOUT

As output power increases, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply; a poor layout increases voltage drops, consequently decreasing efficiency. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. For the lowest dc resistance (DCR) and minimum inductance, ensure that track widths for the outputs are at least 200 mil for every inch of length and use 1 oz. or 2 oz. copper.

To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins must be as wide as possible; this also maintains the minimum trace resistances. In addition, good PCB layout isolates critical analog paths from sources of high interference. Separate high frequency circuits (analog and digital) from low frequency circuits.

PVDD and PGND carry most of the device current, and must be properly decoupled with multiple capacitors at the device pins. To minimize ground bounce, use independent large traces to carry PVDD and PGND to the power supply, thus reducing the amount of noise the amplifier bridges inject in the circuit, particularly if common ground impedance is significant. Proper grounding guidelines help improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal.

Properly designed multilayer PCBs can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane must be directly beneath the analog power plane, and, similarly, the digital ground plane must be directly beneath the digital power plane. There must be no overlap between the analog and digital ground planes or between the analog and digital power planes.

REGISTER SUMMARY

Table 23. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	VENDOR_ID	[7:0]	VENDOR								0x41	R
0x01	DEVICE_ID1	[7:0]	DEVICE1								0x35	R
0x02	DEVICE_ID2	[7:0]	DEVICE2								0x82	R
0x03	REVISION	[7:0]	REV								0x01	R
0x04	POWER_CTRL	[7:0]	APWDN_EN	RESERVED	TEMP_PWDN	MONO	R_PWDN	L_PWDN	RESERVED	SPWDN	0xA1	R/W
0x05	AMP_DAC_CTRL	[7:0]	DAC_LPM	RESERVED	DAC_POL_R	DAC_POL_L	EDGE	RESERVED	ANA_GAIN		0x8A	R/W
0x06	DAC_CTRL	[7:0]	DAC_HV	DAC_MUTE_R	DAC_MUTE_L	DAC_HPF	RESERVED	DAC_FS			0x02	R/W
0x07	VOL_LEFT_CTRL	[7:0]	VOL_L								0x40	R/W
0x08	VOL_RIGHT_CTRL	[7:0]	VOL_R								0x40	R/W
0x09	SAI_CTRL1	[7:0]	RESERVED	BCLK_POL	TDM_BCLKS			FSYNC_MODE	SDATA_FMT	SAI_MODE	0x11	R/W
0x0A	SAI_CTRL2	[7:0]	SDATA_EDGE	RESERVED		DATA_WIDTH	VOL_ZC_ONLY	CLIP_LINK	VOL_LINK	AUTO_SLOT	0x07	R/W
0x0B	SLOT_LEFT_CTRL	[7:0]	RESERVED			TDM_SLOT_L					0x00	R/W
0x0C	SLOT_RIGHT_CTRL	[7:0]	RESERVED			TDM_SLOT_R					0x01	R/W
0x0E	LIM_LEFT_CTRL1	[7:0]	LIM_RRT_L		LIM_ATR_L		RESERVED	VBAT_TRACK_L	LIM_EN_L		0xA0	R/W
0x0F	LIM_LEFT_CTRL2	[7:0]	LIM_THRES_L					RESERVED	SLOPE_L		0x51	R/W
0x10	LIM_LEFT_CTRL3	[7:0]	VBAT_INF_L								0x22	R/W
0x11	LIM_RIGHT_CTRL1	[7:0]	LIM_RRT_R		LIM_ATR_R		LIM_LINK	VBAT_TRACK_R	LIM_EN_R		0xA8	R/W
0x12	LIM_RIGHT_CTRL2	[7:0]	LIM_THRES_R					RESERVED	SLOPE_R		0x51	R/W
0x13	LIM_RIGHT_CTRL3	[7:0]	VBAT_INF_R								0x22	R/W
0x14	CLIP_LEFT_CTRL	[7:0]	DAC_CLIP_L								0xFF	R/W
0x15	CLIP_RIGHT_CTRL	[7:0]	DAC_CLIP_R								0xFF	R/W
0x16	FAULT_CTRL1	[7:0]	RESERVED		OTW_GAIN_R		RESERVED		OTW_GAIN_L		0x00	R/W
0x17	FAULT_CTRL2	[7:0]	MRCV	RESERVED	MAX_AR		RESERVED	ARCV_UV	ARCV_OT	ARCV_OC	0x30	R/W
0x18	STATUS1	[7:0]	UVLO_PVDD	UVLO_VREG	RESERVED				OTF	OTW	0x00	R
0x19	STATUS2	[7:0]	LIM_EG_R	CLIP_R	AMP_OC_R	BAT_WARN_R	LIM_EG_L	CLIP_L	AMP_OC_L	BAT_WARN_L	0x00	R
0x1A	VBAT	[7:0]	VBAT								0x00	R
0x1B	TEMP	[7:0]	TEMP								0x00	R
0x1C	SOFT_RESET	[7:0]	RESERVED							S_RST	0x00	R/W

REGISTER DETAILS

Address: 0x00, Reset: 0x41, Name: VENDOR_ID

Table 24. Bit Descriptions for VENDOR_ID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR		Vendor ID	0x41	R

Address: 0x01, Reset: 0x35, Name: DEVICE_ID1

Table 25. Bit Descriptions for DEVICE_ID1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVICE1		Device ID 1	0x35	R

Address: 0x02, Reset: 0x82, Name: DEVICE_ID2

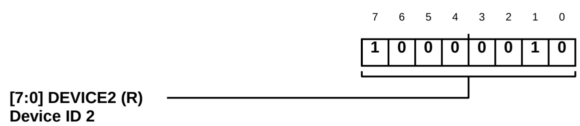


Table 26. Bit Descriptions for DEVICE_ID2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVICE2		Device ID 2	0x82	R

Address: 0x03, Reset: 0x01, Name: REVISION

Table 27. Bit Descriptions for REVISION

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	REV		Revision Code	0x1	R

Address: 0x04, Reset: 0xA1, Name: POWER_CTRL

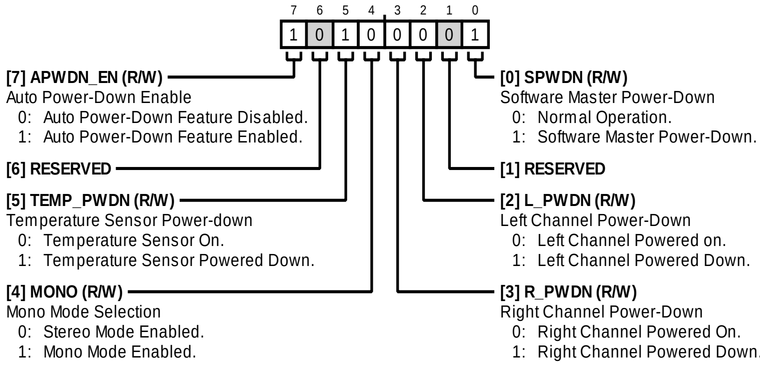


Table 28. Bit Descriptions for POWER_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	APWDN_EN		Automatic Power-Down Enable.	0x1	R/W
		0	Automatic power-down feature disabled.		
		1	Automatic power-down feature enabled.		
6	RESERVED		Reserved.	0x0	R
5	TEMP_PWDN		Temperature Sensor Power-Down.	0x1	R/W
		0	Temperature sensor on.		
		1	Temperature sensor powered down.		
4	MONO		Mono Mode Selection.	0x0	R/W
		0	Stereo mode enabled.		
		1	Mono mode enabled.		
3	R_PWDN		Left Channel Power-Down.	0x0	R/W
		0	Right channel powered on.		
		1	Right channel powered down.		
2	L_PWDN		Left Channel Power-Down.	0x0	R/W
		0	Left channel powered on.		
		1	Left channel powered down.		
1	RESERVED		Reserved.	0x0	R
0	SPWDN		Software Master Power-Down	0x1	R/W
		0	Normal operation.		
		1	Software master power-down.		

Address: 0x05, Reset: 0x8A, Name: AMP_DAC_CTRL

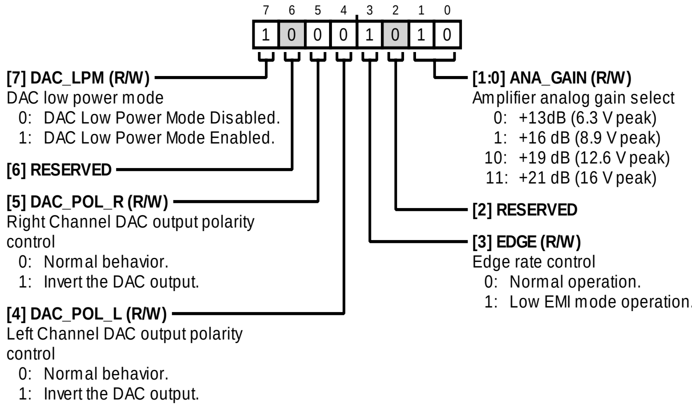


Table 29. Bit Descriptions for AMP_DAC_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC_LPM		DAC Low Power Mode.	0x1	R/W
		0	DAC low power mode disabled.		
		1	DAC low power mode enabled.		
6	RESERVED		Reserved.	0x0	R
5	DAC_POL_R		Right Channel DAC Output Polarity Control.	0x0	R/W
		0	Normal behavior.		
		1	Invert the DAC output.		
4	DAC_POL_L		Left Channel DAC Output Polarity Control.	0x0	R/W
		0	Normal behavior.		
		1	Invert the DAC output.		
3	EDGE		Edge Rate Control.	0x1	R/W
		0	Normal operation.		
		1	Low EMI mode operation.		
2	RESERVED		Reserved.	0x0	R
[1:0]	ANA_GAIN		Amplifier Analog Gain Select.	0x2	R/W
		0	+13 dB (6.3 V peak).		
		1	+16 dB (8.9 V peak).		
		10	+19 dB (12.6 V peak).		
		11	+21 dB (16 V peak).		

Address: 0x06, Reset: 0x02, Name: DAC_CTRL

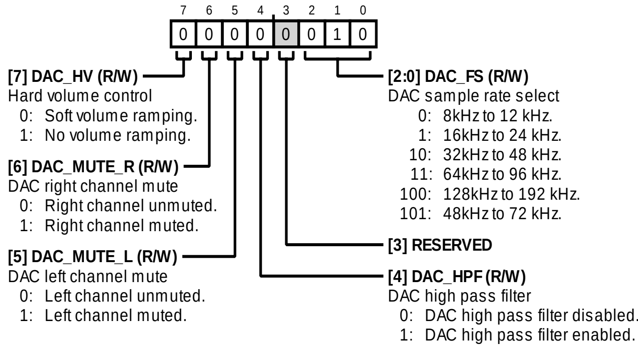


Table 30. Bit Descriptions for DAC_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC_HV		Hard Volume Control.	0x0	R/W
		0	Soft Volume Ramping.		
		1	No Volume Ramping.		
6	DAC_MUTE_R		DAC Right Channel Mute.	0x0	R/W
		0	Right Channel Unmuted.		
		1	Right Channel Muted.		
5	DAC_MUTE_L		DAC Left Channel Mute.	0x0	R/W
		0	Left Channel Unmuted.		
		1	Left Channel Muted.		
4	DAC_HPF		DAC High-Pass Filter.	0x0	R/W
		0	DAC High-Pass Filter Disabled.		
		1	DAC High-Pass Filter Enabled.		
3	RESERVED		Reserved.	0x0	R
[2:0]	DAC_FS		DAC Sample Rate Select.	0x2	R/W
		0	8 kHz to 12 kHz.		
		1	16 kHz to 24 kHz.		
		10	32 kHz to 48 kHz.		
		11	64 kHz to 96 kHz.		
		100	128 kHz to 192 kHz.		
		101	48 kHz to 72 kHz.		

Address: 0x07, Reset: 0x40, Name: VOL_LEFT_CTRL

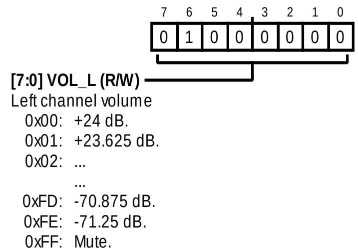


Table 31. Bit Descriptions for VOL_LEFT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VOL_L		Left Channel Volume	0x40	R/W
		0x00	+24 dB		
		0x01	+23.625 dB		
		0x02	…		
		0x3F	+0.375 dB		
		0x40	0 dB		
		0x41	−0.375 dB		
		0x42	…		
		0xFD	−70.875 dB		
		0xFE	−71.25 dB		
		0xFF	Mute		

Address: 0x08, Reset: 0x40, Name: VOL_RIGHT_CTRL

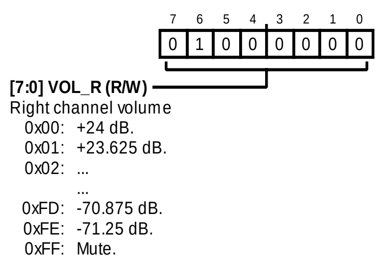


Table 32. Bit Descriptions for VOL_RIGHT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VOL_R		Right Channel Volume	0x40	R/W
		0x00	+24 dB		
		0x01	+23.625 dB		
		0x02	…		
		0x3F	+0.375 dB		
		0x40	0 dB		
		0x41	−0.375 dB		
		0x42	…		
		0xFD	−70.875 dB		
		0xFE	−71.25 dB		
		0xFF	Mute		

Address: 0x09, Reset: 0x11, Name: SAI_CTRL1

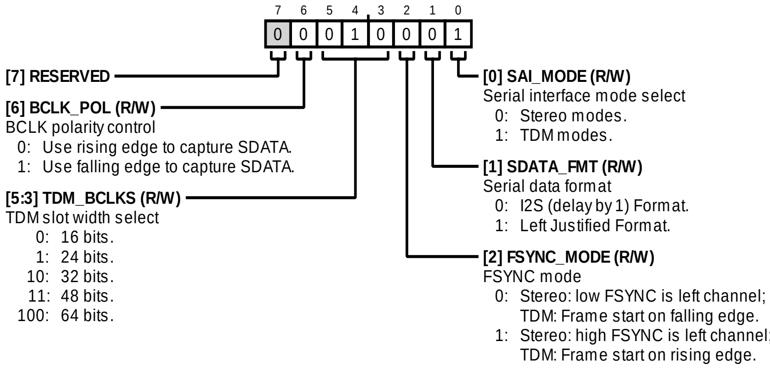


Table 33. Bit Descriptions for SAI_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	BCLK_POL		BCLK Polarity Control	0x0	R/W
		0	Use Rising Edge to Capture SDATA		
		1	Use Falling Edge to Capture SDATA		
[5:3]	TDM_BCLKS		TDM Slot Width Select	0x2	R/W
		0	16 Bits		
		1	24 Bits		
		10	32 Bits		
		11	48 Bits		
		100	64 Bits		
2	FSYNC_MODE		FSYNC Mode	0x0	R/W
		0	Stereo: Low FSYNC is Left Channel; TDM: Frame Start on Falling Edge		
		1	Stereo: High FSYNC is Left Channel; TDM: Frame Start on Rising Edge		
1	SDATA_FMT		Serial Data Format	0x0	R/W
		0	I^2S (Delay by 1) Format		
		1	Left Justified Format		
0	SAI_MODE		Serial Interface Mode Select	0x1	R/W
		0	Stereo Modes		
		1	TDM Modes		

Address: 0x0A, Reset: 0x07, Name: SAI_CTRL2

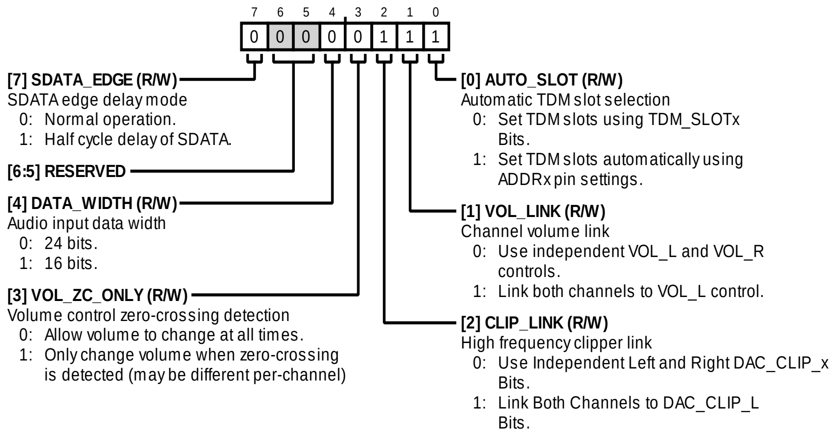


Table 34. Bit Descriptions for SAI_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	SDATA_EDGE		SDATA Edge Delay Mode	0x0	R/W
		0	Normal Operation		
		1	Half Cycle Delay of SDATA		
[6:5]	RESERVED		Reserved	0x0	R
4	DATA_WIDTH		Audio Input Data Width	0x0	R/W
		0	24 Bits		
		1	16 Bits		
3	VOL_ZC_ONLY		Volume Control Zero-Crossing Detection	0x0	R/W
		0	Allow Volume to Change at All Times		
		1	Only Change Volume When Zero-Crossing is Detected (May Be Different Per Channel)		
2	CLIP_LINK		High Frequency Clipper Link	0x1	R/W
		0	Use Independent Left and Right DAC_CLIP_x Bits		
		1	Link Both Channels to DAC_CLIP_L Bits		
1	VOL_LINK		Channel Volume Link	0x1	R/W
		0	Use Independent VOL_L and VOL_R Controls		
		1	Link Both Channels to VOL_L Control		
0	AUTO_SLOT		Automatic TDM Slot Selection	0x1	R/W
		0	Set TDM Slots Using TDM_SLOT_x Bits		
		1	Set TDM Slots Automatically Using the ADDRx Pin Settings		

Address: 0x0B, Reset: 0x00, Name: SLOT_LEFT_CTRL

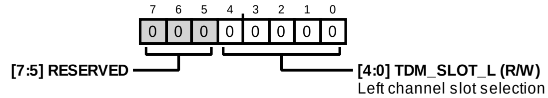


Table 35. Bit Descriptions for SLOT_LEFT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R
[4:0]	TDM_SLOT_L		Left Channel Slot Selection	0x0	R/W

Address: 0x0C, Reset: 0x01, Name: SLOT_RIGHT_CTRL

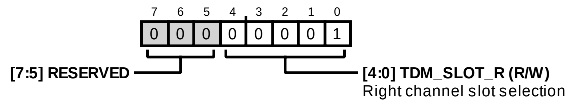


Table 36. Bit Descriptions for SLOT_RIGHT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R
[4:0]	TDM_SLOT_R		Right Channel Slot Selection	0x1	R/W

Address: 0x0E, Reset: 0xA0, Name: LIM_LEFT_CTRL1

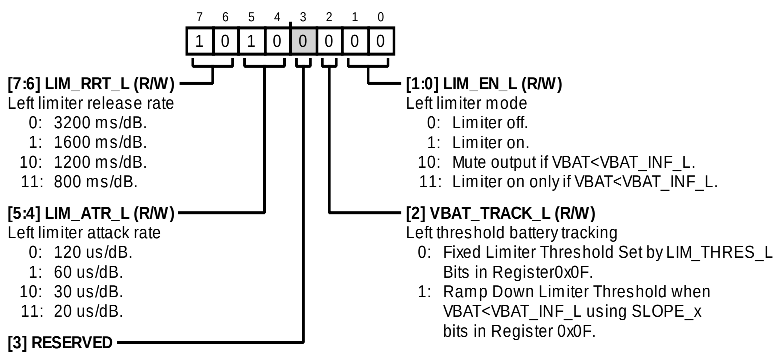


Table 37. Bit Descriptions for LIM_LEFT_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	LIM_RRT_L		Left Limiter Release Rate	0x2	R/W
		0	3200 ms/dB		
		1	1600 ms/dB		
		10	1200 ms/dB		
		11	800 ms/dB		
[5:4]	LIM_ATR_L		Left Limiter Attack Rate	0x2	R/W
		0	120 µs/dB		
		1	60 µs/dB		
		10	30 µs/dB		
		11	20 µs/dB		
3	RESERVED		Reserved	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
2	VBAT_TRACK_L		Left Threshold Battery Tracking	0x0	R/W
		0	Fixed Limiter Threshold Set by LIM_THRES Bits in Register 0x0F		
		1	Ramp Down Limiter Threshold when VBAT < VBAT_INF_L using SLOPE_x bits in Register 0x0F.		
[1:0]	LIM_EN_L		Left Limiter Mode	0x0	R/W
		0	Limiter Off		
		1	Limiter On		
		10	Mute output if VBAT < VBAT_INF_L.		
		11	Limiter on only if VBAT < VBAT_INF_L.		

Address: 0x0F, Reset: 0x51, Name: LIM_LEFT_CTRL2

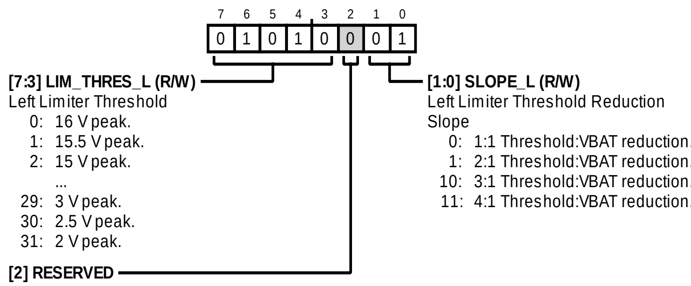


Table 38. Bit Descriptions for LIM_LEFT_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	LIM_THRES_L		Left Limiter Threshold	0xA	R/W
		0	16 V peak		
		1	15.5 V peak		
		2	15 V peak		
		3	14.5 V peak		
		4	14 V peak		
		5	13.5 V peak		
		6	13 V peak		
		7	12.5 V peak		
		8	12 V peak		
		9	11.5 V peak		
		10	11 V peak		
		11	10.5 V peak		
		12	10 V peak		
		13	9.5 V peak		
		14	9.25 V peak		
		15	9 V peak		
		16	8.75 V peak		
		17	8.5 V peak		
		18	8.25 V peak		
		19	8 V peak		
		20	7.5 V peak		

Bits	Bit Name	Settings	Description	Reset	Access
		21	7 V peak		
		22	6.5 V peak		
		23	6 V peak		
		24	5.5 V peak		
		25	5 V peak		
		26	4.5 V peak		
		27	4 V peak		
		28	3.5 V peak		
		29	3 V peak		
		30	2.5 V peak		
		31	2 V peak		
2	RESERVED		Reserved	0x0	R
[1:0]	SLOPE_L		Left Limiter Threshold Reduction Slope	0x1	R/W
		0	1:1 Threshold: VBAT Reduction		
		1	2:1 Threshold: VBAT Reduction		
		10	3:1 Threshold: VBAT Reduction		
		11	4:1 Threshold: VBAT Reduction		

Address: 0x10, Reset: 0x22, Name: LIM_LEFT_CTRL3

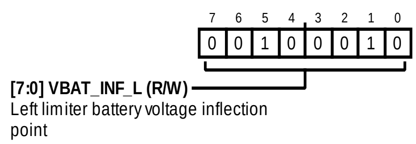


Table 39. Bit Descriptions for LIM_LEFT_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VBAT_INF_L		Left Limiter Battery Voltage Inflection Point	0x22	R/W

Address: 0x11, Reset: 0xA8, Name: LIM_RIGHT_CTRL1

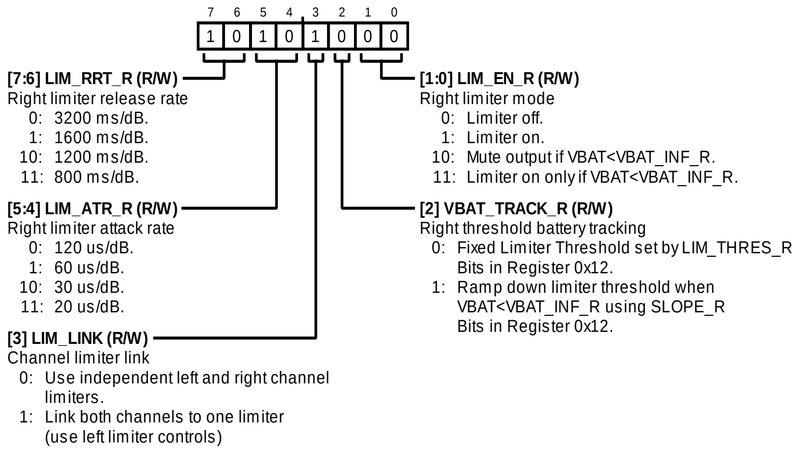


Table 40. Bit Descriptions for LIM_RIGHT_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	LIM_RRT_R		Right Limiter Release Rate	0x2	R/W
		0	3200 ms/dB		
		1	1600 ms/dB		
		10	1200 ms/dB		
		11	800 ms/dB		
[5:4]	LIM_ATR_R		Right Limiter Attack Rate	0x2	R/W
		0	120 µs/dB		
		1	60 µs/dB		
		10	30 µs/dB		
		11	20 µs/dB		
3	LIM_LINK		Channel Limiter Link	0x1	R/W
		0	Use Independent Left and Right Channel Limiters		
		1	Link Both Channels to one Limiter (Use Left Limiter Controls)		
2	VBAT_TRACK_R		Right Threshold Battery Tracking	0x0	R/W
		0	Fixed Limiter Threshold set by LIM_THRES_R Bits in Register 0x12		
		1	Ramp down limiter threshold when VBAT < VBAT_INF_R using SLOPE_R Bits in Register 0x12.		
[1:0]	LIM_EN_R		Right Limiter Mode	0x0	R/W
		0	Limiter Off		
		1	Limiter On		
		10	Mute output if VBAT < VBAT_INF_R.		
		11	Limiter on only if VBAT < VBAT_INF_R.		

Address: 0x12, Reset: 0x51, Name: LIM_RIGHT_CTRL2

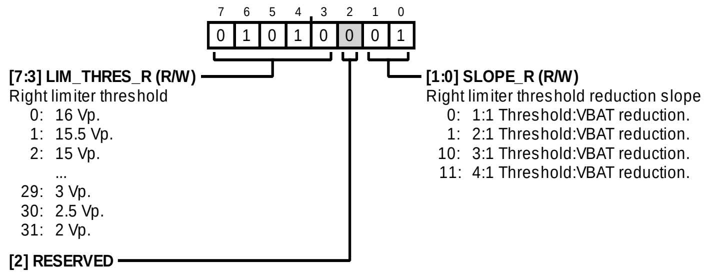


Table 41. Bit Descriptions for LIM_RIGHT_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	LIM_THRES_R		Right Limiter Threshold	0xA	R/W
		0	16 V p-p		
		1	15.5 V p-p		
		2	15 V p-p		
		3	14.5 V p-p		
		4	14 V p-p		
		5	13.5 V p-p		
		6	13 V p-p		
		7	12.5 V p-p		
		8	12 V p-p		
		9	11.5 V p-p		
		10	11 V p-p		
		11	10.5 V p-p		
		12	10 V p-p		
		13	9.5 V p-p		
		14	9.25 V p-p		
		15	9 V p-p		
		16	8.75 V p-p		
		17	8.5 V p-p		
		18	8.25 V p-p		
		19	8 V p-p		
		20	7.5 V p-p		
		21	7 V p-p		
		22	6.5 V p-p		
		23	6 V p-p		
		24	5.5 V p-p		
		25	5 V p-p		
		26	4.5 V p-p		
		27	4 V p-p		
		28	3.5 V p-p		
		29	3 V p-p		
		30	2.5 V p-p		
		31	2 V p-p		

Bits	Bit Name	Settings	Description	Reset	Access
2	RESERVED		Reserved	0x0	R
[1:0]	SLOPE_R		Right Limiter Threshold Reduction Slope	0x1	R/W
		0	1:1 Threshold: VBAT Reduction		
		1	2:1 Threshold: VBAT Reduction		
		10	3:1 Threshold: VBAT Reduction		
		11	4:1 Threshold: VBAT Reduction		

Address: 0x13, Reset: 0x22, Name: LIM_RIGHT_CTRL3

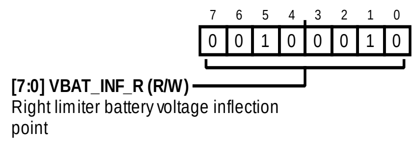


Table 42. Bit Descriptions for LIM_RIGHT_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VBAT_INF_R		Right Limiter Battery Voltage Inflection Point	0x22	R/W

Address: 0x14, Reset: 0xFF, Name: CLIP_LEFT_CTRL

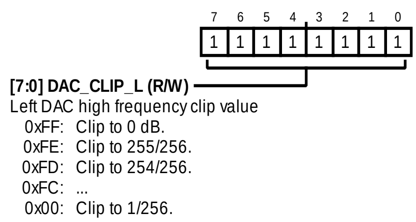


Table 43. Bit Descriptions for CLIP_LEFT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC_CLIP_L		Left DAC High Frequency Clip Value	0xFF	R/W
		0xFF	Clip to 0 dB		
		0xFE	Clip to 255/256		
		0xFD	Clip to 254/256		
		0xFC	…		
		0x00	Clip to 1/256		

Address: 0x15, Reset: 0xFF, Name: CLIP_RIGHT_CTRL

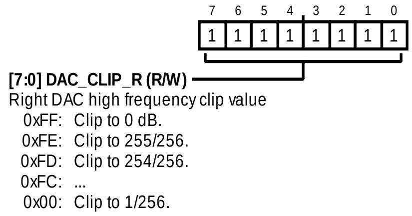


Table 44. Bit Descriptions for CLIP_RIGHT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC_CLIP_R		Right DAC High Frequency Clip Value	0xFF	R/W
		0xFF	Clip to 0 dB		
		0xFE	Clip to 255/256		
		0xFD	Clip to 254/256		
		0xFC	…		
		0x00	Clip to 1/256		

Address: 0x16, Reset: 0x00, Name: FAULT_CTRL1

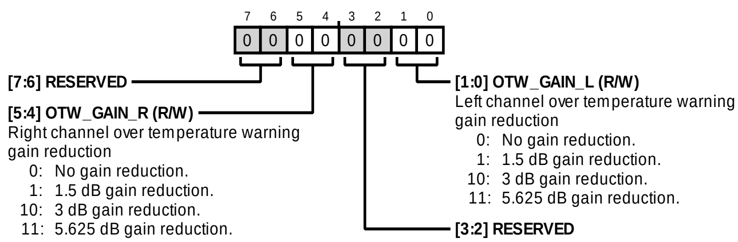


Table 45. Bit Descriptions for FAULT_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
[5:4]	OTW_GAIN_R		Right Channel Over Temperature Warning Gain Reduction	0x0	R/W
		0	No Gain Reduction		
		1	1.5 dB Gain Reduction		
		10	3 dB Gain Reduction		
		11	5.625 dB Gain Reduction		
[3:2]	RESERVED		Reserved	0x0	R
[1:0]	OTW_GAIN_L		Left Channel Over Temperature Warning Gain Reduction	0x0	R/W
		0	No Gain Reduction		
		1	1.5 dB Gain Reduction		
		10	3 dB Gain Reduction		
		11	5.625 dB Gain Reduction		

Address: 0x17, Reset: 0x30, Name: FAULT_CTRL2

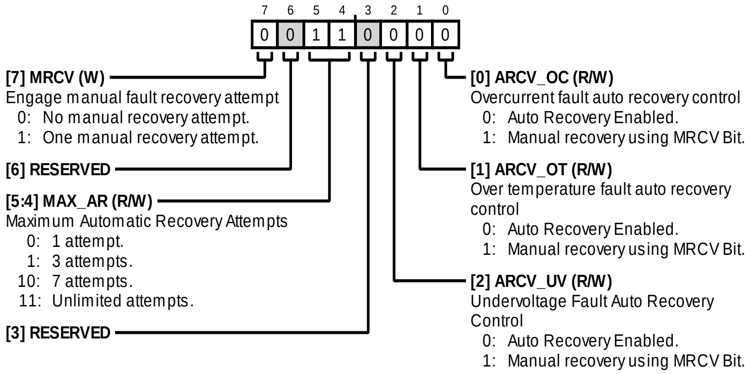


Table 46. Bit Descriptions for FAULT_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	MRCV		Engage Manual Fault Recovery Attempt	0x0	W
6	RESERVED		Reserved	0x0	R
[5:4]	MAX_AR		Maximum Automatic Recovery Attempts	0x3	R/W
		0	1 Attempt		
		1	3 Attempts		
		10	7 Attempts		
		11	Unlimited Attempts		
3	RESERVED		Reserved	0x0	R
2	ARCV_UV		Undervoltage Fault Automatic Recovery Control	0x0	R/W
		0	Automatic Recovery Enabled		
		1	Manual Recovery Using MRCV Register		
1	ARCV_OT		Over Temperature Fault Automatic Recovery Control	0x0	R/W
		0	Automatic Recovery Enabled		
		1	Manual Recovery Using MRCV Bit		
0	ARCV_OC		Over Current Fault Automatic Recovery Control	0x0	R/W
		0	Automatic Recovery Enabled		
		1	Manual Recovery Using MRCV Bit		

Address: 0x18, Reset: 0x00, Name: STATUS1

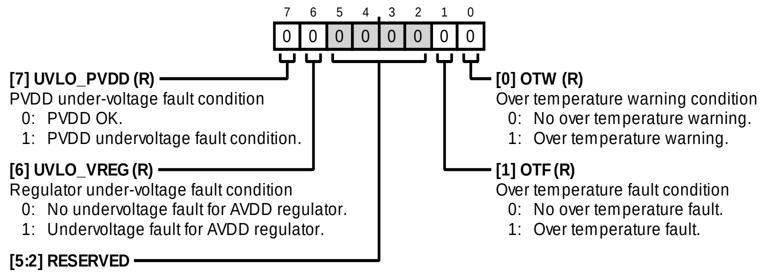


Table 47. Bit Descriptions for STATUS1

Bits	Bit Name	Settings	Description	Reset	Access
7	UVLO_PVDD		PVDD Undervoltage Fault Condition	0x0	R
		0	PVDD OK		
		1	PVDD undervoltage fault condition		
6	UVLO_VREG		Regulator Undervoltage Fault Condition	0x0	R
		0	No undervoltage fault for AVDD regulator		
		1	Undervoltage fault for AVDD regulator		
[5:2]	RESERVED		Reserved	0x0	R
1	OTF		Over Temperature Fault Condition	0x0	R
		0	No overtemperature fault		
		1	Overtemperature fault		
0	OTW		Over Temperature Warning Condition	0x0	R
		0	No overtemperature warning		
		1	Overtemperature warning		

Address: 0x19, Reset: 0x00, Name: STATUS2

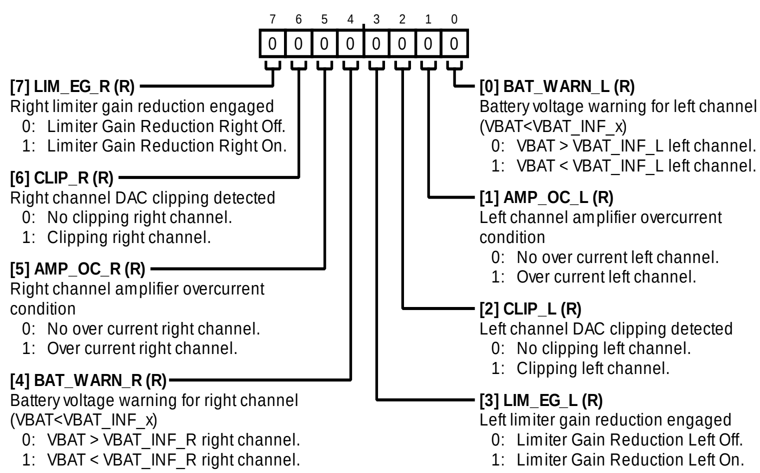


Table 48. Bit Descriptions for STATUS2

Bits	Bit Name	Settings	Description	Reset	Access
7	LIM_EG_R		Right limiter gain reduction engaged	0x0	R
		0	Limiter Gain Reduction Right Off.		
		1	Limiter Gain Reduction Right On.		

Bits	Bit Name	Settings	Description	Reset	Access
6	CLIP_R		Right channel DAC clipping detected	0x0	R
		0	No clipping right channel.		
		1	Clipping right channel.		
5	AMP_OC_R		Right channel amplifier overcurrent condition	0x0	R
		0	No overcurrent right channel.		
		1	Overcurrent right channel.		
4	BAT_WARN_R		Battery voltage warning for right channel (VBAT < VBAT_INF_x)	0x0	R
		0	VBAT > VBAT_INF_R right channel.		
		1	VBAT < VBAT_INF_R right channel.		
3	LIM_EG_L		Left limiter gain reduction engaged	0x0	R
		0	Limiter Gain Reduction Left Off.		
		1	Limiter Gain Reduction Left On.		
2	CLIP_L		Left channel DAC clipping detected	0x0	R
		0	No clipping left channel.		
		1	Clipping left channel.		
1	AMP_OC_L		Left channel amplifier overcurrent condition	0x0	R
		0	No over current left channel.		
		1	Over current left channel.		
0	BAT_WARN_L		Battery voltage warning for left channel (VBAT < VBAT_INF_x)	0x0	R
		0	VBAT > VBAT_INF_L left channel.		
		1	VBAT < VBAT_INF_L left channel.		

Address: 0x1A, Reset: 0x00, Name: VBAT

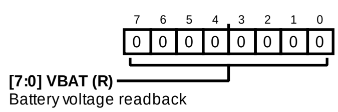


Table 49. Bit Descriptions for VBAT

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VBAT		Battery Voltage Readback	0x0	R

Address: 0x1B, Reset: 0x00, Name: TEMP

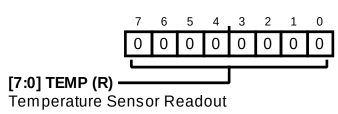


Table 50. Bit Descriptions for TEMP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	TEMP		Temperature Sensor Readout. The actual temperature in degrees Celsius is TEMP – 60 decimal.	0x0	R

Address: 0x1C, Reset: 0x00, Name: SOFT_RESET

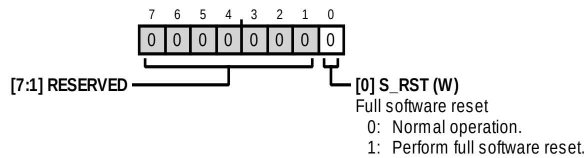


Table 51. Bit Descriptions for SOFT_RESET

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved	0x0	R
0	S_RST		Full Software Reset	0x0	W
		0	Normal Operation		
		1	Perform Full Software Reset		

TYPICAL APPLICATION CIRCUIT

Figure 86 shows a typical application circuit for a stereo output. Figure 87 shows a typical application circuit for a mono output.

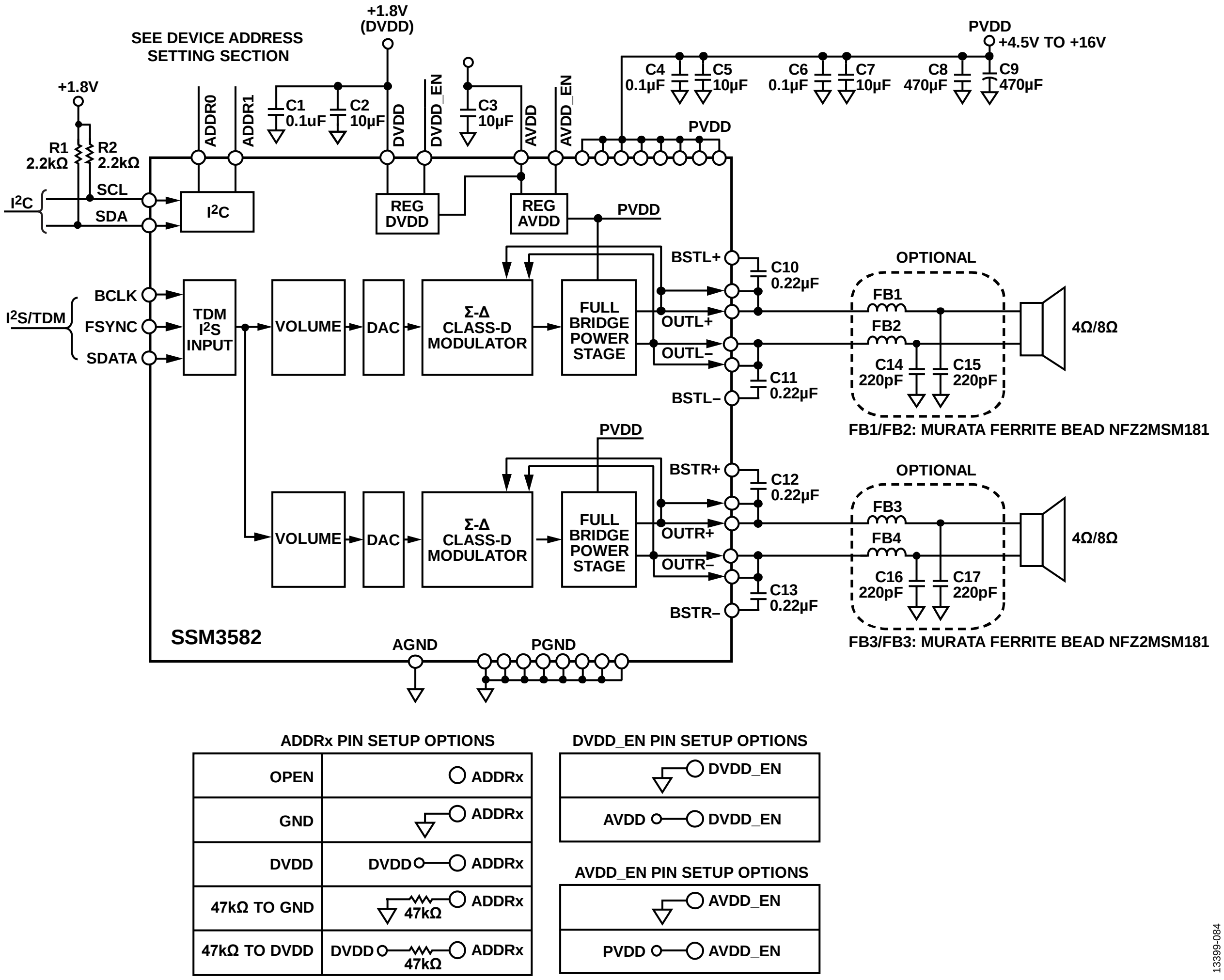
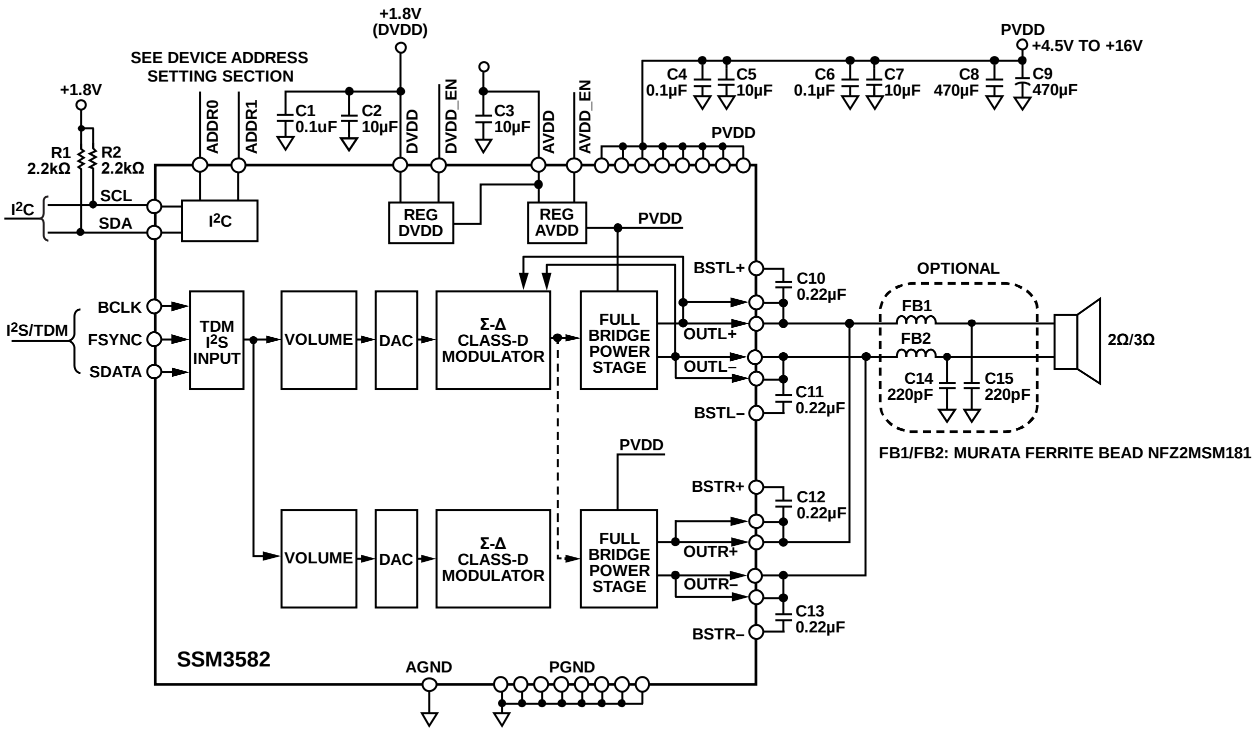


Figure 86. Typical Application Circuit for Stereo Output



ADDRx PIN SETUP OPTIONS

OPEN	ADDRx
GND	ADDRx
DVDD	DVDD — ADDRx
47kΩ TO GND	47kΩ — ADDRx
47kΩ TO DVDD	DVDD — 47kΩ — ADDRx

DVDD_EN PIN SETUP OPTIONS

DVDD_EN
AVDD — DVDD_EN

AVDD_EN PIN SETUP OPTIONS

AVDD_EN
PVDD — AVDD_EN

Figure 87. Typical Application Circuit for Mono Output

OUTLINE DIMENSIONS

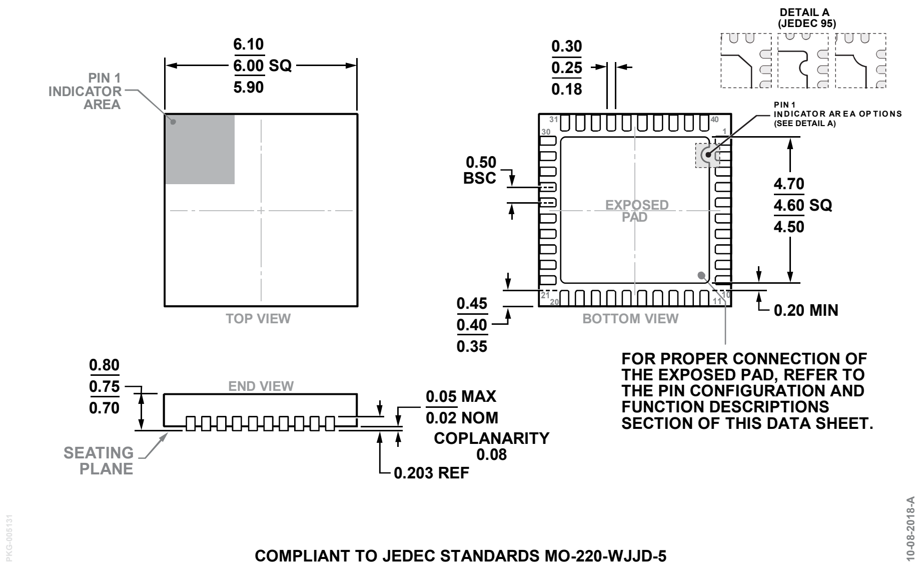


Figure 88. 40-Lead Lead Free Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM3582BCPZ	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP]	CP-40-7
SSM3582BCPZRL	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP]	CP-40-7
SSM3582BCPZR7	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP]	CP-40-7
EVAL-SSM3582Z		Evaluation Board	

[1] Z = RoHs Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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