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REVISION HISTORY

10/2016—Rev. E to Rev. F

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Changes to Compression Ratio Section ... 10
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Deleted Evaluation Board Section and Figure 26; Renumbered Sequentially ... 13
Deleted Figure 27 to Figure 29, Evaluation Board Examples Section, and Table 5; Renumbered Sequentially ... 14
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10/2013—Rev. D to Rev. E

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7/2008—Rev. C to Rev. D

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5/2008—Rev. B to Rev. C

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3/2003—Rev. A to Rev. B

Deleted PDIP Package ... Universal
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Deleted 14-Lead PDIP, Outline Dimensions ... 15
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SPECIFICATIONS

V+ = 5 V, f = 1 kHz, R_L = 100 kΩ, R_{GATE} = 600 kΩ, $R_{ROT\ PT}$ = 3 kΩ, R_{COMP} = 0 Ω, R1 = 0 Ω, R2 = ∞ Ω, T_A = 25°C, unless otherwise noted; V_{IN} = 300 mV rms.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
AUDIO SIGNAL PATH						
Voltage Noise Density	e_n	15:1 Compression		17		nV/√Hz
Noise		20 kHz bandwidth, V_{IN} = GND		−109		dBu[1]
Total Harmonic Distortion and Noise	THD + N	Second and third harmonics, V_{IN} = −20 dBu, 22 kHz low-pass filter		0.25	0.5	%
Input Impedance	Z_{IN}			180		kΩ
Output Impedance	Z_{OUT}			75		Ω
Load Drive		Resistive	5			kΩ
		Capacitive			2	nF
Buffer						
Input Voltage Range		1% THD		1		V rms
Output Voltage Range		1% THD		1		V rms
VCA						
Input Voltage Range		1% THD		1		V rms
Output Voltage Range		1% THD		1.4		V rms
Gain Bandwidth Product		1:1 compression, VCA gain = 60 dB		30		MHz
CONTROL SECTION						
VCA Dynamic Gain Range				60		dB
VCA Fixed Gain Range				−60 to +19		dB
Compression Ratio, Minimum				1:1		
Compression Ratio, Maximum		See Figure 19 for $R_{COMP}/R_{ROT\ PT}$, rotation point = 100 mV rms		15:1		
Control Feedthrough		15:1 compression, rotation point = −10 dBu, R2 = 1.5 kΩ		±5		mV
POWER SUPPLY						
Supply Voltage Range	V+		4.5		5.5	V
Supply Current	I_{SY}			7.5	10	mA
Quiescent Output Voltage Level				2.2		V
Power Supply Rejection Ratio	PSRR			50		dB
POWER DOWN						
Supply Current		Pin 12 = V+[2]		10	100	µA

[1] 0 dBu = 0.775 V rms.
[2] Normal operation for Pin 12 is 0 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	10 V
Audio Input Voltage	Supply voltage
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead SOIC	120	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

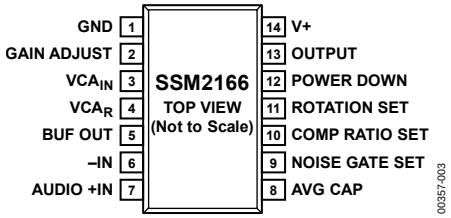

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground.
2	GAIN ADJUST	VCA Gain Adjust Pin. A resistor from this pin to ground sets the fixed gain of the VCA. To check the setting of this pin, make sure the compression ratio set pin (Pin 10) is grounded for no compression. The gain can be varied from 0 dB to 20 dB. For 20 dB, leave the pin open. For 0 dB of fixed gain, a typical resistor value is approximately 1 kΩ. For 10 dB of fixed gain, the resistor value is approximately 2 kΩ to 3 kΩ. For resistor values <1 kΩ, the VCA can attenuate or mute (see Figure 6).
3	VCA_{IN}	VCA Input Pin. A typical connection is a 10 µF capacitor from the buffer output pin (Pin 5) to this pin.
4	VCA_R	Inverting Input to the VCA. This input can be used as a nonground reference for the audio input signal (see the Applications Information section).
5	BUF OUT	Input Buffer Amplifier Output Pin. This pin must not be loaded by capacitance to ground.
6	–IN	Inverting Input to the Buffer. A 10 kΩ feedback resistor, R1, from the buffer output (Pin 5) to this input pin and a resistor, R2, from this pin through a 1 µF capacitor to ground give gains of 6 dB to 20 dB for R2 = 10 kΩ to 1.1 kΩ.
7	AUDIO +IN	Input Audio Signal. AC-coupled (0.1 µF typical) the input signal into this pin.
8	AVG CAP	Detector Averaging Capacitor. A capacitor, 1 µF to 22 µF, to ground from this pin is the averaging capacitor for the detector circuit.
9	NOISE GATE SET	Noise Gate Threshold Set Point. A resistor to V+ sets the level below which input signals are downward expanded. For a 0.7 mV threshold, the resistor value is approximately 380 kΩ. Increasing the resistor value reduces the threshold (see Figure 5).
10	COMP RATIO SET	Compression Ratio Set Pin. A resistor to ground from this pin sets the compression ratio, as shown in Figure 2. Figure 19 gives resistor values for various rotation points.
11	ROTATION SET	Rotation Point Set Pin. This pin is set by adding a resistor to the positive supply. This resistor together with the gain adjust pin determines the onset of limiting. A typical value for this resistor is 17 kΩ for a 100 mV rotation point. Increasing the resistor value reduces the level at which limiting occurs (see Figure 9).
12	POWER DOWN	Power-Down Pin. Connect this pin to ground for normal operation. Connect this pin to the positive supply for power-down mode.
13	OUTPUT	Output Signal.
14	V+	Positive Supply, 5 V Nominal.

TYPICAL PERFORMANCE CHARACTERISTICS

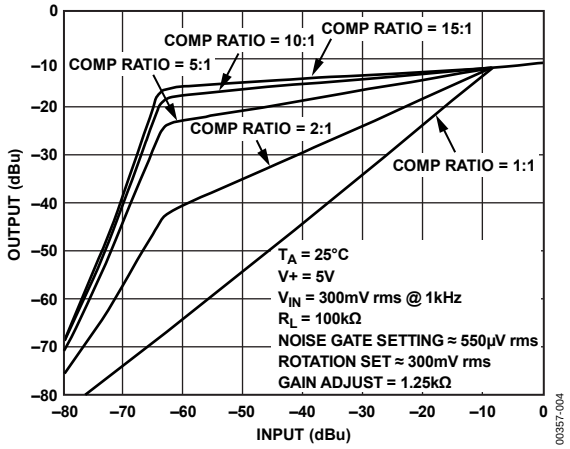

Figure 4. Output vs. Input Characteristics

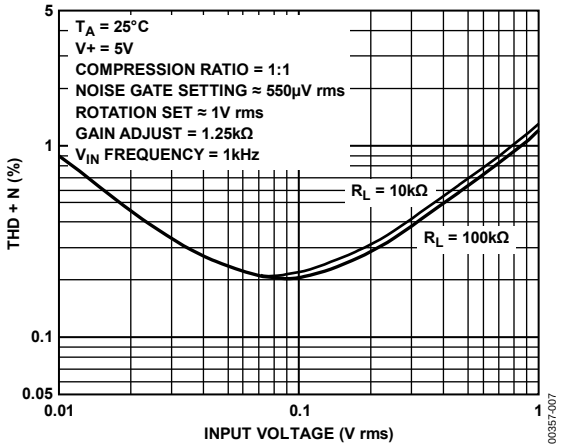

Figure 7. THD + N (%) vs. Input (V rms)

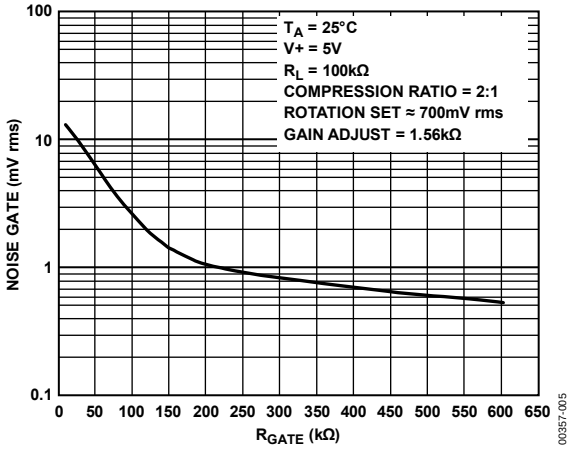

Figure 5. Noise Gate vs. R_{GATE} (Pin 9 to V+)

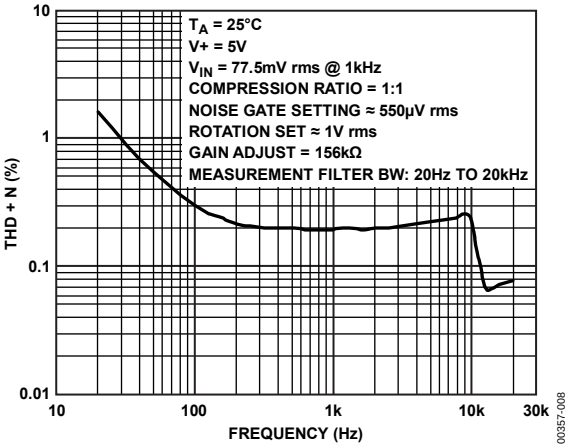

Figure 8. THD + N (%) vs. Frequency (Hz)

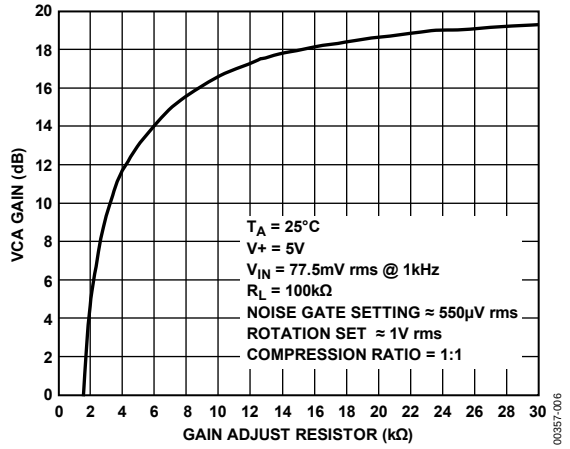

Figure 6. VCA Gain vs. R_{GAIN} (Pin 2 to GND)

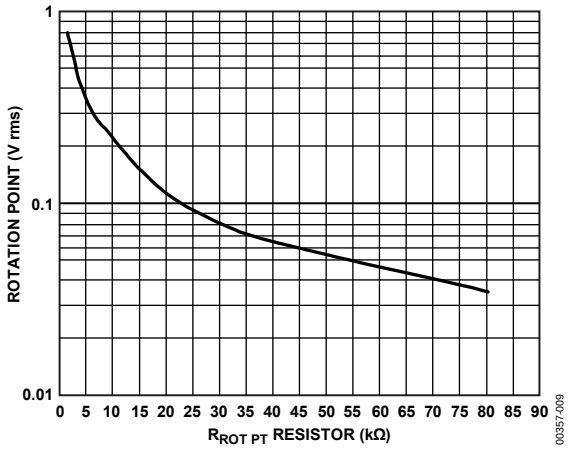

Figure 9. Rotation Point vs. $R_{ROT\ PT}$ (Pin 11 to V+)

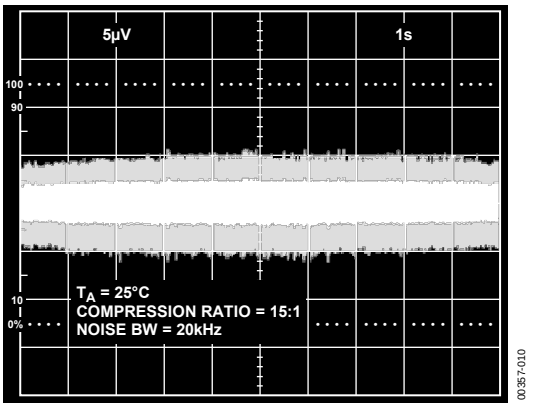

Figure 10. Wideband Peak-to-Peak Output Noise

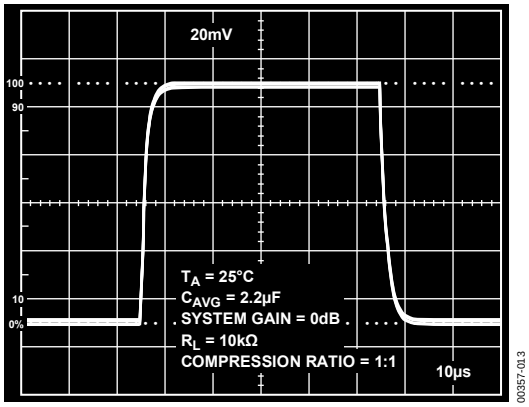

Figure 13. Small Signal Transient Response

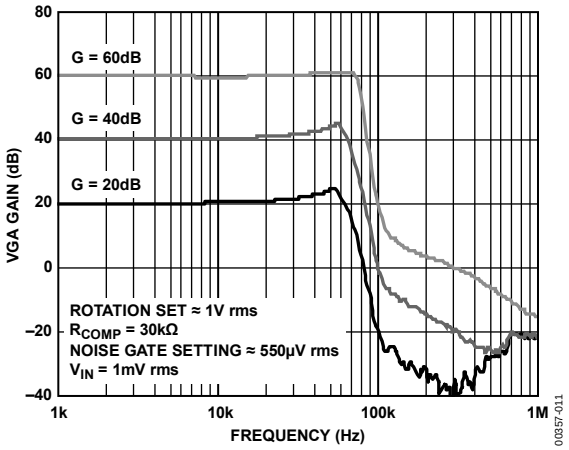

Figure 11. VCA Gain Bandwidth Curves vs. Frequency

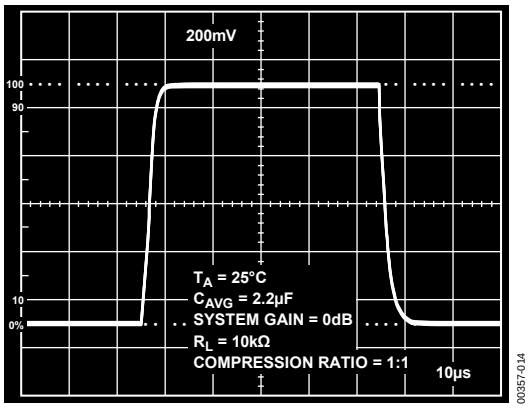

Figure 14. Large Signal Transient Response

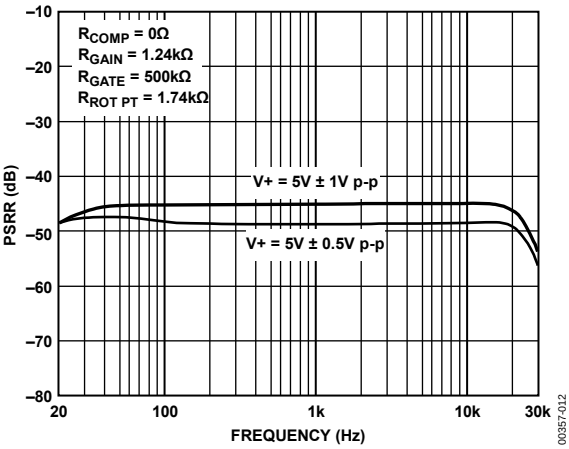

Figure 12. PSRR vs. Frequency

THEORY OF OPERATION

Figure 15 illustrates a typical transfer characteristic for the SSM2166 where the output level in decibels is plotted as a function of the input level in decibels. The dotted line indicates the transfer characteristic for a unity-gain amplifier. For input signals in the range of V_{DE} (downward expansion) to V_{RP} (rotation point), an r dB change in the input level causes a 1 dB change in the output level. Here, r is defined as the compression ratio. The compression ratio can be varied from 1:1 (no compression) to over 15:1 via a single resistor, R_{COMP}. Input signals above V_{RP} are compressed with a fixed compression ratio of approximately 15:1. This region of operation is the limiting region. Varying the compression ratio has no effect on the limiting region. The break-point between the compression region and the limiting region is referred to as the limiting threshold or the rotation point and is user specified in the SSM2166. The rotation point term derives from the observation that the straight line in the compression region rotates about this point on the input/output characteristic as the compression ratio is changed.

The gain of the system with an input signal level of V_{RP} is fixed by R_{GAIN}, regardless of the compression ratio, and is the nominal gain of the system. The user can increase the nominal gain of the system via the on-board VCA by up to 20 dB. Additionally, the input buffer of the SSM2166 can provide fixed gains of 0 dB to 20 dB with R1 and R2.

Input signals below V_{DE} are downward expanded; that is, a −1 dB change in the input signal level causes approximately a −3 dB change in the output level. As a result, the gain of the system is small for very small input signal levels, even though it may be quite large for small input signals above V_{DE}. The user sets the downward expansion threshold, V_{DE}, externally via R_{GATE} at Pin 9 (NOISE GATE SET). The SSM2166 provides an active high, CMOS-compatible digital input whereby a power-down feature reduces the device supply current to less than 100 µA.

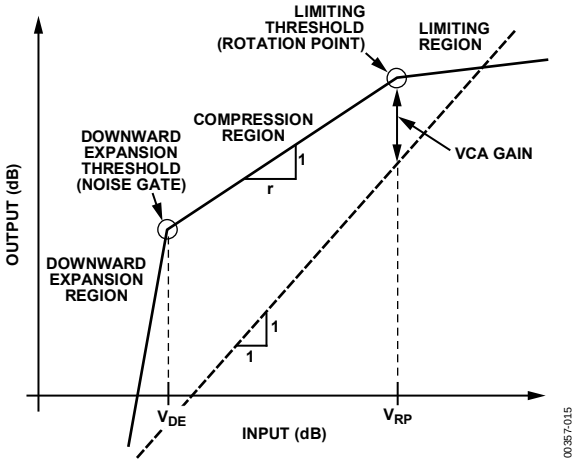

Figure 15. General Input/Output Characteristics

APPLICATIONS INFORMATION

The SSM2166 is a complete microphone signal conditioning system on a single integrated circuit. Designed primarily for voice-band applications, this integrated circuit provides amplification, rms detection, limiting, variable compression, and downward expansion. An integral voltage-controlled amplifier (VCA) provides up to 60 dB of gain in the signal path with approximately 30 kHz bandwidth. An input buffer, op amp circuit can provide additional gain because the circuit can be set anywhere from 0 dB to 20 dB for a total signal path gain of up to 80 dB. The device operates on a single 5 V supply, accepts input signals up to 1 V rms, and produces output signal levels >1 V rms (3 V p-p) into loads >5 kΩ. The internal rms detector has a time constant set by an external capacitor.

The SSM2166 contains an input buffer and automatic gain control (AGC) circuit for audio-band and voice-band signals. Circuit operation is optimized by providing a user-adjustable time constant and compression ratio. A downward expansion (noise gating) feature eliminates circuit noise in the absence of an input signal. The SSM2166 allows the user to set the downward expansion threshold, the limiting threshold (rotation point), the input buffer fixed gain, and the internal VCA nominal gain at the rotation point. The SSM2166 also features a power-down mode and muting capability.

SIGNAL PATH

Figure 16 illustrates the block diagram of the SSM2166. The audio input signal is processed by the input buffer and then by the VCA. The input buffer presents an input impedance of approximately 180 kΩ to the source. A dc voltage of approximately 1.5 V is present at AUDIO +IN (Pin 7), requiring the use of a blocking capacitor (C1) for ground referenced sources. A 0.1 µF capacitor is a good choice for most audio applications. The input buffer is a unity-gain stable amplifier that can drive the low impedance input of the VCA.

The VCA is a low distortion, variable-gain amplifier (VGA) whose gain is set by the side-chain control circuitry. The input to the VCA is a virtual ground in series with approximately 1 kΩ. An external blocking capacitor (C6) must be used between the buffer output and the VCA input. The 1 kΩ impedance between amplifiers determines the value of this capacitor, which is typically between 1 µF and 10 µF. An aluminum electrolytic capacitor is an economical choice. The VCA amplifies the input signal current flowing through C6 and converts this current to a voltage at the OUTPUT pin (Pin 13). The net gain from input to output can be as high as 60 dB (without additional buffer gain), depending on the gain set by the control circuitry.

The gain of the VCA at the rotation point is set by the value of a resistor, R_{GAIN}, connected between Pin 2 and GND. The relationship between the VCA gain and R_{GAIN} is shown in Figure 6. The AGC range can be as high as 60 dB. The VCA_{IN} pin (Pin 3) is the non-inverting input terminal to the VCA. The inverting input of the VCA is available at the VCA_R pin (Pin 4) and exhibits an input impedance of 1 kΩ, as well. As a result, this pin can be used for differential inputs or for the elimination of grounding problems by connecting a capacitor whose value equals that used in series with the VCA_{IN} pin to ground.

The output impedance of the SSM2166 is typically less than 75 Ω, and the external load on Pin 13 must be >5 kΩ. The nominal output dc voltage of the device is approximately 2.2 V. Use a blocking capacitor for grounded loads.

The bandwidth of the SSM2166 is quite wide at all gain settings. The upper 3 dB point is approximately 30 kHz at gains as high as 60 dB (using the input buffer for additional gain, circuit bandwidth is unaffected). The gain bandwidth (GBW) plots are shown in Figure 11. The lower 3 dB cutoff frequency of the SSM2166 is set by the input impedance of the VCA (1 kΩ) and C6. While the noise of the input buffer is fixed, the input referred noise of the VCA is a function of gain. The VCA input noise is designed to be a minimum when the gain is at a maximum, thereby optimizing the usable dynamic range of the device. A plot of wideband peak-to-peak output noise is shown in Figure 10.

LEVEL DETECTOR

The SSM2166 incorporates a full-wave rectifier and true rms level detector circuit whose averaging time constant is set by an external capacitor connected to the AVG CAP pin (Pin 8). For optimal low frequency operation of the level detector down to 10 Hz, the value of the capacitor must be 2.2 µF. Some experimentation with larger values for the AVG CAP may be necessary to reduce the effects of excessive low frequency ambient background noise. The value of the averaging capacitor affects sound quality: too small a value for this capacitor may cause a pumping effect for some signals, while too large a value may result in slow response times to signal dynamics. Electrolytic capacitors are recommended for lowest cost and must be in the range of 2 µF to 47 µF. Capacitor values from 18 µF to 22 µF have been found to be more appropriate in voice-band applications where capacitors on the low end of the range seem more appropriate for music program material.

The rms detector filter time constant is approximately given by 10 × C_{AVG} milliseconds, where C_{AVG} is in µF. This time constant controls both the steady-state averaging in the rms detector as well as the release time for compression; that is, the time it takes for the system gain to react when a large input is followed by a small signal. The attack time, the time it takes for the gain to be reduced when a small signal is followed by a large signal, is controlled partly by the AVG CAP value but is mainly controlled by internal circuitry that speeds up the attack for large level changes. This limits overload time to less than 1 ms in most cases.

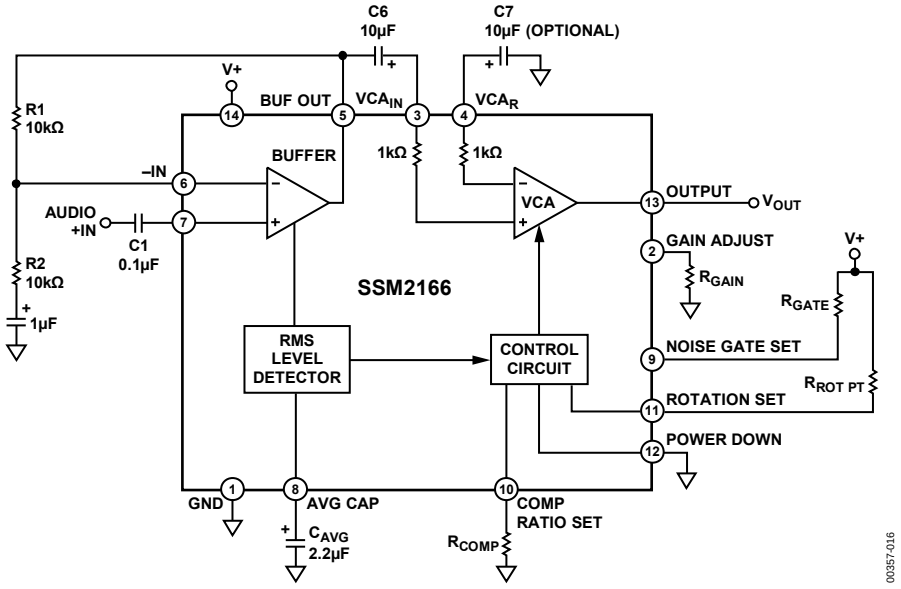

Figure 16. Functional Block Diagram and Typical Application

The performance of the rms level detector is illustrated for a C_{AVG} of 2.2 µF in Figure 17 and for a C_{AVG} of 22 µF in Figure 18. In each of these images, the input signal to the SSM2166 (not shown) is a series of tone bursts in six successive 10 dB steps. The tone bursts range from −66 dBV (0.5 mV rms) to −6 dBV (0.5 V rms). As shown in Figure 17 and Figure 18, the attack time of the rms level detector is dependent only on C_{AVG}, but the release times are linear ramps whose decay times are dependent on both C_{AVG} and the input signal step size. The rate of release is approximately 240 dB/s for a C_{AVG} of 2.2 µF and 12 dB/s for a C_{AVG} of 22 µF.

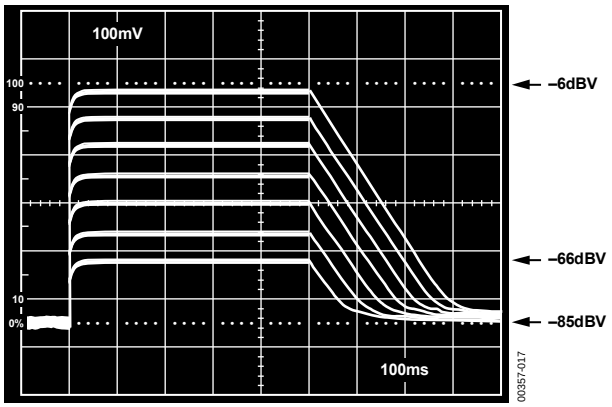

Figure 17. RMS Level Detector Performance with C_{AVG} = 2.2 µF

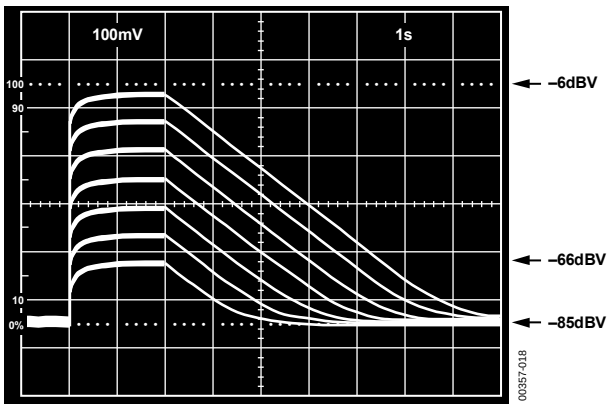

Figure 18. RMS Level Detector Performance with C_{AVG} = 22 µF

CONTROL CIRCUITRY

The output of the rms level detector is a signal proportional to the log of the true rms value of the buffer output with an added dc offset. The control circuitry subtracts a dc voltage from this signal, scales it, and sends the result to the VCA to control the gain. The gain control of the VCA is logarithmic—a linear change in the control signal causes a decibel change in gain. It is this control law that allows linear processing of the log rms signal to provide the flat compression characteristic on the input/output characteristic shown in Figure 15.

Compression Ratio

Changing the scaling of the control signal fed to the VCA causes a change in the circuit compression ratio, r. This effect is shown in Figure 20. The compression ratio can be set by connecting a resistor between the COMP RATIO SET pin (Pin 10) and GND. Lowering R_{COMP} gives smaller compression ratios as shown in Figure 19, with values of approximately 0.17 kΩ or less resulting in a compression ratio of 1:1. AGC performance is achieved with compression ratios between 2:1 and 15:1 and is dependent on the application. A 100 kΩ potentiometer can be used to allow this parameter to be adjusted.

COMPRESSION RATIO / ROTATION POINT	1:1	2:1	5:1	10:1	15:1
100mV rms	0.1	8.7	19.4	45	395
300mV rms	0.1	8.7	19.4	45	N/A
1V rms	0.1	8.7	19.4	45	N/A

TYPICAL R_{COMP} VALUES IN kΩ.

00357-031

Figure 19. Compression Ratio vs. R_{COMP} (Pin 10 to GND)

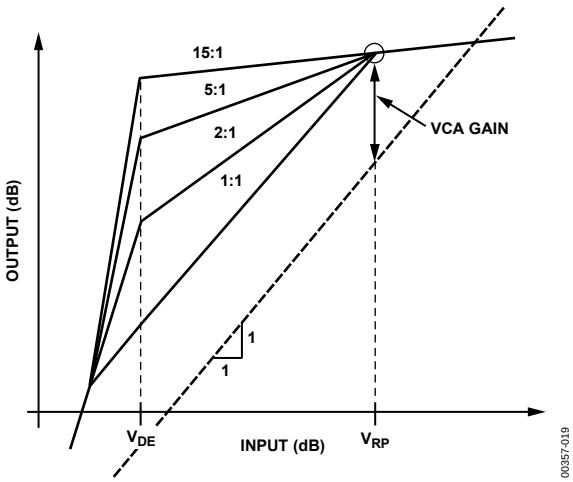

Figure 20. Effect of Varying the Compression Ratio

Rotation Point

An internal dc reference voltage in the control circuitry, used to set the rotation point, is user specified, as illustrated in Figure 9. The effect on rotation point is shown in Figure 21. By varying a resistor, $R_{ROT\ PT}$, connected between the positive supply and the ROTATION SET pin (Pin 11), the rotation point may be varied by approximately 20 mV rms to 1 V rms. From Figure 21, the rotation point is inversely proportional to $R_{ROT\ PT}$. For example, a 1 kΩ resistor typically sets the rotation point at 1 V rms, whereas a 55 kΩ resistor typically sets the rotation point at approximately 30 mV rms.

Because limiting occurs for signals larger than the rotation point ($V_{IN} > V_{RP}$), the rotation point effectively sets the maximum output signal level. It is recommended that the rotation point be set at the upper extreme of the range of typical input signals so that the compression region covers the entire desired input signal range. Occasional larger signal transients are then attenuated by the action of the limiter.

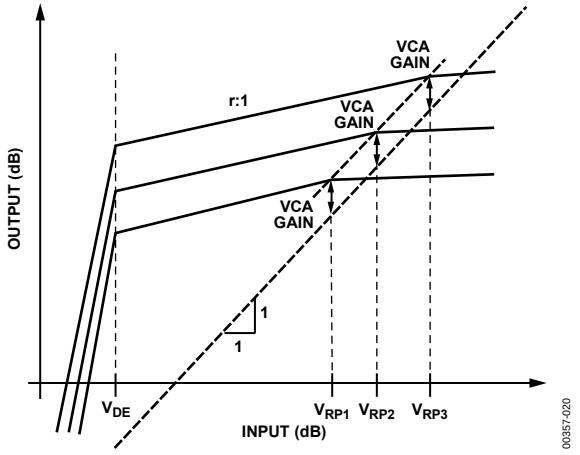

Figure 21. Effect of Varying the Rotation Point

VCA Gain Setting and Muting

The GAIN ADJUST pin (Pin 2) sets the maximum gain of the SSM2166 via R_{GAIN}. This resistor, with a range of 1 kΩ to 20 kΩ, causes the nominal VCA gain to vary from 0 dB to approximately 20 dB, respectively. Setting the VCA gain to its maximum can also be achieved by leaving the GAIN ADJUST pin in an open condition (no connect). Figure 22 illustrates the effect on the transfer characteristic by varying this parameter. For low level signal sources, the VCA must be set to maximum gain using a 20 kΩ resistor.

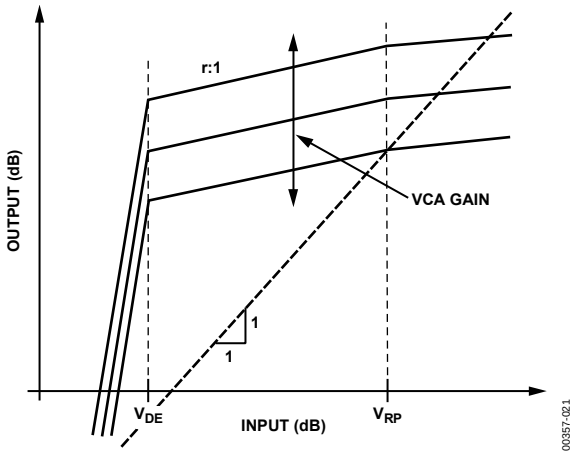

Figure 22. Effect of Varying the VCA Gain Setting

The gain of the VCA can be reduced below 0 dB by making R_{GAIN} smaller than 1 kΩ. Switching Pin 2 through 330 Ω or less to GND mutes the output. Either a switch connected to ground or a transistor can be used, as shown in Figure 23. To avoid audible clicks when using the mute feature, a capacitor (C5) can be connected from Pin 2 to GND. The value of the capacitor is arbitrary and must be determined empirically, but a 0.01 µF capacitor is a good starting value.

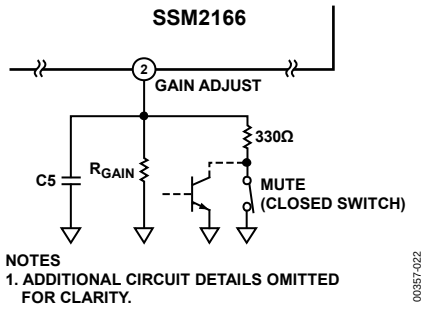

Figure 23. Details of Mute Option

Downward Expansion Threshold

The downward expansion threshold, or noise gate, is determined via a second reference voltage internal to the control circuitry. This second reference can be varied in the SSM2166 using a resistor, R_{GATE}, connected between the positive supply and the NOISE GATE SET pin (Pin 9). The effect of varying this threshold is shown in Figure 24. The downward expansion threshold can be set between 300 µV rms and 20 mV rms by varying the resistance value between Pin 9 and the supply voltage. Like the ROTATION SET pin, the downward expansion threshold is inversely proportional to the value of this resistance: setting this resistance to 1 MΩ sets the threshold at approximately 250 µV rms, whereas a 10 kΩ resistance sets the threshold at approximately 20 mV rms. This relationship is illustrated in Figure 5. In general, the downward expansion threshold must be set at the lower extreme of the desired range of the input signals so that signals below this level are attenuated.

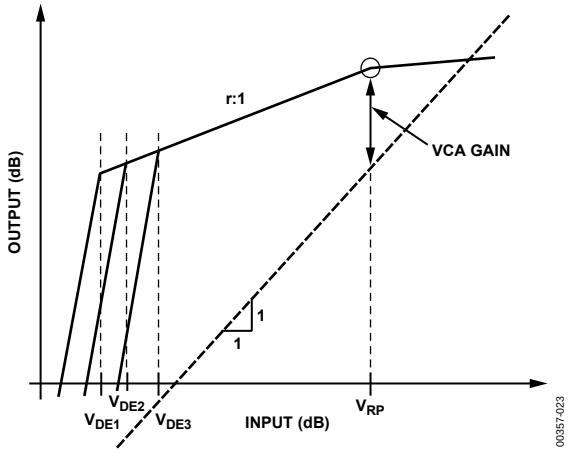

Figure 24. Effect of Varying the Downward Expansion (Noise Gate) Threshold

POWER-DOWN FEATURE

The supply current of the SSM2166 can be reduced to less than 100 µA by applying an active high, 5 V CMOS-compatible input to the POWER DOWN pin (Pin 12). In this state, the input and output circuitry of the SSM2166 assumes a high impedance state; as such, the potentials at the input pin and the output pin are determined by the external circuitry connected to the SSM2166. The SSM2166 takes approximately 200 ms to settle from a power-down to power-on command. For power-on to power-down, the SSM2166 requires more time, typically less than 1 second. Cycling the power supply to the SSM2166 can result in quicker settling times: the off-to-on settling time of the SSM2166 is less than 200 ms, while the on-to-off settling time is less than 1 ms. In either implementation, transients may appear at the output of the device. To avoid these output transients, use mute control of the VCA gain as previously mentioned.

PCB LAYOUT CONSIDERATIONS

Because the SSM2166 is capable of wide bandwidth operation and can be configured for as much as 80 dB of gain, special care must be exercised in the layout of the PCB that contains the IC and its associated components. The following recommendations must be considered and/or followed:

- In some high system gain applications, the shielding of input wires to minimize possible feedback from the output of the SSM2166 back to the input circuit may be necessary.
- A single-point (star) ground implementation is recommended in addition to maintaining short lead lengths and PCB runs. In applications where an analog ground and a digital ground are available, the SSM2166 and its surrounding circuitry must be connected to the analog ground of the system. Because of these recommendations, wire-wrap board connections and grounding implementations must be avoided.
- The internal buffer of the SSM2166 was designed to drive only the input of the internal VCA and its own feedback network. Stray capacitive loading to ground from the BUF OUT pin in excess of 5 pF to 10 pF can cause excessive phase shift and can lead to circuit instability.
- When using high impedance sources (≥5 kΩ), system gains in excess of 60 dB are not recommended. This configuration is rarely appropriate because virtually all high impedance inputs provide larger amplitude signals that do not require as much amplification. When using high impedance sources, however, it can be advantageous to shunt the source with a capacitor to ground at the input pin of the IC (Pin 7) to lower the source impedance at high frequencies, as shown in Figure 25. A capacitor with a value of 1000 pF is a good starting value and sets a low-pass corner at 31 kHz for 5 kΩ sources. In applications where the source ground is not as clean as is desirable, a capacitor from the VCA_R input to the source ground may prove beneficial. This capacitor is used in addition to the grounded capacitor used in the feedback around the buffer, assuming that the buffer is configured for gain.

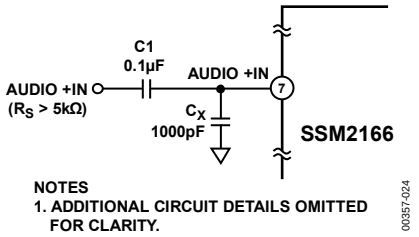

Figure 25. Circuit Configuration for Use with High Impedance Signal Sources

The value of C7 must be the same as C6, which is the capacitor value used between BUF OUT and VCA_{IN}. This connection makes the source ground noise appear as a common-mode signal to the VCA, allowing the common-mode noise to be rejected by the VCA differential input circuitry. C7 can also be useful in reducing ground loop problems and in reducing noise coupling from the power supply by balancing the impedances connected to the inputs of the internal VCA.

OUTLINE DIMENSIONS

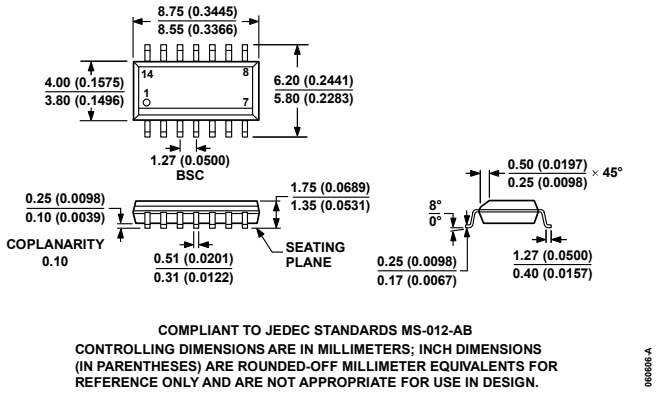

Figure 26. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2166SZ	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
SSM2166SZ-REEL	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
SSM2166SZ-REEL7	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14

[1] Z = RoHS Compliant Part.

Top Branding Revision Reflecting Die Replacement

Version	Original Die Revision (Prior to Rev. C of Data Sheet)	New Die Revision (Rev. C to Current Revision of Data Sheet)
Pb-Free (RoHS) Version	Top Line 1: SSM Top Line 2: 2166 Top Line 3: # XXXX[2]	Top Line 1: SSM Top Line 2: 2166A[1] Top Line 3: # XXXX[2]

[1] Letter A designates new die revision; refer to revised external component values in Figure 5, Figure 6, Figure 9, and Figure 19.
[2] # designates RoHS version.