

## Hardware Specifications

### 32-BIT ARM7TDMI RISC PROCESSOR

- 44 MHz 32-bit ARM CPU
- 15 general purpose 32-bit registers
- 32-bit program counter and status register
- 5 supervisor modes, 1 user mode

### ON-CHIP CACHE

- 8 kB internal cache or 16 kB RAM
- 4-way set associative
- Lockable entries
- Write through

### INTEGRAL 10/100 ETHERNET MAC

- 10/100 Mbs MII PHY
- Full- or half-duplex
- Station, broadcast, multicast address detection and filtering
- 128B transmit buffer
- 2 kB receive buffer
- Intelligent receive side-buffer size selection
- External CAM filtering support

### 10-CHANNEL DMA CONTROLLER

- 2 dedicated to Ethernet transmit/receive
- 4 dedicated to serial transmit/receive
- 2 dedicated to 1284 interface
- 2 dedicated to external peripherals
- Flexible buffer management

### IEEE 1284/ENI/GPIO INTERFACE USING SHARED PINS

- 4 IEEE 1284 parallel ports, host mode
- 64 K shared RAM ENI interface (8- or 16-bit)
- Full-duplex FIFO mode interface (8- or 16-bit)
- 32 B transmit and 32 B receive FIFOs

### SERIAL PORTS

- 2 fully independent HDLC/UART/SPI serial ports
- 32B transmit and 32B receive FIFOs
- Internal programmable bit rate generators
- Bit rates from 75 bps to 230 Kbps 16X mode
- Bit rates from 1200 bps to 4 Mbps: 1X mode
- Odd, even, or no parity
- 5, 6, 7 or 8 bits
- 1 or 2 stop bits
- Both internal & external clock support
- Receive side character and buffer gap timers
- 4 receive side data match detectors

### EXTERNAL BUS INTERFACE/ MEMORY CONTROLLER

- 44 MHz bus speed
- 5 independent programmable chip selects
- Supports 8-, 16-, 32-bit peripherals
- Supports external address decoding and cycle termination
- Supports dynamic bus sizing (8-, 16-, & 32-bit)
- ASYNC and SYNC peripheral timing
- All chip selects support SRAM, EDO DRAM, SDRAM, Flash, EEPROM without external glue logic
- Internal DRAM address multiplexing
- Internal refresh controller
- 256 MB addressing per chip select
- Burst-mode support
- 0-15 wait states per chip select
- Bootstrap support

### TIMERS

- 2 independent 27-bit programmable timers
- Programmable watch-dog timer
- Programmable bus timer

### GENERAL PURPOSE I/O

- 40 programmable I/O pins
- 16 general purpose input only pins
- 36 programmable edge or level interrupts

### CLOCK GENERATOR

- Simple external crystal
- On-board Phase Locked Loop
- Supports direct external clock input

### PACKAGE

- 208-pin BGA, 0.8 mm pitch
- PQFP
- Lead-free; RoHS compliant

### OTHER

- Operating voltage:
  - Core:  $2.5V \pm 10\%$
  - I/O Ring:  $3.3V \pm 10\%$
- Operating temperature range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

## NET+Works Integrated Development Package

NET+ARM network-attached processors are the core of the NET+Works family of solutions that add intelligence and connectivity to electronic devices. We offer extensive networking software to support industrial automation, building automation, point-of-sale, office automation and other enterprise applications.

### DEVELOPMENT TOOLS

- Green Hills® MULTI® IDE or Microcross GNU X-Tools™

### RTOS

- ThreadX® picokernel

### BOARD SUPPORT PACKAGE

- 10/100Base-T Ethernet
- UART
- SPI
- HDLC
- DMA
- Flash
- 1284 peripheral

### NETWORKING PROTOCOLS

- HTTP v1.1 Server
- POP3 and SMTP Email
- FTP Client and Server
- SNMP MIBII and proxy agent
- DHCP Client & DNS Client

### UTILITIES

- HTML-to-C compiler
- Download of Flash images
- Code builds
- File system

### DEVELOPMENT BOARD

- NET+50 based development board with Raven JTAG In Circuit Emulator (ICE)

### TECHNICAL SUPPORT

- Software maintenance and technical support plans are available

### MODEL.....PART NUMBERS

#### Model

For NET+OS Operating System  
For No Operating System, pSOS License  
For No Operating System

#### BGA

NET+50-BIT  
NET+50-BINP  
NET+50-BIN

#### PQFP

NET+50-QIT-3  
NET+50-QINP-3  
NET+50-QIN-3

Note: OS versions contain paid fees for the run-time license.

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