

CMOS μ P-Compatible 12-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND	-0.3V, +7V
V_{DD} to DGND	-0.3V, +7V
AGND to DGND	V_{DD}
DGND to AGND	V_{DD}
Digital Input Voltage to DGND (Pins 4-11, 13)	-0.3V, $V_{DD} + 0.3V$
V_{PIN1} , V_{PIN2} to AGND	-0.3V, $V_{DD} + 0.3V$
V_{REF} to AGND	$\pm 25V$
V_{RFB} to AGND	$\pm 25V$

Power Dissipation	450mW (derate 6mW/°C above +70°C)
Operating Temperature Range	
Commercial MX7542J, K, GK	0°C to +70°C
Industrial MX7542A, B, GB	-25°C to +85°C
Military MX7542S, T, GT	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = +5V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = GND$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Non-Linearity		MX7542J/A/S MX7542K/B/T MX7542GK/GB/GT			± 1 ± 0.5 ± 0.5	LSB
Differential Non-Linearity		MX7542J/A/S (Note 1) MX7542K/B/T (Note 2) MX7542GK/GB/GT (Note 2)			± 2 ± 1 ± 1	LSB
Gain Error		MX7542J/K/A/B/S/T MX7542J/K/A/B MX7542S/T	$T_A = 25^\circ C$ T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}		± 12.3 ± 13.5 ± 14.5	LSB
		MX7542GK/GB/GT MX7542GK/GB MX7542GT	$T_A = 25^\circ C$ T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}		± 1 ± 1 ± 2	
Gain Temperature Coefficient $\Delta \text{Gain}/\Delta \text{Temperature}$ (Note 4)				2	5	ppm/°C
Power Supply Rejection	PSRR	$V_{DD} = +4.75V$ to $+5.25V$	$T_A = 25^\circ C$ T_{MIN} to T_{MAX}		0.005 0.01	%/ V_{DD}
Output Leakage Current I_{OUT1} , I_{OUT2} (Note 3)		MX7542J/K/GK MX7542A/B/GB MX7542S/T/GT	$T_A = 25^\circ C$ T_{MIN} to T_{MAX} T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}		1 10 10 200	nA
DYNAMIC PERFORMANCE (Note 4)						
Output Current Settling Time		To 1/2 LSB, Out1 Load = 100 Ω			2	μs
Feedthrough Error		$V_{REF} = \pm 10V$ 10kHz sine wave			2.5	mVpp
REFERENCE INPUT						
Input Resistance (pin 15)	R_{REF}		8	15	25	k Ω
ANALOG OUTPUT (Note 4)						
Output Capacitance	C_{OUT1}	DAC Register 0000 0000 0000			75	pF
	C_{OUT1}	DAC Register 1111 1111 1111			260	
	C_{OUT2}	DAC Register 1111 1111 1111			75	
	C_{OUT2}	DAC Register 0000 0000 0000			260	

CMOS μ P-Compatible 12-Bit DAC

MX7542

ELECTRICAL CHARACTERISTICS (Continued)

($T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = +5V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = GND$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Logic HIGH Voltage	V _{INH}		+3.0			V
Logic LOW Voltage	V _{INL}				+0.8	
Logic Input Current	I _{IN}	0V or V _{DD}			1	μA
Input Capacitance (Note 4)	C _{IN}				8	pF
SWITCHING CHARACTERISTICS (see Figure 6) (Note 5)						
Write Pulse Width	t _{WR}	T _A = 25°C T _{MIN} to T _{MAX}	120 220			ns
Address-to-Write Hold Time	t _{AWH}	T _A = 25°C T _{MIN} to T _{MAX}	50 65			
Chip Select-to-Write Hold	t _{CWH}	T _A = 25°C T _{MIN} to T _{MAX}	50 100			
Minimum CLEAR Pulse Width	t _{CLR}	T _A = 25°C T _{MIN} to T _{MAX}	200 300			
BYTE LOADING						
Chip Select-to-WRITE Setup	t _{CWS}	T _A = 25°C T _{MIN} to T _{MAX}	60 130			ns
Address Valid-to-Write Setup	t _{AWS}	T _A = 25°C T _{MIN} to T _{MAX}	80 180			
Data Setup Time	t _{DS}	T _A = 25°C T _{MIN} to T _{MAX}	50 65			
Data Hold Time	t _{DH}	T _A = 25°C T _{MIN} to T _{MAX}	50 65			
DAC LOADING						
Chip Select-to-WRITE Setup	t _{CWS}	T _A = 25°C T _{MIN} to T _{MAX}	60 150			ns
Address valid-to-Write Setup	t _{AWS}	T _A = 25°C T _{MIN} to T _{MAX}	120 240			
POWER SUPPLY						
Supply Voltage	V _{DD}	5V ± 5%	4.75		5.25	V
Supply Current	I _{DD}				2.5	mA

Note 1: Monotonic to 11 bits from T_{MIN} to T_{MAX}

Note 2: Monotonic to 12 bits from T_{MIN} to T_{MAX}

Note 3: I_{OUT1} tested with DAC register loaded to all 0's.

I_{OUT2} tested with DAC register loaded to all 1's.

Note 4: Guaranteed by design but not tested.

Note 5: Sample tested at $+25^\circ C$ to ensure compliance.

CMOS μ P-Compatible 12-Bit DAC

Detailed Description

The basic MX7542 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarly weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Although the current at OUT1 or OUT2 will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF} minus the termination resistor current (R_T).

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 4). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 15k Ω and does not change with digital input code. The $I_{REF}/4096$ current source, which is actually the ladder termination resistor (R_T , Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors C_{OUT1} and C_{OUT2} represent the switches ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from approximately 75pF to 260pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

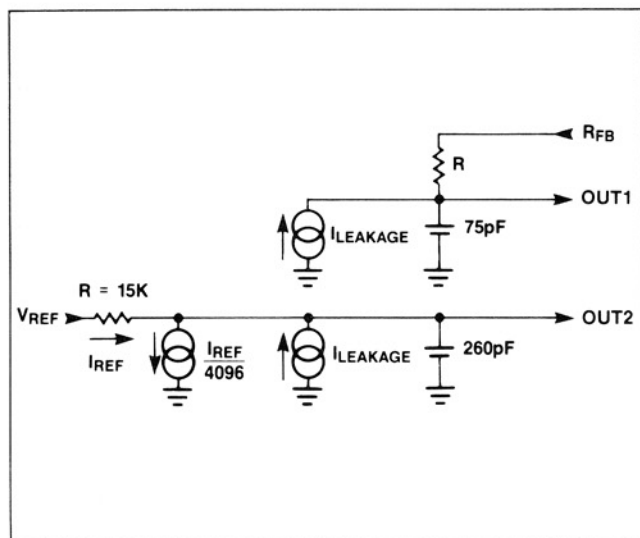


Figure 2. MX7542 DAC Equivalent Circuit, All Digital Inputs LOW

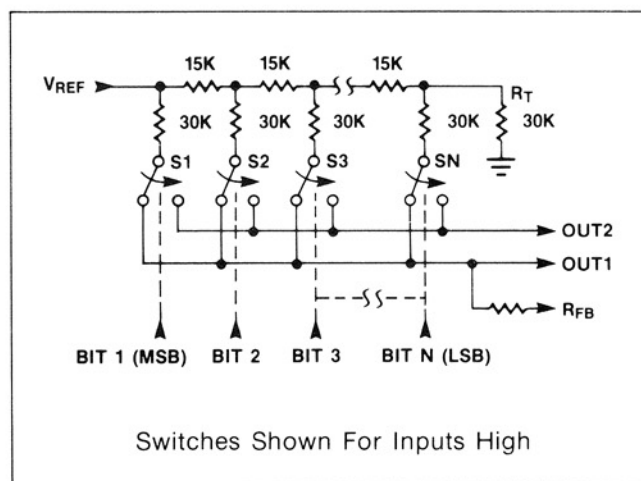


Figure 1. MX7542 Functional Diagram

Circuit Configurations

Unipolar Operation

The most common configuration for the MX7542 is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the MX7542 will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However, if the trims are desired and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/ $^{\circ}$ C) resistors should be used at R1 and R2.

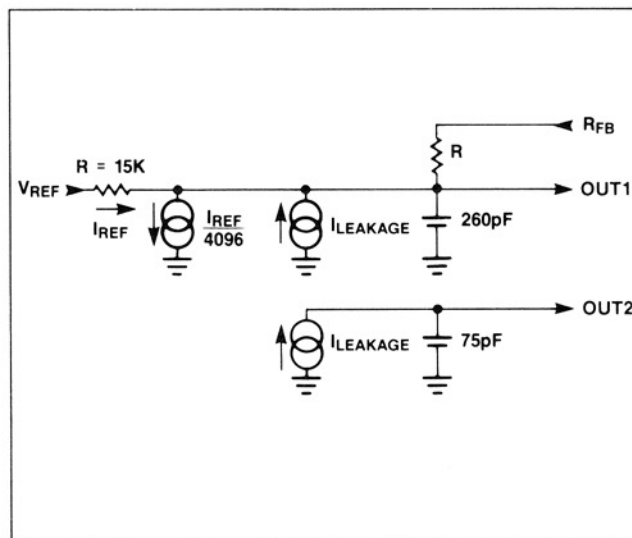


Figure 3. MX7542 DAC Equivalent Circuit, All Digital Inputs HIGH

CMOS μ P-Compatible 12-Bit DAC

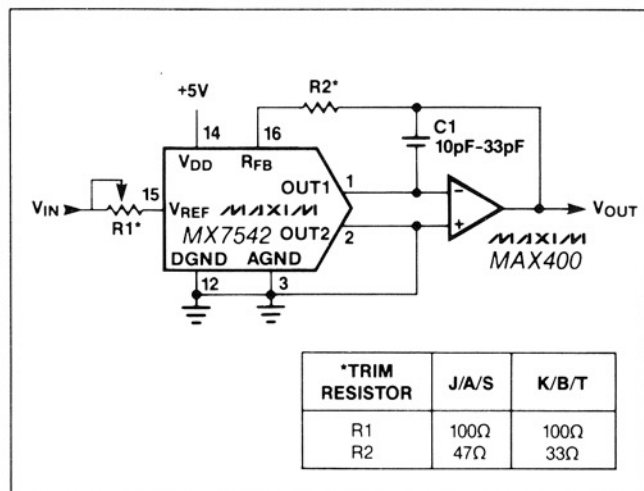


Figure 4. Unipolar Binary Operation

Table 1. Code Table—Unipolar Binary

DIGITAL INPUT		ANALOG OUTPUT
MSB	LSB	
1 1 1 1	1 1 1 1	$-V_{REF} \left(\frac{4095}{4096} \right)$
1 0 0 0	0 0 0 0	$-V_{REF} \left(\frac{2048}{4096} \right) = -\frac{V_{REF}}{2}$
0 0 0 0	0 0 0 0	$-V_{REF} \left(\frac{1}{4096} \right)$
0 0 0 0	0 0 0 0	0V

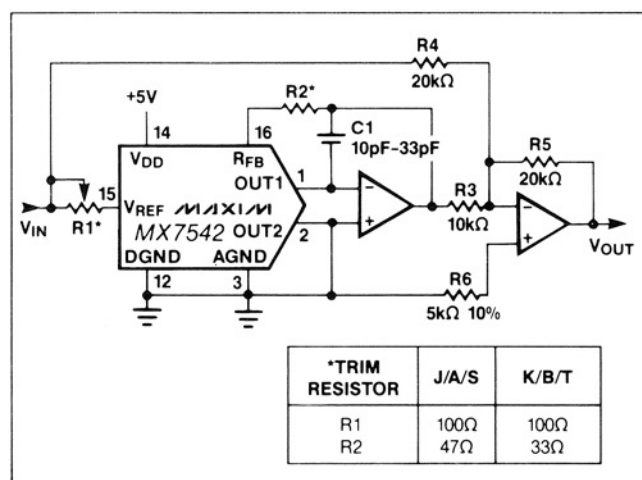


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table 2. Code Table—Bipolar (Offset Binary) Operation

DIGITAL INPUT		ANALOG OUTPUT
MSB	LSB	
1 1 1 1	1 1 1 1	$+V_{REF} \left(\frac{2047}{2048} \right)$
1 0 0 0	0 0 0 0	$+V_{REF} \left(\frac{1}{2048} \right)$
1 0 0 0	0 0 0 0	0V
0 1 1 1	1 1 1 1	$-V_{REF} \left(\frac{1}{2048} \right)$
0 0 0 0	0 0 0 0	$-V_{REF} \left(\frac{2048}{2048} \right)$

Bipolar Operation

With the circuit configuration in Figure 5, the MX7542 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. If gain and offset trims are not required, R1 and R2 in Figure 5 can be omitted.

CMOS μ P-Compatible 12-Bit DAC

Interface Logic

Interface Logic Information

The MX7542 Truth Table is shown in Table 3. The high, middle and low byte, 4 bit data registers are loaded separately. The 12-bit DAC register is then loaded with the contents of the 3 data registers. The interface timing (Figure 6) is the same as writing to static RAM.

The CLR input asynchronously resets the 12-Bit DAC Register to Code 0000 0000 0000. In a unipolar mode the DAC output will be set to 0 volts. In the bipolar mode a CLR input resets the DAC output to $-V_{REF}$.

Notes:

1. 1 indicates logic HIGH
2. 0 indicates logic LOW
3. X indicates don't care
4. $\uparrow$ indicates LOW to HIGH transition
5. MSB $\rightarrow$ $\overline{\text{XXXX}}$ $\overline{\text{XXXX}}$ $\overline{\text{XXXX}}$ $\rightarrow$ LSB
 high middle low
 byte byte byte
6. These control signals are level triggered.

Table 3. MX7542 Truth Table

MX7542 Control Inputs					MX7542 Operation	
A ₁	A ₀	CS	WR	CLR		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	X	1	No Operation Device Not Selected	
0	0	0		1	Load LOW Byte ⁽⁵⁾ Data Register On Edge As Shown	Load Applicable Data Register With Data At D ₀ -D ₃
0	1	0		1	Load MIDDLE Byte ⁽⁵⁾ Data Register On Edge As Shown	
1	0	0		1	Load HIGH Byte ⁽⁵⁾ Data Register On Edge As Shown	
1	1	0		1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers ⁽⁶⁾	

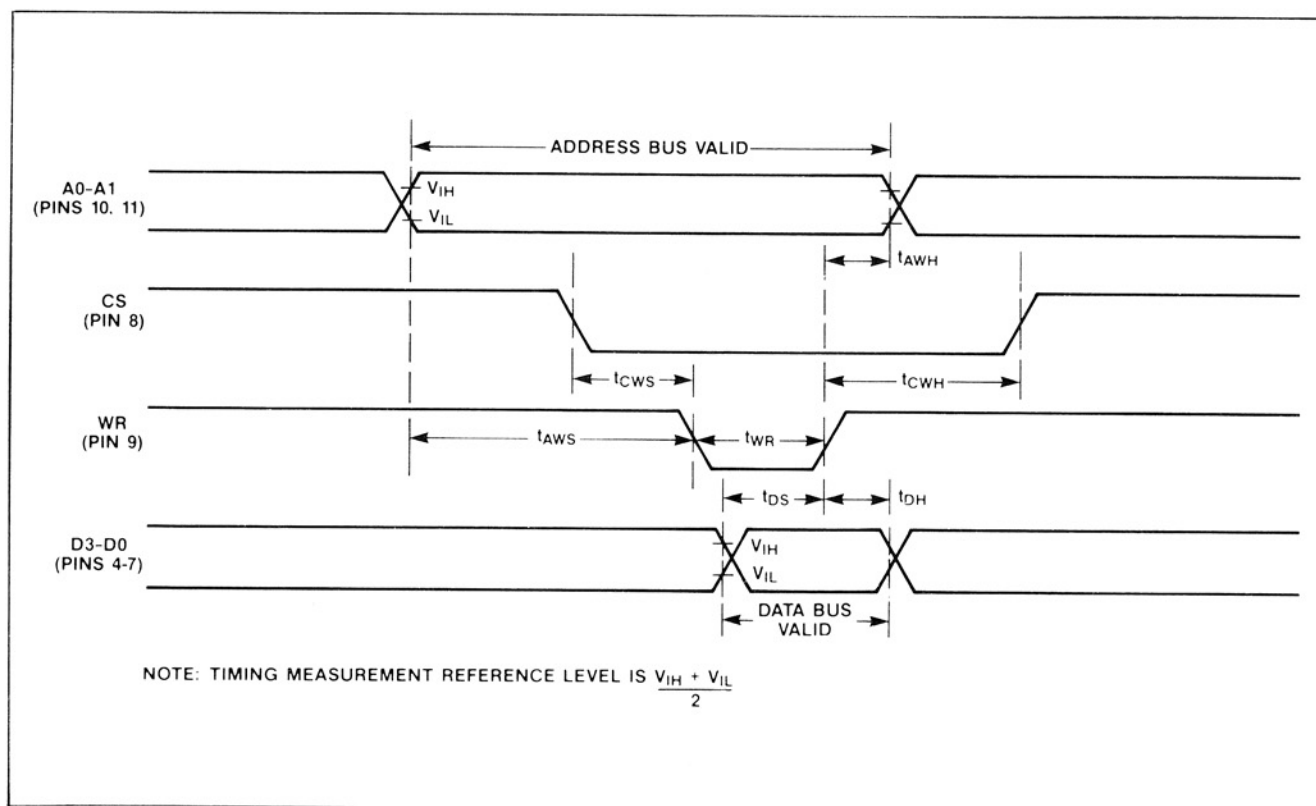


Figure 6. MX7542 Timing Diagram

CMOS μ P-Compatible 12-Bit DAC

MX7542

Application Information

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's input offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O),$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 15k Ω to 45k Ω . The error voltage range is then typically 4/3 V_{OS} to 2 V_{OS} , a change of 2/3 V_{OS} . An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with $V_{REF} = 10V$. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor". This resistor adds to offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF} , and the DAC outputs.

Compensations

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

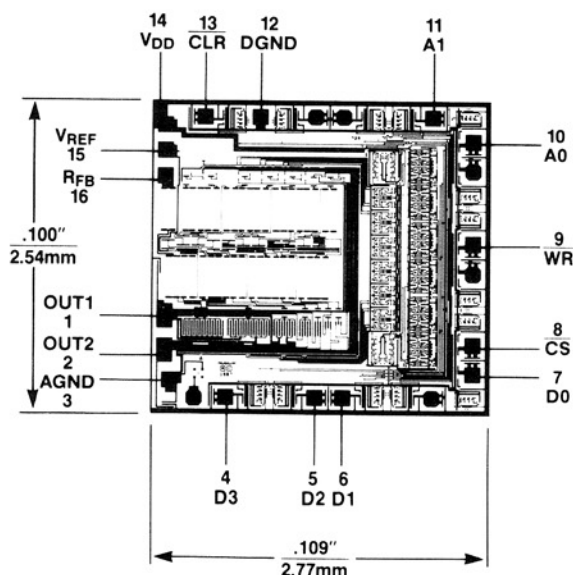
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting inputs are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2 Ω) path. The current at OUT1 and OUT2 varies with input code, creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1 μ F bypass capacitor, in parallel with a 0.01 μ F ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The MX7542 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or GND when not used. It is also good practice to connect active inputs to V_{DD} or GND through high valued resistors (1M Ω) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography



MX7542

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