FIGURE 1-1: TYPICAL APPLICATION SCHEMATIC

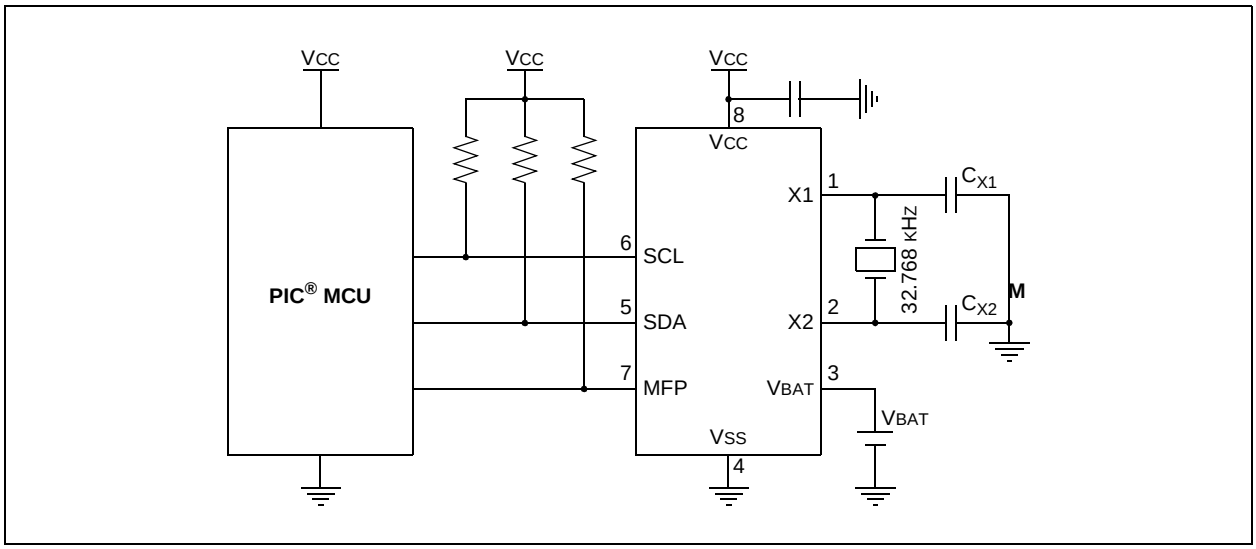
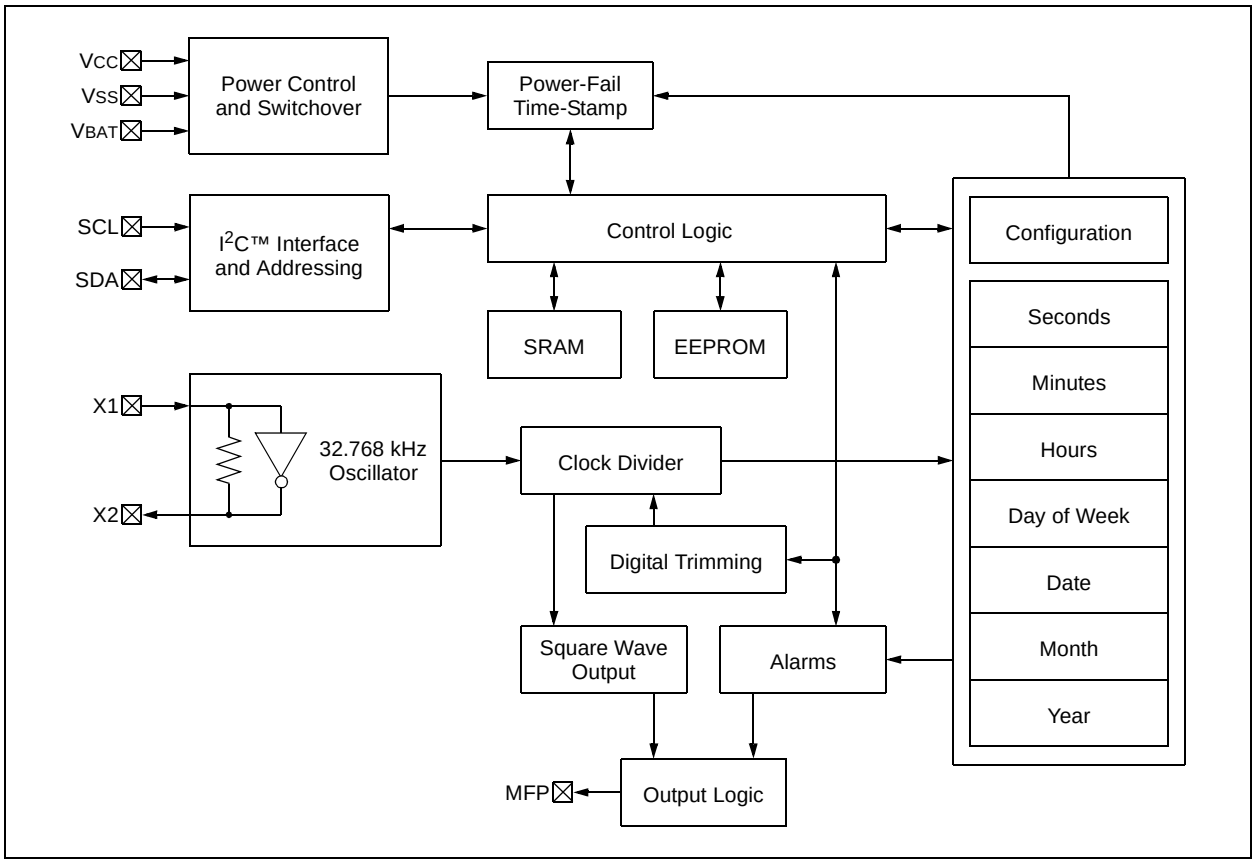


FIGURE 1-2: BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs (except SDA and SCL) w.r.t. VSS.....-0.6V to VCC +1.0V

SDA and SCL w.r.t. VSS.....-0.6V to 6.5V

Storage temperature.....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins.....≥ 4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
D1	VIH	High-level Input Voltage	0.7 VCC	—	—	V	
D2	VIL	Low-level Input Voltage	—	—	0.3 VCC	V	VCC ≥ 2.5V
					0.2 VCC		VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	0.05 VCC	—	—	V	(**Note 1**)
D4	VOL	Low-level Output Voltage (MFP, SDA pins)	—	—	0.40	V	IOL = 3.0 mA; VCC = 4.5V
							IOL = 2.1 mA; VCC = 2.5V
D5	ILI	Input Leakage Current	—	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	—	±1	µA	VOUT = VSS or VCC
D7	CIN	Pin Capacitance (SDA, SCL, MFP pins)	—	—	10	pF	VCC = 5.0V **(Note 1)**
	COUT						TA = 25°C, f = 1 MHz
D8	COSC	Oscillator Pin Capacitance (X1, X2 pins)	—	3	—	pF	(**Note 1**)
D9	Icceerd	EEPROM Operating Current	—	—	400	µA	VCC = 5.5V, SCL = 400 kHz
	Icceewr				3	mA	VCC = 5.5V
D10	Iccread	SRAM/RTCC Register Operating Current	—	—	300	µA	VCC = 5.5V, SCL = 400 kHz
	Iccwrite				400		VCC = 5.5V, SCL = 400 kHz
D11	Iccdat	VCC Data-retention Current (oscillator off)	—	—	1	µA	SCL, SDA, VCC = 5.5V
D12	Icct	Timekeeping Current	—	1.2	—	µA	VCC = 3.3V **(Note 1)**
D13	VTRIP	Power-fail Switchover Voltage	1.3	1.5	1.7	V	
D14	VBAT	Backup Supply Voltage Range	1.3	—	5.5	V	(**Note 1**)

Note 1: This parameter is not tested but ensured by characterization.

2: Typical measurements taken at room temperature.

DC CHARACTERISTICS (Continued)			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
D15	IBATT	Timekeeping Backup Current	—	—	850	nA	VBAT = 1.3V, VCC = VSS **(Note 1)**
				925	1200		VBAT = 3.0V, VCC = VSS **(Note 1)**
				—	9000		VBAT = 5.5V, VCC = VSS **(Note 1)**
D16	IBATDAT	VBAT Data Retention Current (oscillator off)	—	—	750	nA	VBAT = 3.6V, VCC = VSS

Note 1: This parameter is not tested but ensured by characterization.
2: Typical measurements taken at room temperature.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	—	100	kHz	1.8V ≤ VCC < 2.5V
					400		2.5V ≤ VCC ≤ 5.5V
2	THIGH	Clock High Time	4000	—	—	ns	1.8V ≤ VCC < 2.5V
			600				2.5V ≤ VCC ≤ 5.5V
3	Tlow	Clock Low Time	4700	—	—	ns	1.8V ≤ VCC < 2.5V
			1300				2.5V ≤ VCC ≤ 5.5V
4	Tr	SDA and SCL Rise Time **(Note 1)**	—	—	1000	ns	1.8V ≤ VCC < 2.5V
					300		2.5V ≤ VCC ≤ 5.5V
5	Tf	SDA and SCL Fall Time **(Note 1)**	—	—	1000	ns	1.8V ≤ VCC < 2.5V
					300		2.5V ≤ VCC ≤ 5.5V
6	Thd:sta	Start Condition Hold Time	4000	—	—	ns	1.8V ≤ VCC < 2.5V
			600				2.5V ≤ VCC ≤ 5.5V
7	Tsu:sta	Start Condition Setup Time	4700	—	—	ns	1.8V ≤ VCC < 2.5V
			600				2.5V ≤ VCC ≤ 5.5V
8	Thd:dat	Data Input Hold Time	0	—	—	ns	**(Note 3)**
9	Tsu:dat	Data Input Setup Time	250	—	—	ns	1.8V ≤ VCC < 2.5V
			100				2.5V ≤ VCC ≤ 5.5V
10	Tsu:sto	Stop Condition Setup Time	4000	—	—	ns	1.8V ≤ VCC < 2.5V
			600				2.5V ≤ VCC ≤ 5.5V
11	Taa	Output Valid from Clock	—	—	3500	ns	1.8V ≤ VCC < 2.5V
					900		2.5V ≤ VCC ≤ 5.5V
12	Tbuf	Bus Free Time: Bus time must be free before a new transmission can start	4700	—	—	ns	1.8V ≤ VCC < 2.5V
			1300				2.5V ≤ VCC ≤ 5.5V
13	Tsp	Input Filter Spike Suppression (SDA and SCL pins)	—	—	50	ns	**(Note 1)**
14	Twc	Write Cycle Time (byte or page)	—	—	5	ms	
15	Tfvcc	VCC Fall Time	300	—	—	µs	**(Note 1)**
16	Trvcc	VCC Rise Time	0	—	—	µs	**(Note 1)**
17	Fosc	Oscillator Frequency	—	32.768	—	kHz	
18	Tosf	Oscillator Timeout Period	1	—	—	ms	**(Note 1)**
19	—	Endurance	1M	—	—	cycles	Page Mode, 25°C, VCC = 5.5V **(Note 2)**

Note 1: Not 100% tested.

2: This parameter is not tested but ensured by characterization.

3: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

FIGURE 1-3: I²C™ BUS TIMING DATA

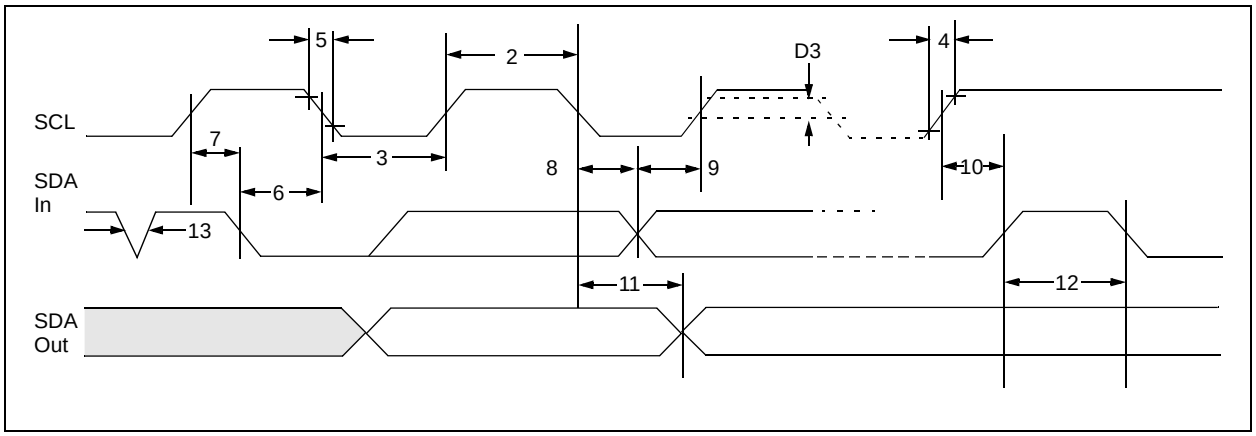
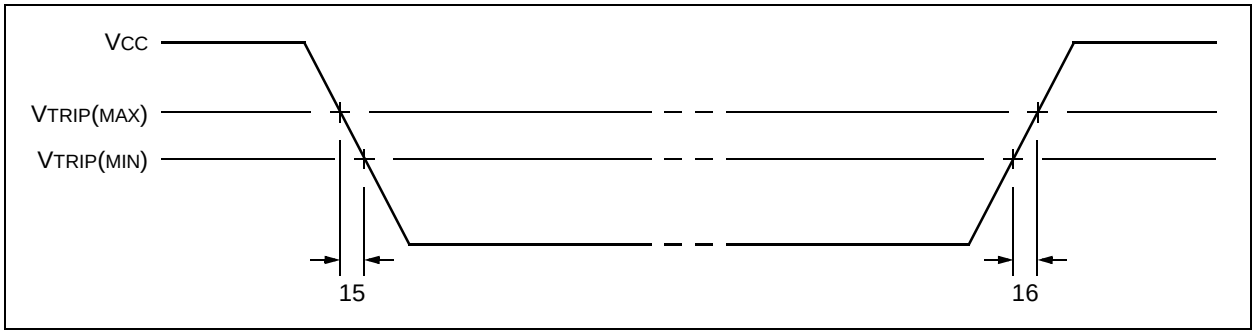


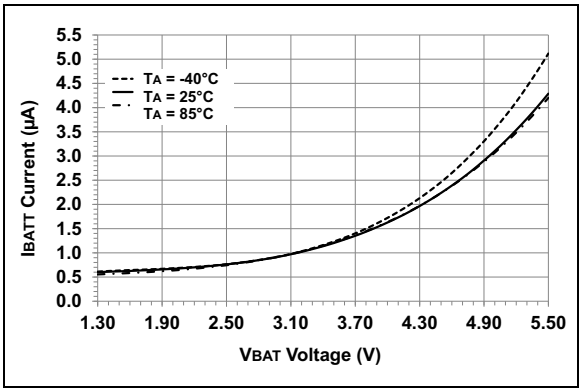
FIGURE 1-4: POWER SUPPLY TRANSITION TIMING



2.0 TYPICAL PERFORMANCE CURVE

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data represented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 2-1: TIMEKEEPING BACKUP CURRENT VS. BACKUP SUPPLY VOLTAGE



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	8-pin SOIC	8-pin MSOP	8-pin TSSOP	8-pin TDFN	Function
X1	1	1	1	1	Quartz Crystal Input, External Oscillator Input
X2	2	2	2	2	Quartz Crystal Output
VBAT	3	3	3	3	Battery Backup Supply Input
Vss	4	4	4	4	Ground
SDA	5	5	5	5	Bidirectional Serial Data (I^2C™)
SCL	6	6	6	6	Serial Clock (I^2C)
MFP	7	7	7	7	Multifunction Pin
Vcc	8	8	8	8	Primary Power Supply

Note: Exposed pad on TFDN can be connected to Vss or left floating.

3.1 Oscillator Input/Output (X1, X2)

These pins are used as the connections for an external 32.768 kHz quartz crystal and load capacitors. X1 is the crystal oscillator input and X2 is the output. The MCP7941X is designed to allow for the use of external load capacitors in order to provide additional flexibility when choosing external crystals. The MCP7941X is optimized for crystals with a specified load capacitance of 6-9 pF.

X1 also serves as the external clock input when the MCP7941X is configured to use an external oscillator.

3.2 Backup Supply (VBAT)

This is the input for a backup supply to maintain the RTCC and SRAM registers during the time when VCC is unavailable.

If the battery backup feature is not being used, the VBAT pin should be connected to VSS.

3.3 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typically 10 kΩ for 100 kHz, 2 kΩ for 400 kHz). For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

3.4 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

3.5 Multifunction Pin (MFP)

This is an output pin used for the alarm and square wave output functions. It can also serve as a general purpose output pin by controlling the OUT bit in the CONTROL register.

The MFP is an open-drain output and requires a pull-up resistor to VCC (typically 10 kΩ). This pin may be left floating if not used.

4.0 I²C BUS CHARACTERISTICS

4.1 I²C Interface

The MCP7941X supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data is defined as receiver. The bus has to be controlled by a master device which generates the Start and Stop conditions, while the MCP7941X works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.1.1 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1.1.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.1.1.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.1.1.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.1.1.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

4.1.1.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note 1:	The MCP7941X does not generate an Acknowledge in response to an EEPROM control byte if an internal EEPROM programming cycle is in progress, but the SRAM and RTCC registers can still be accessed.
2:	The I²C interface is disabled while operating from the backup power supply.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (MCP7941X) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

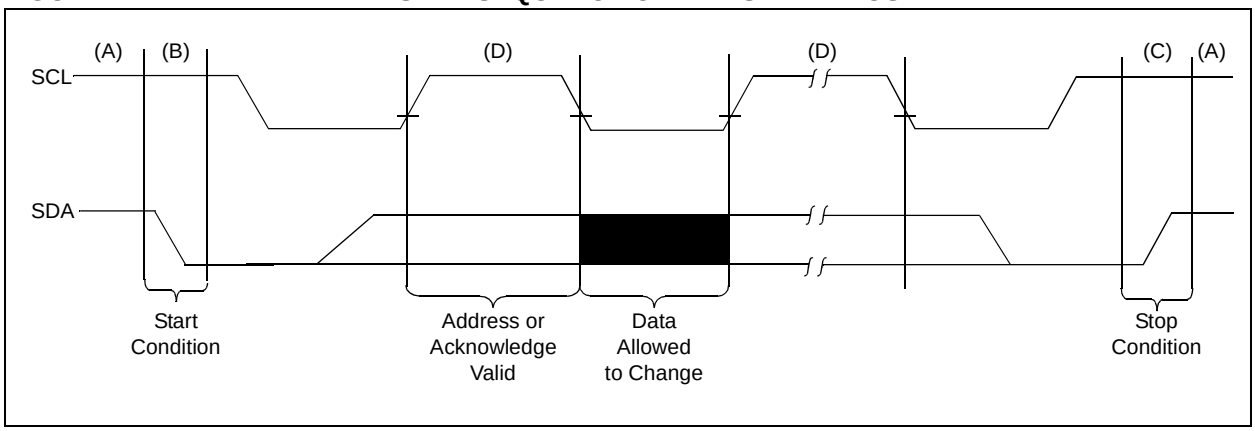
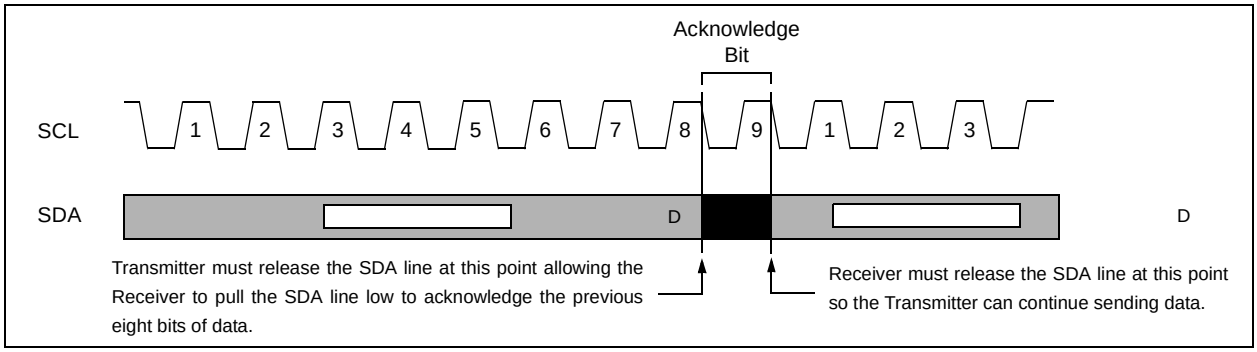


FIGURE 4-2: ACKNOWLEDGE TIMING



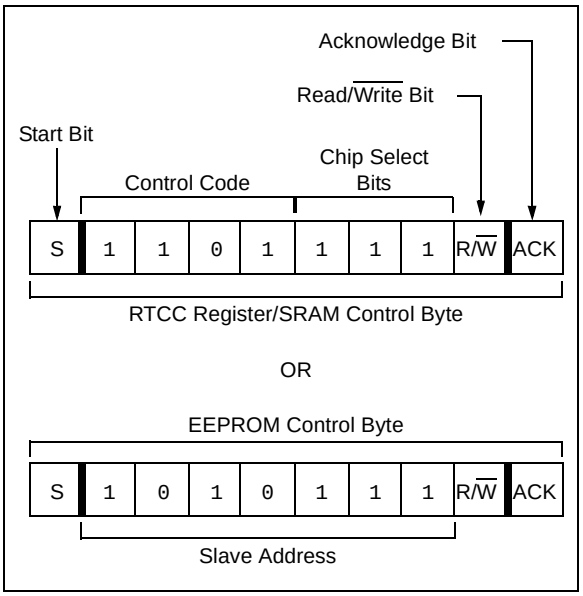
4.1.2 DEVICE ADDRESSING

The control byte is the first byte received following the Start condition from the master device (Figure 4-3). The control byte begins with a 4-bit control code. For the MCP7941X, this is set as '1010' for EEPROM read and write operations, and '1101' for SRAM/RTCC register read and write operations. The next three bits are non-configurable Chip Select bits that must always be set to '1'.

The last bit of the control byte defines the operation to be performed. When set to a '1' a read operation is selected, and when set to a '0' a write operation is selected.

The combination of the 4-bit control code and the three Chip Select bits is called the slave address. Upon receiving a valid slave address, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the MCP7941X will select a read or a write operation.

FIGURE 4-3: CONTROL BYTE FORMAT



5.0 FUNCTIONAL DESCRIPTION

The MCP7941X is a highly-integrated Real-Time Clock/Calendar (RTCC). Using an on-board, low-power oscillator, the current time is maintained in seconds, minutes, hours, day of week, date, month, and year. The MCP7941X also features 64 bytes of general purpose SRAM, 1 Kbit of EEPROM and eight bytes of protected EEPROM. Two alarm modules allow interrupts to be generated at specific times with flexible comparison options. Digital trimming can be used to compensate for inaccuracies inherent with crystals. Using the backup supply input and an integrated power switch, the MCP7941X will automatically switch to backup power when primary power is unavailable, allowing the current time and the SRAM contents to be maintained. The time-stamp module captures the time when primary power is lost and when it is restored.

The RTCC configuration and STATUS registers are used to access all of the modules featured on the MCP7941X.

5.1 Memory Organization

The MCP7941X features four different blocks of memory: the RTCC registers, general purpose SRAM, 1 Kbit EEPROM with software write-protect, and protected EEPROM. The RTCC registers and SRAM share the same address space, accessed through the ‘1101111X’ control byte. The EEPROM regions are in a separate address space and are accessed using the ‘1010111X’ control byte (Figure 5-1). Unused locations are not accessible. The MCP7941X will not acknowledge if the address is out of range, as shown in the shaded region of the memory map in Figure 5-1.

The RTCC registers are contained in addresses 0x00-0x1F. Table 5-1 shows the detailed RTCC register map. There are 64 bytes of user-accessible SRAM, located in the address range 0x20-0x5F. The SRAM is a separate block from the RTCC registers. All RTCC registers and SRAM locations are maintained while operating from backup power.

The EEPROM space is located in addresses 0x00-0x7F while the protected EEPROM section is located in addresses 0xF0-0xF7. A STATUS register, used to protect regions of the EEPROM section, is located at address 0xFF.

FIGURE 5-1: MEMORY MAP

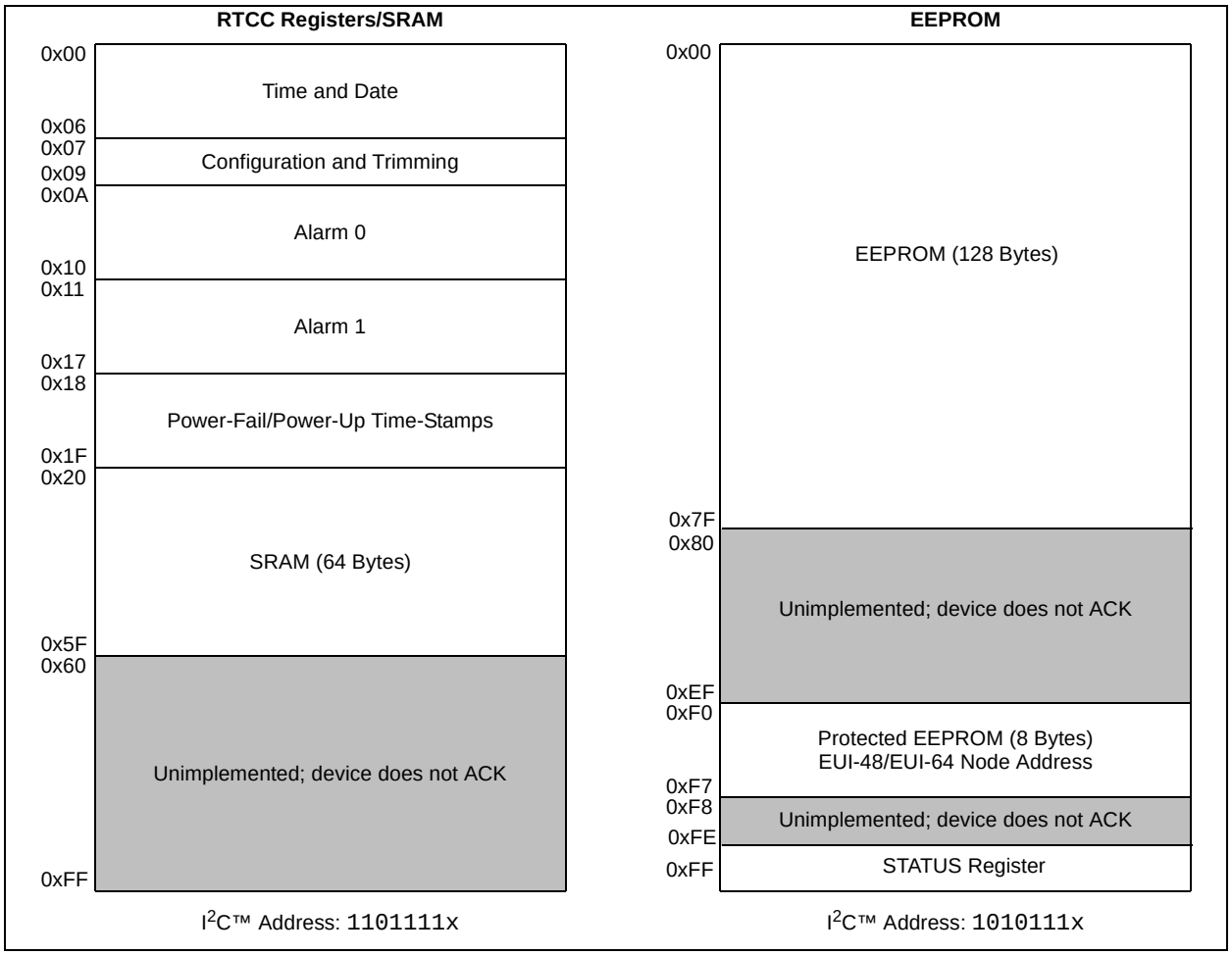


TABLE 5-1: DETAILED RTCC REGISTER MAP

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Section 5.3 "Timekeeping"									
00h	RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
01h	RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
02h	RTCHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
03h	RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0
04h	RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
05h	RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
06h	RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
07h	CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0
08h	OSCTRIM	SIGN	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0
09h	EEUNLOCK	Protected EEPROM Unlock Register (not a physical register)							
Section 5.4 "Alarms"									
0Ah	ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
0Bh	ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
0Ch	ALM0HOUR	—	12/$\overline{24}$(2)	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
0Dh	ALM0WKDAY	ALMPOL	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0
0Eh	ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
0Fh	ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
10h	Reserved	Reserved – Do not use							
Section 5.4 "Alarms"									
11h	ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
12h	ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
13h	ALM1HOUR	—	12/$\overline{24}$(2)	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
14h	ALM1WKDAY	ALMPOL(3)	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0
15h	ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
16h	ALM1MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
17h	Reserved	Reserved – Do not use							
Section 5.7.1 "Power-Fail Time-Stamp"									
Power-Down Time Stamp									
18h	PWRDNMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
19h	PWRDNHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
1Ah	PWRDNDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
1Bh	PWRDNMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
Power-Up Time Stamp									
1Ch	PWRUPMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
1Dh	PWRUPHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
1Eh	PWRUPDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
1Fh	PWRUPMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0

Note 1: Grey areas are unimplemented.

2: The 12/$\overline{24}$ bits in the ALMxHOUR registers are read-only and reflect the value of the 12/$\overline{24}$ bit in the RTCHOUR register.

3: The ALMPOL bit in the ALM1WKDAY register is read-only and reflects the value of the ALMPOL bit in the ALM0WKDAY register.

5.2 Oscillator Configuration

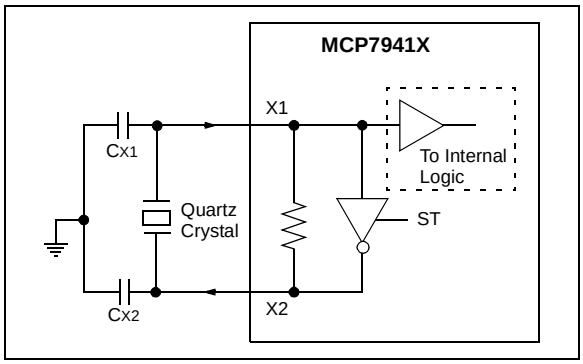
The MCP7941X can be operated in two different oscillator configurations: using an external crystal or using an external clock input.

5.2.1 EXTERNAL CRYSTAL

The crystal oscillator circuit on the MCP7941X is designed to operate with a standard 32.768 kHz tuning fork crystal and matching external load capacitors. By using external load capacitors, the MCP7941X allows for a wide selection of crystals. Suitable crystals have a load capacitance (C_L) of 6-9 pF. Crystals with a load capacitance of 12.5 pF are not recommended.

Figure 5-2 shows the pin connections when using an external crystal.

FIGURE 5-2: CRYSTAL OPERATION



Note 1:	The ST bit must be set to enable the crystal oscillator circuit.
2:	Always verify oscillator performance over the voltage and temperature range that is expected for the application.

5.2.1.1 Choosing Load Capacitors

C_L is the effective load capacitance as seen by the crystal, and includes the physical load capacitors, pin capacitance, and stray board capacitance. Equation 5-1 can be used to calculate C_L.

C_{X1} and C_{X2} are the external load capacitors. They must be chosen to match the selected crystal's specified load capacitance.

Note:	If the load capacitance is not correctly matched to the chosen crystal's specified value, the crystal may give a frequency outside of the crystal manufacturer's specifications.

EQUATION 5-1: LOAD CAPACITANCE CALCULATION

$$C_L = \frac{C_{X1} \times C_{X2}}{C_{X1} + C_{X2}} + C_{STRAY}$$

Where:

C_L = Effective load capacitance
C_{X1} = Capacitor value on X1 + C_{OSC}
C_{X2} = Capacitor value on X2 + C_{OSC}
C_{STRAY} = PCB stray capacitance

5.2.1.2 Layout Considerations

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

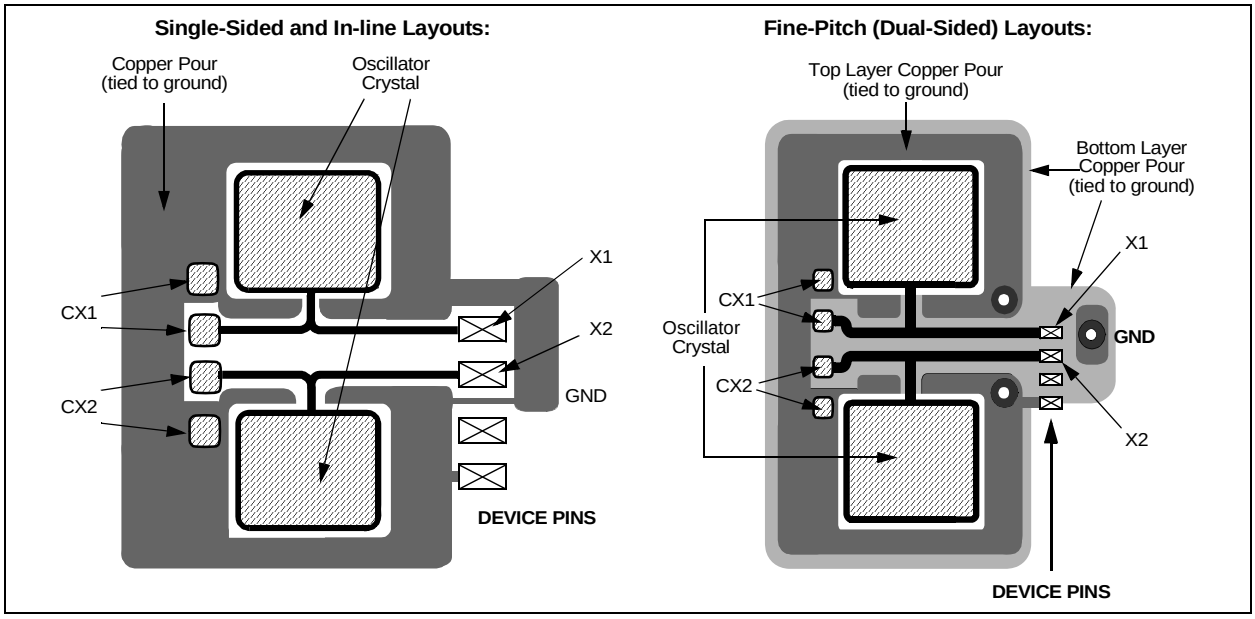
Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to V_{SS}. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 5-3. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN1365, "Recommended Usage of Microchip Serial RTCC Devices"*
- *AN1519, "Recommended Crystals for Microchip Stand-Alone Real-Time Clock Calendar Devices"*

FIGURE 5-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

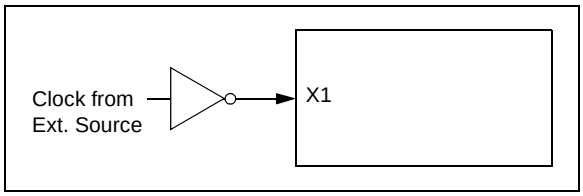


5.2.2 EXTERNAL CLOCK INPUT

A 32.768 kHz external clock source can be connected to the X1 pin (Figure 5-4). When using this configuration, the X2 pin should be left floating.

Note:	The EXTOSC bit must be set to enable an external clock source.

FIGURE 5-4: EXTERNAL CLOCK INPUT OPERATION



5.2.3 OSCILLATOR FAILURE STATUS

The MCP7941X features an oscillator failure flag, OSCRUN, that indicates whether or not the oscillator is running. The OSCRUN bit is automatically set after 32 oscillator cycles are detected. If no oscillator cycles are detected for more than TOSF, then the OSCRUN bit is automatically cleared (Figure 5-5). This can occur if the oscillator is stopped by clearing the ST bit or due to oscillator failure.

FIGURE 5-5: OSCILLATOR FAILURE STATUS TIMING DIAGRAM

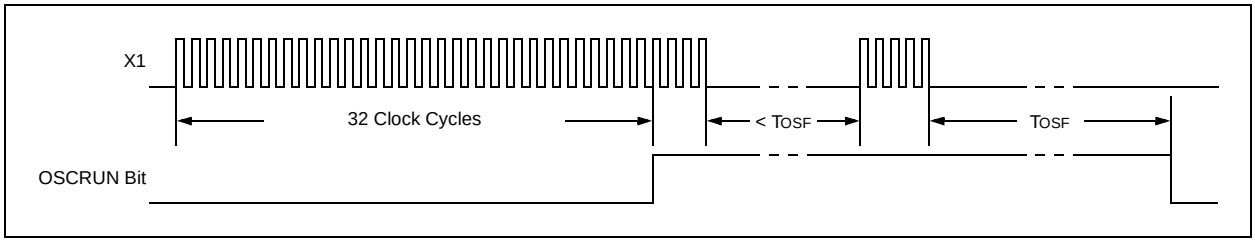


TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH OSCILLATOR CONFIGURATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	17
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	19
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	27

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by oscillator configuration.

5.3 Timekeeping

The MCP7941X maintains the current time and date using an external 32.768 kHz crystal or clock source. Separate registers are used for tracking seconds, minutes, hours, day of week, date, month, and year. The MCP7941X automatically adjusts for months with less than 31 days and compensates for leap years from 2001 to 2399. The year is stored as a two-digit value.

Both 12-hour and 24-hour time formats are supported and are selected using the 12/$\overline{24}$ bit.

The day of week value counts from 1 to 7, increments at midnight, and the representation is user-defined (i.e., the MCP7941X does not require 1 to equal Sunday, etc.).

All time and date values are stored in the registers as binary-coded decimal (BCD) values. The MCP7941X will continue to maintain the time and date while operating off the backup supply.

When reading from the timekeeping registers, the registers are buffered to prevent errors due to rollover of counters. The following events cause the buffers to be updated:

- When a read is initiated from the RTCC registers (addresses 0x00 to 0x1F)
- During an RTCC register read operation, when the register address rolls over from 0x1F to 0x00

The timekeeping registers should be read in a single operation to utilize the on-board buffers and avoid rollover issues.

Note 1: Loading invalid values into the time and date registers will result in undefined operation.

2: To avoid rollover issues when loading new time and date values, the oscillator/clock input should be disabled by clearing the ST bit for External Crystal mode and the EXTOSC bit for External Clock Input mode. After waiting for the OSCRUN bit to clear, the new values can be loaded and the ST or EXTOSC bit can then be re-enabled.

5.3.1 DIGIT CARRY RULES

The following list explains which timer values cause a digit carry when there is a rollover:

- Time of day: from 11:59:59 PM to 12:00:00 AM (12-hour mode) or 23:59:59 to 00:00:00 (24-hour mode), with a carry to the Date and Weekday fields
- Date: carries to the Month field according to Table 5-3
- Weekday: from 7 to 1 with no carry
- Month: from 12/31 to 01/01 with a carry to the Year field
- Year: from 99 to 00 with no carry

TABLE 5-3: DAY TO MONTH ROLLOVER SCHEDULE

Month	Name	Maximum Date
01	January	31
02	February	28 or 29(1)
03	March	31
04	April	30
05	May	31
06	June	30
07	July	31
08	August	31
09	September	30
10	October	31
11	November	30
12	December	31

Note 1: 29 during leap years, otherwise 28.

REGISTER 5-1: RTCSEC: TIMEKEEPING SECONDS VALUE REGISTER (ADDRESS 0x00)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **ST**: Start Oscillator bit
1 = Oscillator enabled
0 = Oscillator disabled

bit 6-4 **SECTEN<2:0>**: Binary-Coded Decimal Value of Second’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>**: Binary-Coded Decimal Value of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-2: RTCMIN: TIMEKEEPING MINUTES VALUE REGISTER (ADDRESS 0x01)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented**: Read as ‘0’

bit 6-4 **MINTEN<2:0>**: Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>**: Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-3: RTCHOUR: TIMEKEEPING HOURS VALUE REGISTER (ADDRESS 0x02)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented**: Read as '0'

bit 6 **12/$\overline{24}$**: 12 or 24 Hour TIme Format bit
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM**: AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0**: Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>**: Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented**: Read as '0'

bit 6 **12/$\overline{24}$**: 12 or 24 Hour TIme Format bit
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>**: Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2

bit 3-0 **HRONE<3:0>**: Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

REGISTER 5-4: RTCWKDAY: TIMEKEEPING WEEKDAY VALUE REGISTER (ADDRESS 0x03)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5 **OSCRUN**: Oscillator Status bit
1 = Oscillator is enabled and running
0 = Oscillator has stopped or has been disabled

bit 4 **PWRFAIL**: Power Failure Status bit(1, 2)
1 = Primary power was lost and the power-fail time-stamp registers have been loaded (must be cleared in software). Clearing this bit resets the power-fail time-stamp registers to '0'.
0 = Primary power has not been lost

bit 3 **VBATEN**: External Battery Backup Supply (V_{BAT}) Enable bit
1 = V_{BAT} input is enabled
0 = V_{BAT} input is disabled

bit 2-0 **WKDAY<2:0>**: Binary-Coded Decimal Value of Day of Week
Contains a value from 1 to 7. The representation is user-defined.

Note 1: The PWRFAIL bit must be cleared to log new time-stamp data. This is to ensure previous time-stamp data is not lost.

2: The PWRFAIL bit cannot be written to a '1' in software. Writing to the RTCWKDAY register will always clear the PWRFAIL bit.

REGISTER 5-5: RTCDATE: TIMEKEEPING DATE VALUE REGISTER (ADDRESS 0x04)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-4 **DATETEN<1:0>**: Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>**: Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

REGISTER 5-6: RTCMTH: TIMEKEEPING MONTH VALUE REGISTER (ADDRESS 0x05)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5 **LPYR**: Leap Year bit
1 = Year is a leap year
0 = Year is not a leap year

bit 4 **MTHTEN0**: Binary-Coded Decimal Value of Month's Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>**: Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

REGISTER 5-7: RTCYEAR: TIMEKEEPING YEAR VALUE REGISTER (ADDRESS 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-4 **YRTEN<3:0>**: Binary-Coded Decimal Value of Year's Tens Digit
Contains a value from 0 to 9

bit 4 **YRONE<3:0>**: Binary-Coded Decimal Value of Year's Ones Digit
Contains a value from 0 to 9

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMEKEEPING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	17
RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	17
RTCHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	18
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	19
RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	19
RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE'	MTHONE0	20
RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0	27

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in timekeeping.

5.4 Alarms

The MCP7941X features two independent alarms. Each alarm can be used to either generate an interrupt at a specific time in the future, or to generate a periodic interrupt every minute, hour, day, day of week, or month.

There is a separate interrupt flag, ALMxIF, for each alarm. The interrupt flags are set by hardware when the chosen alarm mask condition matches (Table 5-5). The interrupt flags must be cleared in software.

If either alarm module is enabled by setting the corresponding ALMxEN bit in the CONTROL register, and if the square wave clock output is disabled (SQWEN = 0), then the MFP will operate in Alarm Interrupt Output mode. Refer to **Section 5.5 "Output Configurations"** for details. The alarm interrupt output is available while operating from the backup power supply.

Both Alarm0 and Alarm1 offer identical operation. All time and date values are stored in the registers as binary-coded decimal (BCD) values.

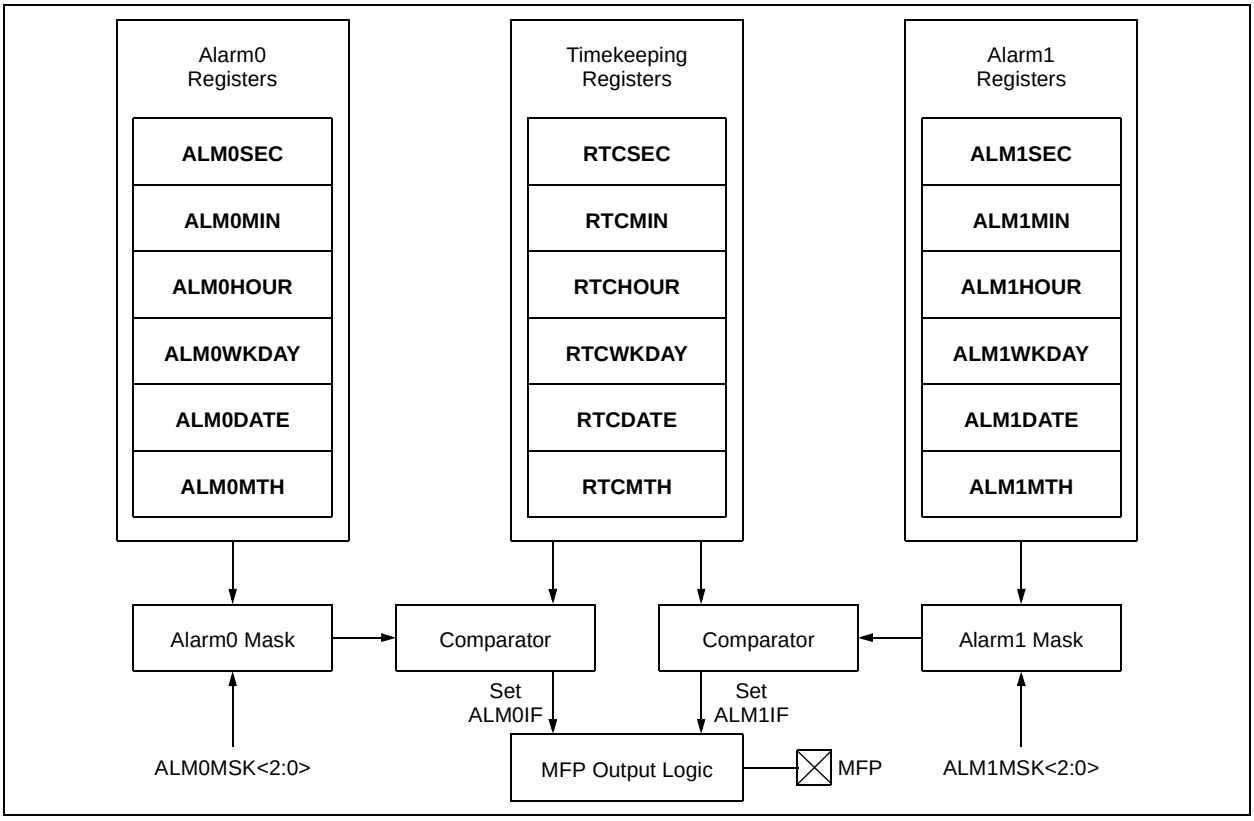
Note:	Throughout this section, references to the register and bit names for the alarm modules are referred to generically by the use of 'x' in place of the specific module number. Thus, "ALMxSEC" might refer to the seconds register for Alarm0 or Alarm1.

TABLE 5-5: ALARM MASKS

ALMxMSK<2:0>	Alarm Asserts on Match of
000	Seconds
001	Minutes
010	Hours
011	Day of Week
100	Date
101	Reserved
110	Reserved
111	Seconds, Minutes, Hours, Day of Week, Date, and Month

Note 1:	The alarm interrupt flags must be cleared by the user. If a flag is cleared while the corresponding alarm condition still matches, the flag will be set again, generating another interrupt.
2:	Loading invalid values into the alarm registers will result in undefined operation.

FIGURE 5-6: ALARM BLOCK DIAGRAM



5.4.1 CONFIGURING THE ALARM

In order to configure the alarm modules, the following steps need to be performed:

1. Load the timekeeping registers and enable the oscillator
2. Configure the ALMxMSK<2:0> bits to select the desired alarm mask
3. Set or clear the ALMPOL bit according to the desired output polarity
4. Ensure the ALMxIF flag is cleared
5. Based on the selected alarm mask, load the alarm match value into the appropriate register(s)
6. Enable the alarm module by setting the ALMxEN bit

REGISTER 5-8: ALMxSEC: ALARM0/1 SECONDS VALUE REGISTER (ADDRESSES 0x0A/0x11)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-9: ALMxMIN: ALARM0/1 MINUTES VALUE REGISTER (ADDRESSES 0x0B/0x12)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-10: ALMxHOUR: ALARM0/1 HOURS VALUE REGISTER (ADDRESSES 0x0C/0x13)

U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit(1)
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit(1)
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

Note 1: This bit is read-only and reflects the value of the 12/$\overline{24}$ bit in the RTCHOUR register.

REGISTER 5-11: ALMxWKDAY: ALARM0/1 WEEKDAY VALUE REGISTER (ADDRESSES 0x0D/0x14)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
ALMPOL	ALMxMSK2	ALMxMSK1	ALMxMSK0	ALMxIF	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **ALMPOL:** Alarm Interrupt Output Polarity bit
1 = Asserted output state of MFP is a logic high level
0 = Asserted output state of MFP is a logic low level

bit 6-4 **ALMxMSK<2:0>:** Alarm Mask bits
000 = Seconds match
001 = Minutes match
010 = Hours match (logic takes into account 12-/24-hour operation)
011 = Day of week match
100 = Date match
101 = Reserved; do not use
110 = Reserved; do not use
111 = Seconds, Minutes, Hour, Day of Week, Date and Month

bit 3 **ALMxIF:** Alarm Interrupt Flag bit(1,2)
1 = Alarm match occurred (must be cleared in software)
0 = Alarm match did not occur

bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day bits
Contains a value from 1 to 7. The representation is user-defined.

Note 1: If a match condition still exists when this bit is cleared, it will be set again automatically.
2: The ALMxIF bit cannot be written to a 1 in software. Writing to the ALMxWKDAY register will always clear the ALMxIF bit.

REGISTER 5-12: ALMxDATE: ALARM0/1 DATE VALUE REGISTER (ADDRESSES 0x0E/0x15)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

REGISTER 5-13: ALMxMTH: ALARM0/1 MONTH VALUE REGISTER (ADDRESSES 0x0F/0x16)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month's Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

TABLE 5-6: SUMMARY OF REGISTERS ASSOCIATED WITH ALARMS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	22
ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	22
ALM0HOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	23
ALM0WKDAY	ALMPOL	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0	24
ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	24
ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	25
ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	22
ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	22
ALM1HOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	23
ALM1WKDAY	ALMPOL	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0	24
ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	24
ALM1MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	25
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	27

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by alarms.

5.5 Output Configurations

The MCP7941X features Square Wave Clock Output, Alarm Interrupt Output, and General Purpose Output modes. All of the output functions are multiplexed onto MFP according to Table 5-7.

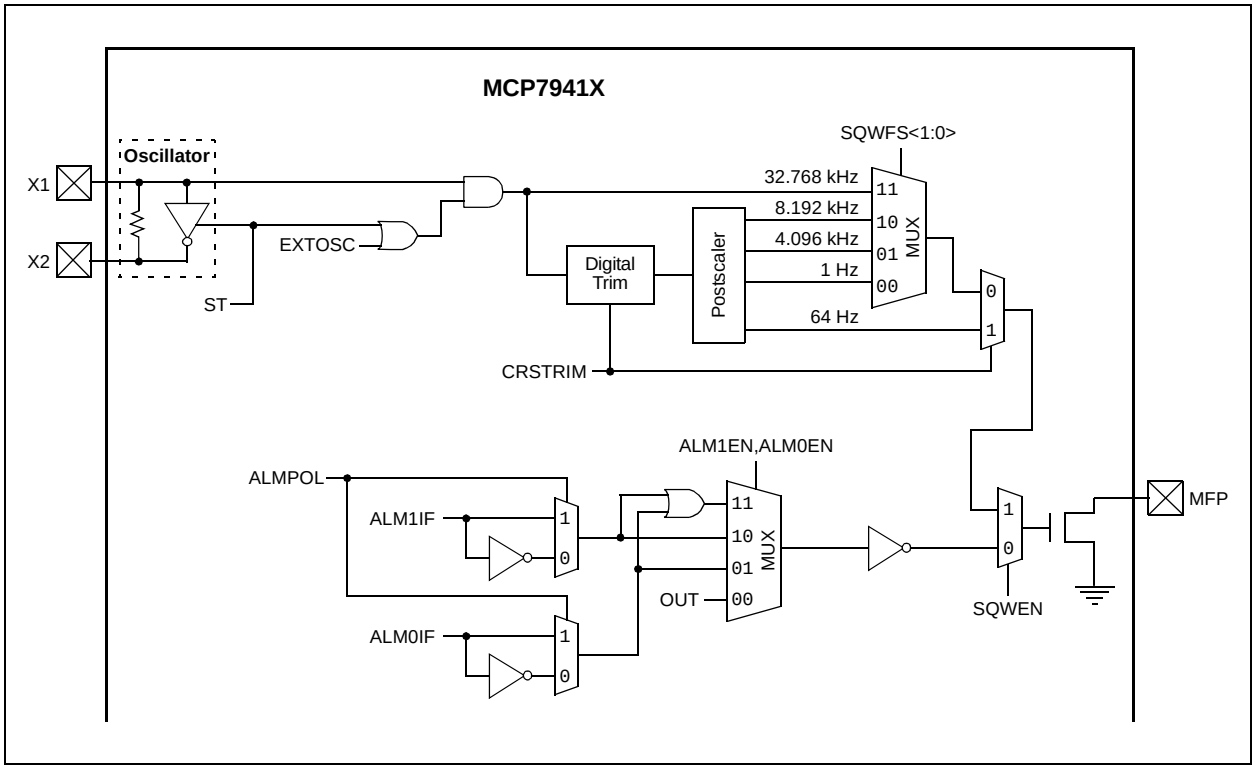
Only the alarm interrupt outputs are available while operating from the backup power supply. If none of the output functions are being used, the MFP can safely be left floating.

Note: The MFP is an open-drain output and requires a pull-up resistor to VCC (typically 10 kΩ).

TABLE 5-7: MFP OUTPUT MODES

SQWEN	ALM0EN	ALM1EN	Mode
0	0	0	General Purpose Output
0	1	0	Alarm Interrupt Output
0	0	1	
0	1	1	
1	x	x	Square Wave Clock Output

FIGURE 5-7: MFP OUTPUT BLOCK DIAGRAM



REGISTER 5-14: CONTROL: RTCC CONTROL REGISTER (ADDRESS 0x07)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **OUT:** Logic Level for General Purpose Output bit

Square Wave Clock Output mode (SQWEN = 1):
Unused.

Alarm Interrupt Output mode (ALM0EN = 1 or ALM1EN = 1):
Unused.

General Purpose Output mode (SQWEN = 0, ALM0EN = 0, and ALM1EN = 0):
1 = MFP signal level is logic high
0 = MFP signal level is logic low

bit 6 **SQWEN:** Square Wave Output Enable bit

1 = Enable Square Wave Clock Output mode
0 = Disable Square Wave Clock Output mode

bit 5 **ALM1EN:** Alarm 1 Module Enable bit

1 = Alarm 1 enabled
0 = Alarm 1 disabled

bit 4 **ALM0EN:** Alarm 0 Module Enable bit

1 = Alarm 0 enabled
0 = Alarm 0 disabled

bit 3 **EXTOSC:** External Oscillator Input bit

1 = Enable X1 pin to be driven by external 32.768 kHz source
0 = Disable external 32.768 kHz input

bit 2 **CRSTRIM:** Coarse Trim Mode Enable bit

Coarse Trim mode results in the MCP7941X applying digital trimming every 64 Hz clock cycle.
1 = Enable Coarse Trim mode. If SQWEN = 1, MFP will output trimmed 64 Hz(1) nominal clock signal.
0 = Disable Coarse Trim mode
See **Section 5.6 "Digital Trimming"** for details

bit 1-0 **SQWFS<1:0>:** Square Wave Clock Output Frequency Select bits

If SQWEN = 1 and CRSTRIM = 0:
Selects frequency of clock output on MFP
00 = 1 Hz(1)
01 = 4.096 kHz(1)
10 = 8.192 kHz(1)
11 = 32.768 kHz

If SQWEN = 0 or CRSTRIM = 1:
Unused.

Note 1: The 8.192 kHz, 4.096 kHz, 64 Hz, and 1 Hz square wave clock output frequencies are affected by digital trimming.

5.5.1 SQUARE WAVE OUTPUT MODE

The MCP7941X can be configured to generate a square wave clock signal on MFP. The input clock frequency, FOSC, is divided according to the SQWFS<1:0> bits as shown in Table 5-8.

The square wave output is not available when operating from the backup power supply.

Note:	All of the clock output rates are affected by digital trimming except for the 1:1 postscaler value (SQWFS<1:0> = 00).

TABLE 5-8: CLOCK OUTPUT RATES

SQWFS<1:0>	Postscaler	Nominal Frequency(1)
00	1:1	32.768 kHz
01	1:4	8.192 kHz
10	1:8	4.096 kHz
11	1:32,768	1 Hz

Note 1: Nominal frequency assumes FOSC is 32.768 kHz.

5.5.2 ALARM INTERRUPT OUTPUT MODE

The MFP will provide an interrupt output when enabled alarms match and the square wave clock output is disabled. This prevents the user from having to poll the alarm interrupt flag to check for a match.

The alarm interrupt output is available when operating from the backup power supply.

The ALMxIF flags control when the MFP is asserted, as described in the following sections.

5.5.2.1 Single Alarm Operation

When only one alarm module is enabled, the MFP output is based on the corresponding ALMxIF flag and the ALMPOL flag. If ALMPOL = 1, the MFP output reflects the value of the ALMxIF flag. If ALMPOL = 0, the MFP output reflects the inverse of the ALMxIF flag (Table 5-9).

TABLE 5-9: SINGLE ALARM OUTPUT TRUTH TABLE

ALMPOL	ALMxIF(1)	MFP
0	0	1
0	1	0
1	0	0
1	1	1

Note 1: ALMxIF refers to the interrupt flag corresponding to the alarm module that is enabled.

5.5.2.2 Dual Alarm Operation

When both alarm modules are enabled, the MFP output is determined by a combination of the ALM0IF, ALM1IF, and ALMPOL flags.

If ALMPOL = 1, the ALM0IF and ALM1IF flags are OR'd together and the result is output on MFP. If ALMPOL = 0, the ALM0IF and ALM1IF flags are AND'd together, and the result is inverted and output on MFP (Table 5-10). This provides the user with flexible options for combining alarms.

Note:	If ALMPOL = 0 and both alarms are enabled, the MFP will only assert when both ALM0IF and ALM1IF are set.

TABLE 5-10: DUAL ALARM OUTPUT TRUTH TABLE

ALMPOL	ALM0IF	ALM1IF	MFP
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

5.5.3 GENERAL PURPOSE OUTPUT MODE

If the square wave clock output and both alarm modules are disabled, the MFP acts as a general purpose output. The output logic level is controlled by the OUT bit.

The general purpose output is not available when operating from the backup power supply.

TABLE 5-11: SUMMARY OF REGISTERS ASSOCIATED WITH OUTPUT CONFIGURATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ALM0WKDAY	ALMPOL	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0	24
ALM1WKDAY	ALMPOL	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0	24
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	27

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in output configuration.

5.6 Digital Trimming

The MCP7941X features digital trimming to correct for inaccuracies of the external crystal or clock source, up to roughly ±129 ppm when CRSTRIM = 0. In addition to compensating for intrinsic inaccuracies in the clock, this feature can also be used to correct for error due to temperature variation. This can enable the user to achieve high levels of accuracy across a wide temperature operating range.

Digital trimming consists of the MCP7941X periodically adding or subtracting clock cycles, resulting in small adjustments in the internal timing. The adjustment occurs once per minute when CRSTRIM = 0. The SIGN bit specifies whether to add cycles or to subtract them. The TRIMVAL<6:0> bits are used to specify by how many clock cycles to adjust. Each step in the TRIMVAL<6:0> value equates to adding or subtracting two clock pulses to or from the 32.768 kHz clock signal. This results in a correction of roughly 1.017 ppm per step when CRSTRIM = 0. Setting TRIMVAL<6:0> to 0x00 disables digital trimming.

Digital trimming also occurs while operating off the backup supply.

REGISTER 5-15: OSCTRIM: OSCILLATOR DIGITAL TRIM REGISTER (ADDRESS 0x08)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SIGN	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **SIGN:** Trim Sign bit

1 = Add clocks to correct for slow time
0 = Subtract clocks to correct for fast time

bit 6-0 **TRIMVAL<6:0>:** Oscillator Trim Value bits

When CRSTRIM = 0:
1111111 = Add or subtract 254 clock cycles every minute
1111110 = Add or subtract 252 clock cycles every minute
•
•
•
0000010 = Add or subtract 4 clock cycles every minute
0000001 = Add or subtract 2 clock cycles every minute
0000000 = Disable digital trimming

When CRSTRIM = 1:
1111111 = Add or subtract 254 clock cycles 128 times per second
1111110 = Add or subtract 252 clock cycles 128 times per second
•
•
•
0000010 = Add or subtract 4 clock cycles 128 times per second
0000001 = Add or subtract 2 clock cycles 128 times per second
0000000 = Disable digital trimming

5.6.1 CALIBRATION

In order to perform calibration, the number of error clock pulses per minute must be found and the corresponding trim value must be loaded into TRIMVAL<6:0>.

There are two methods for determining the trim value. The first method involves measuring an output frequency directly and calculating the deviation from ideal. The second method involves observing the number of seconds gained or lost over a period of time.

Once the OSCTRIM register has been loaded, digital trimming will automatically occur every minute.

5.6.1.1 Calibration by Measuring Frequency

To calibrate the MCP7941X by measuring the output frequency, perform the following steps:

1. Enable the crystal oscillator or external clock input by setting the ST bit or EXTOSC bit, respectively.
2. Ensure TRIMVAL<6:0> is reset to 0x00.
3. Select an output frequency by setting SQWFS<1:0>.
4. Set SQWEN to enable the square wave output.
5. Measure the resulting output frequency using a calibrated measurement tool, such as a frequency counter.
6. Calculate the number of error clocks per minute (see Equation 5-2).

EQUATION 5-2: CALCULATING TRIM VALUE FROM MEASURED FREQUENCY

$$\text{TRIMVAL<6:0>} = \frac{(F_{IDEAL} - F_{MEAS}) \cdot \frac{32768}{F_{IDEAL}} \cdot 60}{2}$$

Where:

F_{IDEAL} = Ideal frequency based on SQWFS<1:0>
F_{MEAS} = Measured frequency

- If the number of error clocks per minute is negative, then the oscillator is *faster* than ideal and the SIGN bit must be cleared.
- If the number of error clocks per minute is positive, then the oscillator is *slower* than ideal and the SIGN bit must be set.

7. Load the correct value into TRIMVAL<6:0>.

Note:	Using a lower output frequency and/or averaging the measured frequency over a number of clock pulses will reduce the effects of jitter and improve accuracy.

5.6.1.2 Calibration by Observing Time Deviation

To calibrate the MCP7941X by observing the deviation over time, perform the following steps:

1. Ensure TRIMVAL<6:0> is reset to 0x00.
2. Load the timekeeping registers to synchronize the MCP7941X with a known-accurate reference time.
3. Enable the crystal oscillator or external clock input by setting the ST bit or EXTOSC bit, respectively.
4. Observe how many seconds are gained or lost over a period of time (larger time periods offer more accuracy).
5. Calculate the PPM deviation (see Equation 5-3).

EQUATION 5-3: CALCULATING ERROR PPM

$$PPM = \frac{SecDeviation}{ExpectedSec} \cdot 1000000$$

Where:

$ExpectedSec$ = Number of seconds in chosen period
$SecDeviation$ = Number of seconds gained or lost

- If the MCP7941X has gained time relative to the reference clock, then the oscillator is *faster* than ideal and the SIGN bit must be cleared.
- If the MCP7941X has lost time relative to the reference clock, then the oscillator is *slower* than ideal and the SIGN bit must be set.

6. Calculate the trim value (see Equation 5-4).

EQUATION 5-4: CALCULATING TRIM VALUE FROM ERROR PPM

$$\text{TRIMVAL<6:0>} = \frac{PPM \cdot 32768 \cdot 60}{1000000 \cdot 2}$$

7. Load the correct value into TRIMVAL<6:0>.

Note 1:	Choosing a longer time period for observing deviation will improve accuracy.
2:	Large temperature variations during the observation period can skew results.

5.6.2 COARSE TRIM MODE

When CRSTRIM = 1, Coarse Trim mode is enabled. While in this mode, the MCP7941X will apply trimming at a rate of 128 Hz. If SQWEN is set, the MFP will output a trimmed 64 Hz nominal clock signal.

Because trimming is applied at a rate of 128 Hz rather than once every minute, each step of the TRIMVAL<6:0> value has a significantly larger effect on the resulting time deviation and output clock frequency.

By monitoring the MFP output frequency while in this mode, the user can easily observe the TRIMVAL<6:0> value affecting the clock timing.

Note 1: The 64 Hz Coarse Trim mode square wave output is not available while operating from the backup power supply.

2: With Coarse Trim mode enabled, the TRIMVAL<6:0> value has a drastic effect on timing. Leaving the mode enabled during normal operation will likely result in inaccurate time.

TABLE 5-12: SUMMARY OF REGISTERS ASSOCIATED WITH DIGITAL TRIMMING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	27
OSCTRIM	SIGN	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0	30

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by digital trimming.

5.7 Battery Backup

The MCP7941X features a backup power supply input (V_{BAT}) that can be used to provide power to the timekeeping circuitry, RTCC registers, and SRAM while primary power is unavailable. The MCP7941X will automatically switch to backup power when V_{CC} falls below V_{TRIP}, and back to V_{CC} when it is above V_{TRIP}.

The VBATEN bit must be set to enable the V_{BAT} input.

The following functionality is maintained while operating on backup power:

- Timekeeping
- Alarms
- Alarm Output
- Digital Trimming
- RTCC Register and SRAM Contents

The following features are not available while operating on backup power:

- I^2C Communication
- Square Wave Clock Output
- General Purpose Output

5.7.1 POWER-FAIL TIME-STAMP

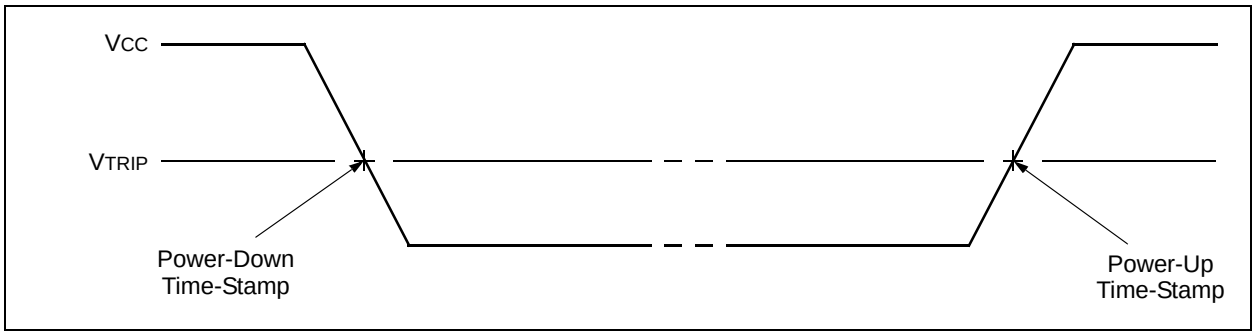
The MCP7941X includes a power-fail time-stamp module that stores the minutes, hours, date, and month when primary power is lost and when it is restored (Figure 5-8). The PWRFAIL bit is also set to indicate that a power failure occurred.

Note:	Throughout this section, references to the register and bit names for the Power-Fail Time-Stamp module are referred to generically by the use of 'x' in place of the specific module name. Thus, "PWRxxMIN" might refer to the minutes register for Power-Down or Power-Up.

To utilize the power-fail time-stamp feature, a backup power supply must be available with the V_{BAT} input enabled, and the oscillator should also be running to ensure accurate functionality.

Note 1:	The PWRFAIL bit must be cleared to log new time-stamp data. This is to ensure previous time-stamp data is not lost.
2:	Clearing the PWRFAIL bit will clear all time-stamp registers.

FIGURE 5-8: POWER-FAIL TIME-STAMP TIMING



REGISTER 5-16: PWRxxMIN: POWER-DOWN/POWER-UP TIME-STAMP MINUTES VALUE REGISTER (ADDRESSES 0x18/0x1C)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute's Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute's Ones Digit
Contains a value from 0 to 9

REGISTER 5-17: PWRxxHOUR: POWER-DOWN/POWER-UP TIME-STAMP HOURS VALUE REGISTER (ADDRESSES 0x19/0x1D)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

REGISTER 5-18: PWRxxDATE: POWER-DOWN/POWER-UP TIME-STAMP DATE VALUE REGISTER (ADDRESSES 0x1A/0x1E)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

REGISTER 5-19: PWRxxMTH: POWER-DOWN/POWER-UP TIME-STAMP MONTH VALUE REGISTER (ADDRESSES 0x1B/0x1F)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-5 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day bits
Contains a value from 1 to 7. The representation is user-defined.

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

TABLE 5-13: SUMMARY OF REGISTERS ASSOCIATED WITH BATTERY BACKUP

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	19
PWRDNMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	34
PWRDNHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	34
PWRDNDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	35
PWRDNMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	35
PWRUPMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	34
PWRUPHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	34
PWRUPDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	35
PWRUPMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	35

Legend: — = unimplemented location, read as '0'. Shaded cells are not used with battery backup.

6.0 ON-BOARD MEMORY

The MCP7941X has 1 Kbits (128 bytes) of EEPROM, eight bytes of protected EEPROM for storing crucial information, and 64 bytes of SRAM for general purpose usage. The SRAM is retained when the primary power supply is removed if a backup supply is present and enabled. Since the EEPROM is nonvolatile, it does not require a supply for data retention.

Although the SRAM is a separate block from the RTCC registers, they are accessed using the same control byte, '1101111X'. The EEPROM is in a different address space and requires the use of a different control byte, '1010111X'. RTCC and SRAM can be accessed for reads or writes immediately after starting an EEPROM write cycle.

6.1 SRAM/RTCC Registers

The RTCC registers are located at addresses 0x00 to 0x1F, and the SRAM is located at addresses 0x20 to 0x5F. The SRAM can be accessed while the RTCC registers are being internally updated. The SRAM is not initialized by a Power-On Reset (POR).

Neither the RTCC registers nor the SRAM can be accessed when the device is operating off the backup power supply.

6.1.1 SRAM/RTCC REGISTER BYTE WRITE

Following the Start condition from the master, the control code and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the address and will be written into the Address Pointer of the MCP7941X. After receiving another Acknowledge bit from the MCP7941X, the master device transmits the data byte to be written into the addressed memory location. The MCP7941X stores the data byte into memory and acknowledges again, and the master generates a Stop condition (Figure 6-1).

If an attempt is made to write to an address past 0x5F, the MCP7941X will not acknowledge the address or data bytes, and no data will be written. After a byte Write command, the internal Address Pointer will point to the address location following the one that was just written.

6.1.2 SRAM/RTCC REGISTER SEQUENTIAL WRITE

The write control byte, address, and the first data byte are transmitted to the MCP7941X in the same way as in a byte write. But instead of generating a Stop condition, the master transmits additional data bytes. Upon receipt of each byte, the MCP7941X responds with an Acknowledge, during which the data is latched into memory and the Address Pointer is internally incremented by one. As with the byte write operation, the master ends the command by generating a Stop condition (Figure 6-2).

There is no limit to the number of bytes that can be written in a single command. However, because the RTCC registers and SRAM are separate blocks, writing past the end of each block will cause the Address Pointer to roll over to the beginning of the same block. Specifically, the Address Pointer will roll over from 0x1F to 0x00, and from 0x5F to 0x20.

FIGURE 6-1: SRAM/RTCC BYTE WRITE

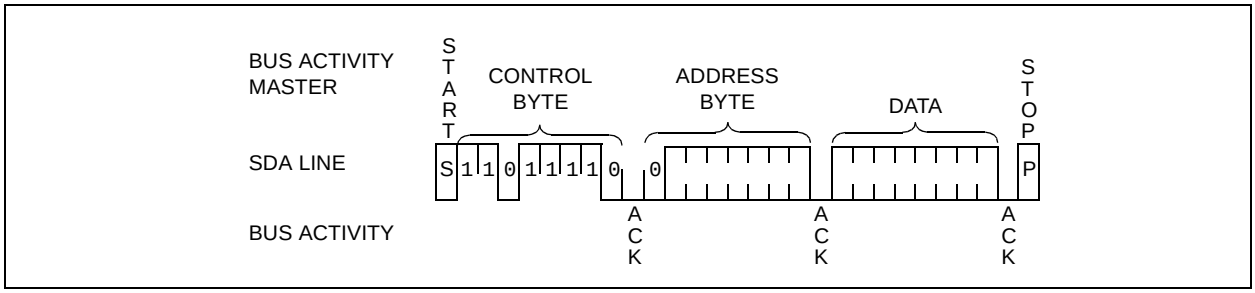
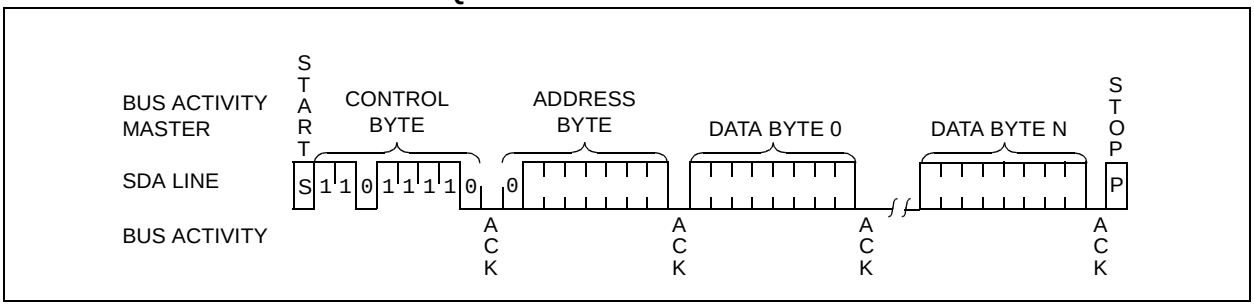


FIGURE 6-2: SRAM/RTCC SEQUENTIAL WRITE



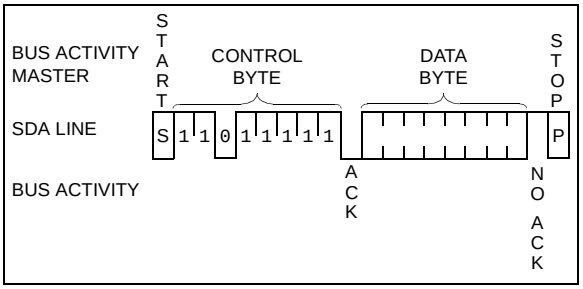
6.1.3 SRAM/RTCC REGISTER CURRENT ADDRESS READ

The MCP7941X contains an address counter that maintains the address of the last byte accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the MCP7941X issues an Acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the MCP7941X discontinues transmission (Figure 6-3).

Note:	The Address Pointer is shared between the SRAM/RTCC registers and the EEPROM.

FIGURE 6-3: SRAM/RTCC CURRENT ADDRESS READ



6.1.4 SRAM/RTCC REGISTER RANDOM READ

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the address must be set. This is done by sending the address to the MCP7941X as part of a write operation (R/$\overline{W}$ bit set to '0'). After the address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the control byte again but with the R/$\overline{W}$ bit set to a '1'. The MCP7941X will then issue an Acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but it does generate a Stop condition which causes the MCP7941X to discontinue transmission (Figure 6-4). After a random Read command, the internal address counter will point to the address location following the one that was just read.

6.1.5 SRAM/RTCC REGISTER SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the MCP7941X transmits the first data byte, the master issues an Acknowledge as opposed to the Stop condition used in a random read. This Acknowledge directs the MCP7941X to transmit the next sequentially addressed 8-bit word (Figure 6-5). Following the final byte transmitted to the master, the master will NOT generate an Acknowledge but will generate a Stop condition. To provide sequential reads, the MCP7941X contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory block to be serially read during one operation.

Because the RTCC registers and SRAM are separate blocks, reading past the end of each block will cause the Address Pointer to roll over to the beginning of the same block. Specifically, the Address Pointer will roll over from 0x1F to 0x00, and from 0x5F to 0x20.

FIGURE 6-4: SRAM/RTCC RANDOM READ

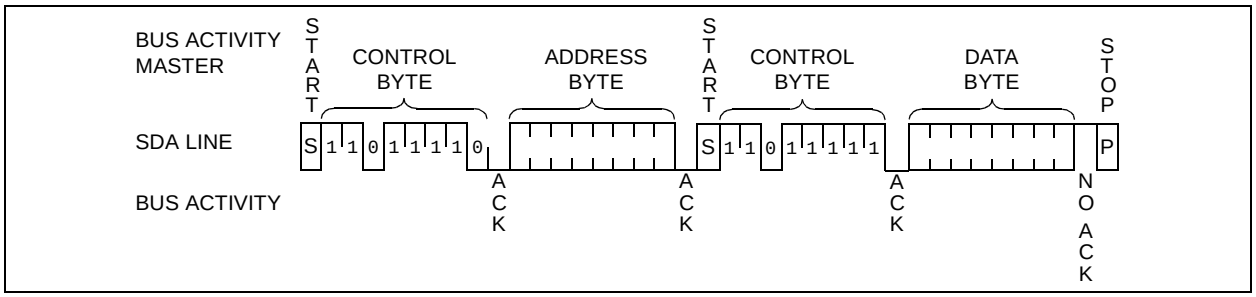
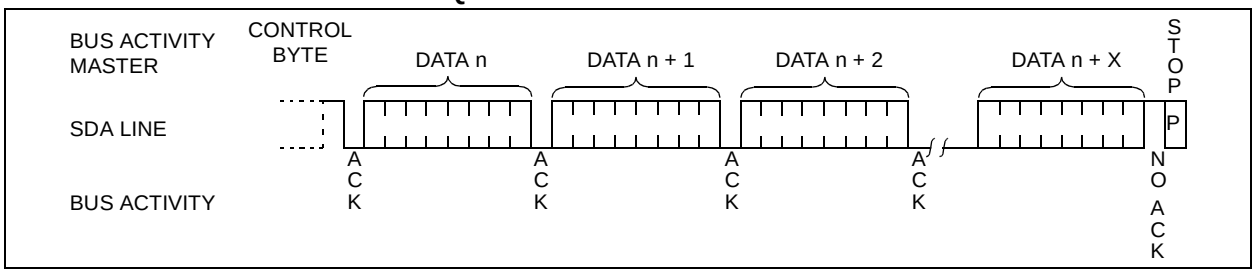


FIGURE 6-5: SRAM/RTCC SEQUENTIAL READ



6.2 EEPROM

The MCP7941X features 1 Kbits of EEPROM organized in 8-byte pages with software write protection configured through the STATUS register.

6.2.1 STATUS REGISTER

The STATUS register contains bits BP<1:0> which are used to set the block write protection for the EEPROM array.

The STATUS register is a nonvolatile Control register in the EEPROM address space at location 0xFF. The STATUS register is accessed using control byte '1010111X'. Setting the BP<1:0> bits in the STATUS register determines which regions are protected in the EEPROM array per Table 6-1.

If multiple bytes are loaded to the STATUS register, only the last byte is written. The write to the STATUS register is initiated by the I^2C Stop condition.

TABLE 6-1: BLOCK PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	None
0	1	Upper 1/4 (60h-7Fh)
1	0	Upper 1/2 (40h-7Fh)
1	1	All (00h-7Fh)

REGISTER 6-1: STATUS: EEPROM BLOCK PROTECTION CONTROL REGISTER (ADDRESS 0xFF)

U	U	U	U	R/W-0	R/W-0	U	U
—	—	—	—	BP1	BP0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	X = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **BP<1:0>:** EEPROM Array Block Protection bits

bit 1-0 **Unimplemented:** Read as '0'

6.2.2 EEPROM BYTE WRITE

Following the Start condition from the master, the control code and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the address and will be written into the Address Pointer of the MCP7941X. After receiving another Acknowledge bit from the MCP7941X, the master device transmits the data byte to be written into the addressed memory location. The MCP7941X acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and, during this time, the MCP7941X does not generate Acknowledge signals for EEPROM commands. Access to the RTCC registers and SRAM is still possible during an EEPROM write cycle.

If an attempt is made to write to an address outside of the defined regions, the MCP7941X will not acknowledge the address or data bytes, no data will be written, and the device will immediately accept a new command. After a Byte Write command, the internal Address Pointer will point to the address location following the one that was just written.

6.2.3 EEPROM SEQUENTIAL WRITE

The write control byte, word address, and the first data byte are transmitted to the MCP7941X in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to seven additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a Stop condition. After receipt of each word, the three lower Address Pointer bits are internally incremented by one. If the master should transmit more than eight bytes prior to generating the Stop condition, the address counter will roll over and the data received previously will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-7).

FIGURE 6-6: EEPROM BYTE WRITE

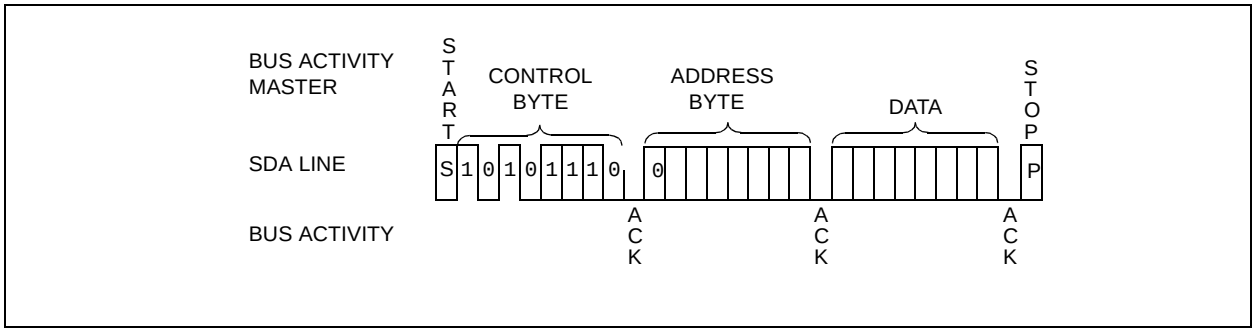
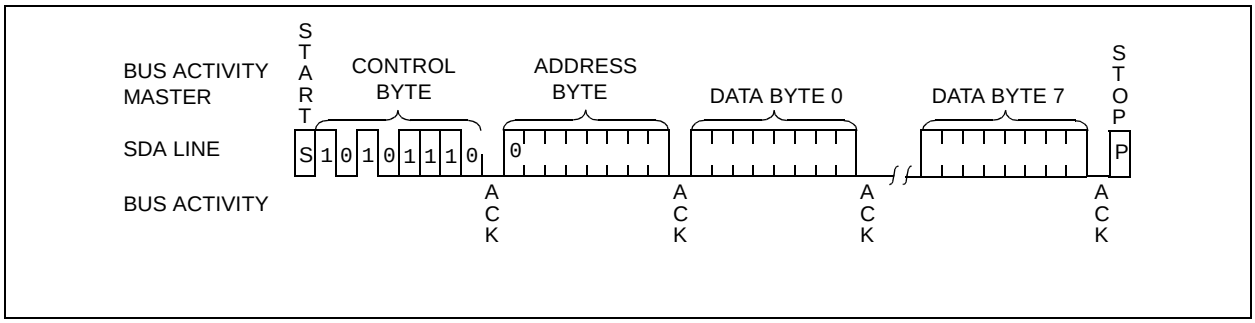


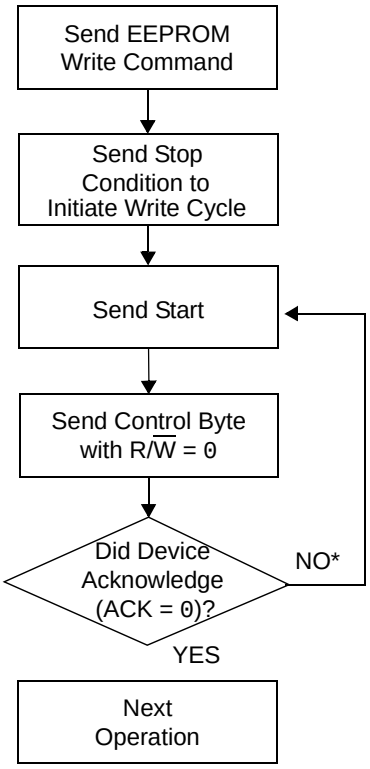
FIGURE 6-7: EEPROM PAGE WRITE



6.2.4 ACKNOWLEDGE POLLING

Since the device will not acknowledge an EEPROM control byte during an internal EEPROM write cycle, this can be used to determine when the cycle is complete. This feature can be used to maximize bus throughput. Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next Read or Write command. See Figure 6-8 for the flow diagram.

FIGURE 6-8: ACKNOWLEDGE POLLING FLOW



Note*: For added system robustness, implement time-out checking to avoid a potential infinite loop.

Note: For added systems robustness, it is recommended that time-out functionality be implemented in the acknowledge polling routine to avoid potentially hanging the system by entering an infinite loop. This can easily be done by designing in a maximum number of loops the routine will execute, or through the use of a hardware timer.

If a time out occurs, polling should be aborted by sending a Stop condition. A user-generated error-handling routine can then be called, allowing the system to recover in a manner appropriate for the application.

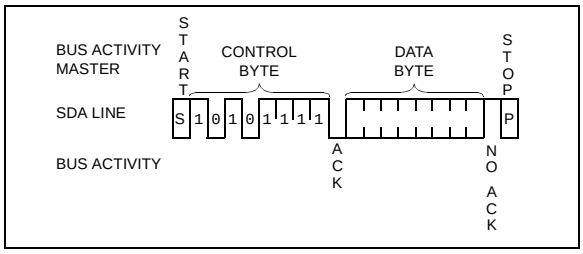
6.2.5 EEPROM CURRENT ADDRESS READ

The MCP7941X contains an address counter that maintains the address of the last byte accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the MCP7941X issues an Acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition, and the MCP7941X discontinues transmission (Figure 6-9).

Note:	The Address Pointer is shared between the SRAM/RTCC registers and the EEPROM.

FIGURE 6-9: EEPROM CURRENT ADDRESS READ



6.2.6 EEPROM RANDOM READ

Random read operations allow the master to access any EEPROM location in a random manner. To perform this type of read operation, first the address must be set. This is done by sending the address to the MCP7941X as part of a write operation (R/$\overline{W}$ bit set to '0'). After the address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the control byte again but with the R/$\overline{W}$ bit set to a '1'. The MCP7941X will then issue an Acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but it does generate a Stop condition which causes the MCP7941X to discontinue transmission (Figure 6-10). After a random Read command, the internal address counter will point to the address location following the one that was just read.

6.2.7 EEPROM SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the MCP7941X transmits the first data byte, the master issues an Acknowledge as opposed to the Stop condition used in a random read. This Acknowledge directs the MCP7941X to transmit the next sequentially addressed 8-bit word (Figure 6-11). Following the final byte transmitted to the master, the master will NOT generate an Acknowledge but will generate a Stop condition. To provide sequential reads, the MCP7941X contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire EEPROM block to be serially read during one operation. The internal Address pointer will automatically roll over from address 0x7F to address 0x00 if the master acknowledges the byte received from address 0x7F.

FIGURE 6-10: EEPROM RANDOM READ

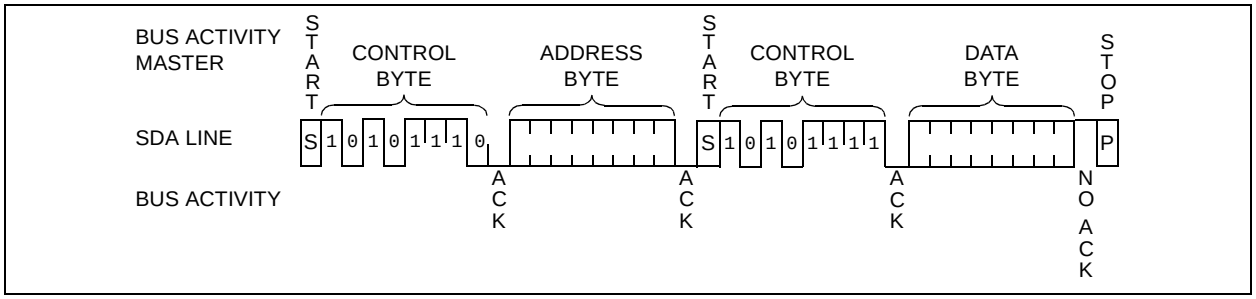
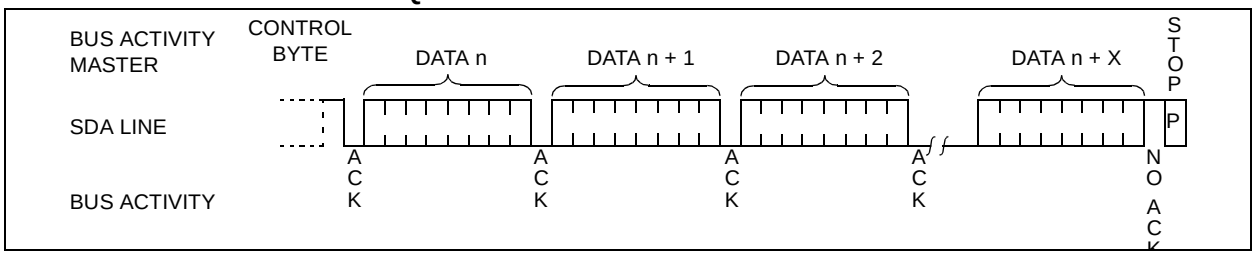


FIGURE 6-11: EEPROM SEQUENTIAL READ



6.3 Protected EEPROM

The MCP7941X features a 64-bit protected EEPROM block that requires a special unlock sequence to be followed in order to write to the memory. Note that reading from the memory does not require the unlock sequence to be performed. The protected EEPROM can be used for storing crucial information such as a unique serial number. The MCP79411 and MCP79412 include an EUI-48 and EUI-64 node address, respectively, pre-programmed into the protected EEPROM block. Custom programming is also available.

The protected EEPROM block is located at addresses 0xF0 to 0xF7 and is accessed using the '1010111X' control byte.

Note:	Attempts to access invalid addresses (Figure 5-1) will result in the MCP7941X not acknowledging the address.

6.3.1 PROTECTED EEPROM UNLOCK SEQUENCE

The protected EEPROM block requires a special unlock sequence to prevent unintended writes, utilizing the EEUNLOCK register. The EEUNLOCK register is not a physical register; it is used exclusively in the EEPROM write sequence. Reading from EEUNLOCK will read all 0's.

To unlock the block, the following sequence must be followed:

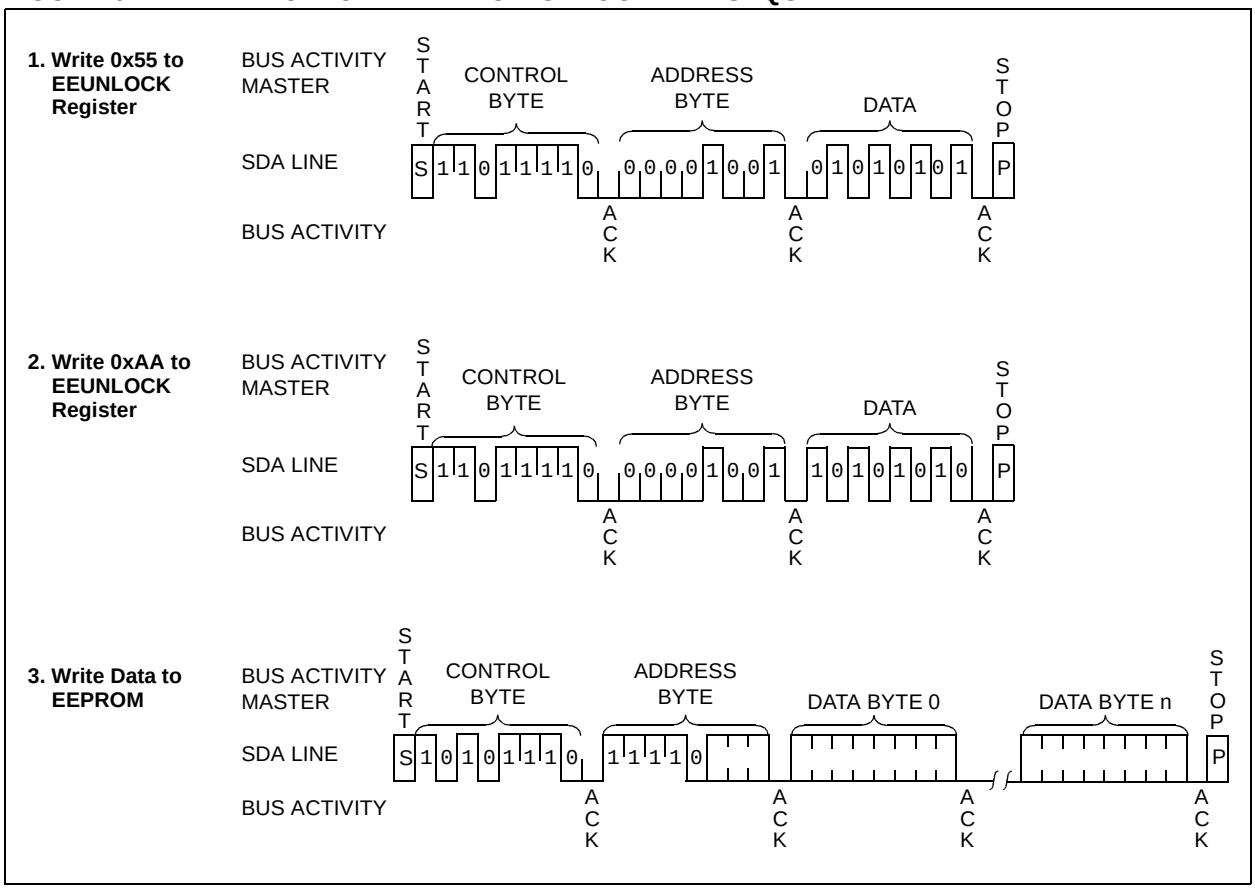
1. Write 0x55 to the EEUNLOCK register
2. Write 0xAA to the EEUNLOCK register
3. Write the desired data bytes to the EEPROM

Figure 6-12 illustrates the sequence.

Note 1:	Diverging from any step of the unlock sequence may result in the EEPROM remaining locked and the write operation being ignored.
2:	Unlocking the EEPROM is not required in order to read from the memory.

The entire EEPROM block does not have to be written in a single operation. However, the block is locked after each write operation and must be unlocked again to start a new Write command.

FIGURE 6-12: PROTECTED EEPROM UNLOCK AND SEQUENTIAL WRITE



6.4 Pre-Programmed EUI-48™ or EUI-64™ Node Address

The MCP79411 and MCP79412 are programmed at the factory with a globally unique node address stored in the protected EEPROM block.

6.4.1 EUI-48™ NODE ADDRESS (MCP79411)

The 6-byte EUI-48™ node address value of the MCP79411 is stored in EEPROM locations 0xF2 through 0xF7, as shown in Figure 6-13. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining three bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 48-bit value.

Note:	Currently, Microchip's OUIs are 0x0004A3, 0x001EC0 and 0xD88039, though this will change as addresses are exhausted.

6.4.1.1 Eui-64™ Support Using The MCP79411

The pre-programmed EUI-48 node address of the MCP79411 can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFE between the OUI and the Extension Identifier, as shown below.

Note:	As an alternative, the MCP79412 features an EUI-64 node address that can be used in EUI-64 applications directly without the need for encapsulation, thereby simplifying system software. See **Section 6.4.2 "Eui-64™ Node Address (MCP79412)"** for details.

6.4.2 EUI-64™ NODE ADDRESS (MCP79412)

The 8-byte EUI-64™ node address value of the MCP79412 is stored in array locations 0xF0 through 0xF7, as shown in Figure 6-14. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining five bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 64-bit value

Note:	Currently, Microchip's OUIs are 0x0004A3, 0x001EC0 and 0xD88039, though this will change as addresses are exhausted.

.

Note:	In conformance with IEEE guidelines, Microchip will not use the values 0xFFFE and 0xFFFF for the first two bytes of the EUI-64 Extension Identifier. These two values are specifically reserved to allow applications to encapsulate EUI-48 addresses into EUI-64 addresses.

FIGURE 6-13: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (MCP79411)

Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	00h	04h	A3h	12h	34h	56h
Array Address	F2h					F7h

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

Corresponding EUI-64™ Node Address After Encapsulation: 00-04-A3-FF-FE-12-34-56

FIGURE 6-14: EUI-64 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (MCP79412)

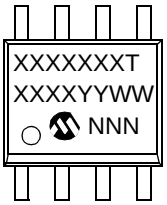
Description	24-bit Organizationally Unique Identifier			40-bit Extension Identifier				
Data	00h	04h	A3h	12h	34h	56h	78h	90h
Array Address	F0h							F7h

Corresponding EUI-64™ Node Address: 00-04-A3-12-34-56-78-90

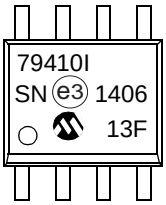
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

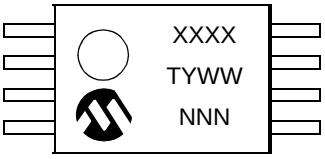
8-Lead SOIC (3.90 mm)



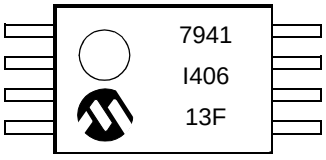
Example:



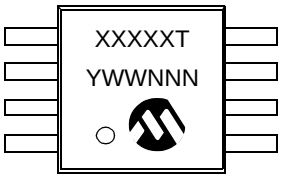
8-Lead TSSOP



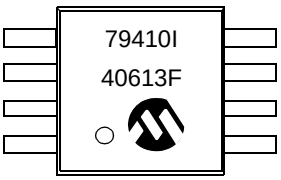
Example:



8-Lead MSOP

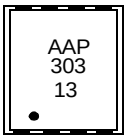


Example:



8-Lead 2x3 TDFN

Example:



Part Number	1st Line Marking Codes			
	SOIC	TSSOP	MSOP	TDFN
MCP79410	79410T	7941	79410T	AAP
MCP79411	79411T	9411	79411T	AAQ
MCP79412	79412T	9412	79412T	AAR

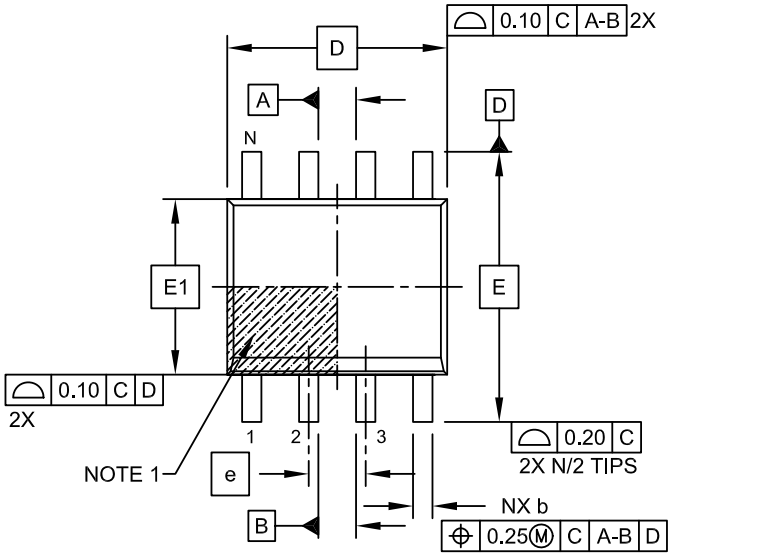
T = Temperature grade

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

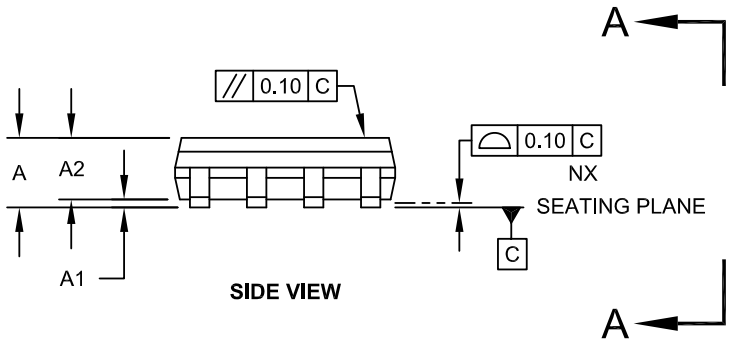
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

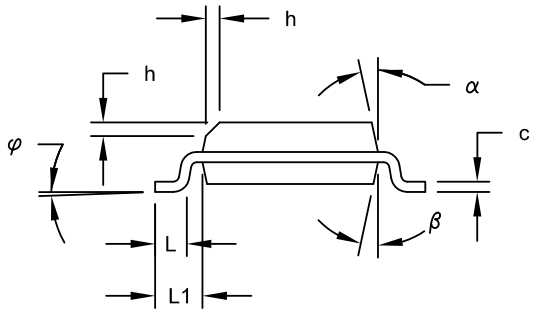
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

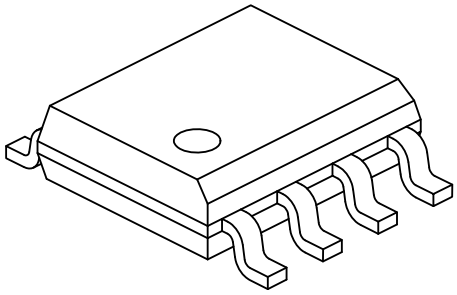


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

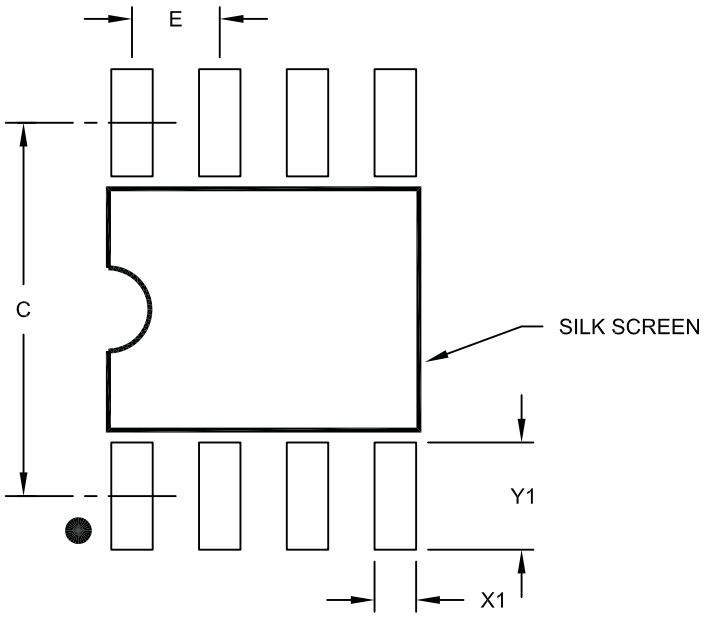
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

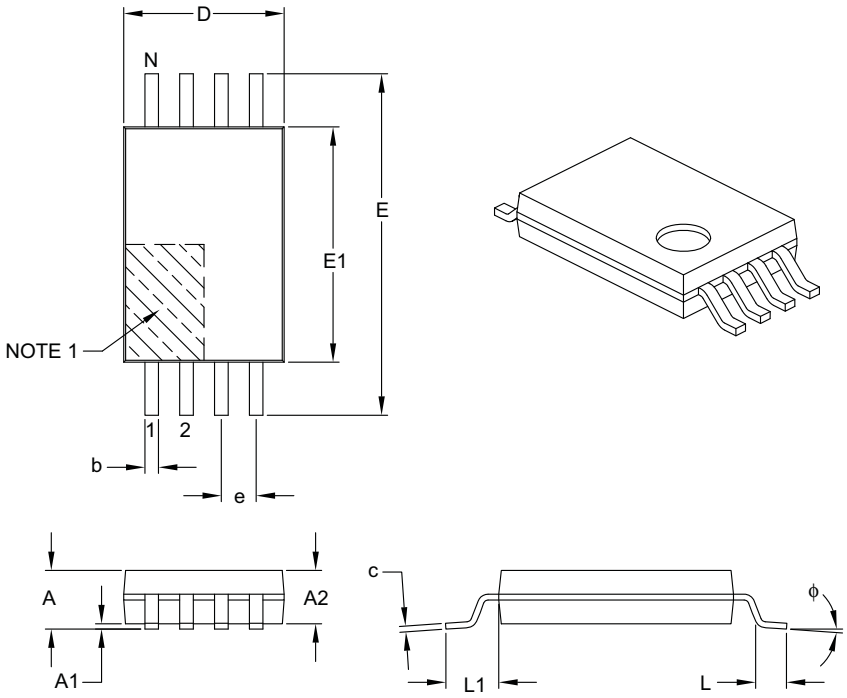
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

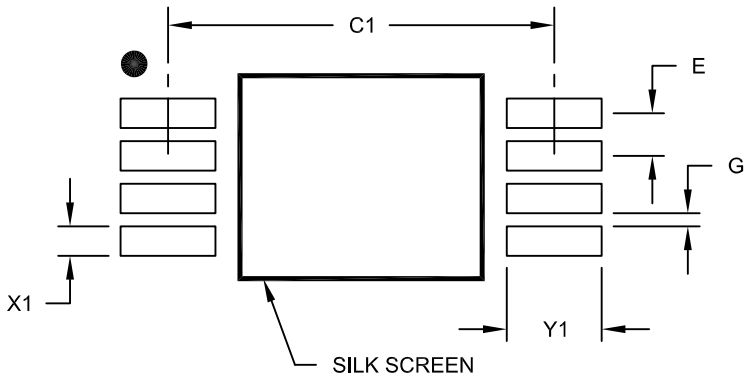
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

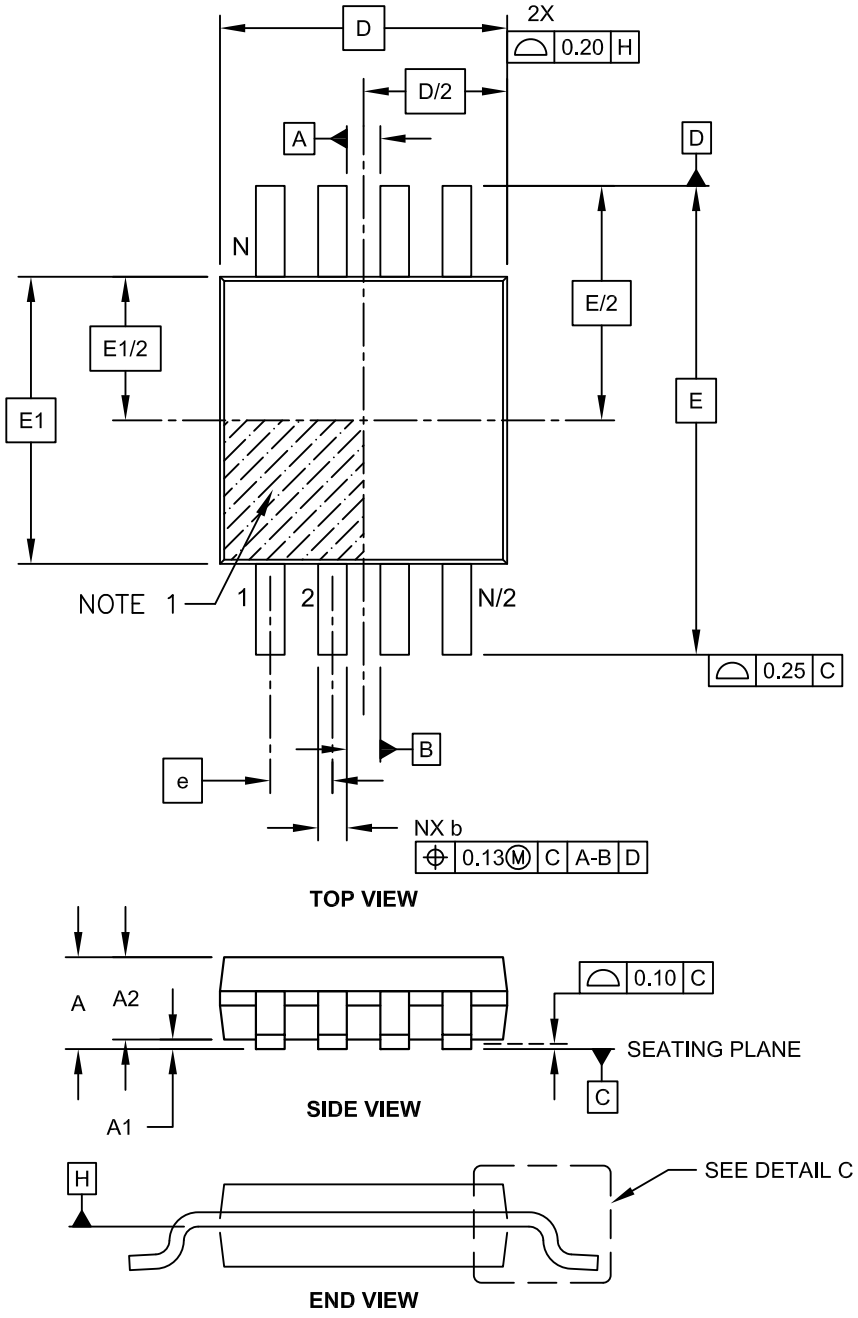
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

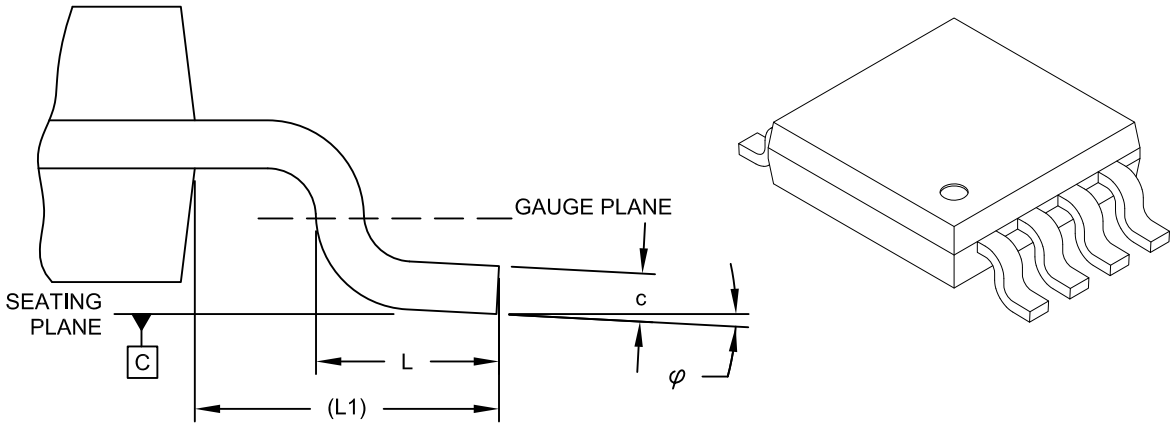
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

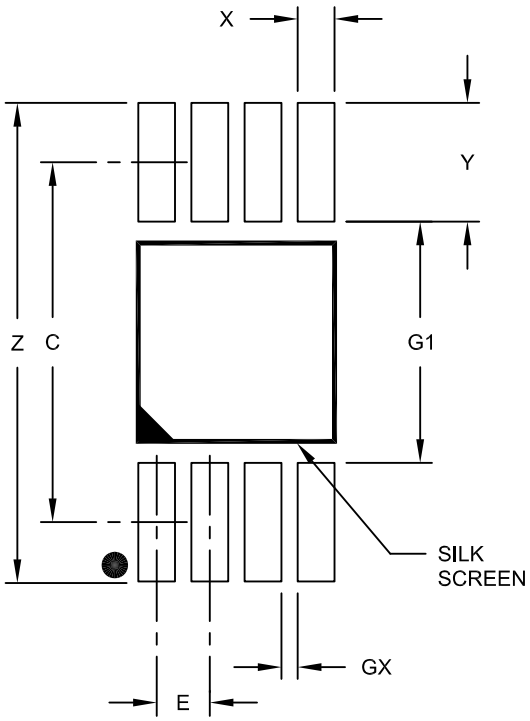
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

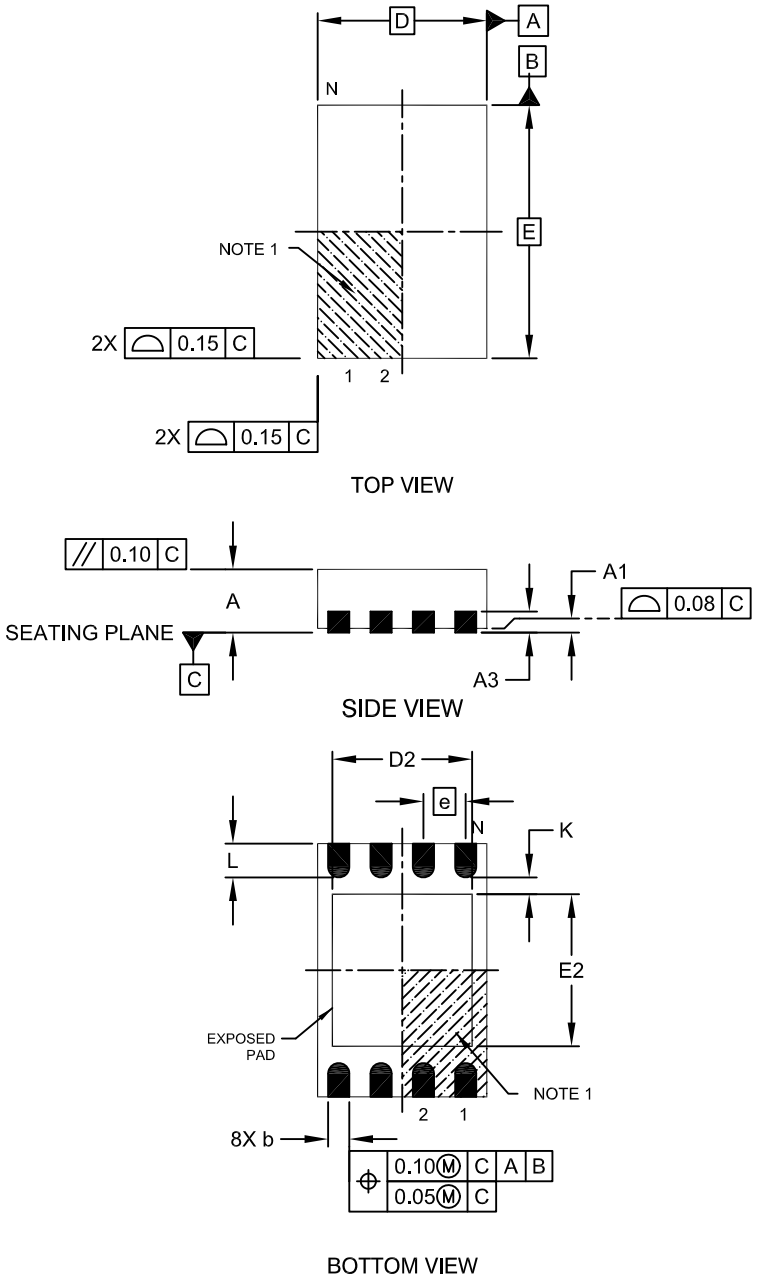
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

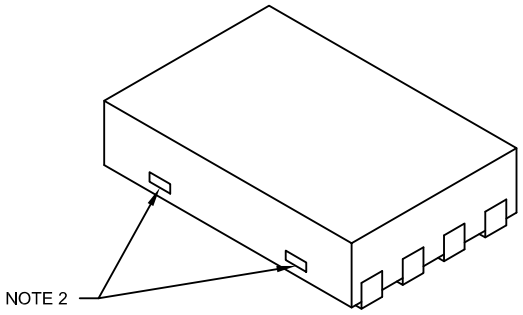
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-129C

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

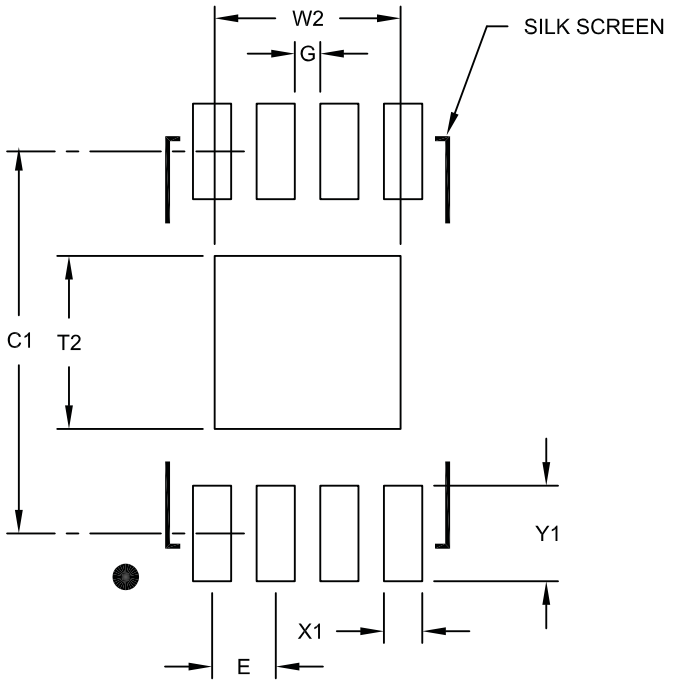
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

APPENDIX A: REVISION HISTORY

Revision A (10/2010)

- Original release of this document.

Revision B (03/2011)

- Minor typographical edits
- Added Appendix B: Device Errata.

Revision C (07/2011)

- Updated Section 4.2.6 “Crystal Specs”
- Revised Figure 4-4.

Revision D (12/2011)

- Added DC/AC Char. Charts.

Revision E (04/2013)

- Revised Features page
- Revised Schematic, Block Diagram
- Added detailed descriptions for Registers
- Minor updates to the overall content.

Revision F (03/2014)

- Updated overall content for improved clarity
- Added detailed descriptions of registers
- Updated block diagram and application schematic.
- Defined names for all bits and registers, and renamed the bits shown in Table 7-1 for clarification.
- Renamed the DC characteristics shown in Table 7-2 for clarification.

TABLE 7-1: BIT NAME CHANGES

Old Bit Name	New Bit Name
OSCON	OSCRUN
VBAT	PWRFAIL
LP	LPYR
SQWE	SQWEN
ALM0	ALM0EN
ALM1	ALM1EN
RS0	SQWFS0
RS1	SQWFS1
RS2	CRSTRIM
CALIBRATION	TRIMVAL<6:0>
ALM0POL	ALMPOL
ALM1POL	ALMPOL
ALM0C<2:0>	ALM0MSK<2:0>
ALM1C<2:0>	ALM1MSK<2:0>

TABLE 7-2: DC CHARACTERISTIC NAME CHANGES

Old Name	Old Symbol	New Name	New Symbol
Operating Current EEPROM	ICC Read	EEPROM Operating Current	ICCEERD
	ICC Write		ICCEEWR
Operating Current SRAM	ICC Read	SRAM/RTCC Register Operating Current	ICCREAD
	ICC Write		ICCWRITE
Operating Current	IVCC	Timekeeping Current	ICCT
	IBAT	Timekeeping Backup Current	IBATT
Standby Current	ICCS	VCC Data Retention Current (oscillator off)	ICCDAT

Revision G (01/2015)

- Updated Section 6.4
- Updated Product Identification System.

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NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office. Not every possible ordering combination is listed below.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	MCP79410 =	1.8V - 5.5V I²C™ Serial RTCC
	MCP79410T =	1.8V - 5.5V I²C Serial RTCC (Tape and Reel)
	MCP79411 =	1.8V - 5.5V I²C Serial RTCC, EUI-48™
	MCP79411T =	1.8V - 5.5V I²C Serial RTCC, EUI-48™ (Tape and Reel)
	MCP79412 =	1.8V - 5.5V I²C Serial RTCC, EUI-64™
	MCP79412T =	1.8V - 5.5V I²C Serial RTCC, EUI-64™ (Tape and Reel)
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	T=	Tape and Reel(1)
Temperature Range:	I =	-40°C to +85°C
Package:	SN =	8-Lead Plastic Small Outline (3.90 mm body)
	ST =	8-Lead Plastic Thin Shrink Small Outline (4.4 mm)
	MS =	8-Lead Plastic Micro Small Outline
	MNY(2) =	8-Lead Plastic Dual Flat, No Lead

Examples:

a) MCP79410-I/SN: Industrial Temperature, SOIC package.

b) MCP79410T-I/SN: Industrial Temperature, SOIC package, Tape and Reel.

c) MCP79410T-I/MNY: Industrial Temperature, TDFN package, Tape and Reel.

d) MCP79411-I/SN: Industrial Temperature, SOIC package, EUI-48™.

e) MCP79411-I/MS: Industrial Temperature MSOP package, EUI-48™.

f) MCP79412-I/SN: Industrial Temperature, SOIC package, EUI-64™.

g) MCP79412-I/ST: Industrial Temperature, TSSOP package, EUI-64™.

h) MCP79412T-I/ST: Industrial Temperature, TSSOP package, Tape and Reel, EUI-64™.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

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