TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF TABLES

LIST OF FIGURES

Absolute Maximum Ratings

BYP to PG_ .....-0.3V to +22V
DC_ to BYP .....-6V to +0.3V
I2CIN, V_{ICHG}, IRQB, SDA, SCL to GND .....-0.3V to +6V
BST to AVL .....-0.3V to +16V
BST to LX_ .....-0.3V to +6V
PVL, SFO, BAT, CS to PG_ .....-0.3V to +6V
AVL, THM to GND .....-0.3V to +6V
PG_ to GND .....-0.3V to +0.3V
DC_, LX_, CS, BAT, BYP Continuous Current .....1.6A_{RMS}

Continuous Power Dissipation (T_A = +70°C)
WLP derate 21.7mW/°C above +70°C 1736mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

*This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (q_{JA}) .....46°C/W
Junction-to-Case Thermal Resistance (q_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DC} = 5V, C_{BYP} = 1µF, I_{FCHG} = 500mA, C_{AVL} = 4.7µF, V_{THM} = AVL/2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC INPUT						
DC Operating Voltage Range			4.0		V_{OVP}	V
DC Undervoltage Lockout (V_{UVLO})	DC rising, 500mV hysteresis		3.6	3.8	4.0	V
DC Overvoltage Threshold (V_{OVP})*	DC rising, 250mV hysteresis		7.25	7.5	7.75	V
DC OVP Interrupt Delay				16		ms
DC to BAT Shutdown Threshold	When charging stops, V_{DC} falling, 150mV hysteresis		0	50	100	mV
DC Supply Current	Charger enabled, V_{DC} = 5.5V			2		mA
BST Leakage Current	V_{BST} = 5.5V, LX_ = PG_	T_A = +25°C		0.01	10	µA
		T_A = -40°C to +85°C		0.1		
LX_ Leakage Current	$V_{LX\_}$ = 0 or 5.5V	T_A = +25°C		0.01	10	
		T_A = -40°C to +85°C		0.1		
BAT Reverse Leakage Current	V_{DC} = 0V, V_{BAT} = 4.2V			1	5	µA
Input-Current Limit Range			0.1		1.5	A

Electrical Characteristics (continued)

(V_{DC} = 5V, C_{BYP} = 1µF, I_{FCHG} = 500mA, C_{AVL} = 4.7µF, V_{THM} = AVL/2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Current Limit Accuracy	DCILMT[5:0] = 0b000000 (100mA)	90	95	100	mA
	DCILMT[5:0] = 0b010100 (500mA)	450	475	500	
	DCILMT[5:0] = 0b111100 (1500mA)	1350	1500	1650	
Adaptive Input-Current Limit (AICL) (Note 4)	DC voltage where charge current is regulated		4.5		V
	DC voltage where charge current is set to 75mA		4.4		
Input Limit Switch	V_{DC} = 5.5V, I_{BYP} = 100mA		35	80	mΩ
BUCK OPERATION					
Switching Frequency	V_{BAT} = 3.6V		4		MHz
Maximum Duty Cycle			99.5		%
Minimum On-Time			55		ns
Maximum On-Time			10		µs
Minimum Off-Time			65		ns
Soft-Start Time			1.5		ms
High-Side Resistance	I_{LX} = 100mA, V_{DC} = 5.5V		120	250	mΩ
Low-Side Resistance	I_{LX} = 100mA, V_{DC} = 5.5V		150	220	mΩ
Thermal Regulation Temperature (T_{REG})	I^2C programmable with REGTEMP[1:0] to 90°C, 105°C, 120°C, and disabled (default 105°C)		105		°C
Thermal Regulation Gain	Percentage decrease in I_{FCHG} above the thermal regulation temperature		5		%/°C
BATTERY CHARGER PRECHARGE					
Battery-Prequalification Lower Threshold (V_{PQLTH})	V_{BAT} rising, 130mV hysteresis		2.1		V
Dead-Battery Charge Current (I_{DBAT})	0V ≤ V_{BAT} ≤ 2.1V		45		mA
Battery-Prequalification Upper Threshold (V_{PQUTH})**	V_{BAT} rising, 150mV hysteresis		2.5		V
Prequalification Charge Current (I_{PQ})	Percentage of fast-charge current programmed		10		%
CONSTANT-CURRENT MODE					
BAT Fast-Charge Current (I_{FCHG}) Range	5 bits: 50mA steps, R_{CS} = 47ml	250		1550	mA
Fast-Charge Current Accuracy	T_A = +15°C to +45°C	-5		+5	%
	JEITA safety region (Figure 4)	-65	-50	-35	%

Electrical Characteristics (continued)

(V_{DC} = 5V, C_{BYP} = 1µF, I_{FCHG} = 500mA, C_{AVL} = 4.7µF, V_{THM} = AVL/2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CONSTANT VOLTAGE MODE						
Battery Regulation Voltage (V_{BATREG})	I_{BAT} = 100mA, operating in voltage-regulation mode, I²C programmable with CHGCV[1:0] to 4.1V, 4.15V, 4.2V, and 4.35V (default 4.2V)	T_A = +25°C	-0.5		+0.5	%
		T_A = -40°C to +85°C	-1		+1	
		JEITA safety region, percentage of battery regulation voltage (Note 6)	96	97	98	
Battery Refresh Threshold	(Below regulation point), 100mV and 150mV selection, default 150mV (Note 5)		120	150	185	mV
Battery Overvoltage Protection	V_{BAT} threshold over regulation voltage to turn off charger during charge (% of regulation voltage) (Note 7)		102	103.5	105	%
	Hysteresis (V_{BAT} falling) at 4.2V			1.4		
Charge-Current Termination Threshold (I_{TOPOFF})	Programmable topoff current independent of JEITA functionality, default 50mA, 200mA hysteresis		50		200	mA
	Deglitch time			16		ms
Charge-Current Termination Accuracy	I_{TOPOFF} = 200mA		-20		+20	%
GSM TEST MODE						
GSM Test-Mode Output Pulse Current	V_{BAT} capacitance ≥ 60µF, peak current pulse frequency = 217Hz, on-duty cycle 12.5%			2.3		A
GSM Test-Mode Minimum Output	V_{BAT} capacitance ≥ 60µF, current pulse frequency = 217Hz, on-duty cycle 12.5% (Note 3)		3.7			V
CHARGER TIMER						
Prequalification Time (t_{PQ})	V_{BAT} < V_{BATPQ_UT}			45		Mins
Fast-Charge Time (t_{FC})	I²C programmable with FCHGT[2:0] from 4 hours to 10 hours (default 5 hours)			5		hrs
Timer Accuracy				20		%
Top-Off Time (t_{TOPOFF})	I²C programmable with TOFFT[2:0] from 0 minutes to 70 minutes in 10-minute steps (default 30 minutes)		0		70	Mins
Top-Off Timer Accuracy				20		%
Timer-Extend Current Threshold (Note 3)	Percentage of fast-charge current below which the timer clock operates at half speed			50		%

Electrical Characteristics (continued)

(V_{DC} = 5V, C_{BYP} = 1µF, I_{FCHG} = 500mA, C_{AVL} = 4.7µF, V_{THM} = AVL/2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25µC.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
THERMISTOR MONITOR						
THM Threshold, Cold, No Charge (0°C)	$V_{THM/AVL}$ rising, 1% hysterisis (thermistor temperature falling)		71.06	74.56	78.06	%
THM Threshold, Cold, Current Foldback (+15°C)	$V_{THM/AVL}$ rising, 1% hysterisis (thermistor temperature falling)		57.00	60.00	63.00	%
THM Threshold, Hot, Voltage Foldback (+45°C)	$V_{THM/AVL}$ falling, 1% hysterisis (thermistor temperature rising)		32.68	34.68	36.68	%
THM Threshold, Hot, No Charge (+60°C)	$V_{THM/AVL}$ falling, 1% hysterisis (thermistor temperature rising)		21.24	22.54	23.84	%
THM Input Bias Current	V_{THM} = V_{AVL} or 0V	T_A = +25°C	-0.2	0.01	+0.2	µA
		T_A = +85°C		0.01		
V_{ICHG}						
V_{ICHG} Output Voltage	I_{BAT} = 100mA			150		mV
	I_{BAT} = 1000mA		1260	1400	1540	mV
	I_{BAT} = 1500mA			2100		mV
IRQB OUTPUT						
Low-Level Output Saturation Voltage	I_{IRQB} =10mA, sinking current				0.4	V
High-Level Leakage Current	V_{IRQB} = 5V	T_A = +25°C	-1	0.01	+1	µA
		T_A = +85°C		0.1		µA
SAFEOUT OUTPUT						
Regulated Output	I_{SFO} = 30mA, V_{DC} = 5.5V		4.75	5	5.25	V
Dropout Voltage	I_{SFO} = 30mA			45		mV
Current Limit				590		mA
Maximum Output Current			100			mA
POK Output Threshold				2.7		V
PVL/AVL OUTPUT						
PVL Output Voltage	5.5V < V_{DC} < 7.5V, no load			5.05		V
AVL Output Voltage	5.5V < V_{DC} < 7.5V, no load			5.05		V
LOGIC LEVELS AND TIMING CHARACTERISTICS (SCL, SDA)						
Output Low Threshold	I_o = 3mA, sink current (SDA)				0.4	V
Input Low Threshold	V_{I2CIN} = 1.8V				0.4	V
Input High Threshold	V_{I2CIN} = 1.8V		1.4			V

Electrical Characteristics (continued)

(V_{DC} = 5V, C_{BYP} = 1µF, I_{FCHG} = 500mA, C_{AVL} = 4.7µF, V_{THM} = AVL/2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current	V_{I2CIN} = 1.8V, T_A = +25°C			1	µA
SCL Clock Frequency		100		400	kHz
Bus Free Time Between START and STOP (Note 3)		1.3			µs
Hold Time REPEATED START Condition (Note 3)		0.6			µs
SCL Low Period (Note 3)		1.3			µs
SCL High Period (Note 3)		0.6			µs
Setup Time REPEATED START Condition (Note 3)		0.6			µs
SDA Hold Time (Note 3)		0			µs
SDA Setup Time (Note 3)		100			ns
Maximum Pulse Width of Spikes (must be suppressed by the input filter of both SDA and SCL signals) (Note 3)			50		ns
Setup Time for STOP Condition (Note 3)		0.6			µs
THERMAL REGULATION AND SHUTDOWN					
Thermal Shutdown Temperature (Note 3)			+160		°C
Thermal Shutdown Hysteresis (Note 3)			15		°C

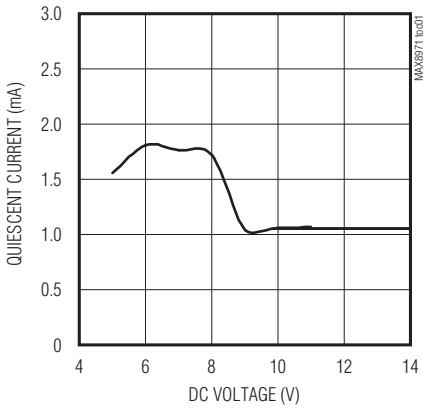
Note 2: Parameters are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.
Note 3: Guaranteed by design, not production tested.
Note 4: Voltage for 4.35V battery mode increases by 100mV.
Note 5: Refresh voltage for 4.15V increases by 50mV.
Note 6: JEITA decreases by 1% for 4.15V termination voltage.
Note 7: Battery overvoltage increases by 1% for 4.15V termination voltage.

** = Contact factory for alternate thresholds (6.7V, 9.7V, and 14V available).*
*** = Contact the factory for 3.0V.*

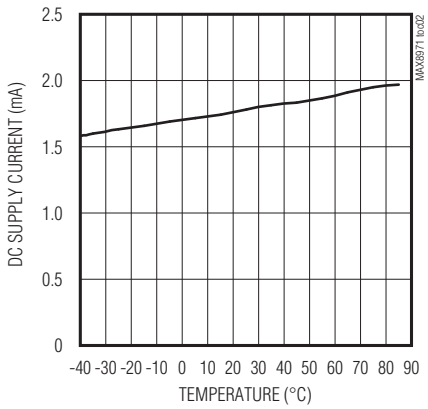
Typical Operating Characteristics

(V_{DC} = 5V, C_{BYP} = 1µF, C_{AVL} = 4.7µF, V_{THM} = 2.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

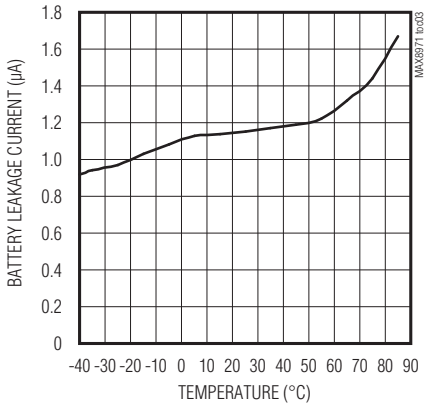
DC QUIESCENT CURRENT vs. DC SUPPLY VOLTAGE



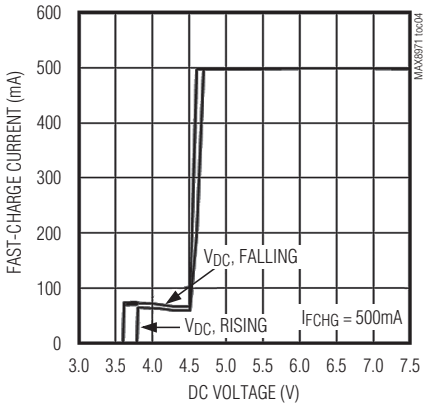
DC SUPPLY CURRENT vs. TEMPERATURE



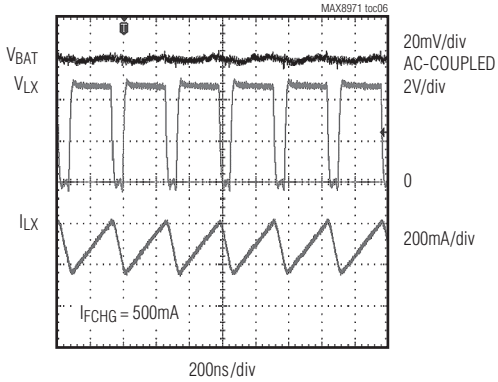
BATTERY LEAKAGE CURRENT vs. TEMPERATURE



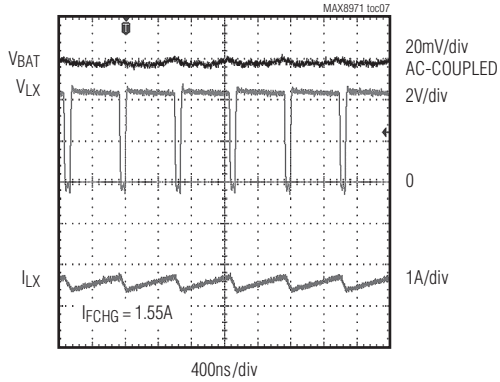
FAST-CHARGE CURRENT vs. DC SUPPLY VOLTAGE



MEDIUM LOAD SWITCHING WAVEFROMS



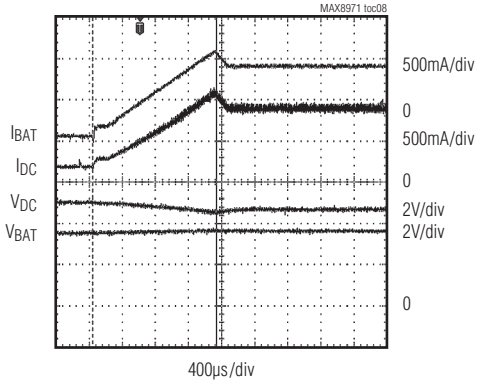
HEAVY LOAD SWITCHING WAVEFROMS



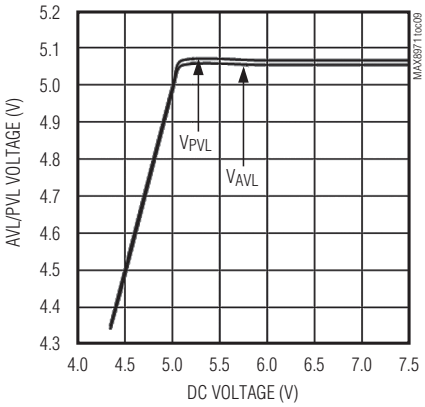
Typical Operating Characteristics (continued)

(V_{DC} = 5V, C_{BYP} = 1µF, C_{AVL} = 4.7µF, V_{THM} = 2.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

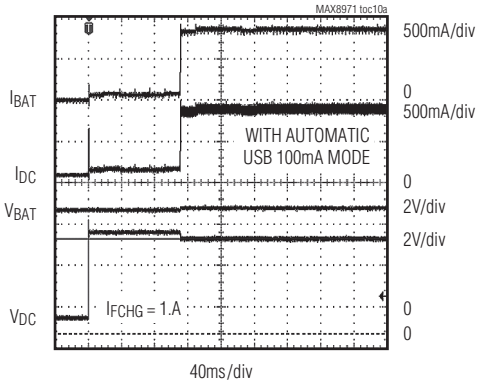
CHARGER ENABLE SOFT-START TIME



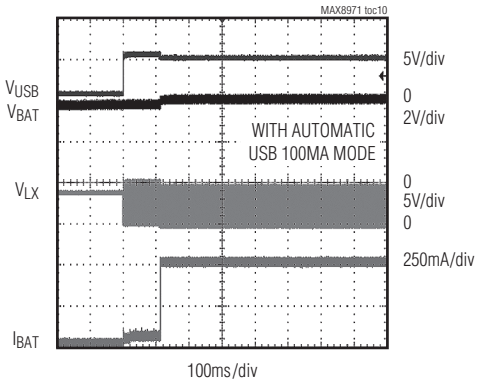
AVL/PVL VOLTAGE vs. DC SUPPLY VOLTAGE



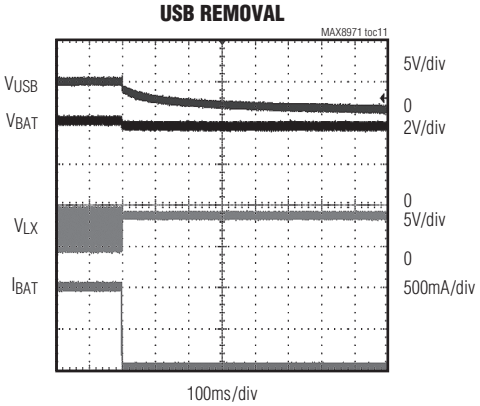
DC PLUG-IN TO 1A DEFAULT FAST-CHARGE CURRENT



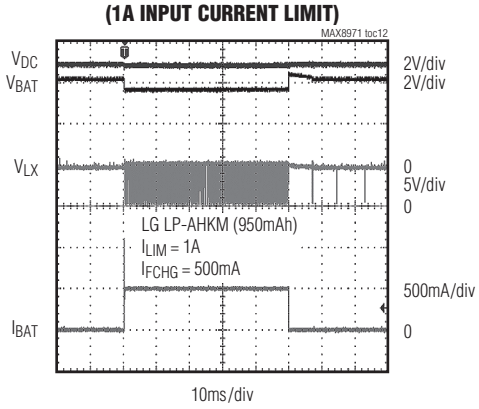
USB INSERTION INTO 500mA DEFAULT FAST-CHARGE CURRENT



USB REMOVAL



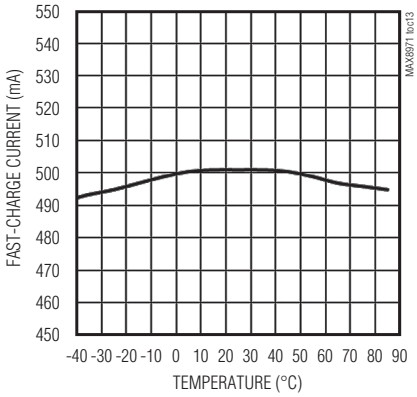
BATTERY INSERTION/REMOVAL (1A INPUT CURRENT LIMIT)



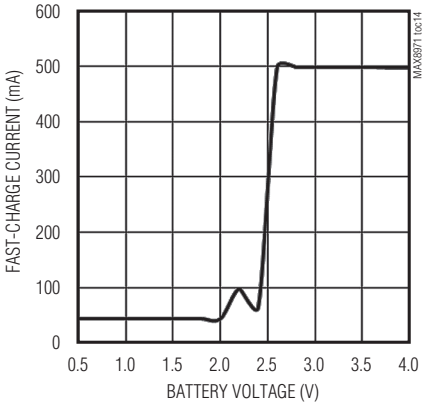
Typical Operating Characteristics (continued)

(V_{DC} = 5V, C_{BYP} = 1µF, C_{AVL} = 4.7µF, V_{THM} = 2.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

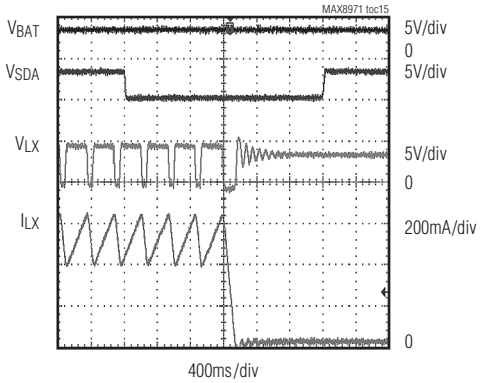
FAST-CHARGE CURRENT vs. TEMPERATURE



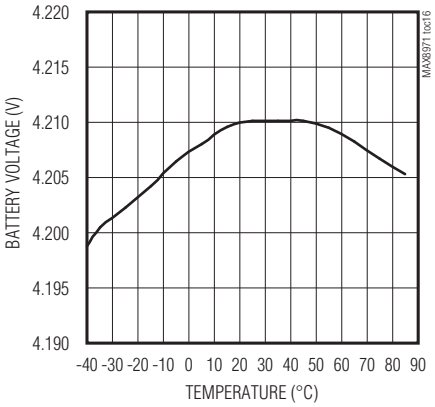
FAST-CHARGE CURRENT vs. BATTERY VOLTAGE



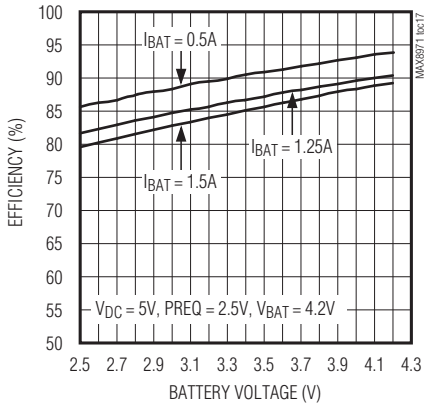
FAST CHARGE TO SUSPEND



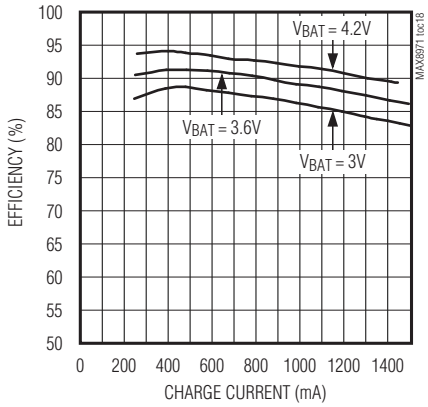
BATTERY REGULATION VOLTAGE vs. TEMPERATURE



BATTERY CHARGER EFFICIENCY vs. BATTERY VOLTAGE



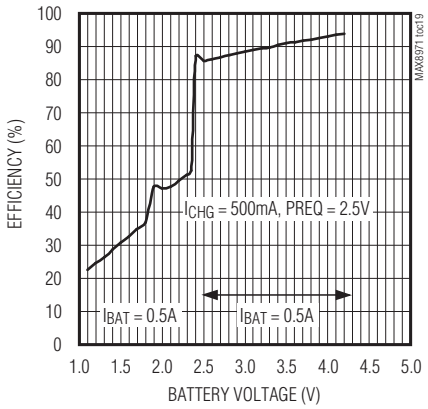
BATTERY CHARGER EFFICIENCY vs. CHARGE CURRENT



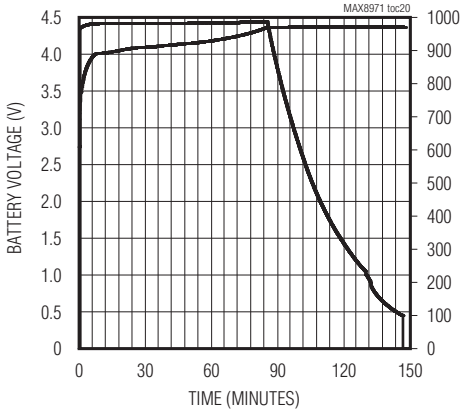
Typical Operating Characteristics (continued)

(V_{DC} = 5V, C_{BYP} = 1µF, C_{AVL} = 4.7µF, V_{THM} = 2.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

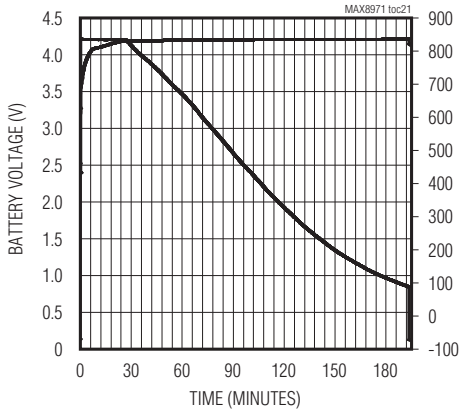
BATTERY CHARGER EFFICIENCY vs. BATTERY VOLTAGE



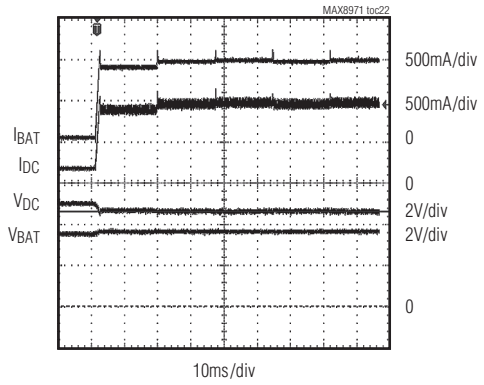
CHARGE PROFILE FOR 1830mAh 4.35V BATTERY CHARGED AT 0.55C



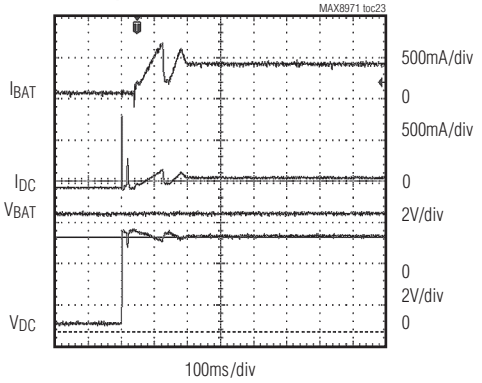
CHARGE PROFILE FOR 1500mAh 4.2V BATTERY WITH 70mA CONSTANT LOAD CHARGED AT 0.6C



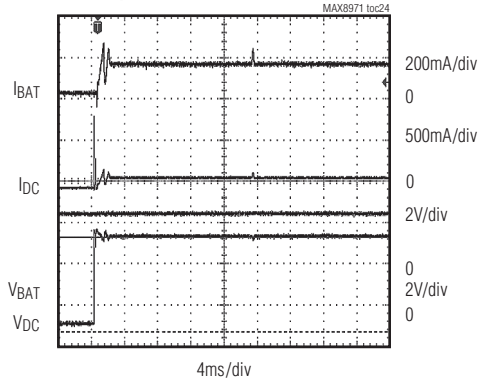
AUTOMATIC INPUT CURRENT LIMIT



AUTOMATIC INPUT CURRENT LIMIT (2Ω CABLE RESISTANCE)



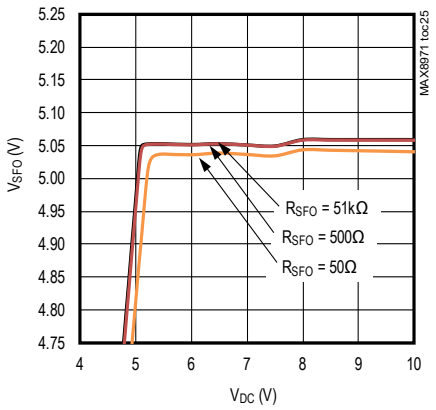
AUTOMATIC INPUT CURRENT LIMIT (1Ω CABLE RESISTANCE)



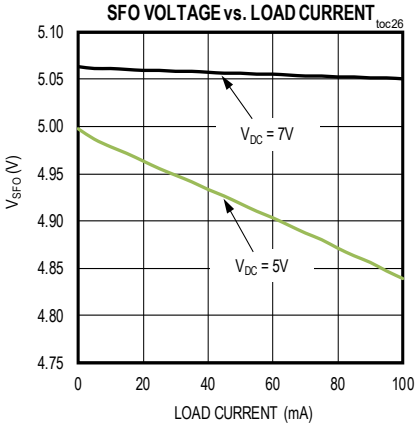
Typical Operating Characteristics (continued)

(V_{DC} = 5V, C_{BYP} = 1µF, C_{AVL} = 4.7µF, V_{THM} = 2.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

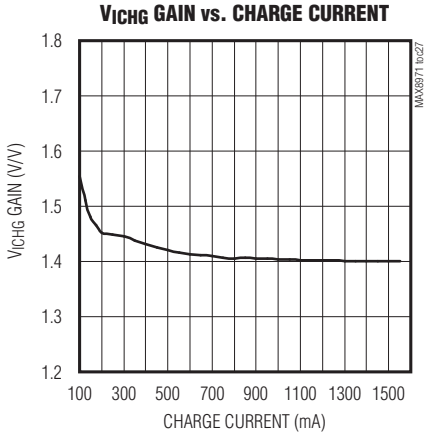
SFO VOLTAGE vs. DC INPUT VOLTAGE



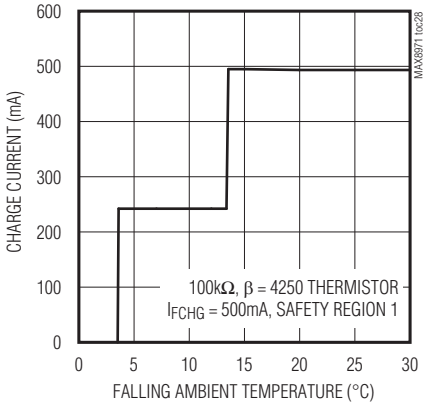
SFO VOLTAGE vs. LOAD CURRENT



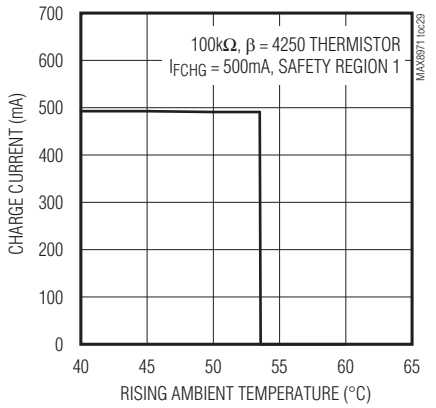
VICHG GAIN vs. CHARGE CURRENT



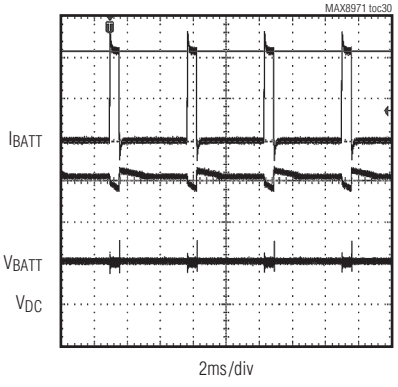
CHARGE CURRENT vs. AMBIENT TEMPERATURE



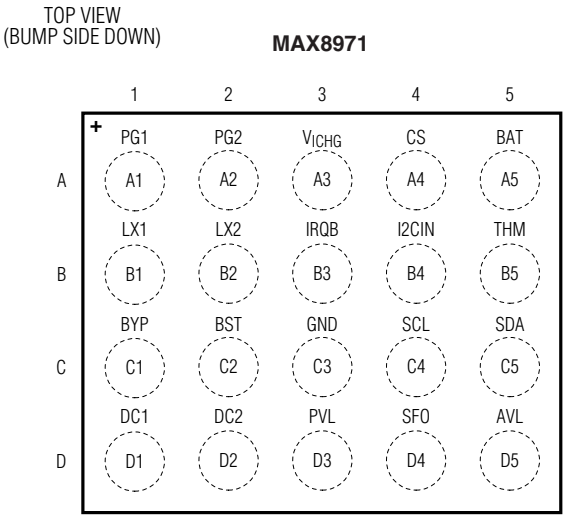
CHARGE CURRENT vs. AMBIENT TEMPERATURE



GSM TEST MODE



Bump Configuration



WLP

Bump Description

PIN	NAME	FUNCTION
A1, A2	PG1, PG2	Power Ground for Step-Down Low-Side FET
A3	V_{ICHG}	Battery-Charging Current Monitor Output. This pin is an analog representation of the charger current at 1.4mV/mA.
A4	CS	Current-Sense Input Power Pin
A5	BAT	Battery Connection. Connect to a single-cell Li+ battery.
B1, B2	LX1, LX2	Buck Inductor Connection. Connect the inductor between LX_ and CS. The LX1 and LX2 pins must be connected together externally.
B3	IRQB	Open-Drain Host Processor Interrupt Pin
B4	I2CIN	I^2C Interface Supply
B5	THM	Thermistor Input. Connect a negative temperature coefficient (NTC) thermistor from THM to GND. Connect a resistor equal to the thermistor +25°C resistance from THM to AVL. Charging is suspended when the thermistor is outside the hot and cold limits. Connect THM to GND to disable the thermistor temperature sensor. If the thermistor function is disable through I^2C, connect THM to GND.
C1	BYP	Connection Point Between Reverse Blocking MOSFET and High-Side Switching MOSFET. Bypass to PG_ with a minimum 1µF ceramic capacitor.
C2	BST	High-Side FET Driver Supply. Bypass BST to LX with a 0.1µF ceramic capacitor.
C3	GND	Analog Ground. GND is the low-noise ground connection for the internal circuitry.

Bump Description (continued)

PIN	NAME	FUNCTION
C4	SCL	I²C Interface Clock. Connect a 10kΩ resistor from SCL to I2CIN.
C5	SDA	I²C interface Data. Connect a 10kΩ resistor from SDA to I2CIN.
D1, D2	DC1, DC2	High-Current Charger Input Supply Pin(s). Bypass to PG_ with a 2.2µF ceramic capacitor. DC is capable of delivering up to 1.5A to BYP. DC supports both AC adapter and USB inputs. Short DC1 and DC2 together externally.
D3	PVL	Internal Bias Regulator High-Current Output Bypass Pin. Supports internal noisy and high-current gate drive loads. Bypass to PGND with a minimum 1µF ceramic capacitor. Do not use PVL to power external loads.
D4	SFO	5V SAFEOUT (SFO) LDO Linear Regulator Output. Bypass SFO to GND with a 1µF or larger ceramic capacitor. SFO can be used to supply low-voltage rated USB systems.
D5	AVL	Internal-Bias-Regulator Quiet Analog Bypass Pin. Internal 10Ω connection between PVL and AVL forms a lowpass filter with external bypass capacitor to GND. Do not use AVL to power external loads.

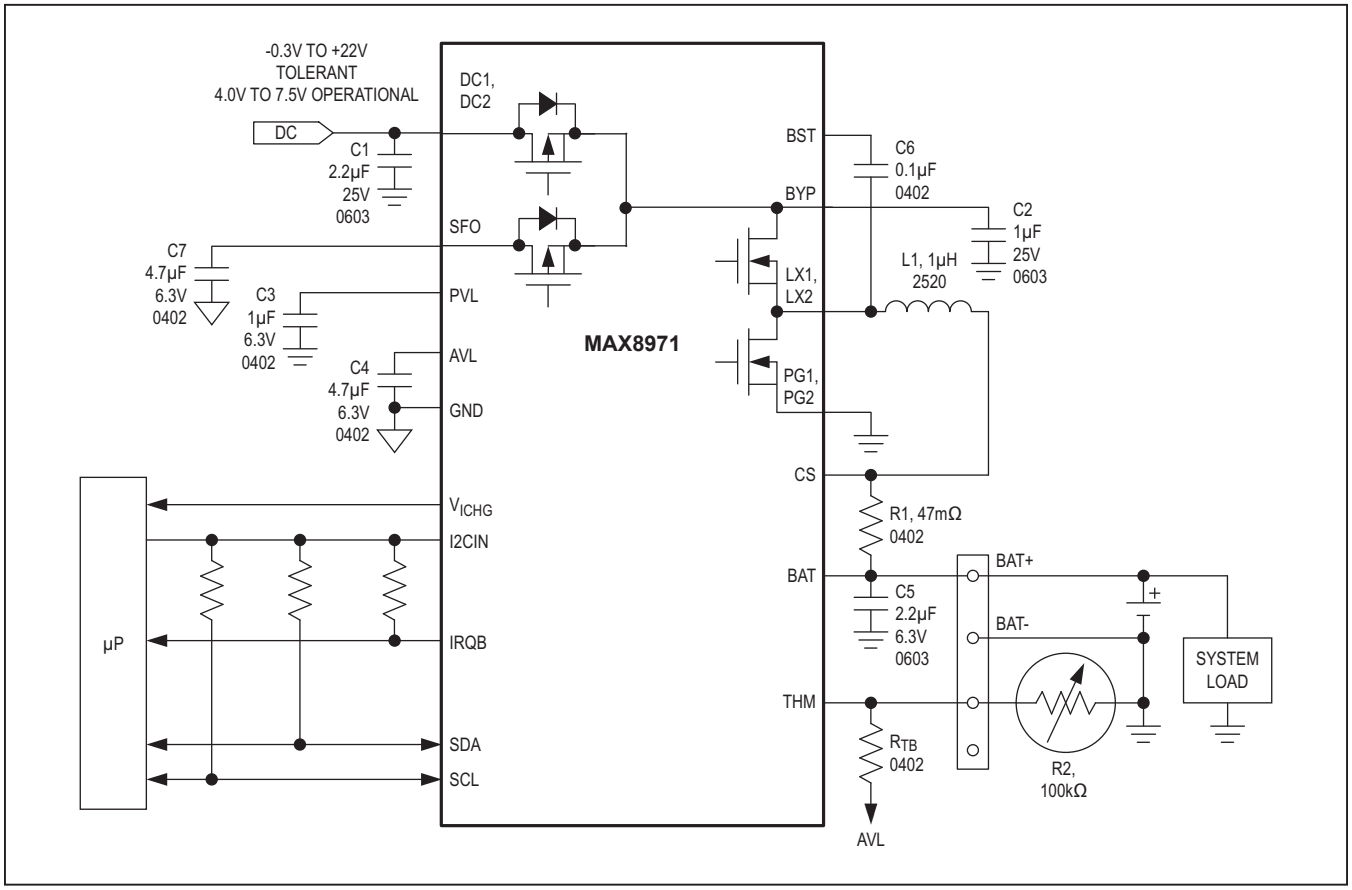


Figure 1. Typical Application Circuit

Detailed Description

The MAX8971 is a JEITA-compliant Li+ switching battery charger that safely charges a single Li+ cell in accordance with JEITA specifications. The IC accepts an input supply range from 4V to 7.5V, but disables charging if the supply voltage exceeds +7.5V, protecting against unqualified or faulty AC adapters. The step-down converter supplies up to 1.5A to the battery. The IC includes charger features thermistor monitor, charger status and fault outputs. Also included are interrupt signals to the processor. Flexibility is maintained with adjustable charge current, input current limit, and a minimum battery voltage (when charging is scaled back to hold the battery voltage up) through an I^2C interface.

DC Input—Fast-Hysteretic Step-Down Regulator

If a valid DC input is present, battery charging is supplied by the high-frequency step-down regulator from DC. The step-down regulation point is then controlled by three feedback signals: maximum step-down output current programmed by the input current limit, maximum charger current programmed for the fast-charge current, and maximum die temperature. The feedback signal requiring the smallest current controls the average output current in the inductor. This scheme minimizes total power dissipation for battery charging, and allows the battery to absorb any load transients with minimum voltage disturbance.

A proprietary hysteretic current PWM control scheme ensures fast switching and physically tiny external components. The feedback control signal that requires the smallest input current, controls the center of the peak and valley currents in the inductor. The ripple current is internally set to provide 4MHz operation. When the input voltage decreases near the output voltage, very high duty cycle occurs. Due to minimum off-time, 4MHz operation is not achievable. The controller then provides minimum off-time, peak current regulation. Similarly, when the input voltage is too high to allow 4MHz operation due to the minimum off-time, the controller becomes a minimum on-time, valley current regulator. In this way, ripple current in the inductor is always as small as possible to reduce ripple voltage-on battery for a given capacitance. The ripple current is made to vary with input voltage and output voltage in a way that reduces frequency variation. However, the frequency still varies somewhat with operating conditions.

Soft-Start

To prevent input current transients, the rate of change of the input current (di/dt) and charge current is limited. When the input is valid the charge current ramps from 0mA to the fast-charge current value in 1.5ms. Charge current also soft-starts when transitioning from the prequalification state to the fast-charge state. There is no di/dt limiting when transitioning from the done state to the fast-charge state.

PVL and AVL

PVL is a 5V linear regulator that the IC uses to power the gate drivers for its step-down charger. PVL also charges the BST capacitor. The PVL linear regulator is on when DC is greater than ~2.5V, otherwise it is off. Bypass PVL with a 1µF ceramic capacitor to PG. Powering external loads from PVL is not recommended.

As shown in Figure 1, AVL is a filtered output from the PVL linear regulator that the IC uses to power its internal analog circuits. The filter consists of an internal 10Ω resistor, and the AVL external bypass capacitor (4.7µF). This filter creates a 100kHz lowpass filter that cleans the 4MHz switching noise from the analog portion of the IC. Connect a 4.7µF ceramic capacitor from AVL to GND. Powering external loads with AVL is not recommended.

Thermistor Input (THM)

The THM input connects to an external negative temperature coefficient (NTC) thermistor to monitor battery or system temperature. Charging is suspended when the thermistor temperature is out of range. The charge timers are suspended and hold their state, but no fault is indicated. When the thermistor comes back into range, charging resumes and the charge timer continues from where it left.

Since the thermistor monitoring circuit employs an external bias resistor from THM to AVL, the thermistor is not limited only to 10kΩ (at +25°C). Any resistance thermistor can be used as long as the value is equivalent to the thermistors +25°C resistance. For example, with a

10kΩ at R_{TB} resistor, the charger enters a temperature suspend state when the thermistor resistance falls below 3.97kΩ (too hot) or rises above 28.7kΩ (too cold). This corresponds to the 0°C to +50°C range when using a 10kΩ NTC thermistor with a beta of 3500. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e^{\left\{\beta\left(\frac{1}{T+273°C} - \frac{1}{298°C}\right)\right\}}$$

where:

R_T = the resistance in Ω of the thermistor at temperature T in Celsius

R_{25}= the resistance in Ω of the thermistor at +25°C

β = the material constant of the thermistor, which typically ranges from 3000k to 5000k

T = the temperature of the thermistor in °C

Some designs might prefer other thermistor temperature limits. Threshold adjustment can be accommodated by changing R_{TB}, connecting a resistor in series and/or in parallel with the thermistor, or using a thermistor with different β. For example, a +45°C hot threshold and 0°C cold threshold can be realized by using a thermistor with a β to 4250, and connecting 120kΩ in parallel. Since the thermistor resistance near 0°C is much higher than it is near +50°C, a large parallel resistance lowers the cold threshold, while only slightly lowering the hot threshold. Conversely, a small series resistance raises the hot threshold, while only slightly raising the cold threshold. Raising R_{TB}, lowers both the hot and cold threshold, while lowering R_{TB} raises both thresholds.

Note that since AVL is active whenever valid input power is connected at DC, thermistor bias current flows at all times. Using a 10kΩ thermistor and a 10kΩ pullup to AVL, results in an additional 250µA load. This load can be reduced to 25µA by instead using a 100kΩ thermistor and 100kΩ pullup resistor.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the IC's junction temperature. When the die temperature exceeds T_{REG}, a thermal limiting circuit reduces the battery charge-current target until the charge current reaches 10% of the fast-charge current setting. The charger maintains 10% of the fast-charge current until the die temperature reaches T_{SHDN}. Please note that the IC is rated for a maximum ambient temperature of +85°C. Furthermore, although the maximum die temperature of the MAX8971 is +150°C, it is common industry practice to design systems in such a way that the die temperature never exceeds +125°C. Limiting the maximum die temperature to +125°C extends long-term reliability.

Charger States

The IC utilizes several charging states to safely and quickly charge batteries as shown in Figure 3.

Figure 2 shows an exaggerated view of a Li+/Li-Poly battery progressing through the following charge states when the die and battery are close to room temperature: dead battery → prequalification → fast charge → top-off → done.

Table 1. Trip Temperatures for Different Thermistors

THERMISTOR	R_{25} (Ω)	10000	10000	47000	100000
	Thermistor Beta (β)	3380	3940	4050	4250
	R_{TB} (Ω)	10000	10000	47000	100000
	R_{15} (Ω)	14826	15826	75342	164083
	R_{45} (Ω)	4900	4354	19993	40781
TRIP TEMPERATURES	T0 (°C)	-0.8	2.6	3.2	4.1
	T1 (°C)	14.7	16.1	16.4	16.8
	T2 (°C)	42.6	40.0	39.6	38.8
	T3 (°C)	61.4	55.7	54.8	53.2

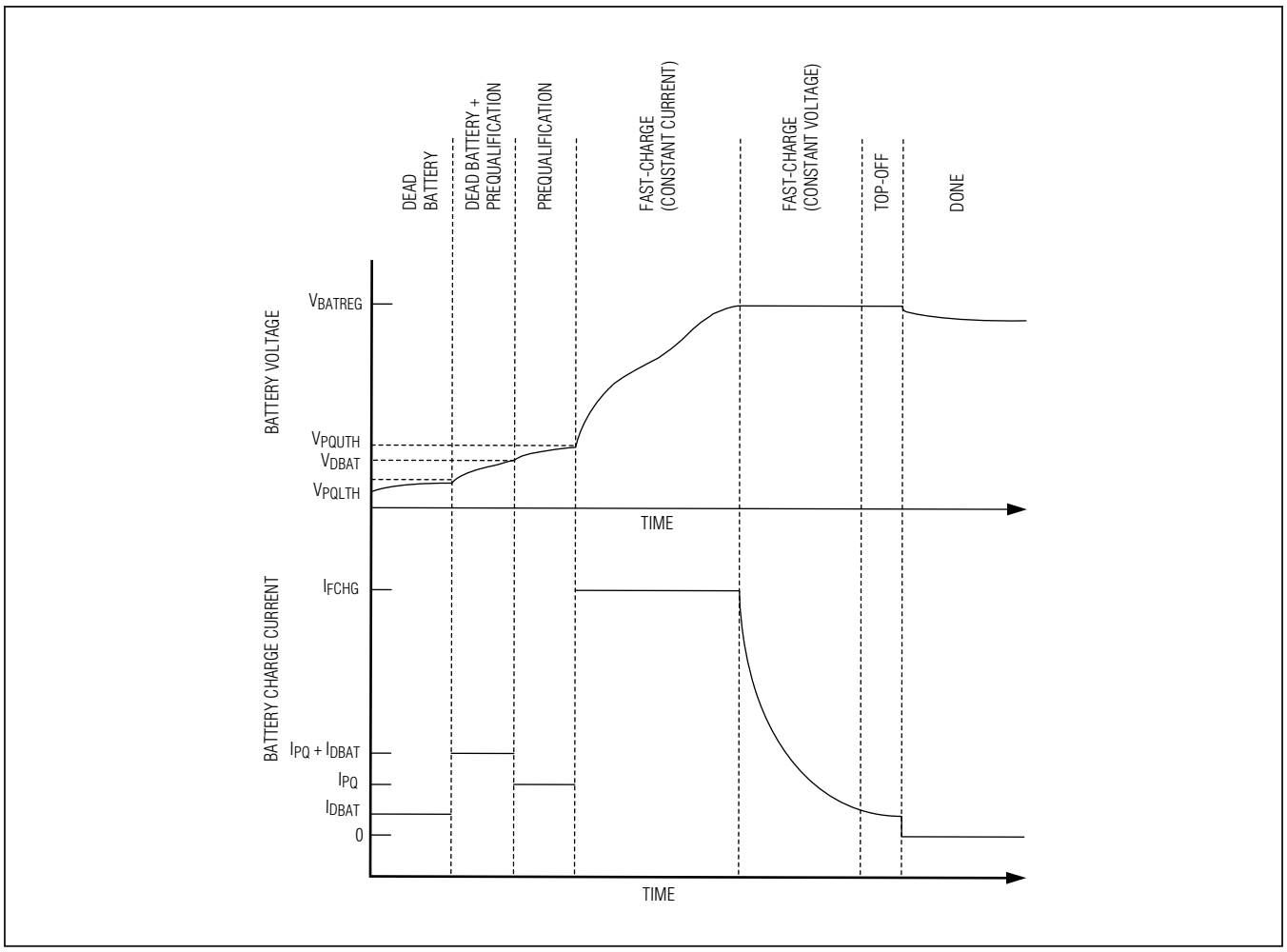


Figure 2. Li/Li-Poly Charge Profile

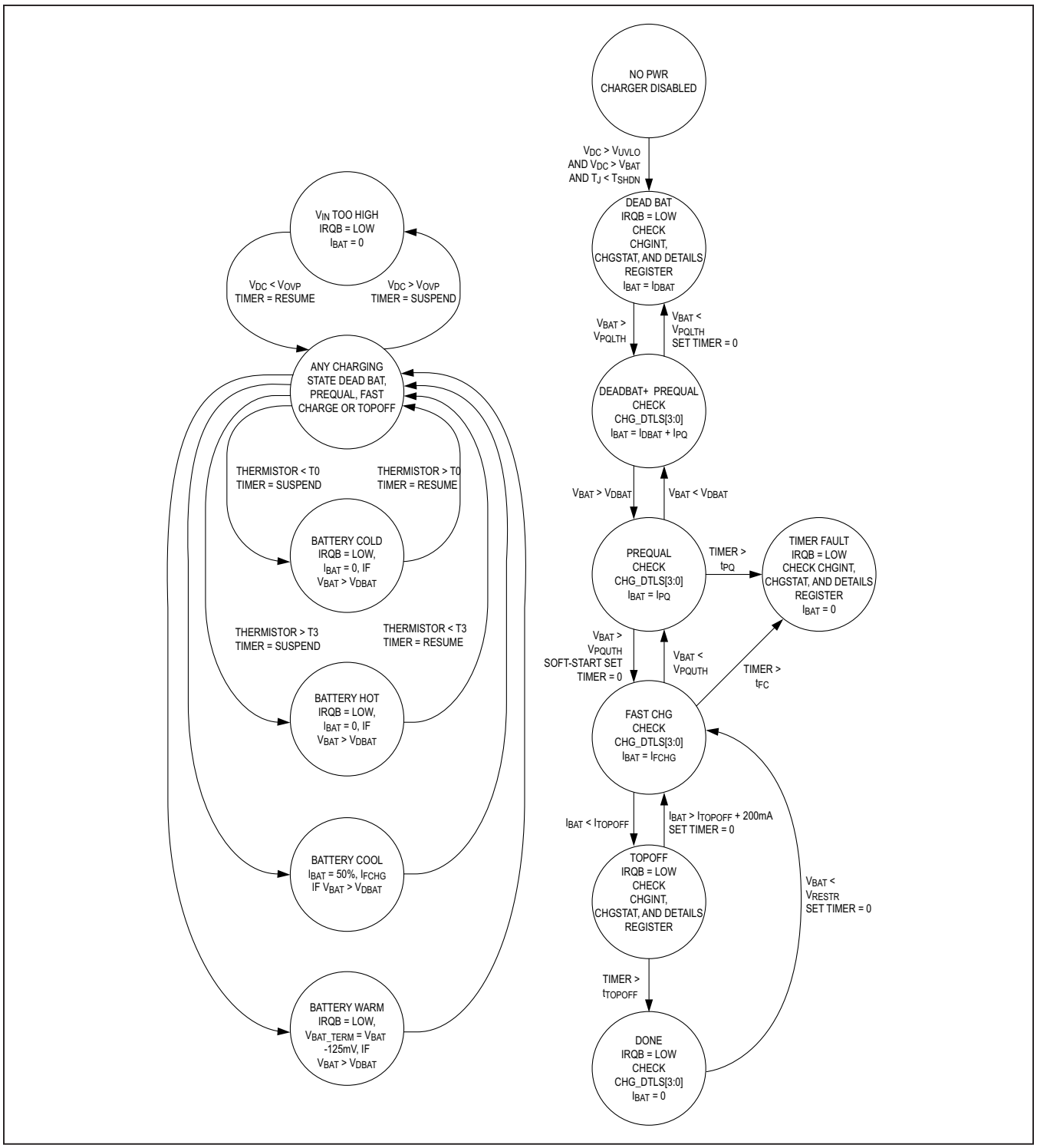


Figure 3. Functional State Diagram

Charger-Disabled State

When DC is low or the input voltage is out of range, the IC disables the charger. To exit this state, the input voltage must be within its valid range.

Dead-Battery State

When a deeply discharged battery is inserted with a voltage of less than V_{PQLTH}, the IC disables the switching charger and linearly charges with I_{DBAT}. Once V_{BAT} increases beyond V_{PQLTH}, the IC clears the prequalification timer, and transitions to the dead battery + prequalification state. This state prevents the IC from dissipating excessive power in the event of a shorted battery. The dead-battery linear charge remains on, except when in the charger disabled state, timer fault state, thermal shutdown and $V_{BAT} > V_{DBAT}$.

Dead-Battery + Prequalification State

The dead battery + prequalification state occurs when the battery voltage is greater than V_{PQLTH}, and less than V_{DBAT}. In this state, both the linear dead-battery charger and the switching charger are on, delivering current to the battery. The total battery current is I_{DBAT} + I_{PQ}. If the IC remains in this state for longer than t_{PQ}, the IC transitions to the timer fault state. A normal battery typically stays in this state for several minutes or less. When the battery voltage rises above V_{DBAT} the IC transitions to the prequalification states. The dead-battery linear charger remains on except when in the charger disabled state, timer fault state, thermal shutdown and $V_{BAT} > V_{DBAT}$.

Prequalification State

The prequalification state occurs when the battery voltage is greater than V_{DBAT} and less than V_{PQUTH}. In this state, the linear dead-battery charger is turned off. Only the switching charger is on and delivering current to the battery. The total battery current is I_{PQ}. If the IC remains in this state for longer than t_{PQ}, then the IC transitions to the timer fault state. A normal battery typically stays in the prequalification state for several minutes or less. When the battery voltage rises above V_{PQUTH}, the IC transitions to the fast-charge constant-current state.

Fast-Charge Constant-Current State

The fast-charge constant-current state occurs when the battery voltage is greater than V_{PQUTH} and less than V_{BATREG}. In this state, the switching charger is on and delivering current to the battery. The total battery current is I_{FCHG}. If the IC remains in this state and the fast-charge constant voltage state for longer than t_{FC}, then the IC transitions to the timer fault state. When the battery voltage rises to V_{BATREG}, the IC transitions to the fast-charge constant voltage state. The fast-charge constant-current is set to 50% of programmed value when 0°C < THM <+15°C, and 100% of programmed value when +15°C < THM <+60°C.

The MAX8971 dissipates the most power in the fast-charge constant-current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds T_{REG}, I_{FCHG} is reduced.

If there is low input-voltage headroom (V_{IN} - V_{BAT}), then I_{FCHG} decreases due to the impedance from IN to BAT.

Fast-Charge Constant Voltage State

The fast-charge constant voltage state occurs when the battery voltage is at the V_{BATREG}, and the charge current is greater than I_{TOPOFF}. In this state, the switching charge is on and delivering current to the battery. The IC maintains V_{BATREG} and monitors the charge current to detect when the battery consumes less than the TOPOFF current. When the charge current decreases below the TOPOFF threshold, the IC transitions to the top-off state. If the IC remains in the fast-charge constant-current state for longer than t_{FC}, then it transitions to the timer fault state.

Top-Off State

The top-off state occurs when the battery voltage is at V_{BATREG} and the battery current decreases below TOPOFF current. In this state, the switching charger is on and delivers current to the battery. The IC maintains V_{BATREG} for a specified time. When this time expires, the IC transitions to the DONE state. If the charging current increases to I_{TOPOFF} + 200mA before this time expires, then the charge reenters the fast-charge constant voltage state.

Done State

The IC enters its done state after the charge has been in the top-off state for t_{TOPOFF}. In this state, the switching charger is off and no current is delivered to the battery. If the system load presented to the battery is low << 10µA, then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold and the IC transitions back into the fast-charge state. There is no soft-start (di/dt limiting) during the done-to-fast-charge state transition.

Timer Fault State

The timer fault state occurs when either the prequalification or fast-charge timers expire. In this state, the charger is off. The charger can exit this timer fault state by cycling input power.

Overvoltage and Protection

The IC provides for a +22V absolute maximum positive input voltage, and a -0.3V absolute maximum negative input voltage. Excursions to the absolute maximum voltage levels should be on a transient basis only, but can be withstood by the IC indefinitely.

Situations that typically require extended input voltage ratings include, but are not limited to the following:

- Inductive kick
- Charge source failure
- Power surge
- Improperly wired wall adapter
- Improperly set universal wall adapter
- Wall adapter with the correct plug, but wrong voltage
- Home-built computer with USB wiring harness connected backwards (negative voltage)
- USB connector failure
- Excessive ripple voltage on a switch-mode wall charger
- USB-powered hub that is powered by a wall charger (typically through a barrel connector) that has any of the aforementioned issues
- Unregulated charger

Automatic Input Current Limit Protection

The IC includes an input-current-limiting feature. The amplifiers required for sensing the currents and associated logic circuitry for making decisions and changing the battery-charger current are fully integrated in the ICs. This not only helps in reducing cost, but also improves the speed of system response.

The IC works by monitoring the current being drawn from the AC adapter and comparing it to the programmed current limit. The current limit should be set based on the current-handling capability of the AC adapter. Generally, this limit is chosen to optimally fulfill the system-power requirements while achieving a satisfactory charging time for the batteries. If the AC-adapter current exceeds its output capability, the charger responds by cutting back on the charger current, thereby keeping the current drawn from the AC adapter within its capability. With such a battery charger, the AC adapter doesn't need to be oversized to meet maximum system and battery-charging requirements simultaneously, thereby reducing AC adapter cost.

The input current limit has two control inputs, one based on voltage and one based on current. The voltage input monitors the input voltage, and when it drops below the desired input (4.5V), it generates a flag (AICL) to decrement the fast-charge current.

When the voltage comparator initially trips at 4.5V, fast-charge current decrements at a slow rate, allowing the charger output to settle until the voltage on DC returns above this voltage threshold. Once the DC voltage resolves itself, the current delivery of the adapter is maximized. In the event of a limited input current source, an example being a 500mA adaptor plugged into a 1A input current limit setting, a second voltage comparator set at 4.4V triggers and throttles the fast-charge current to a minimum of 75mA. Once the DC voltage corrects itself to above 4.5V, the fast-charge level is checked every 16ms to allow the system to recover if the available input power increases.

The current-limit input monitors the current through the input FET and generates a flag (DC_I) to decrement the fast-charge current when the input limit is exceeded. The fast-charge current is slowly decremented until the input-limit condition is cleared. At this point, the fast-charge current is maintained for 16ms and is then sampled again.

V_{ICHG} Charging Current Monitor

V_{ICHG} is a buffered output that can be interpreted to the charge current (V_{ICHG} = 1400mV/I_{FCHG}). See the *Typical Operating Characteristics* section for the V_{ICHG} curve.

SAFEOUT

SAFEOUT (SFO) is a linear regulator that provides an output voltage of 5V and can be used to supply low-voltage rated USB systems. The SFO linear regulator turns on when V_{DC} > 2.5V.

JEITA Description

The IC JEITA-compliant switching Li+ battery charger safely charges a single Li+ cell in accordance with JEITA specifications. The IC monitors the battery temperature while charging, and automatically adjusts the fast-charge current and/or charge termination voltage as the battery temperature varies.

In safety region 1, the IC automatically reduces the fast-charging current for T_{BAT} < +15°C, and reduces the charge termination voltage from 4.200V to 4.074V for T_{BAT} > +45°C. The fast-charge current is reduced to 50% of the nominal fast-charge current with options for 25% and 75%. JEITA never specifically states one or the other. When battery charge current is reduced by 50%, the timer is doubled.

In safety region 2, the IC automatically reduces the charge termination voltage from 4.200V to 4.074V for T_{BAT} < +15°C and for T_{BAT} > +45°C. The fast-charge current is not changed in safety region 2. The safety region is programmable with the SAFETYREG bit.

Maxim Model Gauge M3 Support

Figure 5 illustrates how the IC can easily integrate with Maxim's Model gauge M3 MAX17047 chip. The user just needs to add a Schottky diode between V_{BATT} and V_{TT} on the MAX17047.

Factory-Mode GSM Test Mode Support

The IC supports GSM pulse programming scheme. When DC is inserted with no battery operation, the IC soft-starts and cycles through dead-battery, prequalification, and fast charge, settling at constant voltage-mode operation, and regulating to the termination voltage (4.2V default). At this time, when B4 of register 0x08 is sent, the part can now support GSM pulse. See the *Typical Operating Characteristics* section.

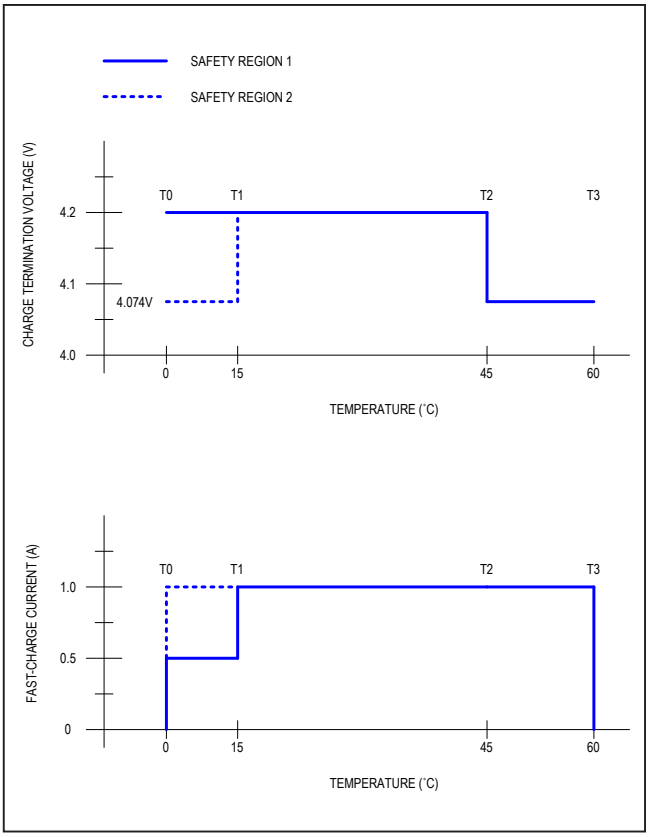


Figure 4. JEITA Safety Region

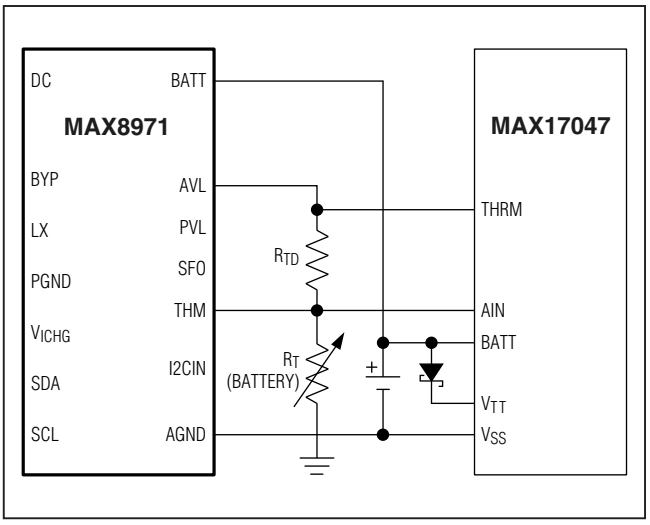


Figure 5. MAX8971 with MAX17047

The battery node should have enough capacitance to hold the battery voltage to some minimum acceptable system value (V_{SYS}) during the done to fast-charge state transition time of 100µs ($t_{DONE2FC}$).

$$C_{BAT} \geq I_{LOAD} \times t_{DONE2FC}/(V_{BATREG} - V_{SYS})$$

For example, if the maximum system load without a battery is 400mA (I_{LOAD}), and the minimum acceptable system voltage is 3.4V (V_{SYS}), then the battery node should have at least 40µF.

$$C_{BAT} \geq 400mA \times 100µs/(4.2V - 3.4V) = 40µF.$$

Applications Information

Inductor Selection

The charger operates with a switching frequency of 4MHz and uses a 1µH or 2.2µH inductor. This operating frequency allows the use of physically small inductors while maintaining high efficiency.

The inductor's DC current rating only needs to match the maximum load of the application because the IC features zero current overshoot during startup and load transients. For optimum transient response and high efficiency, choose an inductor with DC series resistance in the 40mΩ to 120mΩ range. See Table 2 for suggested inductors and manufacturers.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power source and reduces switching noise in the IC. The impedance of the input capacitor at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. A 4.7µF capacitor is recommended. For optimum noise immunity and low input ripple, the input capacitor value can be increased.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature and DC bias. Ceramic capacitors with Z5U or Y5V temperature characteristics should be avoided.

Output Capacitor Selection

For the charger, the output capacitor keeps the output voltage ripple small and ensures regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. A 4.7µF capacitor is recommended. For optimum load-transient performance and very low output ripple, increase the output capacitor value.

Charge Current Resistor Selection

Both the top-off current range and fast-charge current range depends on the sensing resistor (R_{SNS}). The default resistor recommended is a 47mΩ, 0.125W resistor. Select a 0.125W,47mΩ 2% sense resistor, e.g., Panasonic ERJ2BWGR047. This is a standard value.

$$P_{RSNS} = I_{CHARGE}^2 \times R_{SNS}$$

$$P_{RSNS} = 1.5^2 \times 0.047$$

$$P_{RSNS} = 0.105W$$

The charge current step (I_{CHARGE}) is calculated using equation below:

$$I_{CHARGE\_STEP} = V_{(CHGCC<>)}/R_{SNS}$$

Table 3 below shows the charge current settings for two sensing resistors.

$$I_{CHARGE\_CURRENT\_STEP} = V_{(TOPOFF<>)}/R_{SNS}$$

Table 2. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (I)	CURRENT RATING (mA)	DIMENSIONS
FDK	MIPSA2520D1R0	1.0	0.090	1600	2.5mm x 2.0mm x 1.2mm = 6mm^3
Murata	LQM2HPN1R0MG0	1.0	0.055	900	2.5mm x 2.0mm x 0.6mm = 3mm^3
Coilcraft	ELP2014-102ML	1.0	0.059	1680	2.0mm x 2.0mm x 1.4mm = 5.6mm^3
TDK	MLP2520S	1.0	0.06	1500	2.0mm x 2.5mm x 1.0mm = 5mm^3
Murata	DFE252012C	1	0.045	3800	2.5 x 2.0 x 1.2 = 6mm^3
Murata	LQM32PN1R0MG0	1	0.06	1800	3.2 x 2.5 x 0.9 = 7.2mm^3

Table 3. Charge Current Settings for 47mΩ and 68mΩ Sense Resistors

BIT	V_{IREG} (mV)	I_{CHARGE} (mA) R_{SNS} = 47mΩ	I_{CHARGE} (mA) R_{SNS} = 68mΩ
$V_{(CHGCC<11110>)}$	70.5	1500	1037
$V_{(CHGCC<10100>)}$	47	1000	691
$V_{(CHGCC<01010>)}$	23.5	500	345

Table 4. Top-Off Current Settings for 47mΩ and 68mΩ Sense Resistors

BIT	$V_{(TOPOFF)}$	$I_{(TOPOFF)}$ (mA) R_{SNS} = 47mΩ	$I_{(TOPOFF)}$ (mA) R_{SNS} = 68mΩ
$V_{(TOPOFF<>)}$	9.4	200	138.2
$V_{(TOPOFF<>)}$	4.7	100	69.1
$V_{(TOPOFF<>)}$	2.35	50	34.5

Serial Interface

The I²C-compatible, 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the complete register map.

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I²C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 6 shows an example of a typical I²C system. A device on I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When the MAX8971 I²C-compatible interface is operating, it is a slave on I²C bus, and it can be both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the HIGH portion of SCL clock pulse. Changes in SDA while SCL is HIGH are control signals (START and STOP conditions).

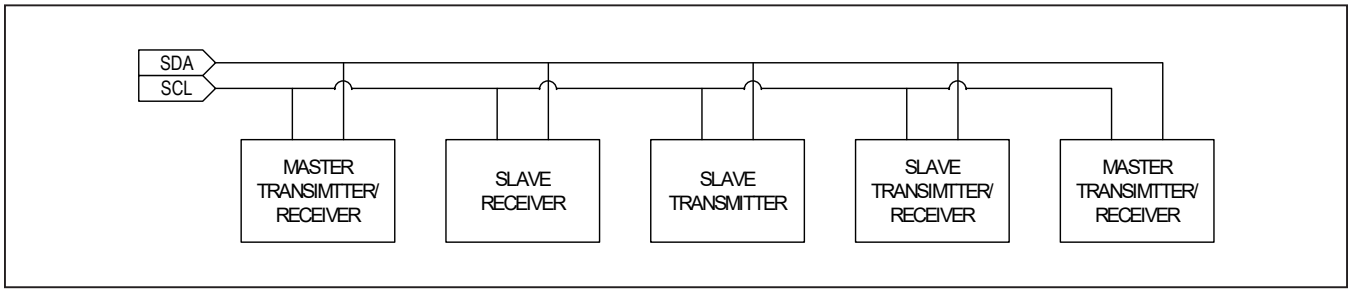


Figure 6. Functional Logic Diagram for Communications Controller

START and STOP Conditions

When the I²C serial interface is inactive, SDA and SCL idle HIGH. A master device initiates communication by issuing a START condition. A START condition is a HIGH-to-LOW transition on SDA with SCL HIGH. A STOP condition is a LOW-to-HIGH transition on SDA, while SCL is HIGH.

A START condition from the master signals the beginning of a transmission to the MAX8971. The master terminates transmission by issuing a NOT-ACKNOWLEDGE followed by a STOP condition.

A STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the MAX8971 internally disconnects SCL from I²C serial interface until the next START condition, minimizing digital noise and feedthrough.

Acknowledge

Both the I²C bus master and MAX8971 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA LOW before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it LOW during the HIGH period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled HIGH before the rising edge of the acknowledge-related clock pulse and leaves it HIGH during the HIGH period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

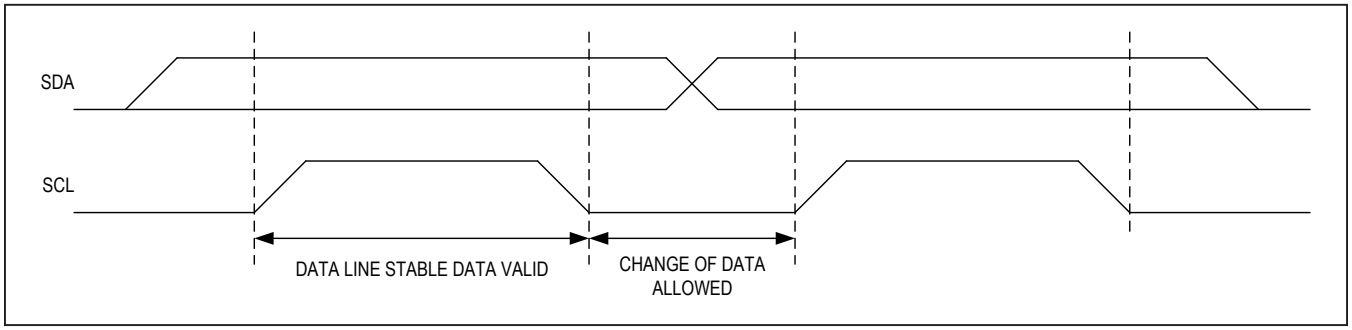


Figure 7. I²C Bit Transfer

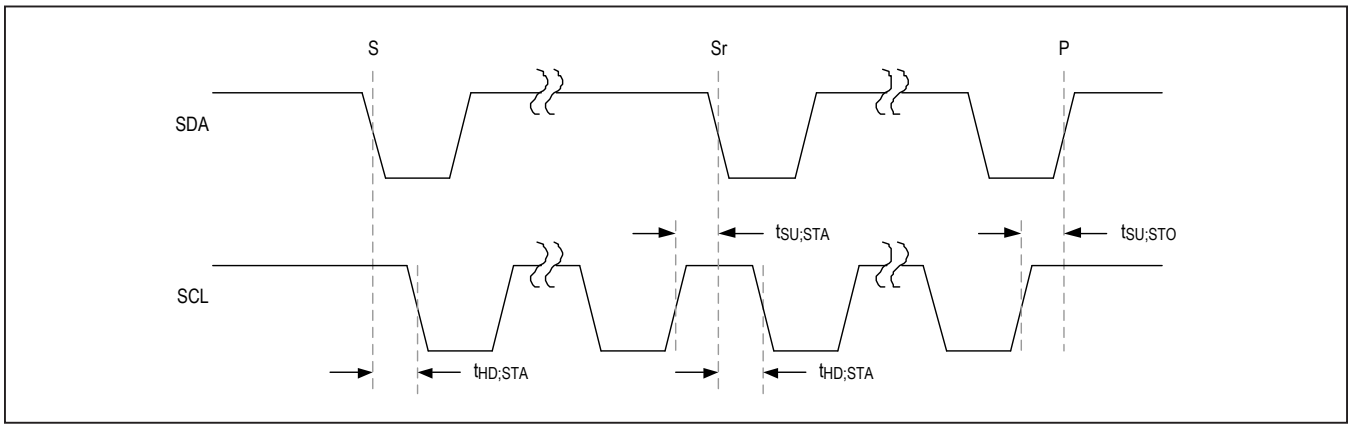


Figure 8. START and STOP Conditions

Slave Address

The I²C slave address of the MAX8971 follows:

Slave Address (7 bit)	**011 0101**
Slave Address (Write)	**0x6A 0110 1010**
Slave Address (Read)	**0x6B 0110 1011**

Clock Stretching

In general, the clock signal generation for I²C bus is the responsibility of the master device. I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX8971 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX8971 does not implement the I²C specification general call address. If the MAX8971 sees the general call address (00000000b), it does not issue an ACKNOWLEDGE (A).

Communication Speed

The MAX8971 provides an I²C-compatible serial interface.

- I²C-compatible serial communications channel
  - 0Hz to 100kHz (standard mode)
  - 0Hz to 400kHz (fast mode)
- Does not utilize I²C clock stretching

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of I²C specification for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors and a 400kHz bus needs about a 1.5kΩ pullup resistors. Note that the pullup resistor is dissipating power when the open-drain bus is LOW. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, see the I²C specification. The major considerations with respect to the MAX8971 are:

- The I²C bus master use current source pullups to shorten the signal rise times.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the MAX8971 inputs filters are set for standard or fast mode. To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in *Communication Protocols* section.

Communication Protocols

The MAX8971 supports both writing and reading from its registers. The following sections show I²C communication protocols.

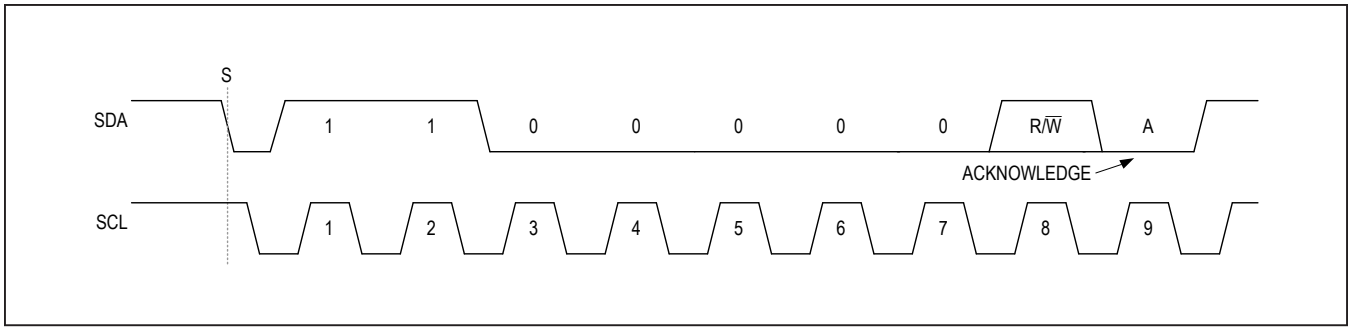


Figure 9. Slave Address Byte Example

Writing to a Single Register

Figure 10 shows the protocol for I²C master device to write one byte of data to the MAX8971. This protocol is the same as SMBus specification's write byte protocol.

The write byte protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

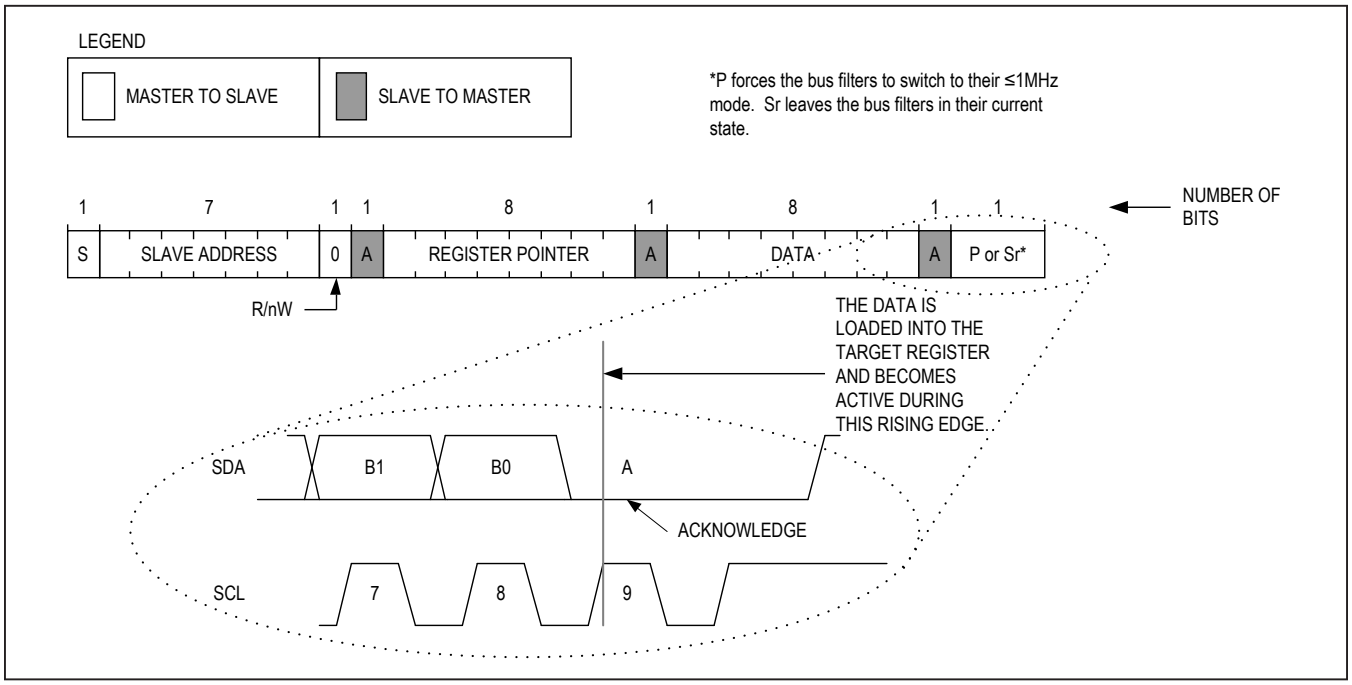


Figure 10. Writing to a Single Register with Write Byte Protocol

Writing to a Sequential Register

Figure 11 shows the protocol for writing to sequential registers. This protocol is similar to the “Write Byte” protocol, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a STOP or REPEATED START.

The writing to sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8) Steps 6 to 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

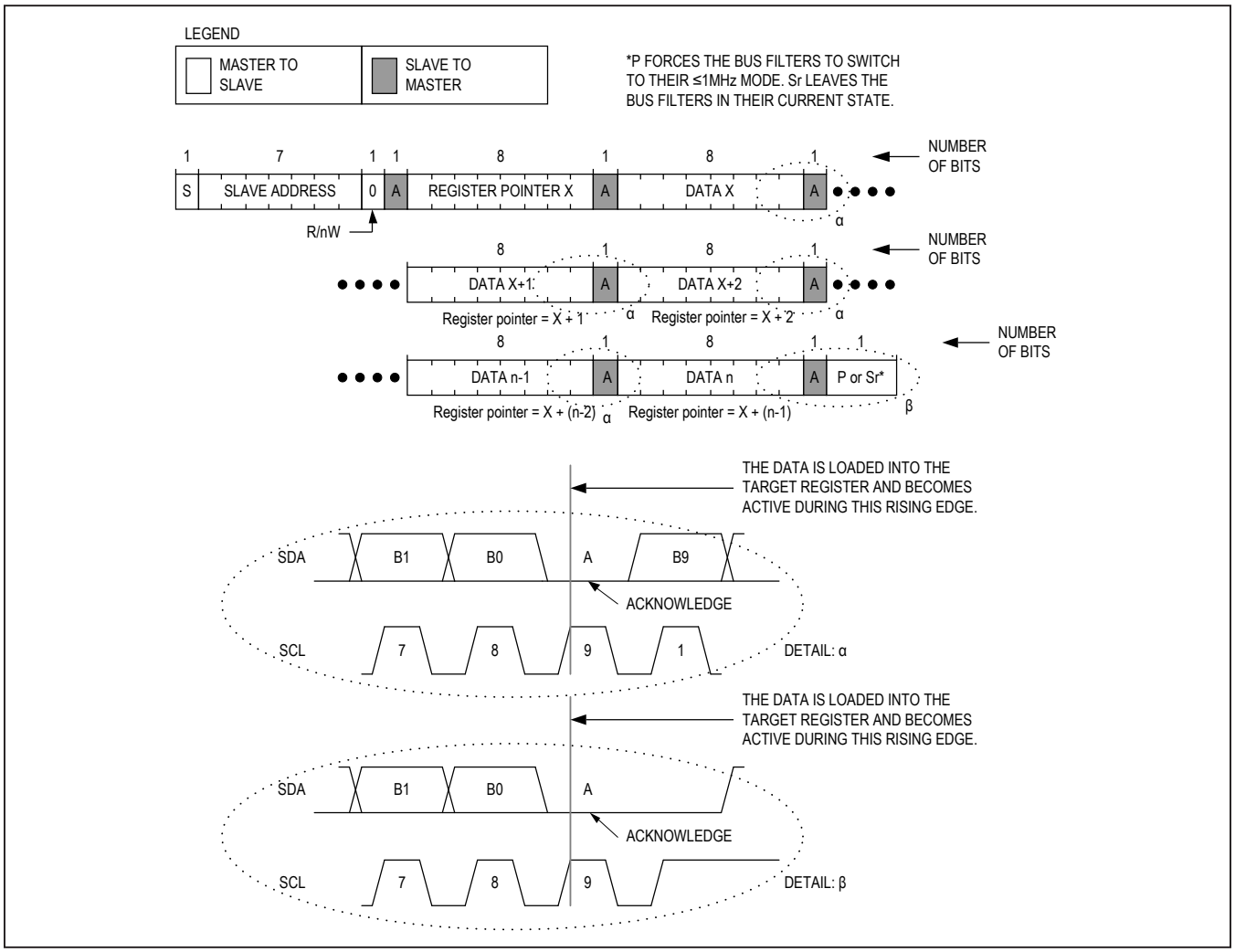


Figure 11. Writing to Sequential Registers x to n

Reading from a Single Register

The I²C master device reads one byte of data to the MAX8971. This protocol is the same as SMBus specification's read byte protocol.

The read byte protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues a NOT-ACKNOWLEDGE (nA).
11) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Reading from a Sequential Register

Figure 12 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data . When the master has all the data it requires, it issues a not-acknowledge (nA) and a STOP (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

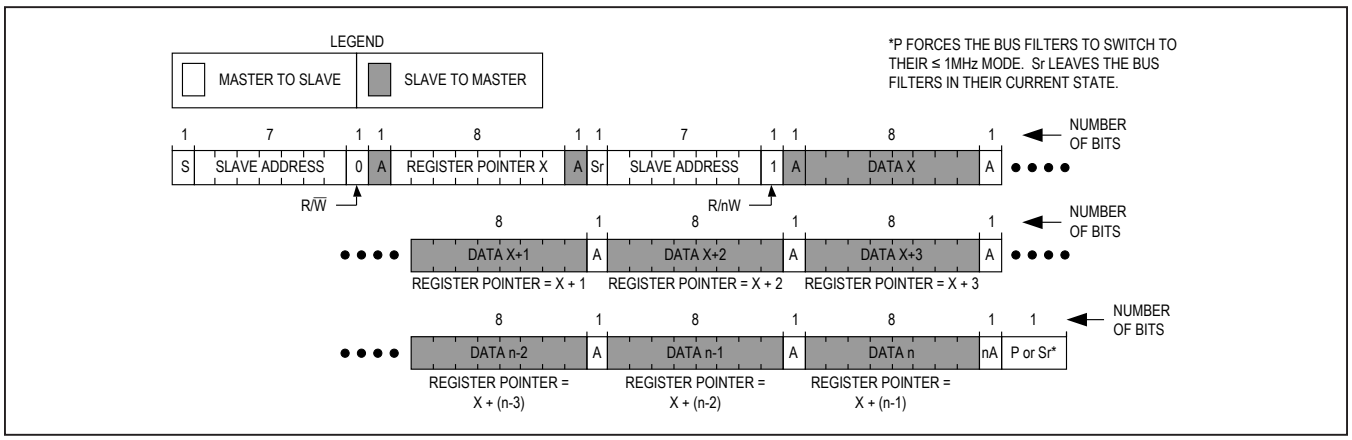


Figure 12. Reading Continuously from Sequential Registers x to n

Table 5. High-Level I²C Register Map

REGISTER NAME	REGISTER ADDRESS	R/W	RESET CONDITION	B7	B6	B5	B4	B3	B2	B1	B0
CHGINT	0x0F	R	VSTBY or rising edge of SFO_POK	AICL_I	TOPOFF	DC_ OVP	DC_ UVP	CHG_I	BAT_I	THM_I	POWERUP
CHGINT_MSK	0x01	R/W	VSTBY or rising edge of SFO_POK	AICL_M	TOPOFF_ M	DC_ OVP_M	DC_ UVP_M	CHG_M	BAT_M	THM_M	—
CHG_STAT	0x02	R	VSTBY or rising edge of SFO_POK	DCV_OK	DCI_OK	DCOVP_ OK	DCUVP_ OK	CHG_OK	BAT_ OK	THM_ OK	—
DETAILS1	0x03	R	VSTBY or rising edge of SFO_POK	DC_V	DC_I	DC_OVP	DC_UVP	RSVD	THM_DTLS[2:0]		
DETAILS2	0x04	R	VSTBY or rising edge of SFO_POK	RSVD	RSVD	BAT_DTLS[1:0]		CHG_DTLS[3:0]			
CHGCNTL1	0x05	R/W	VSTBY or rising edge of SFO_POK	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	DCMON_ DIS	USB_SUS
FCHGCRNT	0x06	R/W	VSTBY or rising edge of SFO_POK	FCHGT[2:0]				CHGCC[3:0]			
DCCRNT	0x07	R/W	VSTBY or rising edge of SFO_POK	RSVD	CHGR STRT	DCILMT[5:0]					
TOPOFF	0x08	R/W	VSTBY or rising edge of SFO_POK	TOFFT[2:0]			IFST2P8	TOFFS[1:0]		CHGCV[1:0]	
TEMPREG	0x09	R/W	VSTBY or rising edge of SFO_POK	REGTEMP[1:0]		RSVD	RSVD	THM_ CNFG	RSVD	RSVD	SAFETY REG
PROTCMD	0x0A	R/W	VSTBY or rising edge of SFO_POK	RSVD	RSVD	RSVD	RSVD	C_PROT[1:0]		RSVD	RSVD

I²C Registers

Charger Interrupt Requests

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	RESET VALUE	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
CHGINT	0x6A	0x0F	0x01	R	Cleared upon read	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME	AICL_I	TOPOFF	DC_OVP	DC_UVP	CHG_I	BAT_I	THM_I	POWERUP

BIT	NAME	BIT DESCRIPTION	DEFAULT
B7	AICL_I	DC Interrupt 0 = The DC status has not changed since the last time this bit was read. 1 = The DC status has changed since the last time this bit was read.	0
B6	TOPOFF	Topoff Interrrupt 0 = The charger topoff status has not changed since the last time this bit was read. 1 = The charger has entered topoff.	0
B5	DC_OVP	DC Overvoltage Interrupt 0 = The DC status has not changed since the last time this bit was read. 1 = The DC status has changed since the last time this bit was read.	0
B4	DC_UVP	DC Undervoltage Interrupt 0 = The DC status has not changed since the last time this bit was read. 1 = The DC status has changed since the last time this bit was read.	0
B3	CHG_I	Charge Current Interrupt 0 = The charger status has not changed since the last time this bit was read. 1 = The charger status has changed since the last time this bit was read.	0
B2	BAT_I	Battery Interrupt 0 = The battery status has not changed since the last time this bit was read. 1 = The battery status has changed since the last time this bit was read.	0
B1	THM_I	Thermistor Interrupt 0 = The THM status has not changed since the last time this bit was read. 1 = The THM status has changed since the last time this bit was read.	0
B0	POWERUP	Power-Up OK Interrupt 0 = The I²C registers have not been reset since the last time this bit was read. 1 = The I²C registers have been reset since the last time this bit was read.	1

Charger Interrupt Masks

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	RESET VALUE	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
CHGINT_MASK	0x6A	0x01	0x00	R/W	N/A	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME	AICL_M	TOPOFF_M	DC_ OVP_M	DC_ UVP_M	CHG_M	BAT_M	THM_M	—

BIT	NAME	BIT DESCRIPTION	DEFAULT
B7	AICL_M	DC Interrupt Mask 0 = unmask 1 = mask	0
B6	TOPOFF_M	Topoff Interrupt Mask 0 = unmask 1 = mask	0
B5	DC_OVP_M	DC Overvoltage Interrupt Mask 0 = unmask 1 = mask	0
B4	DC_UVP_M	DC Undervoltage Interrupt Mask 0 = unmask 1 = mask	0
B3	CHG_M	Charger-Current Interrupt Mask 0 = unmask 1 = mask	0
B2	BAT_M	Battery Interrupt Mask 0 = unmask 1 = mask	0
B1	THM_M	Thermistor Interrupt Mask 0 = unmask 1 = mask	0

Charger Status

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	RESET VALUE	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
CHG_STAT	0x6A	0x02	R	N/A		VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME	DCV_OK	DCI_OK	DCOVP_OK	DCUVP_OK	CHG_OK	BAT_OK	THM_OK	—

BIT	NAME	BIT DESCRIPTION
B7	DCV_OK	Single-Bit DC Input Status Indicator. 1 = The DC input is invalid. DC_V = 1. 0 = The DC input is valid. DC_V = 0.
B6	DCI_OK	1 = DC_I = 1. 0 = DC_I = 0.
B5	DCOVP_OK	1 = The DC input is invalid. 0 = The DC input is valid. DC_OVP = 0.
B4	DCUVP_OK	1 = The DC UVP is invalid. 0 = The DC input is valid. DC_UVP = 1.
B3	CHG_OK	Single-Bit Charger Status Indicator. See CHG_DTLS[3:0] for more information. 1 = The charger has suspended charging. CHG_DTLS[3:0] = 0b0101 or 0b0110 or 0b0111 or 0b1000. 0 = The charger is okay. CHG_DTLS[3:0] ≠ 0b0101 or 0b0110 or 0b0111 or 0b1000.
B2	BAT_OK	Single-Bit Battery Status Indicator. See BAT_DTLS[1:0] for more information. 1 = The battery has an issue and the charger has been suspended. BAT_DTLS[1:0] = 0b01 or 0b11. 0 = The battery is okay. BAT_DTLS[1:0] = 0b10 or 0b00.
B1	THM_OK	Single-Bit Thermistor Status Indicator. See the THM_DTLS[2:0] for more information. 1 = The thermistor temperature is outside of the allowable range for charging. THM_DTLS[2:0] ≠ 0b100 or 0b101. 0 = The thermistor temperature is inside of the allowable range for charging. THM_DTLS[2:0] = 0b100 or 0b101.

DETAILS1

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
DETAILS1	0x6A	0x03	R	N/A	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME	DC_V	DC_I	DC_OVP	DC_UVP	RSVD	THM_DTLS[2:0]		

BIT NAME	DESCRIPTION	DEFAULT
DC_V	DC Details 0b0= V_{DC} is valid, V_{DC} > 4.5V 0b1= V_{DC} is invalid.	Valid
DC_I	DC Details 0b0 = I_{DC} is not limited 0b1 = I_{DC} is limited by input current limit	Valid
DC_OVP	DC Details 0b0 = V_{DC} is valid. V_{DC} < V_{OVP} 0b1 = V_{DC} is invalid. V_{DC} > V_{OVP}	Valid
DC_UVP	DC Details 0b0 = V_{DC} is invalid. V_{DC} < V_{BAT} 0b1 = V_{DC} is valid. V_{DC} > V_{BAT}	Valid
RSVD	Reserved	—
THM_DTLS[2:0]	Thermistor Details 0b001 = Low temperature and charging suspended (cold, < 0°C) 0b010 = Low temperature charging (cool, > 0°C and < 15°C) 0b011 = Standard temperature charging (normal, > 15°C and < 45°C) 0b100 = High temperature charging (warm, > 45°C and < 60°C) 0b101 = High temperature and charging suspended (> 60°C)	Valid

DETAILS2

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
DETAILS2	0x6A	0x04	R	N/A	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME			BAT_DTLS[1:0]		CHG_DTLS[3:0]			

NAME	DESCRIPTION	DEFAULT
BAT_DTLS[1:0]	Battery Details 0b00 = V_{BAT} < 2.1V. This condition is also reported in the CHG_DTLS[3:0] as 0b0000 0b01 = The battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery or something else. Charging has suspended and the charger is in its timer fault mode. This condition is also reported in the CHG_DTLS[3:0] as 0b0110. 0b10 = The battery is OK. 0b11=The battery voltage is greater than the battery overvoltage flag threshold (BATOV), BATOV is set to a percentage above the V_{BATREG} target as programmed by CHGCV. Note that this flag is only generated when there is a valid DC input.	N/A
CHG_ DTLS[3:0]	Charger Details 0b0000 = Charger is in dead-battery region. 0b0001 = Charger is in prequalification mode. 0b0010 = Charger is in fast-charge constant-current mode. 0b0011 = Charger is in fast-charge constant voltage mode. 0b0100 = Charger is in top-off mode. 0b0101 = Charger is in done mode. 0b0110 = Charger is in timer fault mode. 0b0111 = Charger is in temperature suspend mode, see THM_DTLS[2:0]. 0b1000 = Charger is off, DC is invalid and/or charger is disabled. 0b1001 = Charger is in prequalification, fast-charge or top-off modes and is operating with its thermal loop active (i.e., the junction temperature is greater than the value set by REGTEMP[1:0].	N/A

Input Voltage Disable and USB Suspend

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
CHGCNTL1	0x6A	0x05	R/W	N/A	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME							DCMON_DIS	USB_SUS

BIT NAME	BIT DESCRIPTION	DEFAULT
—	—	0
—	—	0
—	—	0
—	—	0
—	—	0
—	—	0
DCMON_DIS	0: enable the monitoring of input voltage by the input power limiter 1: disable the monitoring of input voltage by the input power limiter	0
USB_SUS	0: disable USB suspend mode 1: enable USB suspend mode, low quiescent current standby mode	0

Fast-Charge Current and Timer Control

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
FCHGCRNT	0x6A	0x06	R/W	Protected with CPROT[1:0]	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME	FCHGT[2:0]			CHGCC[4:0]				

BIT	NAME	DESCRIPTION	DEFAULT
B4–B0	CHGCC[4:0]	Fast-Charge Current Selection When the charger is enabled, the charge current limit is set by these bits. These bits range from 250mA to 1.55A in 50mA steps. See Table 6 for a complete listing of codes for CHGCC[4:0]	500mA
B7, B6, B5	FCHGT[2:0]	Fast-Charge Timer Duration (t_{FC}) 0x00 = 0b000 = disable 0x01 = 0b001 = 4hrs 0x02 = 0b010 = 5hrs 0x03 = 0b011 = 6hrs 0x04 = 0b100 = 7hrs 0x05 = 0b101 = 8hrs 0x06 = 0b110 = 9hrs 0x07 = 0b111 = 10hrs	0b010

Table 6. CHGCC[4:0] Decoding

CHGCC[4:0]					CHARGE CURRENT WITH 47mΩ SENSE (mA)
0	0	0	0	0	250
0	0	0	0	1	250
0	0	0	1	0	250
0	0	0	1	1	250
0	0	1	0	0	250
0	0	1	0	1	250
0	0	1	1	0	300
0	0	1	1	1	350
0	1	0	0	0	400
0	1	0	0	1	450
0	1	0	1	0	500
0	1	0	1	1	550
0	1	1	0	0	600
0	1	1	0	1	650
0	1	1	1	0	700
0	1	1	1	1	750

CHGCC[4:0]					CHARGE CURRENT WITH 47mΩ SENSE (mA)
1	0	0	0	0	800
1	0	0	0	1	850
1	0	0	1	0	900
1	0	0	1	1	950
1	0	1	0	0	1000
1	0	1	0	1	1050
1	0	1	1	0	1100
1	0	1	1	1	1150
1	1	0	0	0	1200
1	1	0	0	1	1250
1	1	0	1	0	1300
1	1	0	1	1	1350
1	1	1	0	0	1400
1	1	1	0	1	1450
1	1	1	1	0	1500
1	1	1	1	1	1550

Input-Current Limit and Charger Restart Threshold

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
DCCRNT	0x6A	0x07	R/W	Protected with CPROT[1:0]	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME		CHGRSTRT	DCILMT[5:0]					

NAME	DESCRIPTION	DEFAULT
CHGRSTRT	Fast-Charge Restart Threshold 0b0 = -150mV 0b1 = -100mV	0b0
DCILMT[5:0]	Input-Current Limit Selection When the DC-DC converter is on, the V_{DC} input current limit is set by this register. See Table 7 for a complete listing of the codes for DCILMT[5:0].	500mA

Table 7. DCILMT[5:0] Bit Code

DCILMT[5:0]						TARGET INPUT LIMIT (mA)
0	0	0	0	0	0	100
0	0	0	0	0	1	100
0	0	0	0	1	0	100
0	0	0	0	1	1	100
0	0	0	1	0	0	100
0	0	0	1	0	1	100
0	0	0	1	1	0	100
0	0	0	1	1	1	100
0	0	1	0	0	0	100
0	0	1	0	0	1	100
0	0	1	0	1	0	250
0	0	1	0	1	1	275
0	0	1	1	0	0	300
0	0	1	1	0	1	325
0	0	1	1	1	0	350
0	0	1	1	1	1	375
0	1	0	0	0	0	400
0	1	0	0	0	1	425
0	1	0	0	1	0	450
0	1	0	0	1	1	475
0	1	0	1	0	0	500
0	1	0	1	0	1	525
0	1	0	1	1	0	550
0	1	0	1	1	1	575
0	1	1	0	0	0	600
0	1	1	0	0	1	625
0	1	1	0	1	0	650
0	1	1	0	1	1	675
0	1	1	1	0	0	700
0	1	1	1	0	1	725
0	1	1	1	1	0	750
0	1	1	1	1	1	775
1	0	0	0	0	0	800
1	0	0	0	0	1	825
1	0	0	0	1	0	850
1	0	0	0	1	1	875
1	0	0	1	0	0	900
1	0	0	1	0	1	925
1	0	0	1	1	0	950
1	0	0	1	1	1	975
1	0	1	0	0	0	1000

Table 7. DCILMT[5:0] Bit Code (continued)

DCILMT[5:0]						TARGET INPUT LIMIT (mA)
1	0	1	0	0	1	1025
1	0	1	0	1	0	1050
1	0	1	0	1	1	1075
1	0	1	1	0	0	1100
1	0	1	1	0	1	1125
1	0	1	1	1	0	1150
1	0	1	1	1	1	1175
1	1	0	0	0	0	1200
1	1	0	0	0	1	1225
1	1	0	0	1	0	1250
1	1	0	0	1	1	1275
1	1	0	1	0	0	1300
1	1	0	1	0	1	1325
1	1	0	1	1	0	1350
1	1	0	1	1	1	1375
1	1	1	0	0	0	1400
1	1	1	0	0	1	1425
1	1	1	0	1	0	1450
1	1	1	0	1	1	1475
1	1	1	1	0	0	1500
1	1	1	1	1	1	Disable

Note: *DCILIM threshold is 95% of target.*

Done Current, Timer, GSM Test Mode, and Battery Regulation Voltage

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
TOPOFF	0x6A	0x08	R/W	Protected with CPROT[1:0]	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME	TOFFT[2:0]			IFST2p8	TOFFS[1:0]		CHGCV[1:0]	

NAME	DESCRIPTION	DEFAULT
TOFFT[2:0]	Topoff Timer Setting 0x00 = 0b000 = 0min 0x01 = 0b001 = 10min 0x02 = 0b010 = 20min 0x03 = 0b011 = 30min 0x04 = 0b100 = 40min 0x05 = 0b101 = 50min 0x06 = 0b110 = 60min 0x07 = 0b111 = 70min	0b011
IFST2P8	Scales Maximum Fast-Charge Current to 2.8A This is used as a pulsed customer test mode and the part cannot run 2.8A continuously. 0: disable 1: enable	0b0
TOFFS[1:0]	Topoff Current Threshold Topoff timer starts when ICHG reaches this current setting. 0x0 = 0b00 = 50mA 0x1 = 0b01 = 100mA 0x2 = 0b10 = 150mA 0x3 = 0b11 = 200mA	0b00
CHGCV[1:0]	Charge Termination Voltage Setting 0x00 = 0b00 = 4.2V 0x01 = 0b01 = 4.10V 0x02 = 0b10 = 4.35V 0x03 = 0b11 = 4.15V	0b00

Temperature Regulation

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
TEMPREG	0x6A	0x09	R/W	Protected with CPROT[1:0]	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME	REGTEMP[1:0]		RSVD	—	THM_CNFG	RSVD		SAFETYREG

NAME	BIT DESCRIPTION	DEFAULT
REGTEMP[1:0]	Die-Temperature Thermal Regulation Loop Setpoint 0x0 = 0b00 = 105°C 0x1 = 0b01 = 90°C 0x2 = 0b10 =120°C 0x3 = 0b11 = Disabled	0b00
RSVD	—	—
RSVD	—	—
THM_CNFG	Thermistor Monitor Configuration 0b0 = The thermistor is continuously monitored. 0b1 = The thermistor is not being monitored.	0b0 (MAX8971G) 0b1 (MAX8971)
Reserved	Reserved	NA
Reserved	Reserved	NA
SAFETYREG	JEITA Safety Region Selection 0 = Safety region 1 1 = Safety region 2	0b0

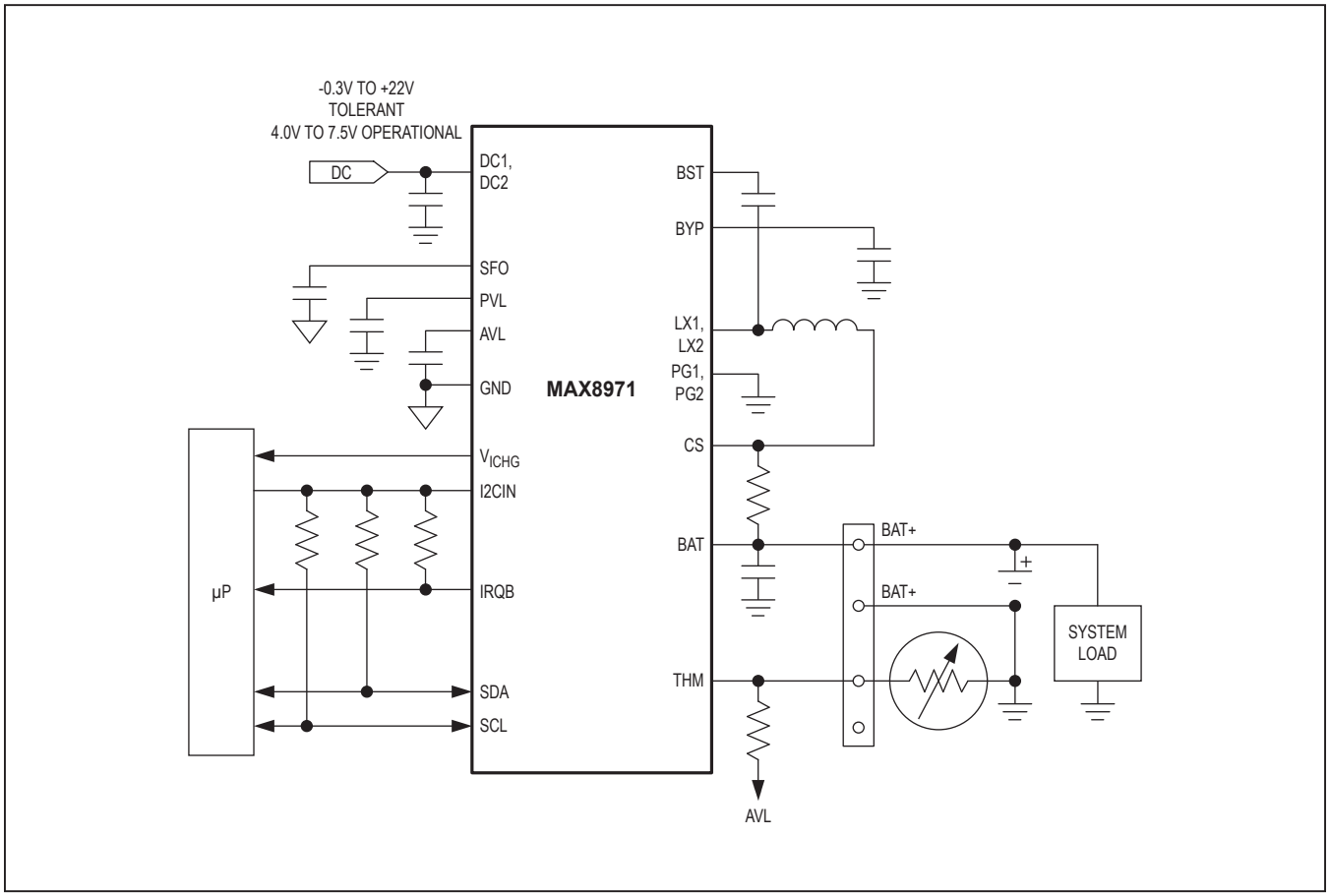
Charger Protection

REGISTER NAME	I²C SLAVE ADDRESS	REGISTER ADDRESS	ACCESS TYPE	SPECIAL FEATURES	RESET CONDITION
PROTCMD	0x6A	0x0A	R/W	N/A	VSTBY INVALID or rising edge of SFO_POK

BITS	B7	B6	B5	B4	B3	B2	B1	B0
NAME	—	—	—	—	CPROT[1:0]		—	—

NAME	DESCRIPTION	DEFAULT
CPROT[1:0]	Charger-Setting Protection Bits Writing 11 to these bits unlocks the settings for the above registers. Writing any value besides 11 locks these registers. 0b00 = locked 0b01 = locked 0b10 = locked 0b11 = unlocked	0b00

Simplified Applications Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	OPTION
MAX8971EWP+	-40°C to +85°C	20 WLP (0.4mm pitch)	Thermistor voltage is not monitored by default (THM_CNFG = 1)
MAX8971EWP+T	-40°C to +85°C	20 WLP (0.4mm pitch)	Thermistor voltage is not monitored by default (THM_CNFG = 1)
MAX8971GEWP+	-40°C to +85°C	20 WLP (0.4mm pitch)	Thermistor voltage is monitored by default (THM_CNFG = 0)
MAX8971GEWP+T	-40°C to +85°C	20 WLP (0.4mm pitch)	Thermistor voltage is monitored by default (THM_CNFG = 0)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel

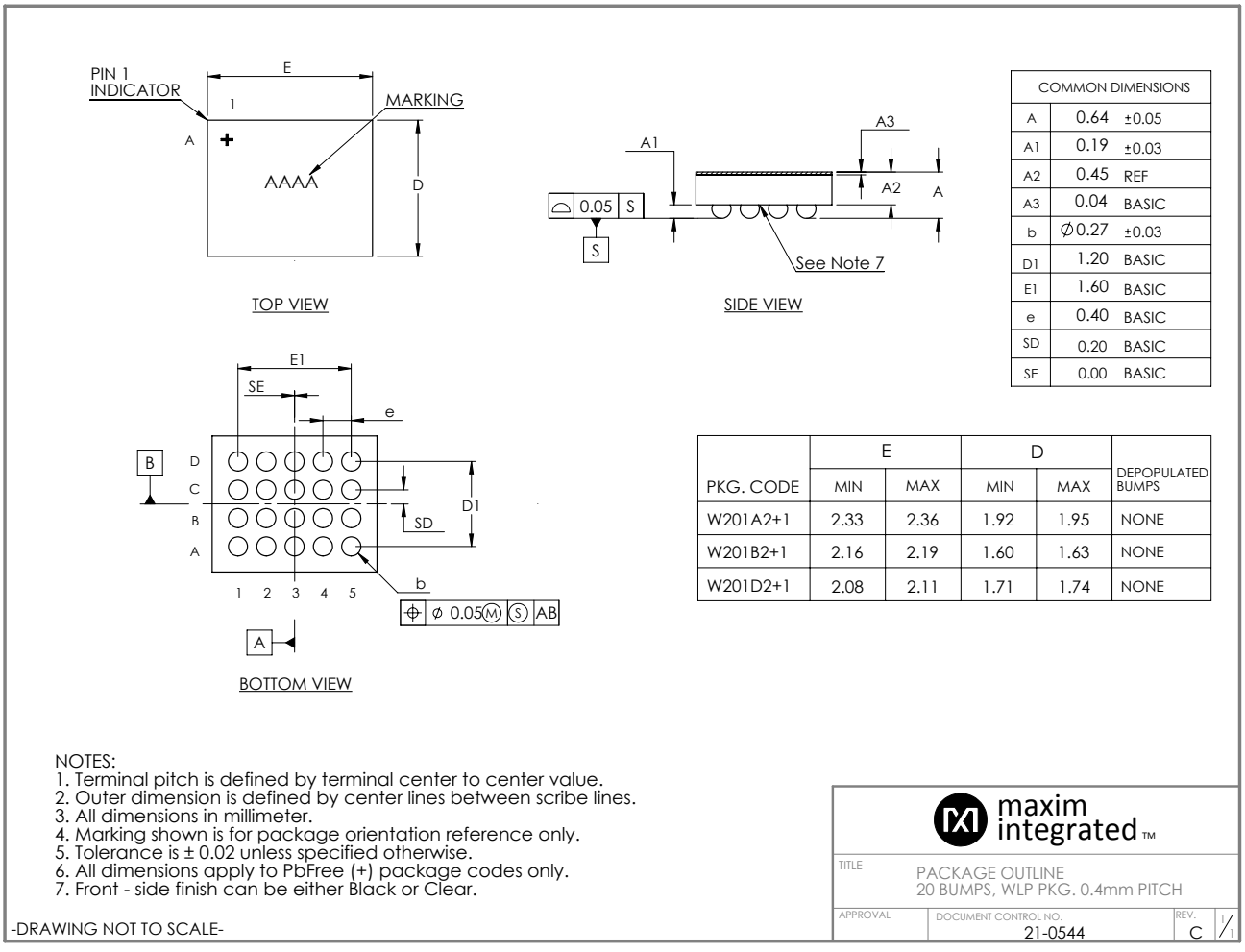
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 WLP	W201B2-1	21-0544	Refer to Application Note 1891



COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.19	±0.03
A2	0.45	REF
A3	0.04	BASIC
b	ø0.27	±0.03
D1	1.20	BASIC
E1	1.60	BASIC
e	0.40	BASIC
SD	0.20	BASIC
SE	0.00	BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W201A2+1	2.33	2.36	1.92	1.95	NONE
W201B2+1	2.16	2.19	1.60	1.63	NONE
W201D2+1	2.08	2.11	1.71	1.74	NONE

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/12	Initial release	—
1	7/17	Updated *General Description*, *Applications*, *Electrical Characteristics* table, TOC 25, TOC 26, *Bump Description*, Figure 1, Equation 1, Table 1, Figure 2, Figure 3, *Fast-Charge Constant-Current State* section, *SAFEOUT* section, *JEITA Description* section, Figure 4, Figure 5, Table 2, Table 5, Charger Status register, DETAILS1 register, DETAILS2 register, Temperature Regulation register, and *Ordering Information*; added *Serial Interface* section, *System Configuration* section, *Bit Transfer* section, *START and STOP Conditions* section, *Acknowledge* section, *Slave Address* section, *Clock Stretching* section, *General Call Address* section, *Communication Speed* section, *Communication Protocols* section, *Writing to a Single Register* section, *Writing to a Sequential Register* section, *Reading from a Single Register* section, and *Reading from a Sequential Register* section	1, 4–6, 13, 15, 17–20, 22–44
2	8/18	Updated *General Description* and *Benefits and Features* sections, replaced TOC25, updated Figure 1, Table 5, descriptions, and *Simplified Applications Circuit*	1, 14, 16, 18, 37, 38, 41, 43

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

