+3V/+5V, 12-Bit, Serial Voltage-Output DACs with Internal Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND .....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
Digital Inputs to DGND.....-0.3V to +6V
Digital Outputs (DOUT, UPO) to DGND.....-0.3V to (V_{DD} + 0.3V)
OUT to AGND.....-0.3V to (V_{DD} + 0.3V)
OS to AGND .....(AGND - 4V) to (V_{DD} + 0.3V)
REF, REFADJ to AGND .....-0.3V to (V_{DD} + 0.3V)

Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.00mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5120 (+5V)

(V_{DD} = +5V ±10%, OS = AGND = DGND = 0V, 33nF capacitor at REFADJ, internal reference, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5120A	-0.5		0.5	LSB
		MAX5120B	-1		1	
Differential Nonlinearity	DNL		-1		1	LSB
Offset Error (Note 2)	V_{OS}		-10		10	mV
Gain Error	GE		-3	-0.2	3	mV
Full-Scale Voltage	V_{FS}	Code = FFF hex, T_A = +25°C	4.0458	4.095	4.1442	V
Full-Scale Temperature Coefficient (Note 3)	TCV_{FS}	MAX5120A		3	10	ppm/°C
		MAX5120B		10	30	
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		20	250	µV/V
REFERENCE						
Output Voltage	V_{REF}	T_A = +25°C		2.5		V
Output Voltage Temperature Coefficient	TCV_{REF}	MAX5120A		3		ppm/°C
		MAX5120B		10		
Reference External Load Regulation	V_{OUT}/I_{OUT}	0 ≤ I_{OUT} ≤ 100µA (sourcing)		0.1	1	µV/µA
Reference Short-Circuit Current				4		mA
REFADJ Current		REFADJ = V_{DD}		3.3	7	µA
DIGITAL INPUT						
Input High Voltage	V_{IH}		3			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}	-1	0.001	1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V

ELECTRICAL CHARACTERISTICS—MAX5120 (+5V) (continued)

(V_{DD} = +5V ±10%, OS = AGND = DGND = 0V, 33nF capacitor at REFADJ, internal reference, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±0.5LSB, V_{STEP} = 4V		20		µs
Output Voltage Swing (Note 4)				0 to V_{DD}		V
OS Input Resistance	R_{OS}		83	121		kΩ
Time Required to Exit Shutdown				2		ms
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{SCLK} = 100kHz, V_{SCLK} = 5Vp-p		5		nV-s
POWER REQUIREMENTS						
Power-Supply Voltage (Note 5)	V_{DD}		4.5		5.5	V
Power-Supply Current (Note 5)	I_{DD}			500	600	µA
Power-Supply Current in Shutdown	I_{SHDN}			3	20	µA

ELECTRICAL CHARACTERISTICS—MAX5121 (+3V)

(V_{DD} = +3V ±10%, OS = AGND = DGND = 0V, 33nF capacitor at REFADJ, internal reference, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5121A	-1		1	LSB
		MAX5121B	-2		2	
Differential Nonlinearity	DNL		-1		1	LSB
Offset Error (Note 2)	V_{OS}		-10		10	mV
Gain Error	GE		-5	-0.2	5	mV
Full-Scale Voltage	V_{FS}	Data = FFF hex, T_A = +25°C	2.0229	2.0475	2.0721	V
Full-Scale Temperature Coefficient (Note 3)	TCV_{FS}	MAX5121A		3	10	ppm/°C
		MAX5121B		10	30	
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{DD} ≤ 3.3V		20	250	µV/V
REFERENCE						
Output Voltage	V_{REF}	T_A = +25°C		1.25		V
Output Voltage Temperature Coefficient	TCV_{REF}	MAX5121A		3		ppm/°C
		MAX5121B		10		
Reference External Load Regulation	V_{OUT}/I_{OUT}	0 ≤ I_{OUT} ≤ 100µA (sourcing)		0.1	1	µV/µA
Reference Short-Circuit Current				4		mA
REFADJ Current		REFADJ = V_{DD}		3.3	7	µA
DIGITAL INPUT						
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			200		mV

ELECTRICAL CHARACTERISTICS—MAX5121 (+3V) (continued)

(V_{DD} = +3V ±10%, OS = AGND = DGND = 0V, 33nF capacitor at REFADJ, internal reference, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}	-1	0.001	1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±0.5LSB, V_{STEP} = 2V		20		µs
Output Voltage Swing (Note 4)				0 to V_{DD}		V
OS Input Resistance	R_{OS}		83	121		kΩ
Time Required to Exit Shutdown				2		ms
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{SCLK} = 100kHz, V_{SCLK} = 3Vp-p		5		nV-s
POWER REQUIREMENTS						
Power-Supply Voltage (Note 5)	V_{DD}		2.7		3.6	V
Power-Supply Current (Note 5)	I_{DD}			500	600	µA
Power-Supply Current in Shutdown	I_{SHDN}			3	20	µA

TIMING CHARACTERISTICS—MAX5120 (+5V)

(V_{DD} = +5V ±10%, OS = AGND = DGND = 0V, 33nF capacitor at REFADJ, internal reference, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
SDI Setup Time	t_{DS}		40			ns
SDI Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay Time	t_{DO1}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay Time	t_{DO2}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay Time	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

TIMING CHARACTERISTICS—MAX5121 (+3V)

(V_{DD} = +3V ±10%, OS = AGND = DGND = 0V, 33nF capacitor at REFADJ, internal reference, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		150			ns
SCLK Pulse Width High	t_{CH}		75			ns
SCLK Pulse Width Low	t_{CL}		75			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		60			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
SDI Setup Time	t_{DS}		60			ns
SDI Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay Time	t_{DO1}	C_{LOAD} = 200pF			200	ns
SCLK Fall to DOUT Valid Propagation Delay Time	t_{DO2}	C_{LOAD} = 200pF			200	ns
SCLK Rise to $\overline{CS}$ Fall Delay Time	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		75			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		150			ns

Note 1: Accuracy is guaranteed as shown in the following table:

V_{DD} (V)	Accuracy Guaranteed	
	From Code:	To Code:
5	10	4095
3	20	4095

Note 2: Offset is measured at the code closest to 10mV.

Note 3: The temperature coefficient is determined by the "box" method in which the maximum ΔV_{OUT} over the temperature range is divided by ΔT.

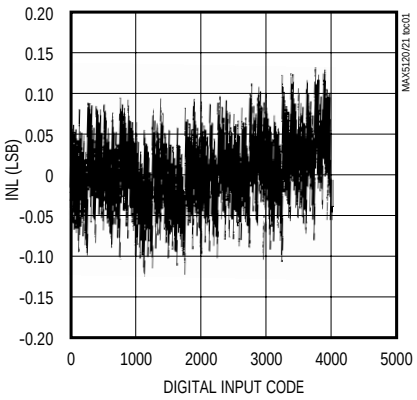
Note 4: Accuracy is better than 1.0LSB for V_{OUT} = 10mV to (V_{DD} - 180mV). Guaranteed by PSR test on end points.

Note 5: R_{LOAD} = ∞ and digital inputs are at either V_{DD} or DGND.

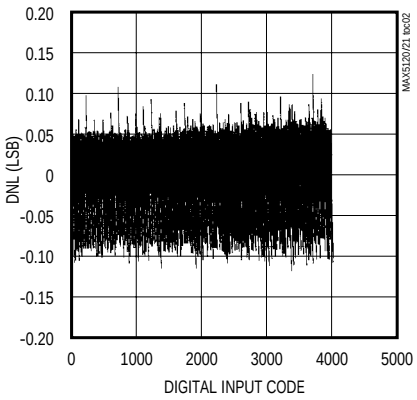
Typical Operating Characteristics

(V_{DD} = +5V (MAX5120), V_{DD} = +3V (MAX5121), R_L = 5kΩ, C_L = 100pF, OS = AGND, T_A = +25°C, unless otherwise noted.)

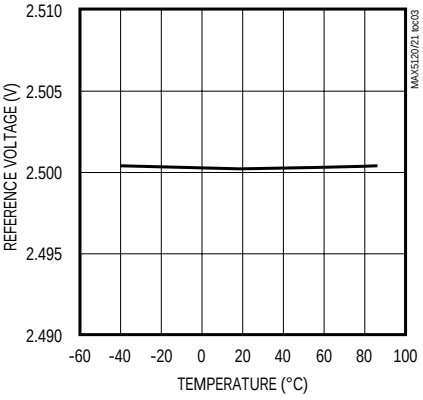
MAX5120
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



MAX5120
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



MAX5120
REFERENCE VOLTAGE vs. TEMPERATURE

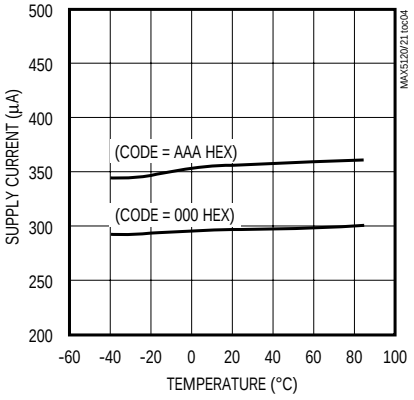


+3V/+5V, 12-Bit, Serial Voltage-Output DACs with Internal Reference

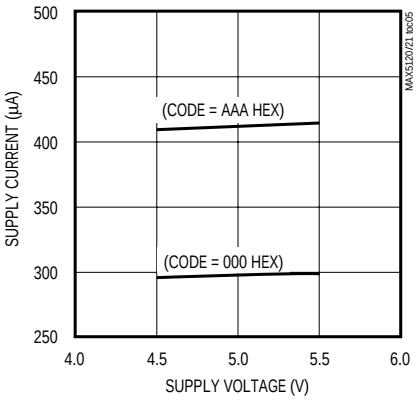
Typical Operating Characteristics (continued)

(V_{DD} = +5V (MAX5120), V_{DD} = +3V (MAX5121), R_L = 5kΩ, C_L = 100pF, OS = AGND, T_A = +25°C, unless otherwise noted.)

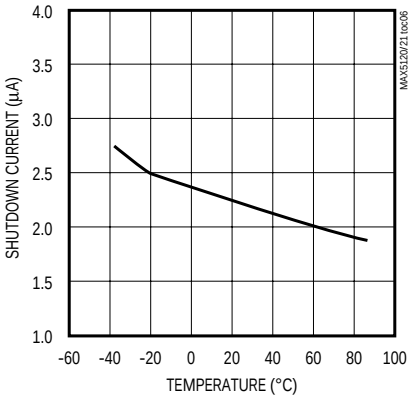
MAX5120
SUPPLY CURRENT vs. TEMPERATURE



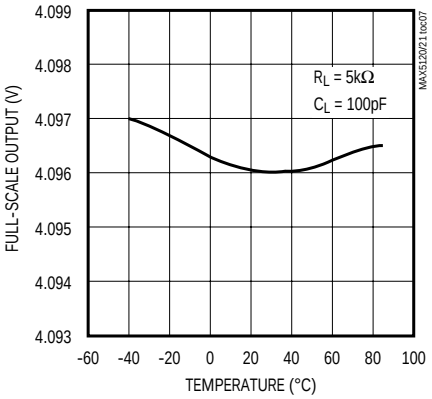
MAX5120
SUPPLY CURRENT vs. SUPPLY VOLTAGE



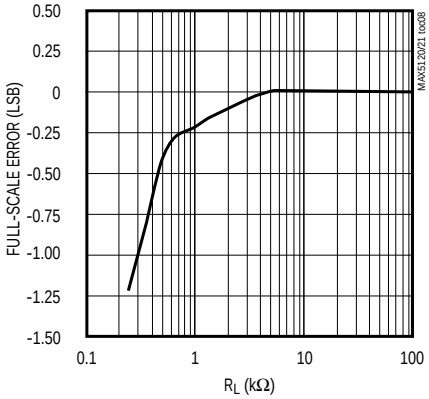
MAX5120
SHUTDOWN CURRENT vs. TEMPERATURE



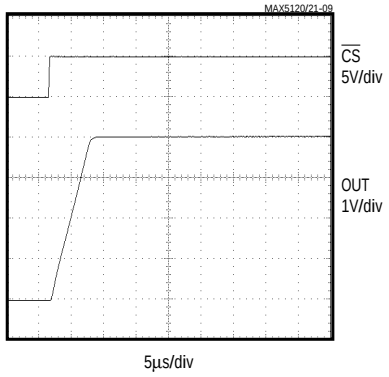
MAX5120
FULL-SCALE OUTPUT vs. TEMPERATURE



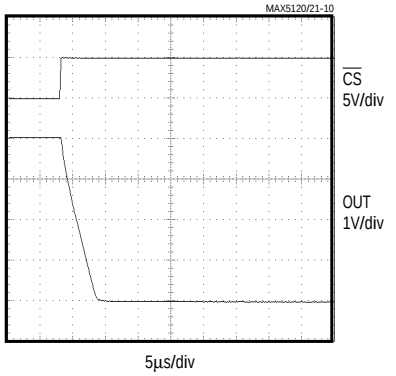
MAX5120
FULL-SCALE ERROR vs. RESISTIVE LOAD



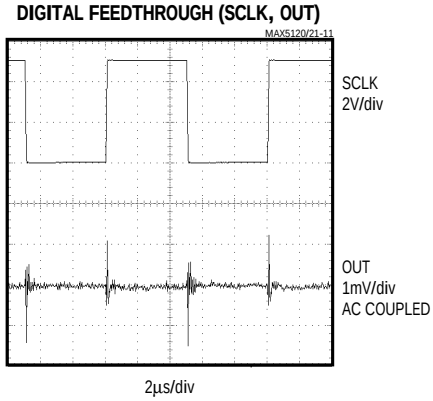
MAX5120
DYNAMIC RESPONSE RISE TIME



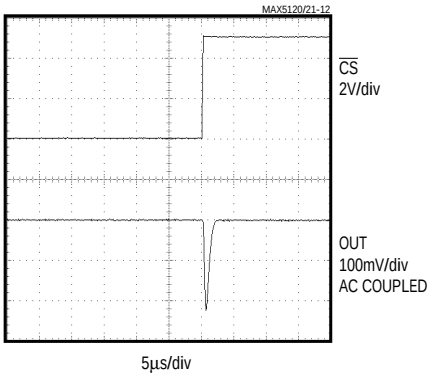
MAX5120
DYNAMIC RESPONSE FALL TIME



MAX5120
DIGITAL FEEDTHROUGH (SCLK, OUT)



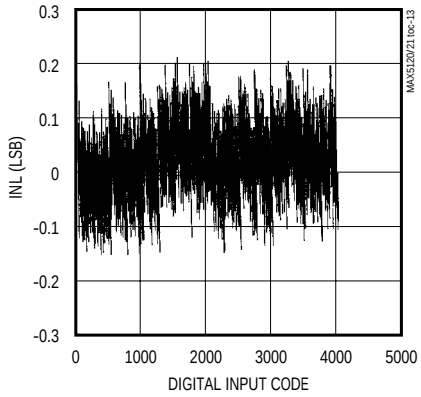
MAX5120
MAJOR CARRY TRANSITION



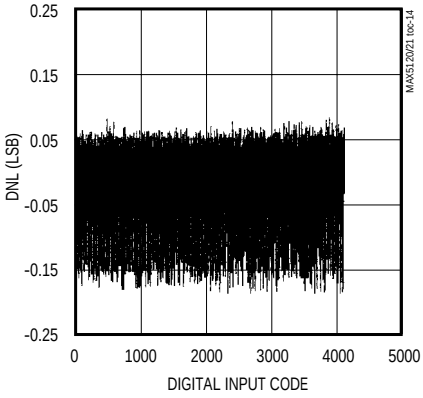
Typical Operating Characteristics (continued)

(V_{DD} = +5V (MAX5120), V_{DD} = +3V (MAX5121), R_L = 5kΩ, C_L = 100pF, OS = AGND, T_A = +25°C, unless otherwise noted.)

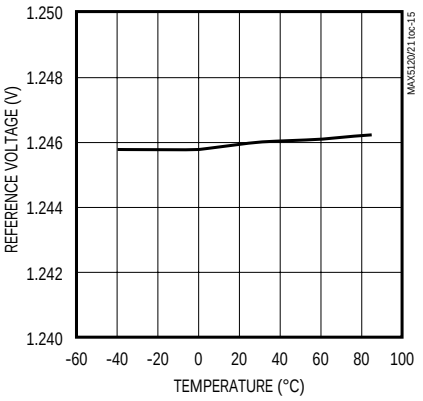
MAX5121
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



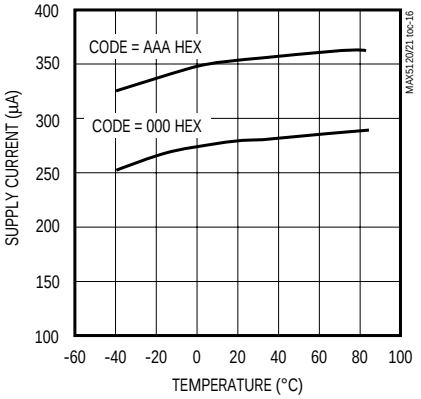
MAX5121
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



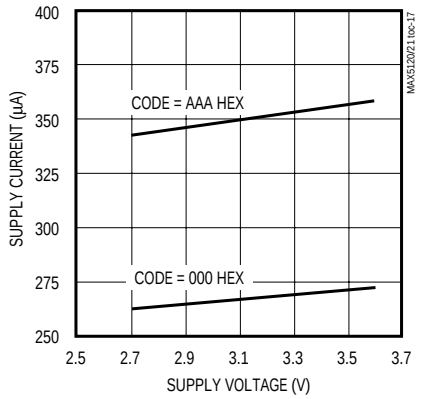
MAX5121
REFERENCE VOLTAGE vs. TEMPERATURE



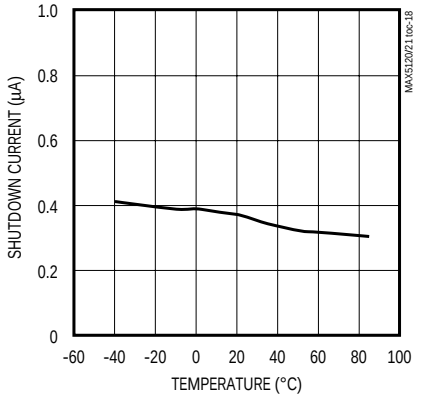
MAX5121
SUPPLY CURRENT vs. TEMPERATURE



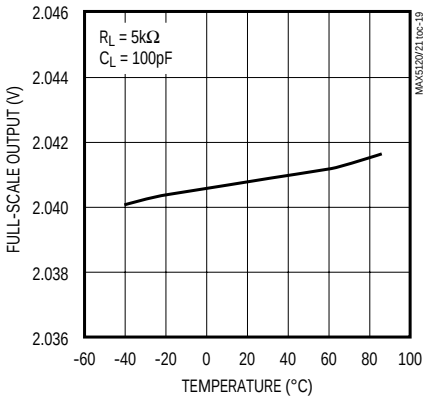
MAX5121
SUPPLY CURRENT vs. SUPPLY VOLTAGE



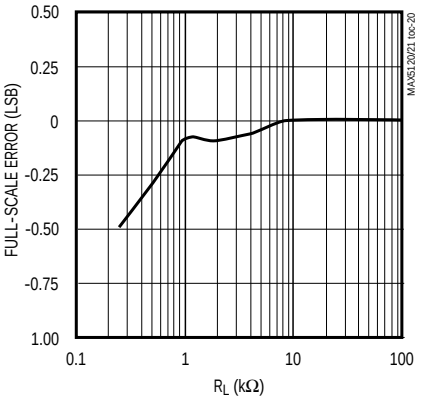
MAX5121
SHUTDOWN CURRENT vs. TEMPERATURE



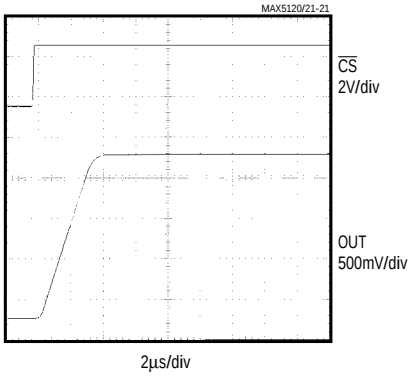
MAX5121
FULL-SCALE OUTPUT vs. TEMPERATURE



MAX5121
FULL-SCALE OUTPUT vs. RESISTIVE LOAD



MAX5121
DYNAMIC RESPONSE RISE TIME

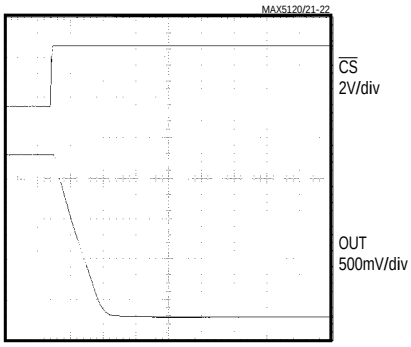


+3V/+5V, 12-Bit, Serial Voltage-Output DACs with Internal Reference

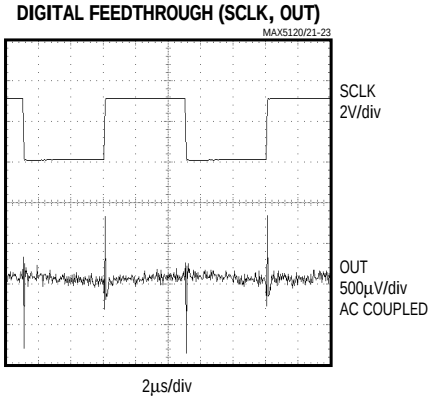
Typical Operating Characteristics (continued)

(V_{DD} = +5V (MAX5120), V_{DD} = +3V (MAX5121), R_L = 5kΩ, C_L = 100pF, OS = AGND, T_A = +25°C, unless otherwise noted.)

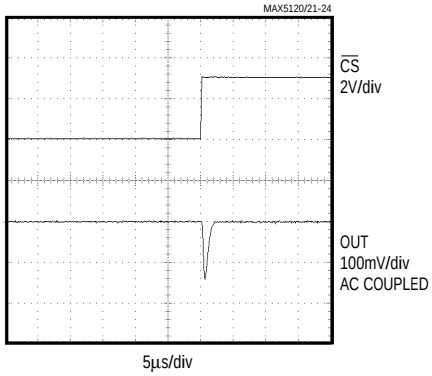
MAX5121
DYNAMIC RESPONSE FALL TIME



MAX5121
DIGITAL FEEDTHROUGH (SCLK, OUT)



MAX5121
MAJOR CARRY TRANSITION



Pin Description

PIN	NAME	FUNCTION
1	OS	Offset Adjust (Analog Input)
2	OUT	Analog Output Voltage. High impedance if part is in shutdown.
3	RSTVAL	Reset Value Input (Digital Input) 1: Tie to V_{DD} to select midscale as the output reset value. 0: Tie to DGND to select 0V as the output reset value.
4	$\overline{PDL}$	Power-Down Lockout (Digital Input) 1: Normal operation. 0: Disallows shutdown (device cannot be powered down).
5	$\overline{CLR}$	Reset DAC Input (Digital Input). Clears the DAC to its predetermined (RSTVAL) output state. Clearing the DAC will cause it to exit a software shutdown state.
6	$\overline{CS}$	Active-Low Chip-Select Input (Digital Input)
7	DIN	Serial Data Input. Data is clocked in on the rising edge of SCLK.
8	SCLK	Serial Clock Input
9	DGND	Digital Ground
10	DOUT	Serial Data Output
11	UPO	User-Programmable Output (Digital Output)
12	PD	Power-Down Input (Digital Input). Pulling PD high when $\overline{PDL}$ = V_{DD} places the IC into shutdown with a maximum shutdown current of 20µA.
13	AGND	Analog Ground
14	REF	Buffered Reference Output/Input. In internal reference mode, the reference buffer provides a +2.5V (MAX5120) or +1.25V (MAX5121) nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal reference by pulling REFADJ to V_{DD} and applying the external reference to REF.
15	REFADJ	Analog Reference Adjust Input. Bypass with a 33nF capacitor to AGND. Connect to V_{DD} when using an external reference.
16	V_{DD}	Positive Power Supply. Bypass with a 0.1µF capacitor in parallel with a 4.7µF capacitor to AGND.

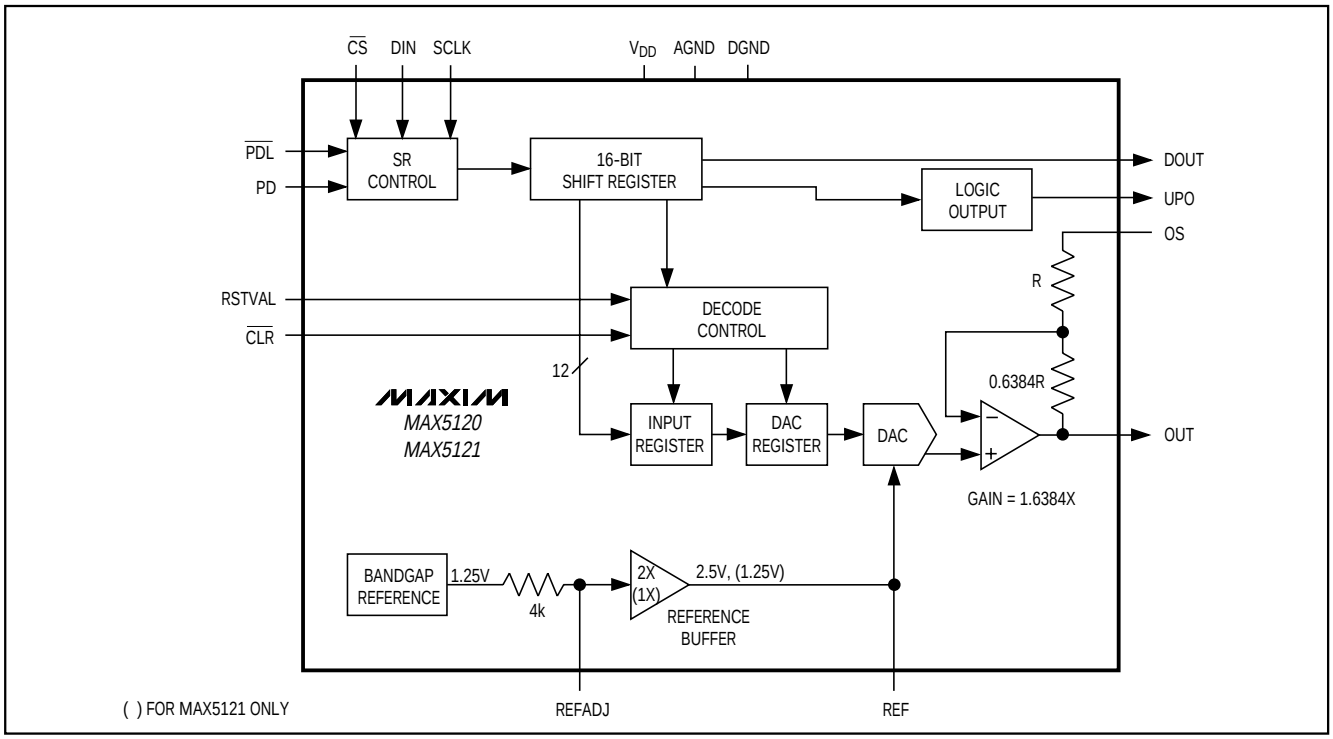


Figure 1. Simplified Functional Diagram

Detailed Description

The MAX5120/MAX5121 12-bit, voltage-output DACs are easily configured with a 3-wire serial interface. They include a 16-bit data-in/data-out shift register and have a double-buffered input consisting of an input register and a DAC register. In addition, these devices employ precision bandgap references and trimmed internal resistors to produce a gain of 1.6384V/V, maximizing the output voltage swing (Figure 1). The MAX5120/MAX5121 output amplifier's offset-adjust pin allows for a DC shift in the DAC outputs. The full-scale output voltage is +4.095V for the MAX5120 and +2.0475V for the MAX5121. These DACs are designed with an inverted R-2R ladder network (Figure 2) that produces a weighted output voltage proportional to the digital input code.

Internal Reference

Both the MAX5120 and MAX5121 use an on-board precision bandgap reference to generate an output voltage of +2.5V (MAX5120) or +1.25V (MAX5121). With a low temperature coefficient of only 10ppm/°C (max), the REF pin can source up to 100µA and may become unstable with capacitive loads exceeding 100pF. REFADJ can be used for minor adjustments (1%) to the reference voltage. Use the circuits shown in Figure 3a

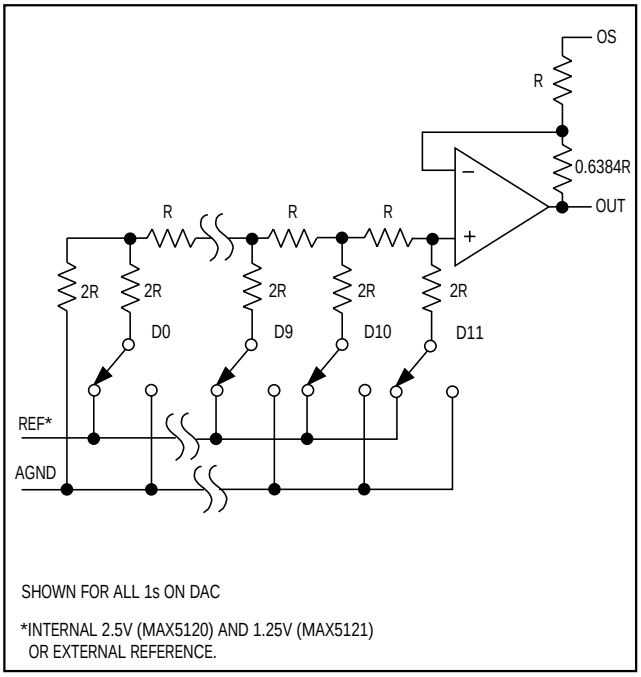


Figure 2. Simplified Inverted R-2R DAC Structure

+3V/+5V, 12-Bit, Serial Voltage-Output DACs with Internal Reference

(MAX5120) and Figure 3b (MAX5121) to achieve these adjustments. Connect a 33nF capacitor from REFADJ to AGND to establish low-noise operation of the DAC. Larger capacitor values may be used, but will result in increased start-up delay. The time constant (τ) for the start-up delay is determined by the REFADJ input impedance of 4kΩ and C_{REFADJ}:

$$\tau = 4k\Omega \cdot C_{REFADJ}$$

External Reference

An external reference may be applied to the REF pin. Disable the internal reference by pulling REFADJ to V_{DD}. This allows an external reference signal (AC- or DC-based) to be fed into the REF pin. For proper operation, **do not** exceed the input voltage range limits of 0V to (V_{DD} - 1.4V) for V_{REF}.

Determine the output voltage using the following equation (REFADJ = V_{DD}; OS = AGND):

$$V_{OUT} = [V_{REF} \cdot (NB / 4096)] \cdot 1.6384V/V$$

where NB is the numeric value of the MAX5120/MAX5121 input code (0 to 4095), V_{REF} is the external reference voltage, and 1.6384V/V is the gain of the internal output amplifier. The REF pin has a minimum input resistance of 40kΩ and is code-dependent.

Output Amplifier

The output amplifier of the MAX5120/MAX5121 employs a trimmed resistor-divider to set a gain of +1.6384V/V and minimize the gain error. With its on-board laser-trimmed +1.25V reference and the output buffer gain, the MAX5121 achieves a full-scale output of +2.0475V, while the MAX5120 provides a +4.095V full-scale output with a +2.5V reference.

The output amplifier has a typical slew rate of 0.6V/µs and settles to ±0.5LSB within 20µs, with a load of 5kΩ in parallel with 100pF. Loads less than 1kΩ may result in degraded performance.

The OS pin may be used to adjust the output offset voltage. For instance, to achieve a +1V offset, apply -1.566V (Offset = -[Output Buffer Gain - 1] · V_{OS}) to OS to produce an output voltage range from +1V to (1V + V_{REF} · 1.6384V/V). Note that the DAC's output range is still limited by the maximum output voltage specification.

Power-Down Mode

The MAX5120/MAX5121 feature software- and hardware-programmable (PD pin) shutdown modes that reduce the typical supply current to 3µA. To enter software shutdown mode, program the control sequence for the DAC as shown in Table 1.

In shutdown mode, the amplifier output becomes high impedance and the serial interface remains active. Data in the input registers is saved, allowing the MAX5120/MAX5121 to recall the output state prior to entering shutdown when returning to normal operation mode. To exit shutdown mode, load both input and DAC registers simultaneously or update the DAC register from the input register. When returning from shutdown mode, wait 2ms for the reference to settle. When using an external reference, the DAC requires only 20µs for the output to stabilize.

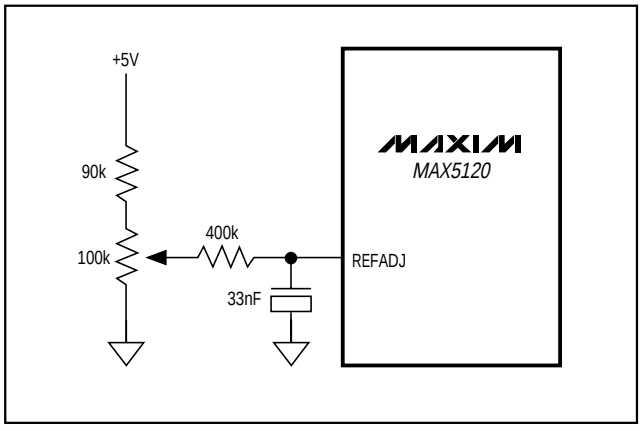


Figure 3a. MAX5120 Reference Adjust Circuit

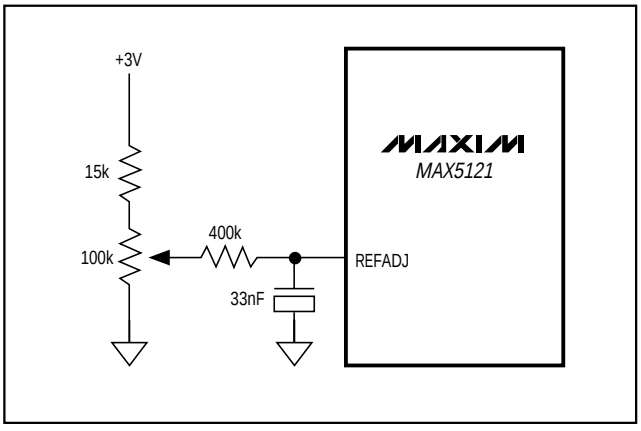


Figure 3b. MAX5121 Reference Adjust Circuit

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
C2	C1	C0	D11 ..... D0	S0*	
0	0	0	XXXXXXXXXXXX	0	No operation.
0	0	1	12-Bit DAC Data	0	Load input register; DAC register unchanged.
0	1	0	12-Bit DAC Data	0	Simultaneously load input and DAC registers; exit shutdown.
0	1	1	XXXXXXXXXXXX	0	Update DAC register from input register; exit shutdown.
1	0	1	XXXXXXXXXXXX	0	Shutdown DAC (provided $\overline{PDL}$ = 1)
1	0	0	XXXXXXXXXXXX	0	UPO goes low (default).
1	1	0	XXXXXXXXXXXX	0	UPO goes high.
1	1	1	1XXXXXXXXXXX	0	Mode 1; DOUT clocked out on SCLK's rising edge.
1	1	1	00XXXXXXXXXX	0	Mode 0; DOUT clocked out on SCLK's falling edge (default).

X = Don't care

** S0 is a sub-bit and is always zero.*

Power-Down Lockout Input ($\overline{PDL}$)

The power-down lockout pin ($\overline{PDL}$) disables shutdown when low. When in shutdown mode, a high-to-low transition on $\overline{PDL}$ will wake up the DAC with its output still set to the state prior to power-down. $\overline{PDL}$ can also be used to wake up the device asynchronously.

Power-Down Input (PD)

Pulling PD high places the MAX5120/MAX5121 in shutdown mode. Pulling PD low will not return the MAX5120/MAX5121 to normal operation. A high-to-low transition on $\overline{PDL}$ or appropriate commands (Table 1) via the serial interface are required to exit power-down.

Serial-Interface Configuration (SPI/QSPI/MICROWIRE/PIC16/PIC17)

The MAX5120/MAX5121 3-wire serial interface is compatible with SPI, QSPI, PIC16/PIC17 (Figure 4) and MICROWIRE (Figure 5) interface standards. The 2-byte-long serial input word contains three control bits, 12 data bits in MSB-first format and one sub-bit, which is always zero (Table 2).

The MAX5120/MAX5121's digital inputs are double buffered, which allows the user to:

- Load the input register without updating the DAC register;
- Update the DAC register with data from the input register;
- Update the input and DAC registers concurrently.

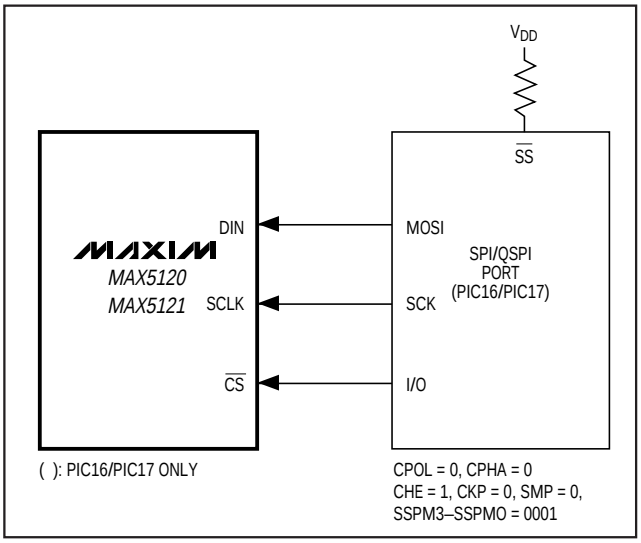


Figure 4. SPI/QSPI Interface Connections (PIC16/PIC17)

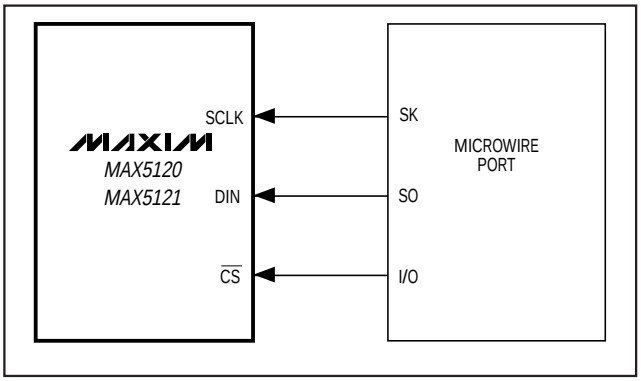


Figure 5. MICROWIRE Interface Connections

+3V/+5V, 12-Bit, Serial Voltage-Output DACs with Internal Reference

The 16-bit input word may be sent in two 1-byte packets (SPI-, MICROWIRE- and PIC16/PIC17-compatible), with $\overline{CS}$ low during this period. The control bits C2, C1, and C0 (Table 1) determine:

- The clock edge on which DOUT is to be clocked out via the serial interface;
- The state of the user-programmable logic output;
- The configuration of the device after shutdown.

The general timing diagram in Figure 6 illustrates how data is acquired. $\overline{CS}$ must be low for the part to receive data. With $\overline{CS}$ low, data at DIN is clocked into the register on the rising edge of SCLK. When $\overline{CS}$ transitions high, data is latched into the input and/or DAC registers, depending on the setting of the three control bits C2, C1, and C0. The maximum serial clock frequency guaranteed for proper operation is 10MHz for the MAX5120 and 6.6MHz for the MAX5121. Figure 7 depicts a more detailed timing diagram of the serial interface.

Table 2. Serial Data Format

MSB ..... LSB		
⇐	16 BITS OF SERIAL DATA	⇒
Control Bits	MSB .... Data Bits ..... LSB	Sub-Bit
C2, C1, C0	D11.....D0	S0

PIC16 with SSP Module and PIC17 Interface

The MAX5120/MAX5121 are compatible with a PIC16/PIC17 controller (µC), using the synchronous serial port (SSP) module. To establish SPI communication connect the controller as shown in Figure 4 and configure the PIC16/PIC17 as system master by initializing its synchronous serial port control register (SSPCON) and synchronous serial port status register (SSPSTAT) to the bit patterns shown in Tables 3 and 4.

In SPI mode, the PIC16/PIC17 µCs allow 8 bits of data to be transmitted synchronously and received simultaneously. Two consecutive 8-bit writings (Figure 6) are necessary to feed the DAC with three control bits and 12 data bits plus one sub-bit. DIN data transitions on the serial clock's falling edge and is clocked into the DAC on SCLK's rising edge. The first 8 bits on DIN contain the 3 control bits (C2, C1, and C0) and the first five data bits (D11–D7). The second 8-bit word contains the remaining bits (D6–D0), and the sub-bit S0.

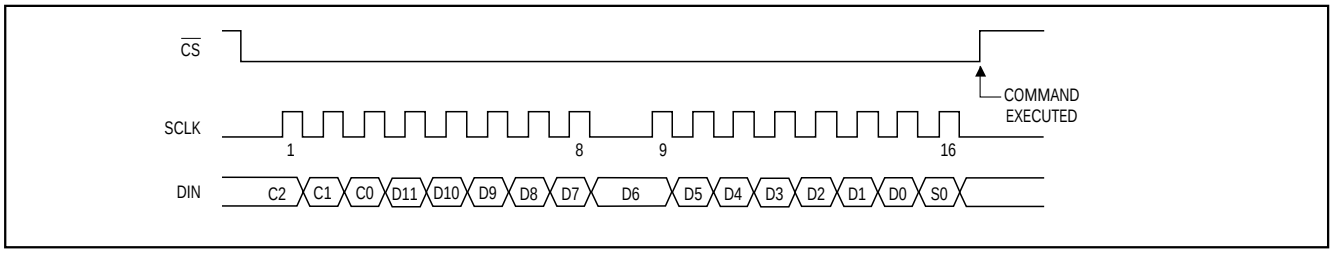


Figure 6. Serial-Interface Timing

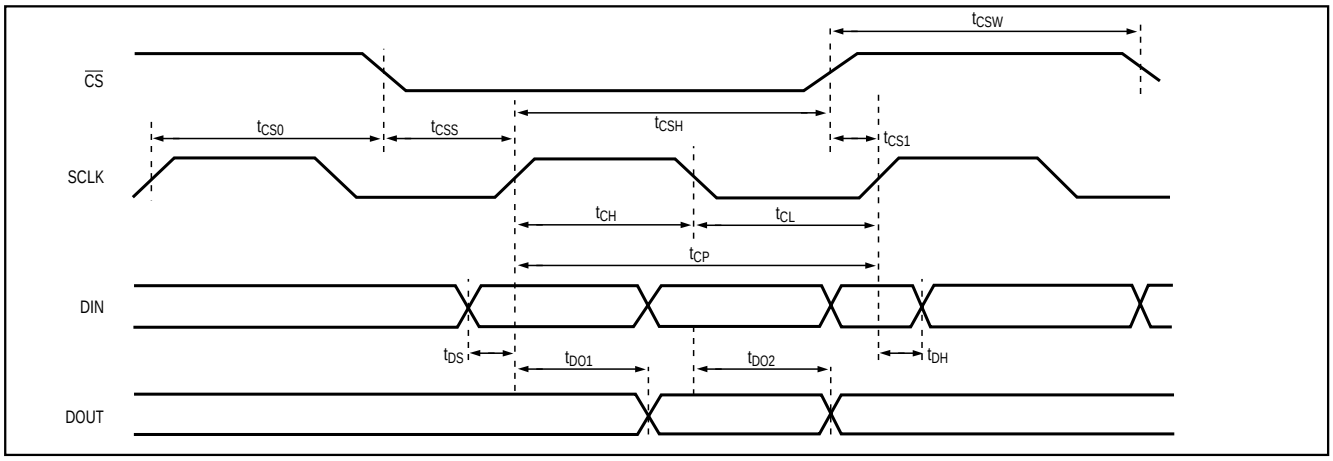


Figure 7. Detailed Serial-Interface Timing

Table 3. Detailed SSPCON Register Contents

CONTROL BIT		MAX5120/MAX5121 SETTINGS	SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPCON)
WCOL	BIT7	X	Write Collision Detection Bit
SSPOV	BIT6	X	Receive Overflow Detection Bit
SSPEN	BIT5	1	Synchronous Serial Port Enable Bit. 0: Disables serial port and configures these pins as I/O port pins. 1: Enables serial port and configures SCK, SDO, and SCI as serial-port pins.
CKP	BIT4	0	Clock Polarity Select Bit. CKP = 0 for SPI master-mode selection.
SSPM3	BIT3	0	Synchronous Serial Port Mode Select Bit. Sets SPI master mode and selects $f_{CLK} = f_{OSC} / 16$.
SSPM2	BIT2	0	
SSPM1	BIT1	0	
SSPM0	BIT0	1	

X = *Don't care*

Table 4. Detailed SSPSTAT Register Contents

CONTROL BIT		MAX5120/MAX5121 SETTINGS	SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPSTAT)
SMP	BIT7	0	SPI Data Input Sample Phase. Input data is sampled at the middle of the data output time.
CKE	BIT6	1	SPI Clock Edge Select Bit. Data will be transmitted on the rising edge of the serial clock.
D/A	BIT5	X	Data Address Bit
P	BIT4	X	Stop Bit
S	BIT3	X	Start Bit
R/W	BIT2	X	Read/Write Bit Information
UA	BIT1	X	Update Address
BF	BIT0	X	Buffer Full Status Bit

X = *Don't care*

Serial Data Output

The contents of the internal shift register are output serially on DOUT, which allows for daisy-chaining (see *Applications Information*) of multiple devices as well as data readback. The MAX5120/MAX5121 may be programmed to shift data out on DOUT on the serial clock's rising edge (Mode 1) or falling edge (Mode 0). The latter is the default during power-up and provides a lag of 16 clock cycles, maintaining SPI, QSPI, MICROWIRE, and PIC16/PIC17 compatibility. In Mode 1, the output data lags DIN by 15.5 clock cycles. During power-down, DOUT retains its last digital state prior to shutdown.

User-Programmable Output (UPO)

The UPO feature allows an external device to be controlled through the serial-interface setup (Table 1), thereby reducing the number of microcontroller I/O ports required. During power-down, this output will retain the last digital state before shutdown. With $\overline{CLR}$ pulled low, UPO will reset to the default state after wake up.

+3V/+5V, 12-Bit, Serial Voltage-Output DACs with Internal Reference

Applications Information

Definitions

Integral Nonlinearity (INL)

Integral nonlinearity (Figure 8a) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every single step.

Differential Nonlinearity (DNL)

Differential nonlinearity (Figure 8b) is the difference between an actual step height and the ideal value of 1LSB. If the magnitude of the DNL is less than 1LSB, the DAC guarantees no missing codes and is monotonic.

Offset Error

The offset error (Figure 8c) is the difference between the ideal and the actual offset point. For a DAC, the offset point is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by trimming.

Gain Error

Gain error (Figure 8d) is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

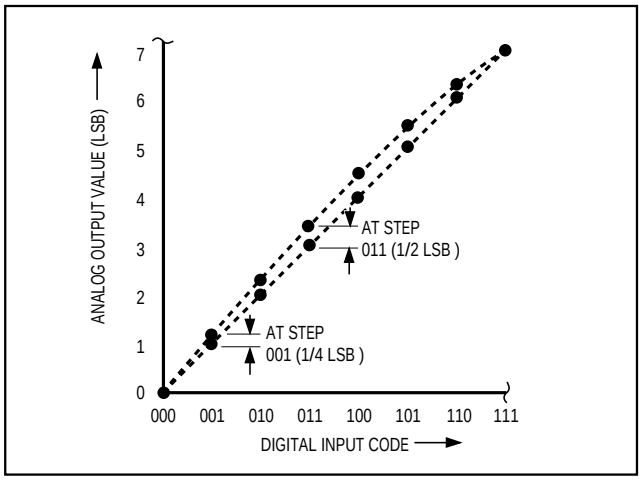


Figure 8a. Integral Nonlinearity

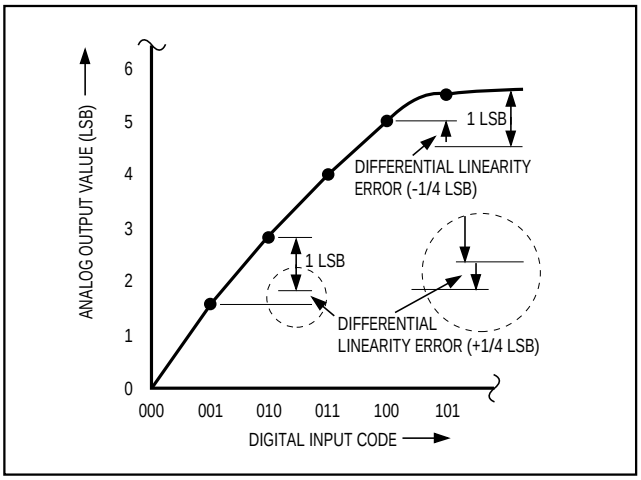


Figure 8b. Differential Nonlinearity

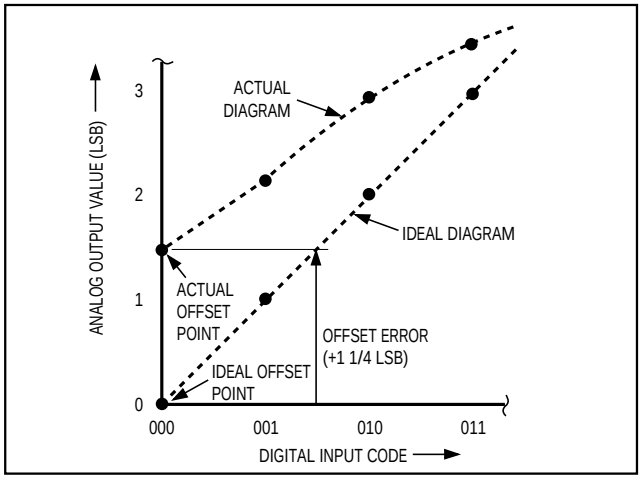


Figure 8c. Offset Error

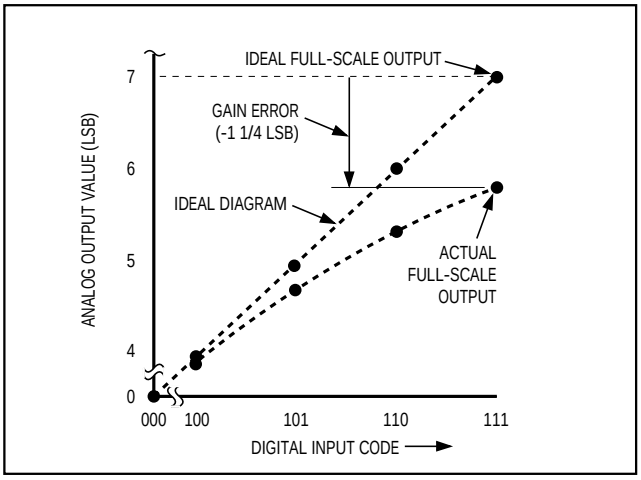


Figure 8d. Gain Error

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles to its new output value within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is noise generated on the DAC's output when any digital input transitions. Proper board layout and grounding will significantly reduce this noise, but there will always be some feedthrough caused by the DAC itself.

Unipolar Output

Figure 9 shows the MAX5120/MAX5121 setup for unipolar, Rail-to-Rail® operation with a gain of 1.6384V/V. With its +2.5V internal reference, the MAX5120 can generate a unipolar output range of 0V to +4.095V. The MAX5121 produces a range of 0V to +2.0475V with its on-board +1.25V reference. Table 5 lists example codes for unipolar output voltages. An offset to the output voltage can be achieved by simply connecting the appropriate voltage to the OS pin, as shown in Figure 10.

Bipolar Output

The MAX5120/MAX5121 can be configured for unity-gain bipolar operation (OS = OUT) using the circuit shown in Figure 11. The output voltage V_{OUT} is thereby given by the following equation:

$$V_{OUT} = V_{REF} \cdot [\{G \cdot (NB / 4096)\} - 1]$$

where NB is the numeric value of the DAC's binary input code, V_{REF} is the voltage of the internal (or external) precision reference, and G is the overall gain. The application circuit in Figure 11 uses a low-cost operational amplifier (MAX4162) external to the MAX5120/MAX5121 in a unity-gain configuration. This provides an overall circuit gain of 2V/V. Table 6 lists example codes for bipolar output voltages.

Reset (RSTVAL) and Clear ($\overline{CLR}$) Functions

The MAX5120/MAX5121 DACs offer a clear pin ($\overline{CLR}$) that resets the output to a certain value, depending upon how RSTVAL is set. RSTVAL = DGND sets the output to 0, and RSTVAL = V_{DD} sets the output to mid-scale when $\overline{CLR}$ is pulled low.

The $\overline{CLR}$ pin has a minimum input resistance of 40kΩ in series with a diode to the supply voltage (V_{DD}). If the digital voltage is higher than the supply voltage for the part, a small input current may flow, but this current will be limited to ($V_{\overline{CLR}}$ - V_{DD} - 0.5V) / 40kΩ.

Note: Clearing the DAC will also cause the part to exit software shutdown (PD = 0).

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

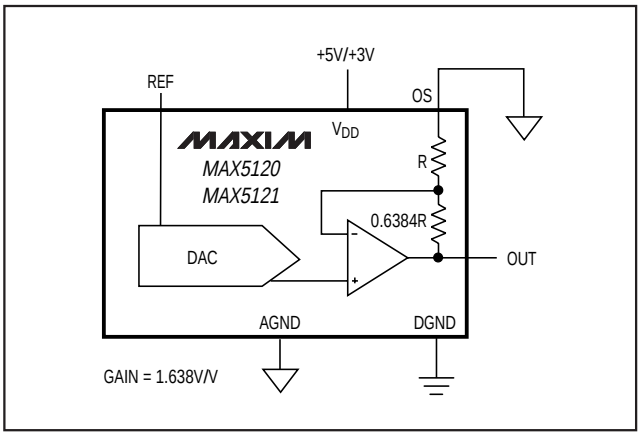


Figure 9. Unipolar Output Circuit (OS = AGND) Using Internal (1.25V/2.5V) or External Reference. With external reference, pull REFADJ to V_{DD}.

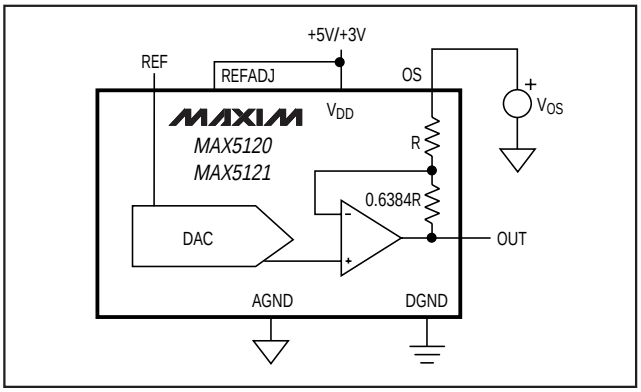


Figure 10. Circuit for Adding Offset to the DAC's Output

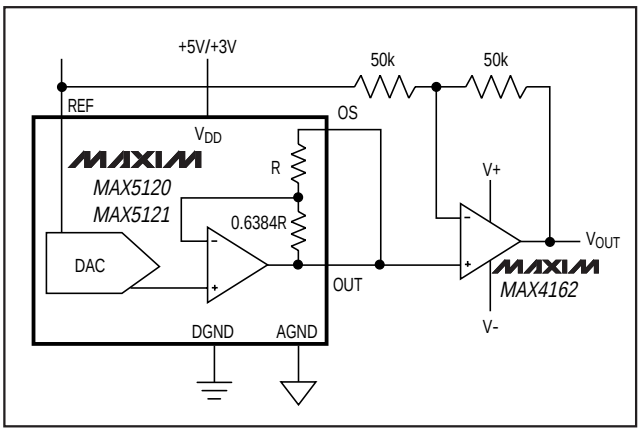


Figure 11. Unity-Gain Bipolar Output Circuit Using Internal (+1.25V/+2.5V) or External Reference. With external reference, pull REFADJ to V_{DD}.

Table 5. Unipolar Code Table (Gain = 1.6384V/V)

DAC CONTENTS		ANALOG OUTPUT		
MSB LSB	SUB-BIT S0	INTERNAL REFERENCE		EXTERNAL REFERENCE
		MAX5120	MAX5121	
1111 1111 1111	0	+4.0950V	+2.0475V	$+V_{REF}$ (4095 / 4096) • 1.6384
1000 0000 0001	0	+2.049V	+1.0245V	$+V_{REF}$ (2049 / 4096) • 1.6384
1000 0000 0000	0	+2.048V	+1.024V	$+V_{REF}$ (2048 / 4096) • 1.6384
0111 1111 1111	0	+2.047V	+1.0235V	$+V_{REF}$ (2047 / 4096) • 1.6384
0000 0000 0001	0	+1mV	+0.5mV	$+V_{REF}$ (1 / 4096) • 1.6384
0000 0000 0000	0	0V	0V	0V

Table 6. Bipolar Code Table for Figure 11

DAC CONTENTS		ANALOG OUTPUT		
MSB LSB	SUB-BIT SO	INTERNAL REFERENCE		EXTERNAL REFERENCE
		MAX5120	MAX5121	
1111 1111 1111	0	+2.49878V	+1.24939V	V_{REF} • [{2 · (4095 / 4096)} - 1]
1000 0000 0001	0	+1.2207mV	+610.35µV	V_{REF} • [{2 · (2049 / 4096)} - 1]
1000 0000 0000	0	0V	0V	V_{REF} • [{2 · (2048 / 4096)} - 1]
0111 1111 1111	0	-1.2207µV	-610.35µV	V_{REF} • [{2 · (2047 / 4096)} - 1]
0000 0000 0001	0	-2.49878V	-1.24939V	V_{REF} • [{2 · (14096)} - 1]
0000 0000 0000	0	-2.5V	-1.25V	$-V_{REF}$

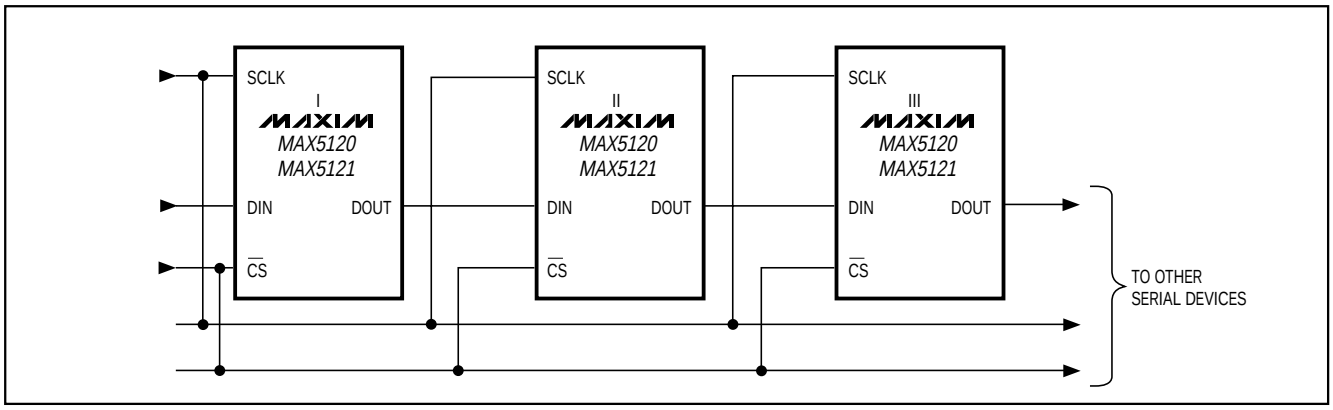


Figure 12. Daisy-Chaining Multiple Devices with the Digital I/Os DIN/DOUT

Daisy-Chaining Devices

Any number of MAX5120/MAX5121s can be daisy-chained simply by connecting the serial data output pin (DOUT) of one device to the digital input pin (DIN) of the following device in the chain (Figure 12).

Another configuration allows several MAX5120/MAX5121 DACs to share one common DIN signal line (Figure 13). In this configuration, the data bus is common to all devices; data is not shifted through a daisy-chain. However, more I/O lines are required in this configuration, because each IC needs a dedicated $\overline{CS}$ line.

Using an External Reference with AC Components

The MAX5120/MAX5121 have multiplying capabilities within the reference input voltage range specifications. Figure 14 shows a technique for applying a sinusoidal input to REF, where the AC signal is offset before being applied to the reference input.

Power-Supply and Bypassing Considerations

On power-up, the input and DAC registers are cleared to either zero (RSTVAL = DGND) or midscale (RSTVAL = V_{DD}). Bypass the power supply with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Minimize lead lengths to reduce lead inductance.

Layout Considerations

Digital and AC transient signals coupling to AGND can create noise at the output. Connect AGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Wire-wrapped boards and sockets are not recommended. If noise becomes an issue, shielding may be required.

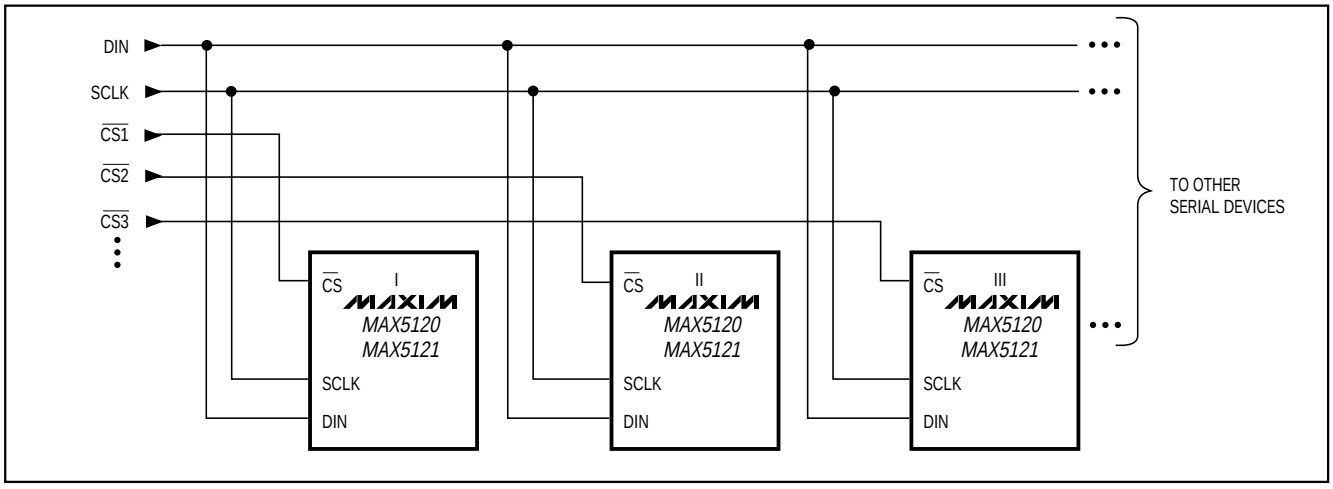


Figure 13. Multiple Devices Share One Common Digital Input (DIN)

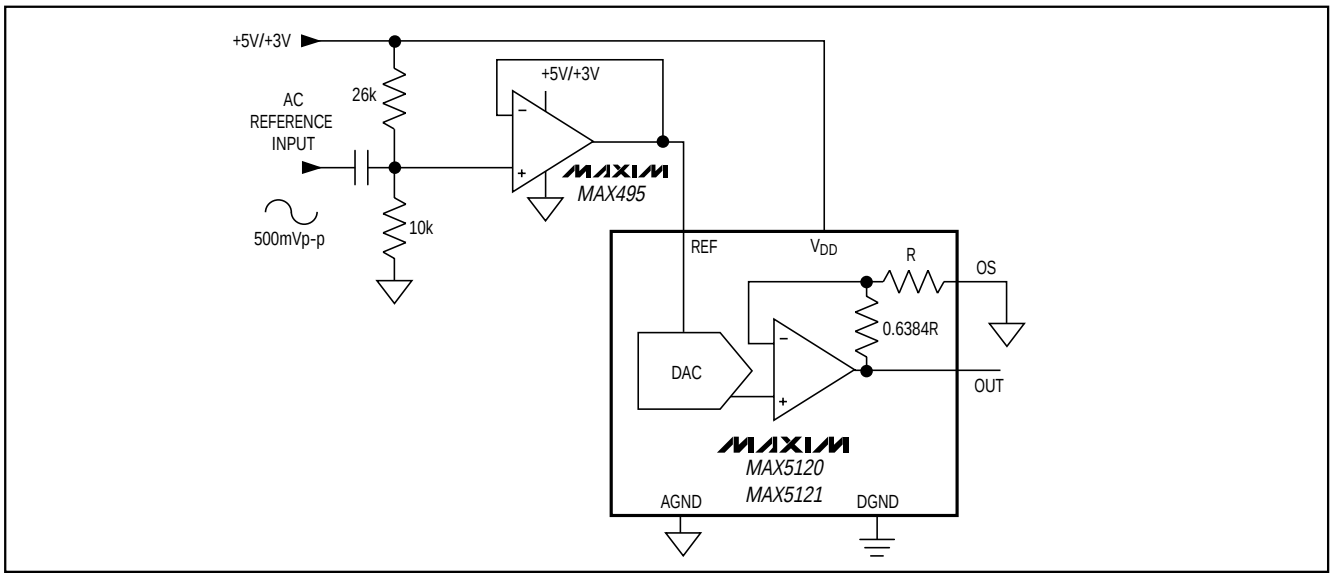


Figure 14. External Reference with AC Components

+3V/+5V, 12-Bit, Serial Voltage-Output DACs with Internal Reference

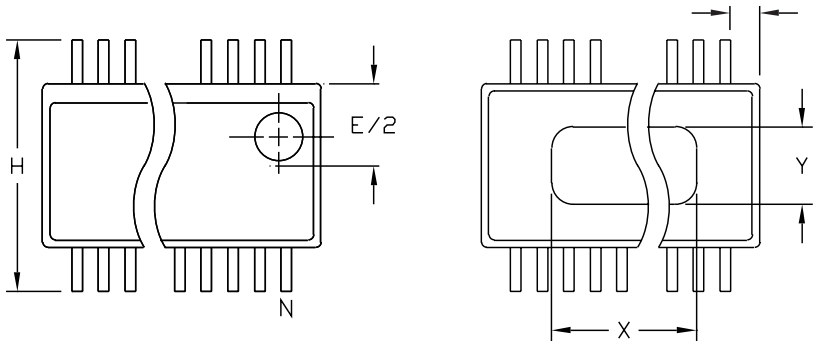
Chip Information

TRANSISTOR COUNT: 3308

SUBSTRATE CONNECTED TO AGND.

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1

NOTES

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