

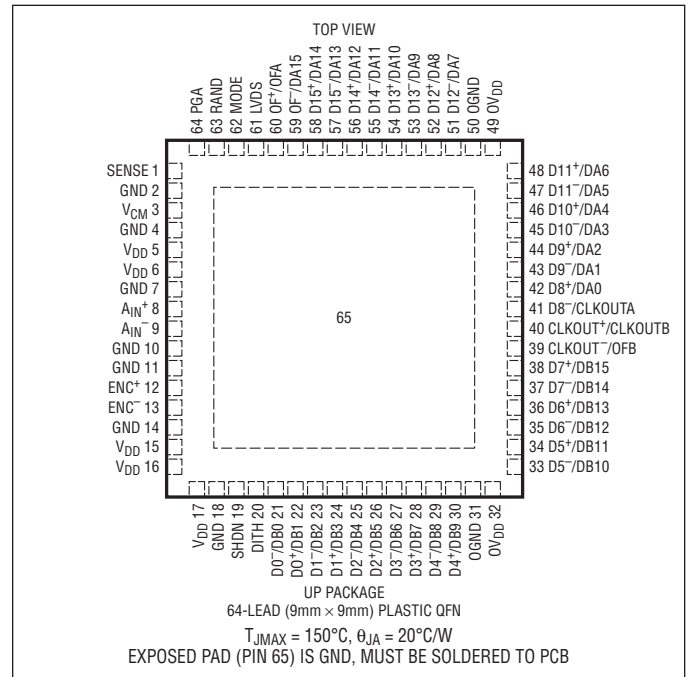
LTC2208

ABSOLUTE MAXIMUM RATINGS

$OV_{DD} = V_{DD}$ (Notes 1 and 2)

Supply Voltage (V_{DD})	–0.3V to 4V
Digital Output Ground Voltage (OGND)	–0.3V to 1V
Analog Input Voltage (Note 3)	–0.3V to ($V_{DD} + 0.3V$)
Digital Input Voltage	–0.3V to ($V_{DD} + 0.3V$)
Digital Output Voltage	–0.3V to ($OV_{DD} + 0.3V$)
Power Dissipation	2000mW
Operating Temperature Range	
LTC2208C	0°C to 70°C
LTC2208I	–40°C to 85°C
Storage Temperature Range	–65°C to 150°C
Digital Output Supply Voltage (OV_{DD})	–0.3V to 4V

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2208CUP#PBF	LTC2208CUP#TRPBF	LTC2208UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2208IUP#PBF	LTC2208IUP#TRPBF	LTC2208UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Integral Linearity Error	Differential Analog Input (Note 5) $T_A = 25^{\circ}C$		±1.2	±4.0	LSB
Integral Linearity Error	Differential Analog Input (Note 5)	●	±1.5	±4.5	LSB
Differential Linearity Error	Differential Analog Input	●	±0.3	±1	LSB
Offset Error	(Note 6)	●	±2	±8.5	mV
Offset Drift			±10		μV/°C
Gain Error	External Reference	●	±0.2	±1.5	%FS
Full-Scale Drift	Internal Reference		±30		ppm/°C
	External Reference		±15		ppm/°C
Transition Noise	External Reference		2.9		LSB _{RMS}

2208fc

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	$3.135V \leq V_{DD} \leq 3.465V$			1.5 or 2.25		V_{P-P}
$V_{IN, CM}$	Analog Input Common Mode	Differential Input (Note 7)	●	1	1.25	1.5	V
I_{IN}	Analog Input Leakage Current	$0V \leq A_{IN}^+, A_{IN}^- \leq V_{DD}$	●	-1		1	μA
I_{SENSE}	SENSE Input Leakage Current	$0V \leq SENSE \leq V_{DD}$	●	-3		3	μA
I_{MODE}	MODE Pin Pull-Down Current to GND				10		μA
I_{LVDS}	LVDS Pin Pull-Down Current to GND				10		μA
C_{IN}	Analog Input Capacitance	Sample Mode $ENC^+ < ENC^-$ Hold Mode $ENC^+ > ENC^-$			6.5 1.8		pF pF
t_{AP}	Sample-and-Hold Acquisition Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				70		fs RMS
CMRR	Analog Input Common Mode Rejection Ratio	$1V < (A_{IN}^+ = A_{IN}^-) < 1.5V$			80		dB
BW-3dB	Full Power Bandwidth	$R_S < 25\Omega$			700		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $A_{IN} = -1\text{dBFS}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input (2.25V Range, PGA = 0)			77.7		dBFS
		5MHz Input (1.5V Range, PGA = 1)			75.3		dBFS
		30MHz Input (2.25V Range, PGA = 0) $T_A = 25^\circ\text{C}$		76.5	77.6		dBFS
		30MHz Input (2.25V Range, PGA = 0)	●	76.1	77.3		dBFS
		30MHz Input (1.5V Range, PGA = 1)			75.2		dBFS
		70MHz Input (2.25V Range, PGA = 0)			77.5		dBFS
		70MHz Input (1.5V Range, PGA = 1)			75.1		dBFS
		140MHz Input (2.25V Range, PGA = 0)			76.9		dBFS
		140MHz Input (1.5V Range, PGA = 1) $T_A = 25^\circ\text{C}$		73.8	74.8		dBFS
		140MHz Input (1.5V Range, PGA = 1)	●	73.4	74.5		dBFS
SFDR	Spurious Free Dynamic Range 2 nd or 3 rd Harmonic	250MHz Input (2.25V Range, PGA = 0)			75.4		dBFS
		250MHz Input (1.5V Range, PGA = 1)			73.8		dBFS
		5MHz Input (2.25V Range, PGA = 0)			100		dBc
		5MHz Input (1.5V Range, PGA = 1)			100		dBc
		30MHz Input (2.25V Range, PGA = 0) $T_A = 25^\circ\text{C}$		88	95		dBc
		30MHz Input (2.25V Range, PGA = 0)	●	87	94		dBc
		30MHz Input (1.5V Range, PGA = 1)			100		dBc
		70MHz Input (2.25V Range, PGA = 0)			90		dBc
		70MHz Input (1.5V Range, PGA = 1)			95		dBc
		140MHz Input (2.25V Range, PGA = 0)			85		dBc
		140MHz Input (1.5V Range, PGA = 1) $T_A = 25^\circ\text{C}$		86	90		dBc
		140MHz Input (1.5V Range, PGA = 1)	●	84	89		dBc
		250MHz Input (2.25V Range, PGA = 0)			78		dBc
		250MHz Input (1.5V Range, PGA = 1)			83		dBc

DYNAMIC ACCURACY The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $A_{IN} = -1\text{dBFS}$ unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SFDR	Spurious Free Dynamic Range 4 th Harmonic or Higher	5MHz Input (2.25V Range, PGA = 0)		100		dBc
		5MHz Input (1.5V Range, PGA = 1)		100		dBc
		30MHz Input (2.25V Range, PGA = 0)	● 90	100		dBc
		30MHz Input (1.5V Range, PGA = 1)		100		dBc
		70MHz Input (2.25V Range, PGA = 0)		100		dBc
		70MHz Input (1.5V Range, PGA = 1)		100		dBc
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	140MHz Input (2.25V Range, PGA = 0)		95		dBc
		140MHz Input (1.5V Range, PGA = 1)	● 88	95		dBc
		250MHz Input (2.25V Range, PGA = 0)		90		dBc
		250MHz Input (1.5V Range, PGA = 1)		90		dBc
		5MHz Input (2.25V Range, PGA = 0)		77.7		dBFS
		5MHz Input (1.5V Range, PGA = 1)		75.3		dBFS
SFDR	Spurious Free Dynamic Range at -25dBFS Dither "OFF"	30MHz Input (2.25V Range, PGA = 0) $T_A = 25^\circ\text{C}$	● 76.3	77.5		dBFS
		30MHz Input (2.25V Range, PGA = 0)		77.5		dBFS
		30MHz Input (1.5V Range, PGA = 1)		75.2		dBFS
		70MHz Input (2.25V Range, PGA = 0)		77.4		dBFS
		70MHz Input (1.5V Range, PGA = 1)		75		dBFS
		140MHz Input (2.25V Range, PGA = 0)		76.4		dBFS
SFDR	Spurious Free Dynamic Range at -25dBFS Dither "ON"	140MHz Input (1.5V Range, PGA = 1) $T_A = 25^\circ\text{C}$	● 73.6	74.5		dBFS
		140MHz Input (1.5V Range, PGA = 1)		74.5		dBFS
		250MHz Input (2.25V Range, PGA = 0)		73.6		dBFS
		250MHz Input (1.5V Range, PGA = 1)		72.9		dBFS
		5MHz Input (2.25V Range, PGA = 0)		105		dBFS
		5MHz Input (1.5V Range, PGA = 1)		105		dBFS
SFDR	Spurious Free Dynamic Range at -25dBFS Dither "ON"	30MHz Input (2.25V Range, PGA = 0)		105		dBFS
		30MHz Input (1.5V Range, PGA = 1)		105		dBFS
		70MHz Input (2.25V Range, PGA = 0)		105		dBFS
		70MHz Input (1.5V Range, PGA = 1)		105		dBFS
		140MHz Input (2.25V Range, PGA = 0)		100		dBFS
		140MHz Input (1.5V Range, PGA = 1)		100		dBFS
SFDR	Spurious Free Dynamic Range at -25dBFS Dither "ON"	250MHz Input (2.25V Range, PGA = 0)		100		dBFS
		250MHz Input (1.5V Range, PGA = 1)		100		dBFS
		5MHz Input (2.25V Range, PGA = 0)		115		dBFS
		5MHz Input (1.5V Range, PGA = 1)		115		dBFS
		30MHz Input (2.25V Range, PGA = 0)	● 100	115		dBFS
		30MHz Input (1.5V Range, PGA = 1)		115		dBFS
SFDR	Spurious Free Dynamic Range at -25dBFS Dither "ON"	70MHz Input (2.25V Range, PGA = 0)		115		dBFS
		70MHz Input (1.5V Range, PGA = 1)		115		dBFS
		140MHz Input (2.25V Range, PGA = 0)		110		dBFS
		140MHz Input (1.5V Range, PGA = 1)		110		dBFS
		250MHz Input (2.25V Range, PGA = 0)		105		dBFS
		250MHz Input (1.5V Range, PGA = 1)		105		dBFS

COMMON MODE BIAS CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	$I_{OUT} = 0$	1.15	1.25	1.35	V
V_{CM} Output Tempco	$I_{OUT} = 0$		+40		ppm/ $^\circ\text{C}$
V_{CM} Line Regulation	$3.135\text{V} \leq V_{DD} \leq 3.465\text{V}$		1		mV/V
V_{CM} Output Resistance	$1\text{mA} \leq I_{OUT} \leq 1\text{mA}$		2		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
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ENCODE INPUTS (ENC^+ , ENC^-)

V_{ID}	Differential Input Voltage	(Note 7)	●	0.2		V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 7)		1.2	1.6 3.0	V V
R_{IN}	Input Resistance	(See Figure 2)		6		k Ω
C_{IN}	Input Capacitance	(Note 7)		3		pF

LOGIC INPUTS ($DITH$, PGA , $SHDN$, $RAND$)

V_{IH}	High Level Input Voltage	$V_{DD} = 3.3\text{V}$	●	2		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 3.3\text{V}$	●		0.8	V
I_{IN}	Digital Input Current	$V_{IN} = 0\text{V}$ to V_{DD}	●		± 10	μA
C_{IN}	Digital Input Capacitance	(Note 7)		1.5		pF

LOGIC OUTPUTS (CMOS MODE)

$OV_{DD} = 3.3\text{V}$

V_{OH}	High Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = -10\mu\text{A}$ $I_O = -200\mu\text{A}$	●	3.1	3.299 3.29	V V
V_{OL}	Low Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = 160\mu\text{A}$ $I_O = 1.6\text{mA}$	●		0.01 0.10	V V
I_{SOURCE}	Output Source Current	$V_{OUT} = 0\text{V}$				-50	mA
I_{SINK}	Output Sink Current	$V_{OUT} = 3.3\text{V}$				50	mA

$OV_{DD} = 2.5\text{V}$

V_{OH}	High Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = -200\mu\text{A}$			2.49	V
V_{OL}	Low Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = 1.60\text{mA}$			0.1	V

$OV_{DD} = 1.8\text{V}$

V_{OH}	High Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = -200\mu\text{A}$			1.79	V
V_{OL}	Low Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = 1.60\text{mA}$			0.1	V

LOGIC OUTPUTS (LVDS MODE)

STANDARD LVDS

V_{OD}	Differential Output Voltage	100 Ω Differential Load	●	247	350	454	mV
V_{OS}	Output Common Mode Voltage	100 Ω Differential Load	●	1.125	1.2	1.375	V

LOW POWER LVDS

V_{OD}	Differential Output Voltage	100 Ω Differential Load	●	125	175	250	mV
V_{OS}	Output Common Mode Voltage	100 Ω Differential Load	●	1.125	1.2	1.375	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $A_{IN} = -1\text{dBFS}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 8)	●	3.135	3.3	3.465	V
P_{SHDN}	Shutdown Power	$SHDN = V_{DD}$			0.2		mW

STANDARD LVDS OUTPUT MODE

OV_{DD}	Output Supply Voltage	(Note 8)	●	3	3.3	3.6	V
I_{VDD}	Analog Supply Current		●		380	450	mA
I_{OVDD}	Output Supply Current		●		74	90	mA
P_{DIS}	Power Dissipation		●		1498	1782	mW

LOW POWER LVDS OUTPUT MODE

OV_{DD}	Output Supply Voltage	(Note 8)	●	3	3.3	3.6	V
I_{VDD}	Analog Supply Current		●		380	450	mA
I_{OVDD}	Output Supply Current		●		31	50	mA
P_{DIS}	Power Dissipation		●		1356	1650	mW

CMOS OUTPUT MODE

OV_{DD}	Output Supply Voltage	(Note 8)	●	0.5		3.6	V
I_{VDD}	Analog Supply Current		●		380	450	mA
P_{DIS}	Power Dissipation		●		1250	1485	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Note 8)	●	1		130	MHz
t_L	ENC Low Time	Duty Cycle Stabilizer Off (Note 7)	●	3.65	3.846	1000	ns
		Duty Cycle Stabilizer On (Note 7)	●	2.6	3.846	1000	ns
t_H	ENC High Time	Duty Cycle Stabilizer Off (Note 7)	●	3.65	3.846	1000	ns
		Duty Cycle Stabilizer On (Note 7)	●	2.6	3.846	1000	ns
t_{AP}	Sample-and-Hold Aperture Delay				-1		ns

LVDS OUTPUT MODE (STANDARD and LOW POWER)

t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.5	3.8	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1.3	2.5	3.8	ns
t_{SKEW}	DATA to CLKOUT Skew	$(t_C - t_D)$ (Note 7)	●	-0.6	0	0.6	ns
t_{RISE}	Output Rise Time				0.5		ns
t_{FALL}	Output Fall Time				0.5		ns
Data Latency	Data Latency				7		Cycles

CMOS OUTPUT MODE

t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.7	4.0	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1.3	2.7	4.0	ns
t_{SKEW}	DATA to CLKOUT Skew	$(t_C - t_D)$ (Note 7)	●	-0.6	0	0.6	ns
Data Latency	Data Latency	Full Rate CMOS Demuxed			7		Cycles
					7		Cycles

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND, with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD} , they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: $V_{DD} = 3.3V$, $f_{SAMPLE} = 130MHz$, LVDS outputs, differential ENC⁺/ENC⁻ = 2V_{P-P} sine wave with 1.6V common mode, input range = 2.25V_{P-P} with differential drive (PGA = 0), unless otherwise specified.

Note 5: Integral nonlinearity is defined as the deviation of a code from a “best fit straight line” to the transfer curve. The deviation is measured from the center of the quantization band.

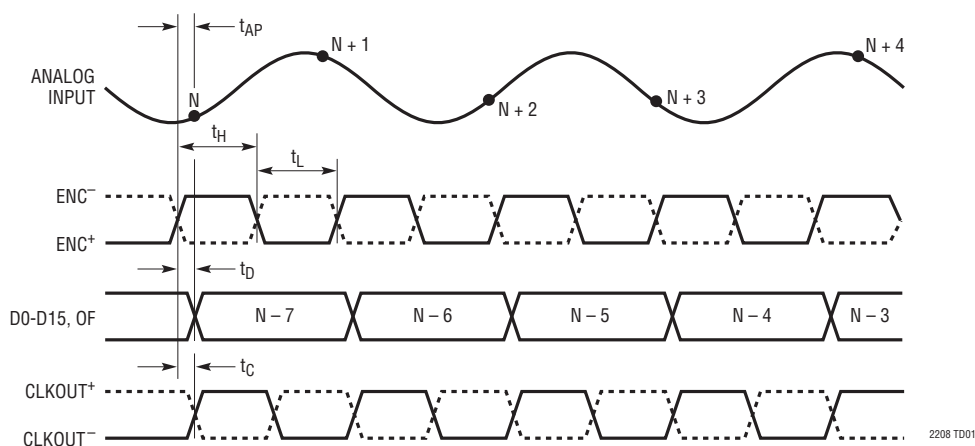
Note 6: Offset error is the offset voltage measured from $-1/2LSB$ when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2's complement output mode.

Note 7: Guaranteed by design, not subject to test.

Note 8: Recommended operating conditions.

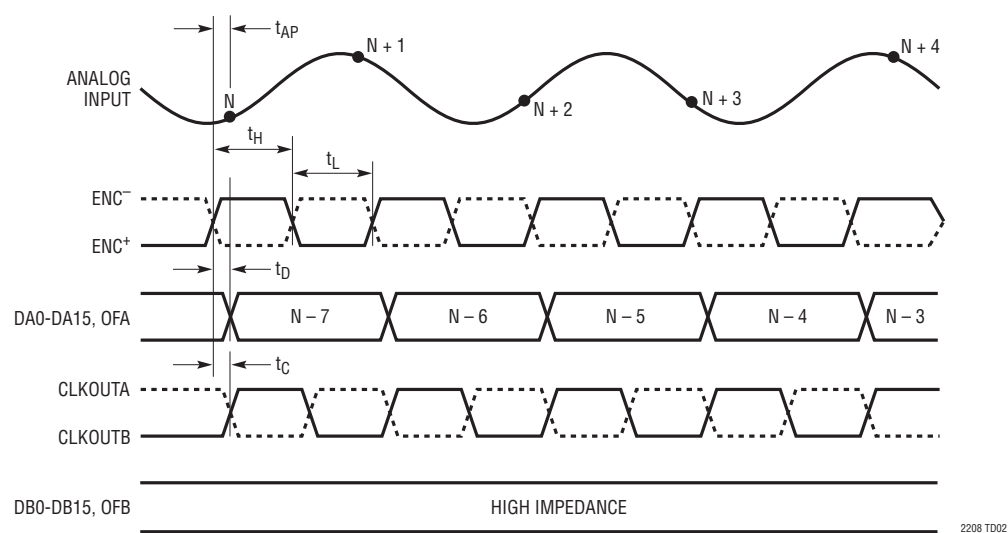
TIMING DIAGRAMS

LVDS Output Mode Timing
All Outputs are Differential and Have LVDS Levels

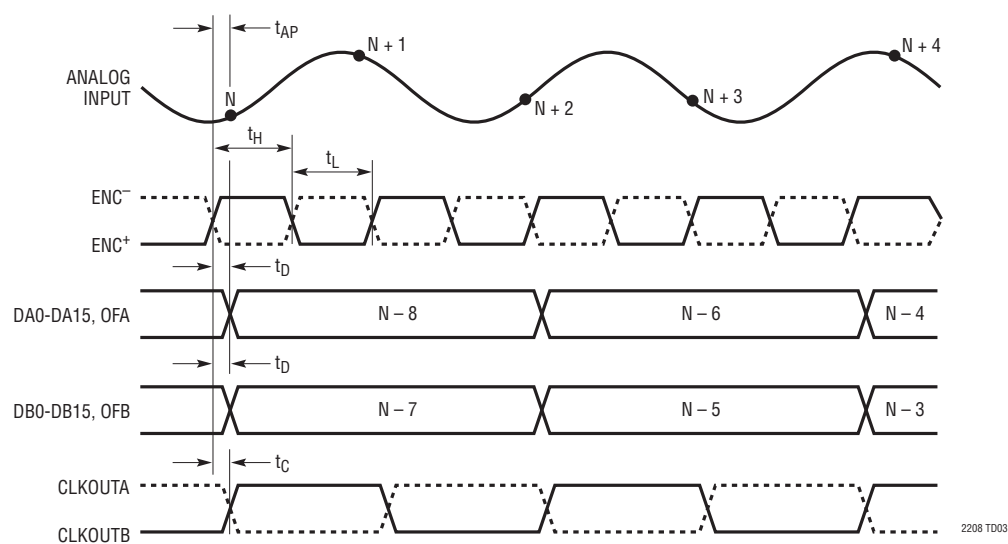


TIMING DIAGRAMS

Full-Rate CMOS Output Mode Timing
All Outputs are Single-Ended and Have CMOS Levels

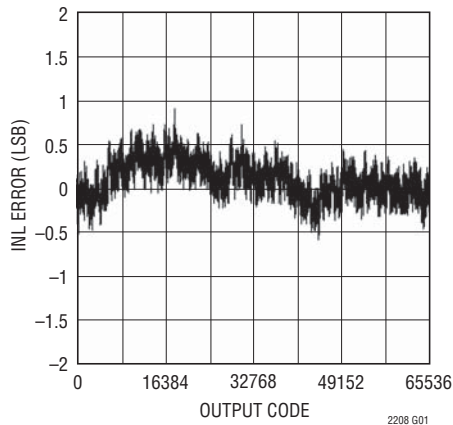


Demultiplexed CMOS Output Mode Timing
All Outputs are Single-Ended and Have CMOS Levels

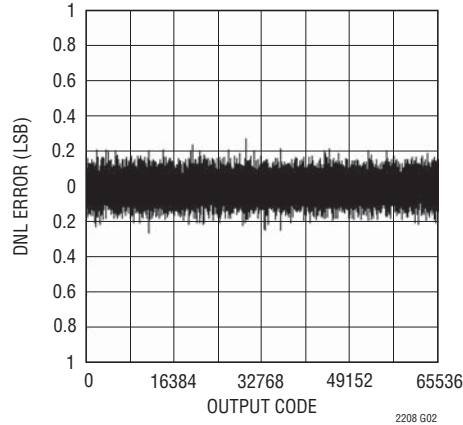


TYPICAL PERFORMANCE CHARACTERISTICS

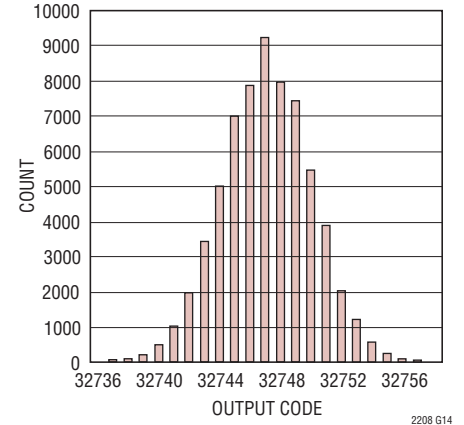
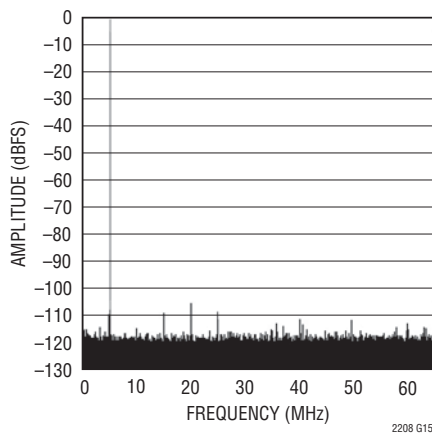
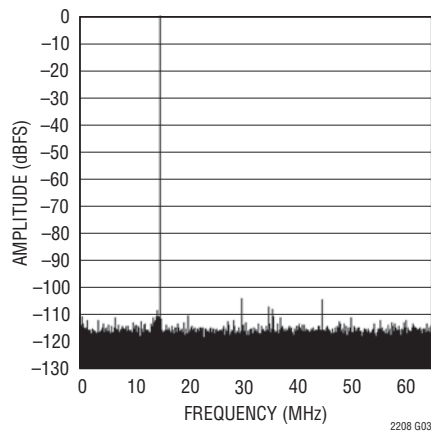
Integral Nonlinearity (INL) vs Output Code



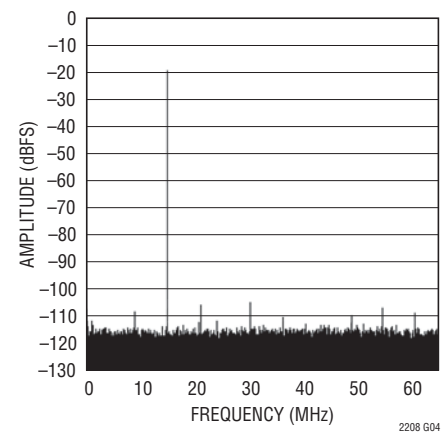
Differential Nonlinearity (DNL) vs Output Code



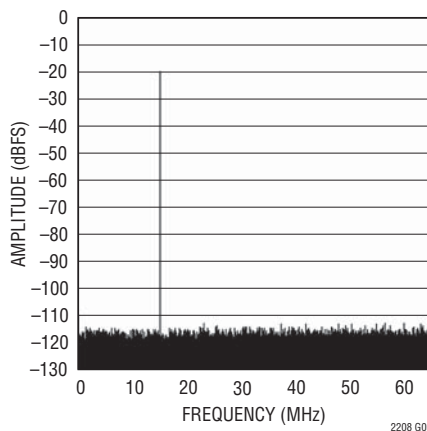
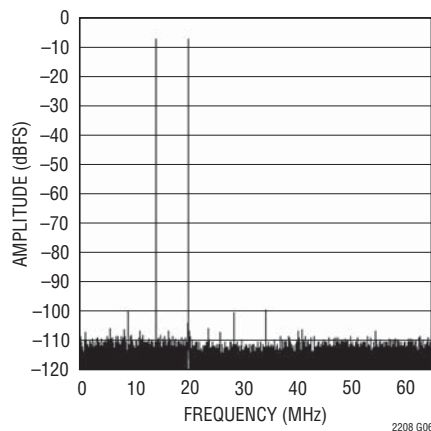
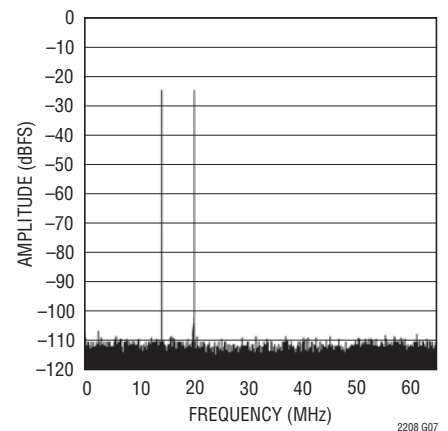
AC Grounded Input Histogram

128k Point FFT, $f_{IN} = 4.93\text{MHz}$, -1dBFS, PGA = 064k Point FFT, $f_{IN} = 15.1\text{MHz}$, -1dBFS, PGA = 0

64k Point FFT, 15.1MHz, -20dBFS, PGA = 0, Internal Dither "Off"

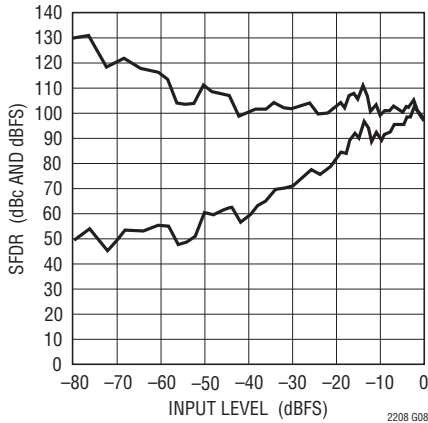


64k Point FFT, 15.1MHz, -20dBFS, PGA = 0, Internal Dither "On"

32k Point 2-Tone FFT, $f_{IN} = 21.14\text{MHz}$ and 14.25MHz , -7dBFS, PGA = 032k Point 2-Tone FFT, $f_{IN} = 20.14\text{MHz}$ and 14.25MHz , -25dBFS, PGA = 0

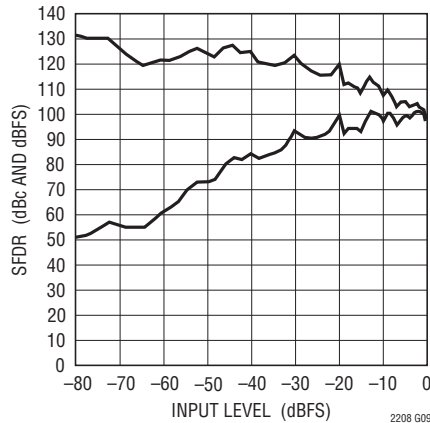
TYPICAL PERFORMANCE CHARACTERISTICS

**SFDR vs Input Level, $f_{IN} = 15\text{MHz}$,
PGA = 0, Dither "Off"**



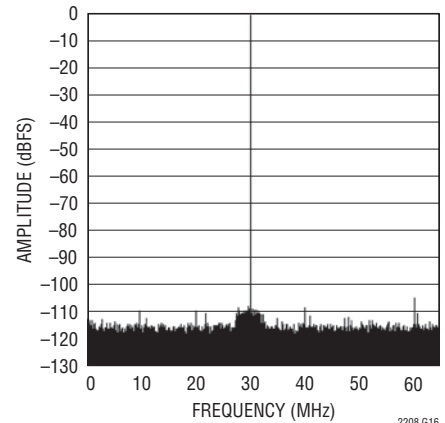
2208 G08

**SFDR vs Input Level, $f_{IN} = 15\text{MHz}$,
PGA = 0, Dither "On"**



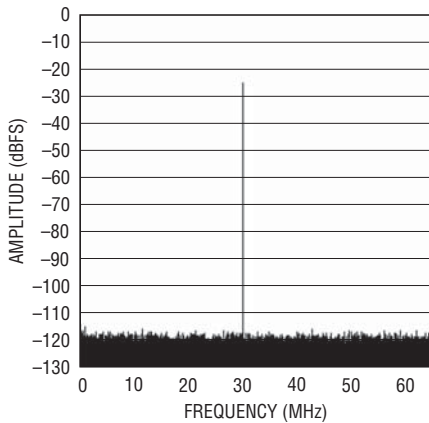
2208 G09

**64k Point FFT, $f_{IN} = 30.1\text{MHz}$,
-1dBFS, PGA = 0**



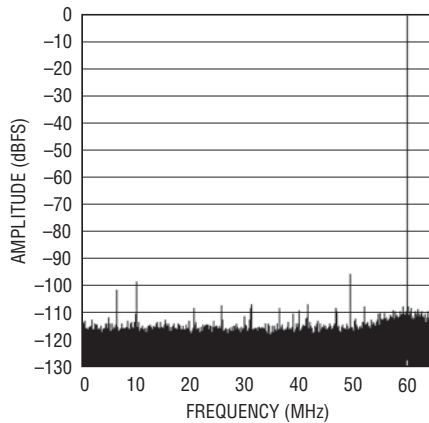
2208 G16

**128k Point FFT, $f_{IN} = 30.1\text{MHz}$,
-25dBFS, PGA = 0, Dither "On"**



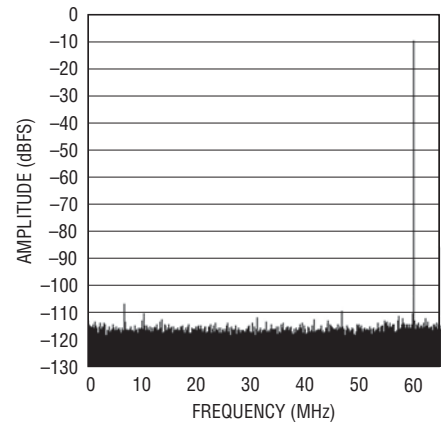
2208 G17

**64k Point FFT, $f_{IN} = 70.1\text{MHz}$,
-1dBFS, PGA = 0**



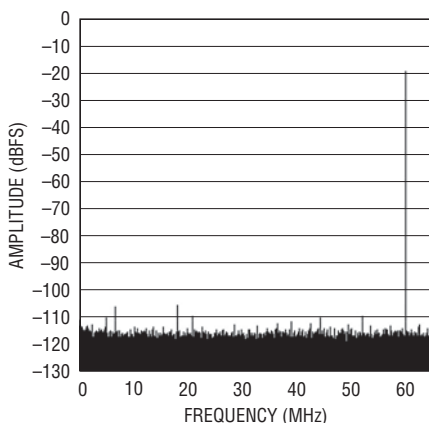
2208 G18

**64k Point FFT, $f_{IN} = 70.1\text{MHz}$,
-10dBFS, PGA = 0**



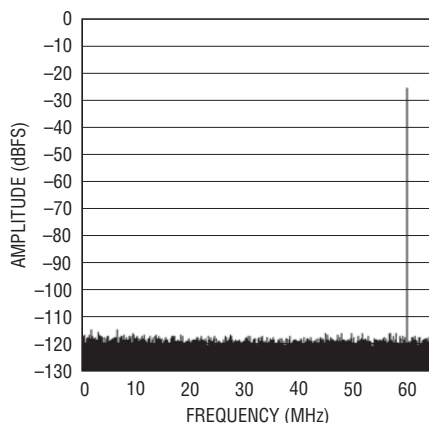
2208 G19

**64k Point FFT, $f_{IN} = 70.1\text{MHz}$,
-20dBFS, PGA = 0**



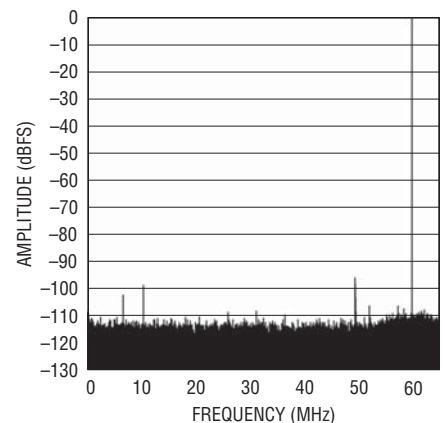
2208 G20

**128k Point FFT, $f_{IN} = 70.1\text{MHz}$,
-25dBFS, PGA = 0, Dither "On"**



2208 G21

**64k Point FFT, $f_{IN} = 70.1\text{MHz}$,
-1dBFS, PGA = 1**

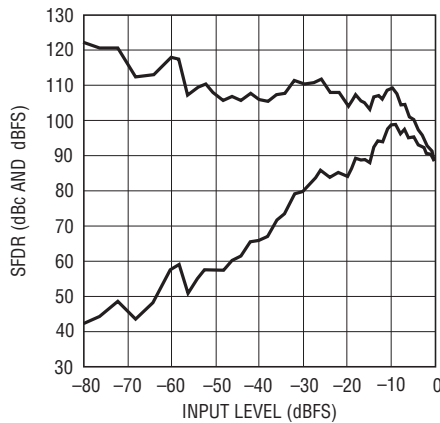


2208 G22

2208fc

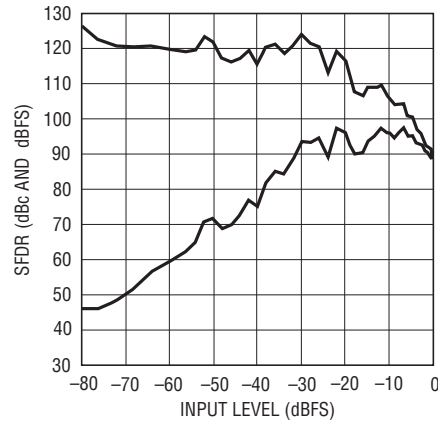
TYPICAL PERFORMANCE CHARACTERISTICS

SFDR vs Input Level,
 $f_{IN} = 70.2\text{MHz}$,
 PGA = 0, Dither "Off"



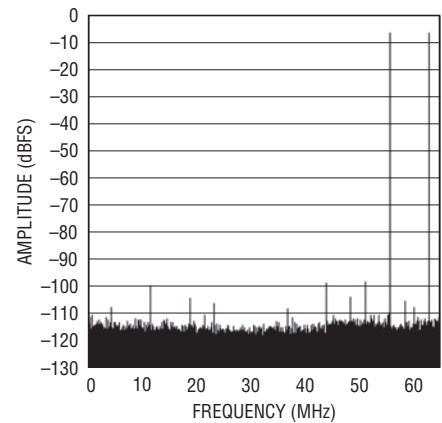
2208 G28

SFDR vs Input Level,
 $f_{IN} = 70.2\text{MHz}$,
 PGA = 0, Dither "On"



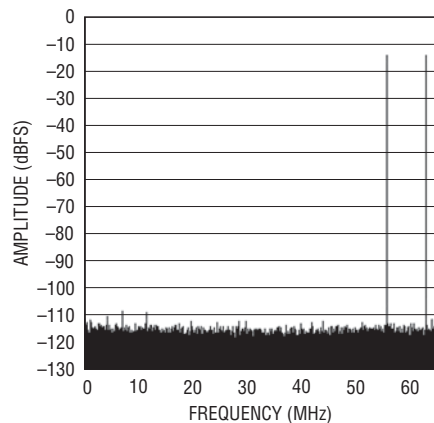
2208 G29

**64k Point FFT, $f_{IN} = 67.2\text{MHz}$ and
 74.4MHz , -7dBFS, PGA = 0**



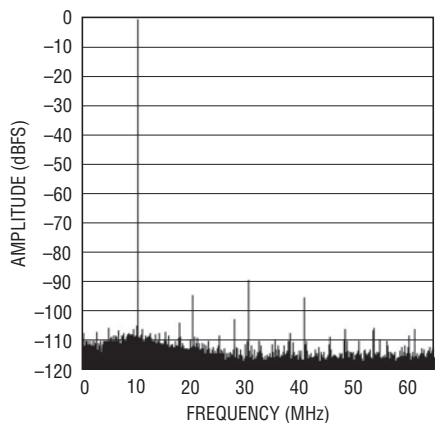
2208 G24

**64k Point FFT, $f_{IN} = 67.2\text{MHz}$ and
 74.4MHz , -15dBFS, PGA = 0**



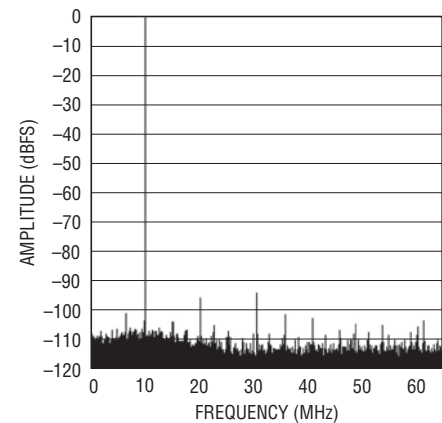
2208 G25

**64k Point FFT, $f_{IN} = 140.1\text{MHz}$,
 -1dBFS, PGA = 0**



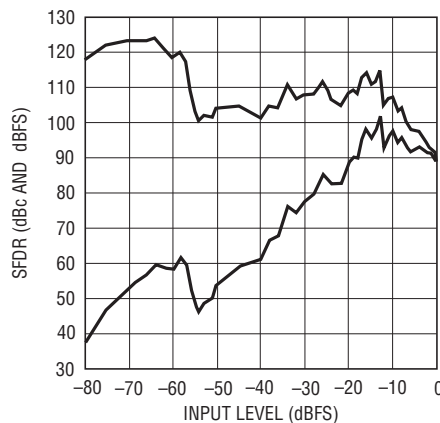
2208 G27

**64k Point FFT, $f_{IN} = 140.1\text{MHz}$,
 -1dBFS, PGA = 1**



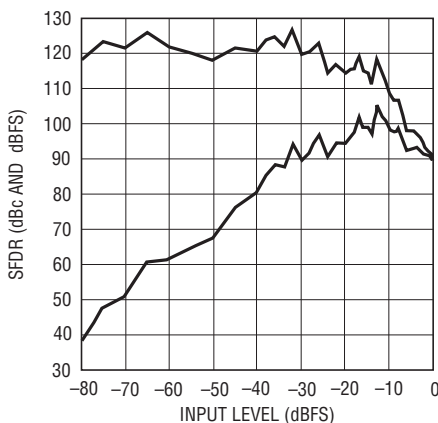
2208 G26

SFDR vs Input Level,
 $f_{IN} = 140.2\text{MHz}$,
 PGA = 1, Dither "Off"



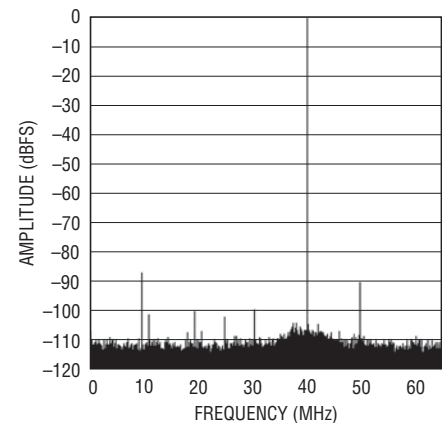
2208 G30

SFDR vs Input Level,
 $f_{IN} = 140.2\text{MHz}$,
 PGA = 1, Dither "On"



2208 G31

**64k Point FFT, $f_{IN} = 170.1\text{MHz}$,
 -1dBFS, PGA = 1**

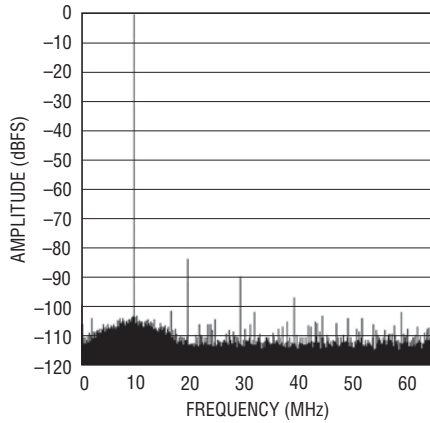


2208 G34

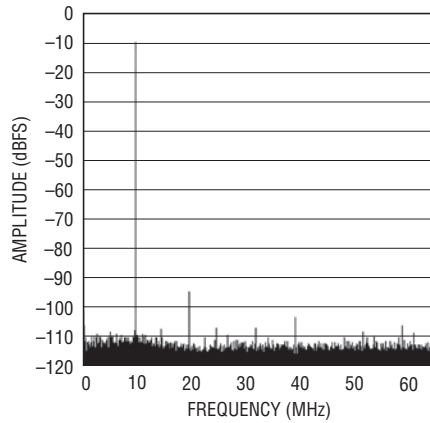
2208fc

TYPICAL PERFORMANCE CHARACTERISTICS

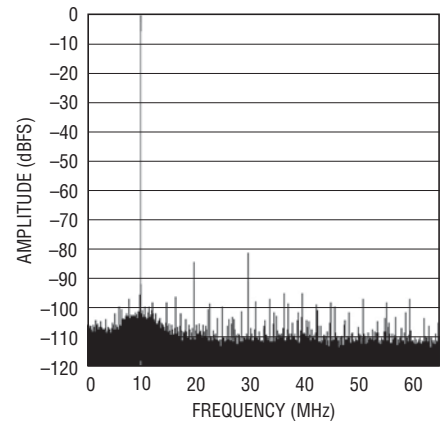
64k Point FFT, $f_{IN} = 250.1\text{MHz}$,
-1dBFS, PGA = 1



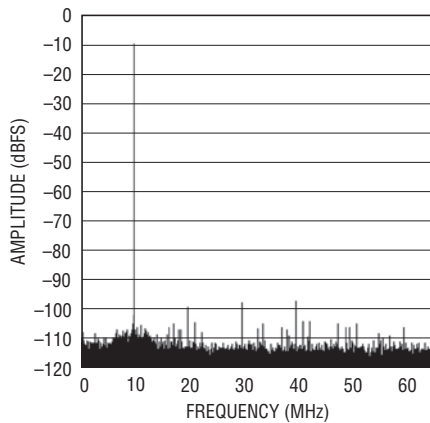
64k Point FFT, $f_{IN} = 250.1\text{MHz}$,
-10dBFS, PGA = 1



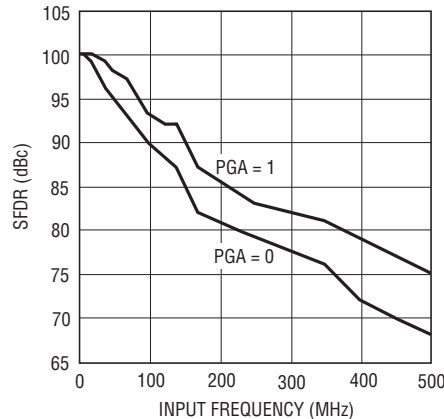
64k Point FFT, $f_{IN} = 380\text{MHz}$,
-1dBFS, PGA = 1



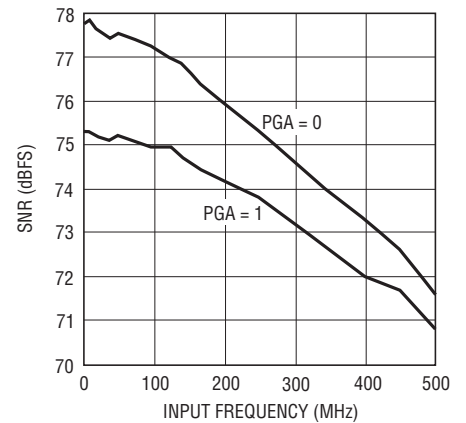
64k Point FFT, $f_{IN} = 380\text{MHz}$,
-10dBFS, PGA = 1



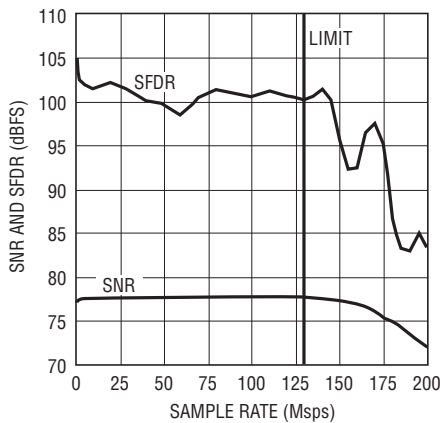
SFDR (HD2 and HD3) vs
Input Frequency



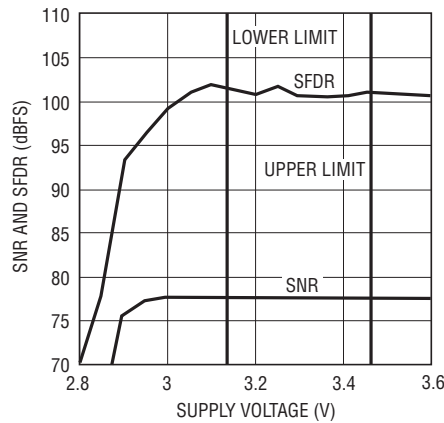
SNR vs Input Frequency



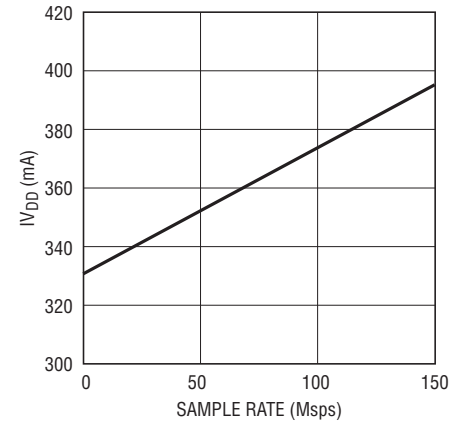
SNR and SFDR vs Sample Rate,
 $f_{IN} = 5\text{MHz}$



SNR and SFDR vs Supply
Voltage (V_{DD}), $f_{IN} = 5\text{MHz}$



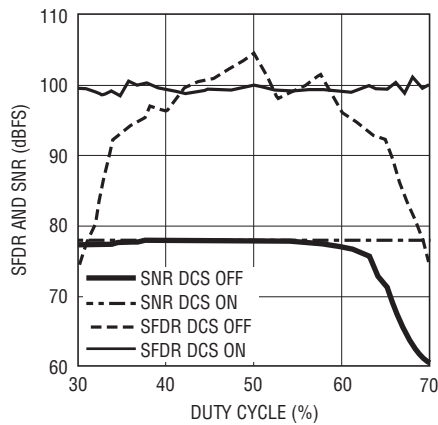
I_{VDD} vs Sample Rate, 5MHz Sine
Wave, -1dBFS



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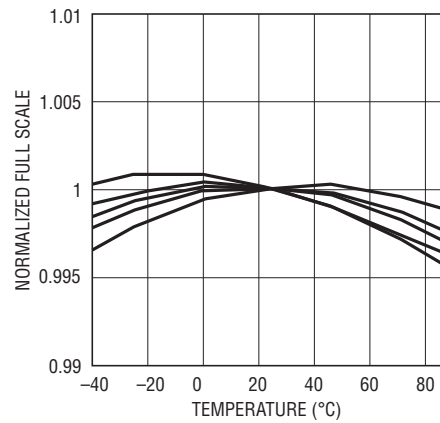
TYPICAL PERFORMANCE CHARACTERISTICS

SNR and SFDR vs Duty Cycle



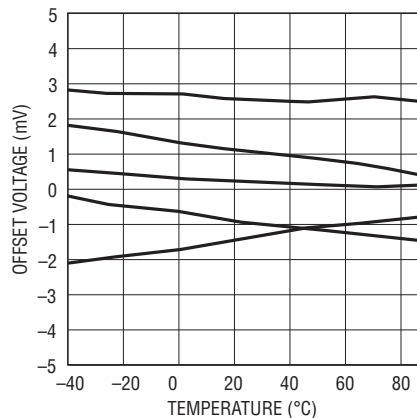
2208 G10

Normalized Full Scale vs Temperature, Internal Reference, 5 Units



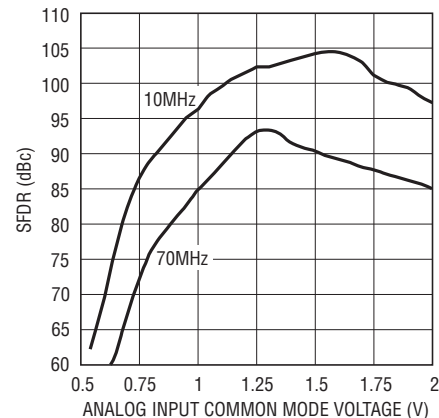
2208 G11

Input Offset Voltage vs Temperature, 5 Units



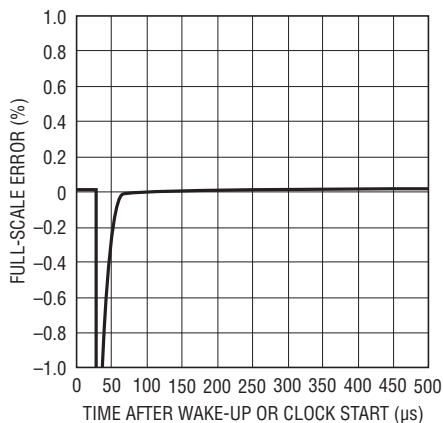
2208 G12

SFDR vs Analog Input Common Mode Voltage, 10MHz and 70MHz, -1dBFS, PGA = 0



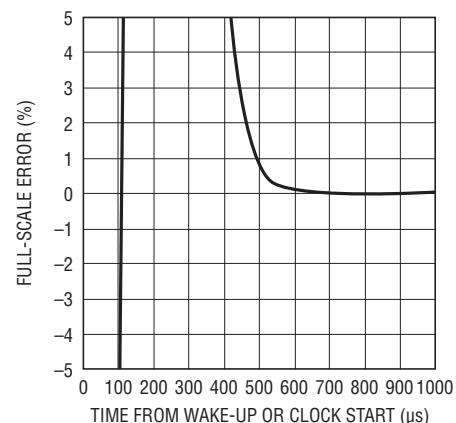
2208 G41

Mid-Scale Settling After Wake Up from Shutdown or Starting Encode Clock



2208 G42

Full-Scale Settling After Wake Up from Shutdown or Starting Encode Clock



2208 G43

2208fc

PIN FUNCTIONS

For CMOS Mode. Full Rate or Demultiplexed

SENSE (Pin 1): Reference Mode Select and External Reference Input. Tie SENSE to V_{DD} to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full scale ADC range of 2.25V ($PGA = 0$).

GND (Pins 2, 4, 7, 10, 11, 14, 18): ADC Power Ground.

V_{CM} (Pin 3): 1.25V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2 μ F. Ceramic chip capacitors are recommended.

V_{DD} (Pins 5, 6, 15, 16, 17): 3.3V Analog Supply Pin. Bypass to GND with 1 μ F ceramic chip capacitors.

A_{IN}^+ (Pin 8): Positive Differential Analog Input.

A_{IN}^- (Pin 9): Negative Differential Analog Input.

ENC⁺ (Pin 12): Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC⁺. Internally biased to 1.6V through a 6.2k resistor. Output data can be latched on the rising edge of ENC⁺.

ENC⁻ (Pin 13): Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC⁻. Internally biased to 1.6V through a 6.2k resistor. Bypass to ground with a 0.1 μ F capacitor for a single-ended Encode signal.

SHDN (Pin 19): Power Shutdown Pin. SHDN = low results in normal operation. SHDN = high results in powered down analog circuitry and the digital outputs are placed in a high impedance state.

DITH (Pin 20): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation.

DB0-DB15 (Pins 21-30 and 33-38): Digital Outputs, B Bus. DB15 is the MSB. Active in demultiplexed mode. The B bus is in high impedance state in full rate CMOS.

OGND (Pins 31 and 50): Output Driver Ground.

OV_{DD} (Pins 32 and 49): Positive Supply for the Output Drivers. Bypass to ground with 1 μ F capacitor.

OFB (Pin 39): Over/Under Flow Digital Output for the B Bus. OFB is high when an over or under flow has occurred on the B bus. At high impedance state in full rate CMOS mode.

CLKOUTB (Pin 40): Data Valid Output. CLKOUTB will toggle at the sample rate in full rate CMOS mode or at 1/2 the sample rate in demultiplexed mode. Latch the data on the falling edge of CLKOUTB.

CLKOUTA (Pin 41): Inverted Data Valid Output. CLKOUTA will toggle at the sample rate in full rate CMOS mode or at 1/2 the sample rate in demultiplexed mode. Latch the data on the rising edge of CLKOUTA.

DA0-DA15 (Pins 42-48 and 51-59): Digital Outputs, A Bus. DA15 is the MSB. Output bus for full rate CMOS mode and demultiplexed mode.

OFA (Pin 60): Over/Under Flow Digital Output for the A Bus. OFA is high when an over or under flow has occurred on the A bus.

LVDS (Pin 61): Data Output Mode Select Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to 1/3 V_{DD} selects demultiplexed CMOS mode. Connecting LVDS to 2/3 V_{DD} selects Low Power LVDS mode. Connecting LVDS to V_{DD} selects Standard LVDS mode.

MODE (Pin 62): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to 1/3 V_{DD} selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to 2/3 V_{DD} selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to V_{DD} selects 2's complement output format and disables the clock duty cycle stabilizer.

RAND (Pin 63): Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. This mode of operation reduces the effects of digital output interference.

PGA (Pin 64): Programmable Gain Amplifier Control Pin. Low selects a front-end gain of 1, input range of 2.25V_{P-P}. High selects a front-end gain of 1.5, input range of 1.5V_{P-P}.

GND (Exposed Pad): ADC Power Ground. The exposed pad on the bottom of the package must be soldered to ground.

PIN FUNCTIONS

For LVDS Mode. STANDARD or LOW POWER

SENSE (Pin 1): Reference Mode Select and External Reference Input. Tie SENSE to V_{DD} to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full scale ADC range of 2.25V ($PGA = 0$).

GND (Pins 2, 4, 7, 10, 11, 14, 18): ADC Power Ground.

V_{CM} (Pin 3): 1.25V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2 μ F. Ceramic chip capacitors are recommended.

V_{DD} (Pins 5, 6, 15, 16, 17): 3.3V Analog Supply Pin. Bypass to GND with 1 μ F ceramic chip capacitors.

A_{IN}^+ (Pin 8): Positive Differential Analog Input.

A_{IN}^- (Pin 9): Negative Differential Analog Input.

ENC⁺ (Pin 12): Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC⁺. Internally biased to 1.6V through a 6.2k resistor. Output data can be latched on the rising edge of ENC⁺.

ENC⁻ (Pin 13): Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC⁻. Internally biased to 1.6V through a 6.2k resistor. Bypass to ground with a 0.1 μ F capacitor for a single-ended Encode signal.

SHDN (Pin 19): Power Shutdown Pin. SHDN = low results in normal operation. SHDN = high results in powered down analog circuitry and the digital outputs are set in high impedance state.

DITH (Pin 20): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of the data sheet for details on dither operation.

D0⁻/D0⁺ to D15⁻/D15⁺ (Pins 21-30, 33-38, 41-48 and 51-58): LVDS Digital Outputs. All LVDS outputs require differential 100 Ω termination resistors at the LVDS receiver. D15⁺/D15⁻ is the MSB.

OGND (Pins 31 and 50): Output Driver Ground.

OV_{DD} (Pins 32 and 49): Positive Supply for the Output Drivers. Bypass to ground with 0.1 μ F capacitor.

CLKOUT⁻/CLKOUT⁺ (Pins 39 and 40): LVDS Data Valid Output. Latch data on the rising edge of CLKOUT⁺, falling edge of CLKOUT⁻.

OF⁻/OF⁺ (Pins 59 and 60): Over/Under Flow Digital Output. OF is high when an over or under flow has occurred.

LVDS (Pin 61): Data Output Mode Select Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to 1/3 V_{DD} selects demultiplexed CMOS mode. Connecting LVDS to 2/3 V_{DD} selects Low Power LVDS mode. Connecting LVDS to V_{DD} selects Standard LVDS mode.

MODE (Pin 62): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to 1/3 V_{DD} selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to 2/3 V_{DD} selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to V_{DD} selects 2's complement output format and disables the clock duty cycle stabilizer.

RAND (Pin 63): Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. The mode of operation reduces the effects of digital output interference.

PGA (Pin 64): Programmable Gain Amplifier Control Pin. Low selects a front-end gain of 1, input range of 2.25V_{P-P}. High selects a front-end gain of 1.5, input range of 1.5V_{P-P}.

GND (Exposed Pad Pin 65): ADC Power Ground. The exposed pad on the bottom of the package must be soldered to ground.

BLOCK DIAGRAM

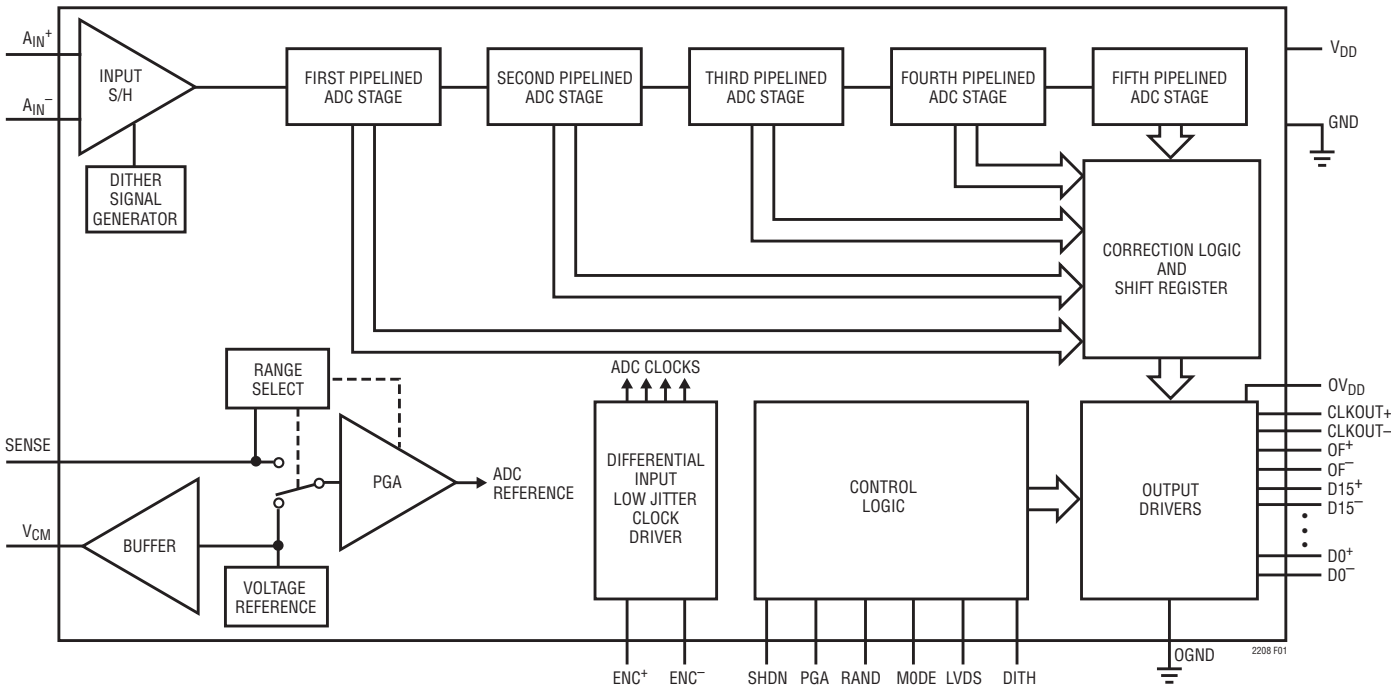


Figure 1. Functional Block Diagram

OPERATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$\text{THD} = -20\log\left(\sqrt{(V_2^2 + V_3^2 + V_4^2 + \dots V_N^2)} / V_1\right)$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through nth harmonics.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of $m f_a \pm n f_b$, where m and $n = 0, 1, 2, 3$, etc. For example, the 3rd order IMD terms include $(2f_a + f_b)$, $(f_a + 2f_b)$, $(2f_a - f_b)$ and $(f_a - 2f_b)$. The 3rd order IMD is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

Spurious Free Dynamic Range (SFDR)

The ratio of the RMS input signal amplitude to the RMS value of the peak spurious spectral component expressed in dBc. SFDR may also be calculated relative to full scale and expressed in dBFS.

Full Power Bandwidth

The Full Power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when a rising ENC^+ equals the ENC^- voltage to the instant that the input signal is held by the sample-and-hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$\text{SNR}_{\text{JITTER}} = -20\log(2\pi \cdot f_{\text{IN}} \cdot t_{\text{JITTER}})$$

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2208 is a CMOS pipelined multistep converter with a front-end PGA. As shown in Figure 1, the converter has five pipelined ADC stages; a sampled analog input will result in a digitized value seven cycles later (see the Timing Diagrams section). The analog input is differential for improved common mode noise immunity and to maximize the input range. Additionally, the differential input drive will reduce even order harmonics of the sample and hold circuit. The encode input is also differential for improved common mode noise immunity.

The LTC2208 has two phases of operation, determined by the state of the differential ENC^+/ENC^- input pins. For brevity, the text will refer to ENC^+ greater than ENC^- as ENC high and ENC^+ less than ENC^- as ENC low.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "input S/H" shown in the block diagram. At the instant that ENC transitions from low to high, the voltage on the sample capacitors is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H amplifier during the high phase of ENC . When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage for final evaluation.

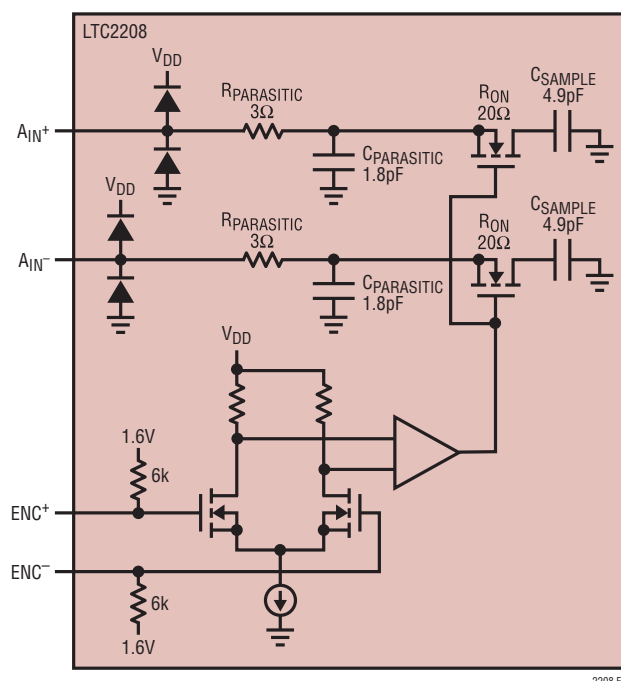
Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally delayed such that the results can be properly combined in the correction logic before being sent to the output buffer.

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2208 CMOS differential sample and hold. The differential analog inputs are sampled directly onto sampling capacitors (C_{SAMPLE}) through NMOS transistors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when ENC is low, the NMOS transistors connect the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When ENC transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when ENC is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC transitions for high to low, the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the



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Figure 2. Equivalent Input Circuit

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APPLICATIONS INFORMATION

input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

Common Mode Bias

The ADC sample-and-hold circuit requires differential drive to achieve specified performance. Each input should swing $\pm 0.5625V$ for the 2.25V range ($PGA = 0$) or $\pm 0.375V$ for the 1.5V range ($PGA = 1$), around a common mode voltage of 1.25V. The V_{CM} output pin (Pin 3) is designed to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with 2.2 μF or greater.

Input Drive Impedence

As with all high performance, high speed ADCs the dynamic performance of the LTC2208 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of ENC the sample and hold circuit will connect the 4.9pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when ENC rises, holding the sampled input on the sampling capacitor. Ideally, the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{encode})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance it is recommended to have a source impedance of 100 Ω or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

INPUT DRIVE CIRCUITS

Input Filtering

A first order RC low pass filter at the input of the ADC can serve two functions: limit the noise from input circuitry and

provide isolation from ADC S/H switching. The LTC2208 has a very broadband S/H circuit, DC to 700MHz; it can be used in a wide range of applications; therefore, it is not possible to provide a single recommended RC filter.

Figures 3, 4a and 4b show three examples of input RC filtering at three ranges of input frequencies. In general it is desirable to make the capacitors as large as can be tolerated—this will help suppress random noise as well as noise coupled from the digital circuitry. The LTC2208 does not require any input filter to achieve data sheet specifications; however, no filtering will put more stringent noise requirements on the input drive circuitry.

Transformer Coupled Circuits

Figure 3 shows the LTC2208 being driven by an RF transformer with a center-tapped secondary. The secondary center tap is DC biased with V_{CM} , setting the ADC input signal at its optimum DC level. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used; however, as the turns ratio increases so does the impedance seen by the ADC. Source impedance greater than 50 Ω can reduce the input bandwidth and increase high frequency distortion. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

Center-tapped transformers provide a convenient means of DC biasing the secondary; however, they often show poor balance at high input frequencies, resulting in large 2nd order harmonics.

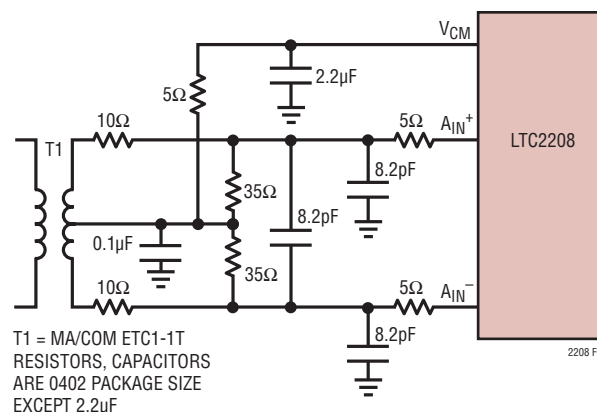
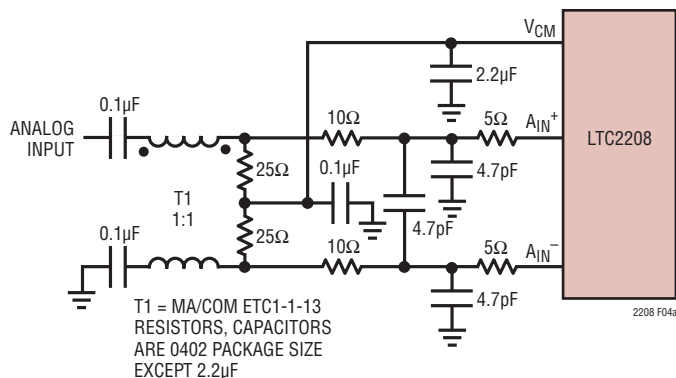


Figure 3. Single-Ended to Differential Conversion Using a Transformer. Recommended for Input Frequencies from 5MHz to 100MHz

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APPLICATIONS INFORMATION

Figure 4a shows transformer coupling using a transmission line balun transformer. This type of transformer has much better high frequency response and balance than flux coupled center tap transformers. Coupling capacitors are added at the ground and input primary terminals to allow the secondary terminals to be biased at 1.25V. Figure 4b shows the same circuit with components suitable for higher input frequencies.



**Figure 4a. Using a Transmission Line Balun Transformer.
Recommended for Input Frequencies from 100MHz to 250MHz**

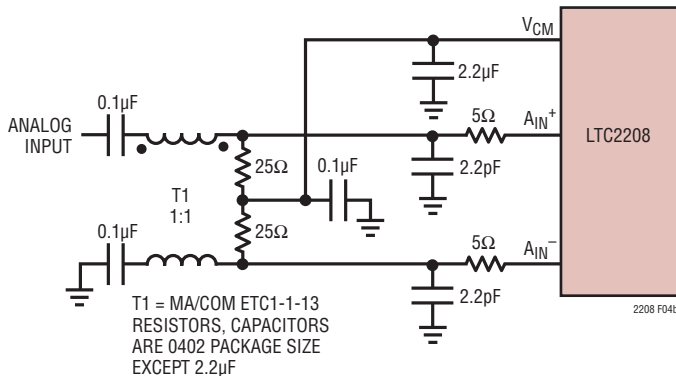


Figure 4b. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 250MHz to 500MHz

Direct Coupled Circuits

Figure 5 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of any op amp or closed-loop amplifier will degrade the ADC SFDR at high input frequencies. Additionally, wideband op amps or differential amplifiers tend to have high noise. As a result, the SNR will be degraded unless the noise bandwidth is limited prior to the ADC input.

Reference Operation

Figure 6 shows the LTC2208 reference circuitry consisting of a 2.5V bandgap reference, a programmable gain amplifier and control circuit. The LTC2208 has three modes of

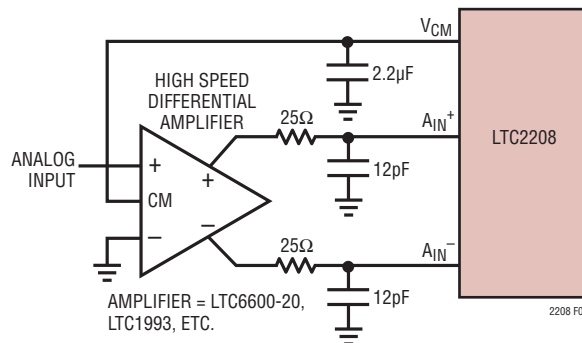


Figure 5. DC-Coupled Input with Differential Amplifier

reference operation: Internal Reference, 1.25V external reference or 2.5V external reference. To use the internal reference, tie the SENSE pin to V_{DD} . To use an external reference, simply apply either a 1.25V or 2.5V reference voltage to the SENSE input pin. Both 1.25V and 2.5V applied to SENSE will result in a full scale range of $2.25V_{P-P}$ ($PGA = 0$). A 1.25V output, V_{CM} is provided for a common mode bias for input drive circuitry. An external bypass capacitor is required for the V_{CM} output. This provides a high frequency low impedance path to ground for internal and external circuitry. This is also the compensation capacitor for the reference; it will not be stable without this capacitor. The minimum value required for stability is $2.2\mu F$.

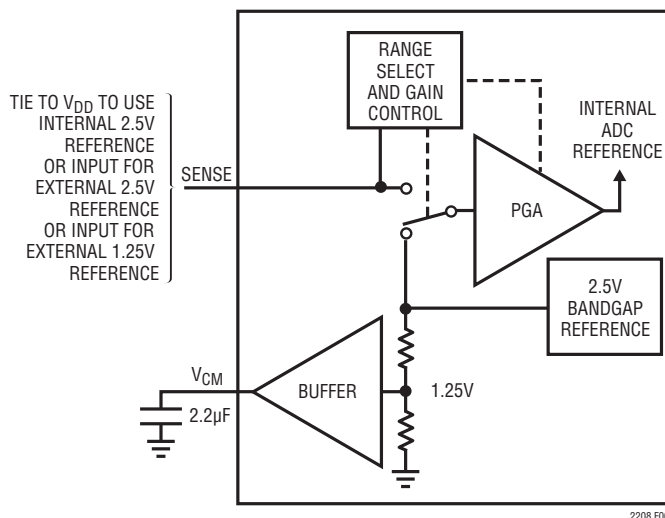


Figure 6. Reference Circuit

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The internal programmable gain amplifier provides the internal reference voltage for the ADC. This amplifier has very stringent settling requirements and is not accessible for external use.

The SENSE pin can be driven $\pm 5\%$ around the nominal 2.5V or 1.25V external reference inputs. This adjustment range can be used to trim the ADC gain error or other system gain errors. When selecting the internal reference, the SENSE pin should be tied to V_{DD} as close to the converter as possible. If the sense pin is driven externally it should be bypassed to ground as close to the device as possible with 1 μ F ceramic capacitor.

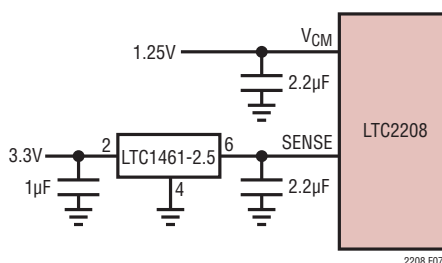


Figure 7. A 2.25V Range ADC with an External 2.5V Reference

PGA Pin

The PGA pin selects between two gain settings for the ADC front-end. PGA = 0 selects an input range of 2.25V_{P-P}; PGA = 1 selects an input range of 1.5V_{P-P}. The 2.25V input range has the best SNR; however, the distortion will be higher for input frequencies above 100MHz. For applications with high input frequencies, the low input range will have improved distortion; however, the SNR will be 1.8dB worse. See the typical performance curves section.

Driving the Encode Inputs

The noise performance of the LTC2208 can depend on the encode signal quality as much as for the analog input. The encode inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies), take the following into consideration:

1. Differential drive should be used.
2. Use as large an amplitude possible. If using transformer coupling, use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a fixed frequency sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs such that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.2V to V_{DD} . Each input may be driven from ground to V_{DD} for single-ended drive.

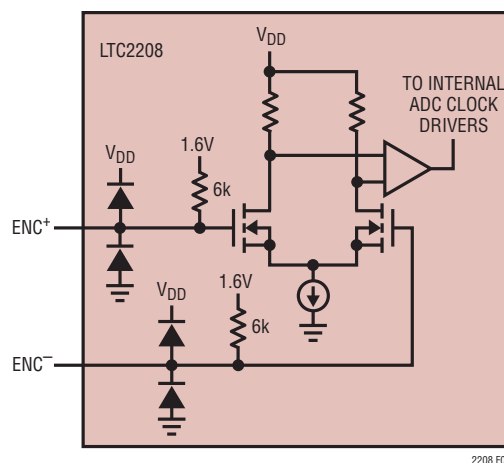
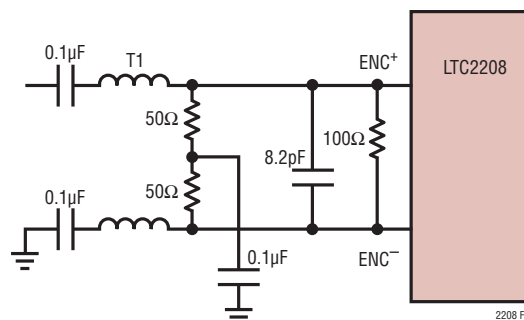


Figure 8a. Equivalent Encode Input Circuit



T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 8b. Transformer Driven Encode

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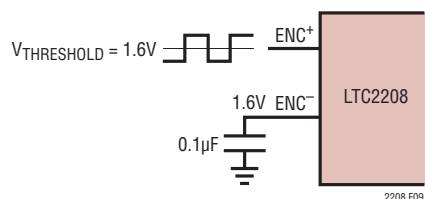


Figure 9. Single-Ended ENC Drive, Not Recommended for Low Jitter

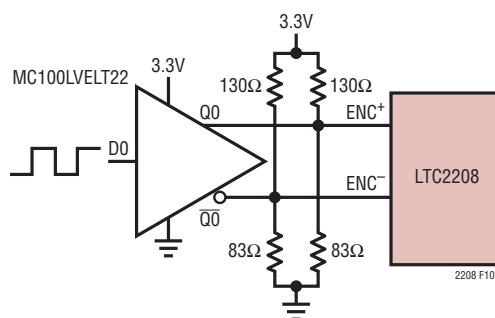


Figure 10. ENC Drive Using a CMOS to PECL Translator

Maximum and Minimum Encode Rates

The maximum encode rate for the LTC2208 is 130MSPS. For the ADC to operate properly the encode signal should have a 50% ($\pm 5\%$) duty cycle. Each half cycle must have at least 3.65ns for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS. When using a single-ended ENCODE signal asymmetric rise and fall times can result in duty cycles that are far from 50%.

An optional clock duty cycle stabilizer can be used if the input clock does not have a 50% duty cycle. This circuit uses the rising edge of ENC pin to sample the analog input. The falling edge of ENC is ignored and an internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 30% to 70% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin must be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the LTC2208 sample rate is determined by droop of the sample and hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2208 is 1MSPS.

DIGITAL OUTPUTS

Digital Output Modes

The LTC2208 can operate in four digital output modes: standard LVDS, low power LVDS, full rate CMOS, and demultiplexed CMOS. The LVDS pin selects the mode of operation. This pin has a four level logic input, centered at 0, $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD} . An external resistor divider can be used to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 1 shows the logic states for the LVDS pin.

Table 1. LVDS Pin Function

LVDS	DIGITAL OUTPUT MODE
0V(GND)	Full-Rate CMOS
$1/3V_{DD}$	Demultiplexed CMOS
$2/3V_{DD}$	Low Power LVDS
V_{DD}	LVDS

Digital Output Buffers (CMOS Modes)

Figure 11 shows an equivalent circuit for a single output buffer in CMOS Mode, Full-Rate or Demultiplexed. Each buffer is powered by $0V_{DD}$ and $0GND$, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and eliminates the need for external damping resistors.

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2208 should drive a minimum capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as a ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF. A resistor in series with the

APPLICATIONS INFORMATION

output may be used but is not required since the ADC has a series resistor of 43Ω on chip.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

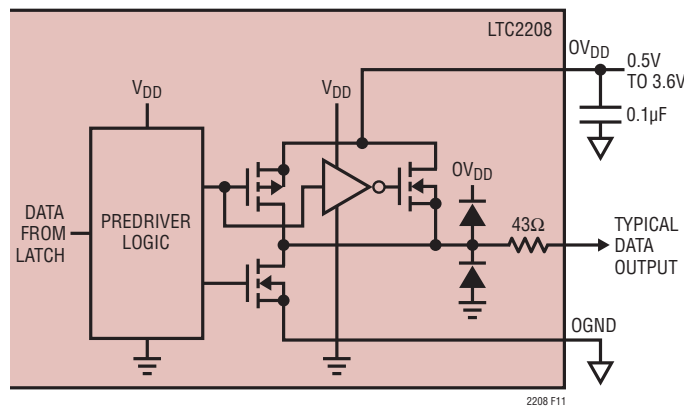


Figure 11. Equivalent Circuit for a Digital Output Buffer

Digital Output Buffers (LVDS Modes)

Figure 12 shows an equivalent circuit for an LVDS output pair. A $3.5mA$ current is steered from OUT^+ to OUT^- or vice versa, which creates a $\pm 350mV$ differential voltage across the 100Ω termination resistor at the LVDS receiver. A feedback loop regulates the common mode output voltage to $1.20V$. For proper operation each LVDS output pair must be terminated with an external 100Ω termination

resistor, even if the signal is not used (such as OF^+/OF^- or $CLKOUT^+/CLKOUT^-$). To minimize noise the PC board traces for each LVDS output pair should be routed close together. To minimize clock skew all LVDS PC board traces should have about the same length.

In Low Power LVDS Mode $1.75mA$ is steered between the differential outputs, resulting in $\pm 175mV$ at the LVDS receiver's 100Ω termination resistor. The output common mode voltage is $1.20V$, the same as standard LVDS Mode.

Data Format

The LTC2208 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. This pin has a four level logic input, centered at 0 , $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD} . An external resistor divider can be used to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 2 shows the logic states for the MODE pin.

Table 2. MODE Pin Function

MODE	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0(GND)	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

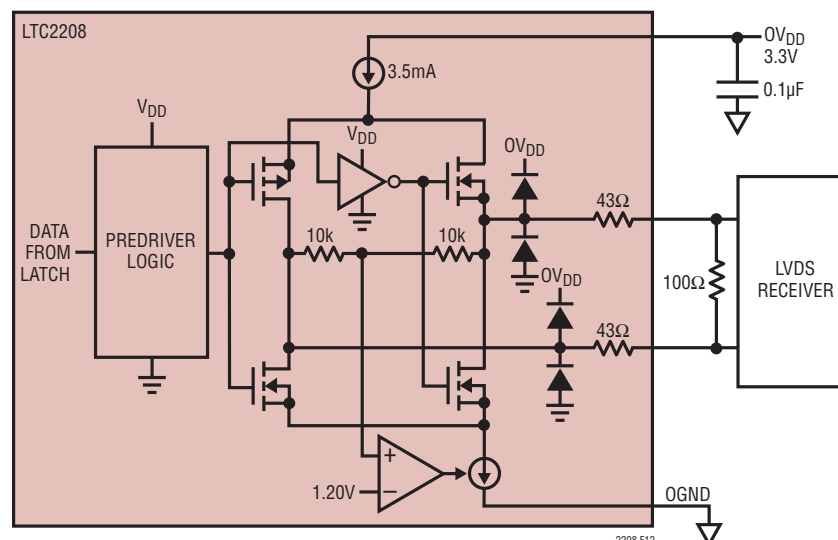


Figure 12. Equivalent Output Buffer in LVDS Mode

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Overflow Bit

An overflow output bit (OF) indicates when the converter is over-ranged or under-ranged. In CMOS mode, a logic high on the OFA pin indicates an overflow or underflow on the A data bus, while a logic high on the OFB pin indicates an overflow on the B data bus. In LVDS mode, a differential logic high on OF⁺/OF⁻ pins indicates an overflow or underflow.

Output Clock

The ADC has a delayed version of the encode input available as a digital output, CLKOUT. The CLKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. In both CMOS modes, A bus data will be updated as CLKOUTA falls and CLKOUTB rises. In demultiplexed CMOS mode the B bus data will be updated as CLKOUTA falls and CLKOUTB rises.

In Full Rate CMOS Mode, only the A data bus is active; data may be latched on the rising edge of CLKOUTA or the falling edge of CLKOUTB.

In demultiplexed CMOS mode CLKOUTA and CLKOUTB will toggle at 1/2 the frequency of the encode signal. Both the A bus and the B bus may be latched on the rising edge of CLKOUTA or the falling edge of CLKOUTB.

Digital Output Randomizer

Interference from the ADC digital outputs is sometimes unavoidable. Interference from the digital outputs may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can result in discernible unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized, trading a slight increase in the noise floor for a large reduction in unwanted tone amplitude.

The digital output is “Randomized” by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied; that is, an exclusive-OR operation is applied between the

LSB and all other bits. The LSB, OF and CLKOUT output are not affected. The output Randomizer function is active when the RAND pin is high.

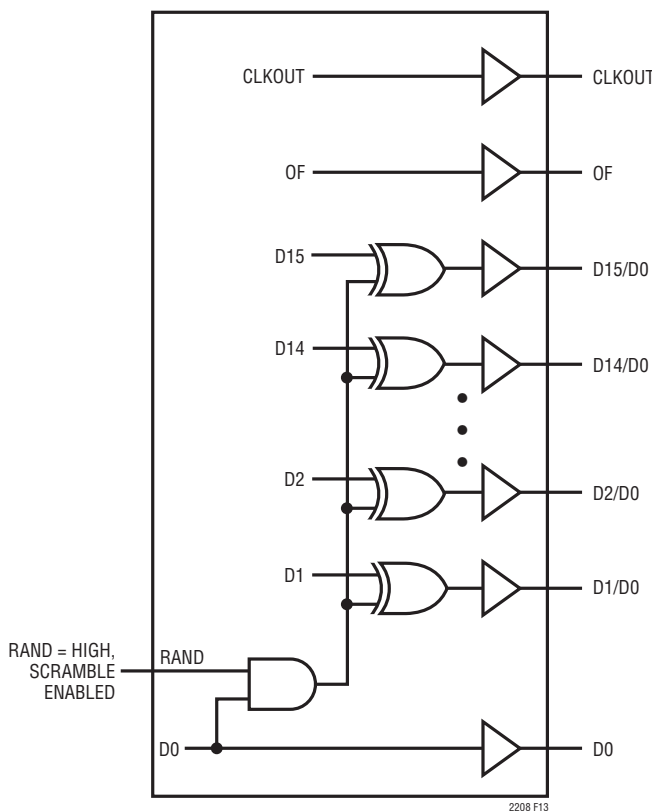
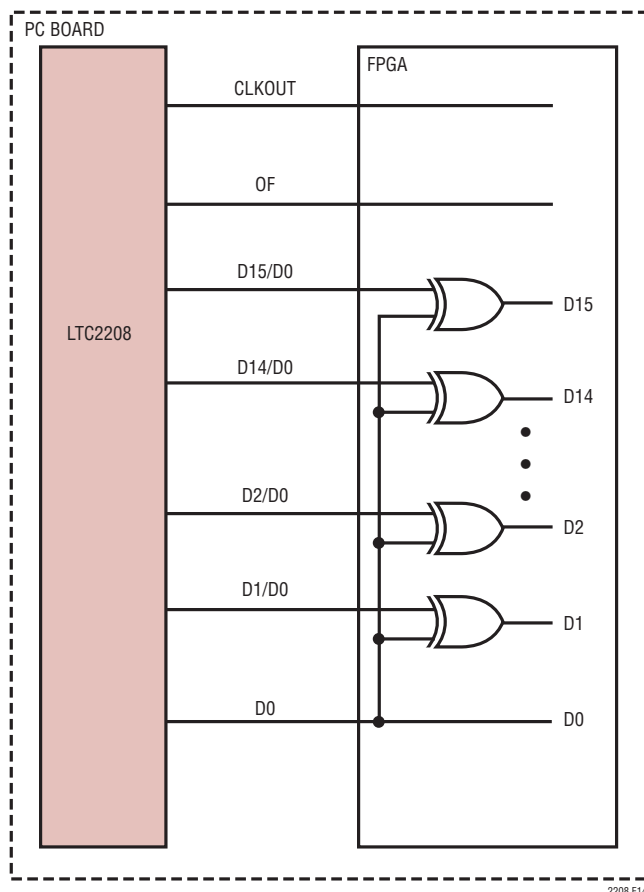


Figure 13. Functional Equivalent of Digital Output Randomizer

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For example, if the converter is driving a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply. In CMOS mode OV_{DD} can be powered with any logic voltage up to the 3.6V. OGND can be powered with any voltage from ground up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}. In LVDS Mode, OV_{DD} should be connected to a 3.3V supply and OGND should be connected to GND.



The LTC2208 is a 16-bit ADC with a very linear transfer function; however, at low input levels even slight imperfections in the transfer function will result in unwanted tones. Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input location on the ADC transfer curve, resulting in improved SFDR for low signal levels.

As shown in Figure 15, the output of the sample-and-hold amplifier is summed with the output of a dither DAC. The dither DAC is driven by a long sequence pseudo-random number generator; the random number fed to the dither DAC is also subtracted from the ADC result. If the dither DAC is precisely calibrated to the ADC, very little of the dither signal will be seen at the output. The dither signal that does leak through will appear as white noise. The dither DAC is calibrated to result in less than 0.5dB elevation in the noise floor of the ADC, as compared to the noise floor with dither off.

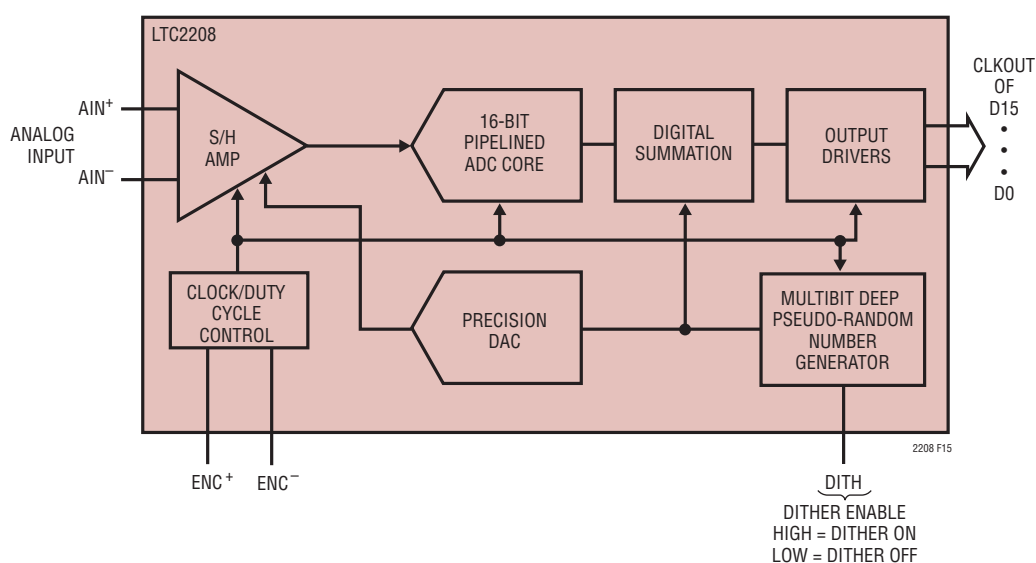


Figure 15. Functional Equivalent Block Diagram of Internal Dither Circuit

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Grounding and Bypassing

The LTC2208 requires a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTC2208 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD} , V_{CM} , and OV_{DD} pins. Bypass capacitors must be located as close to the pins as possible. The traces

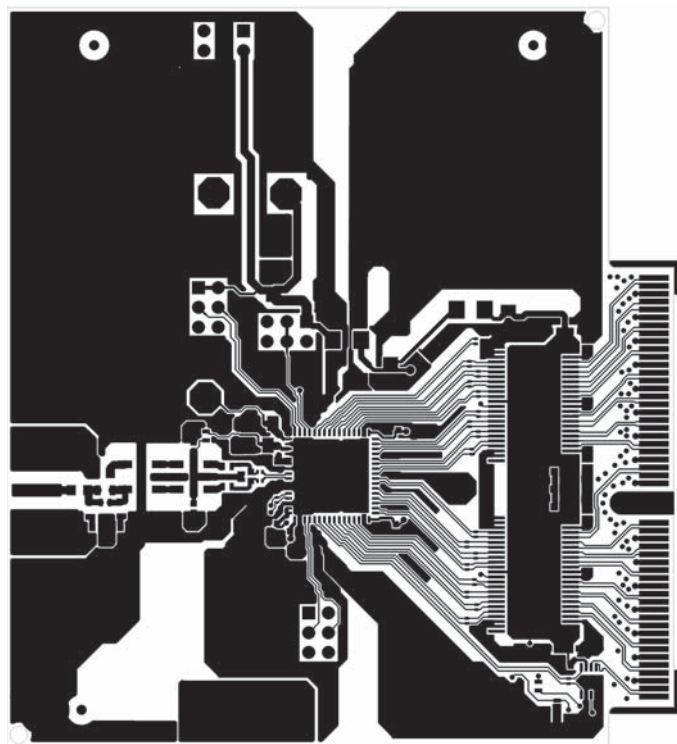
connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2208 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

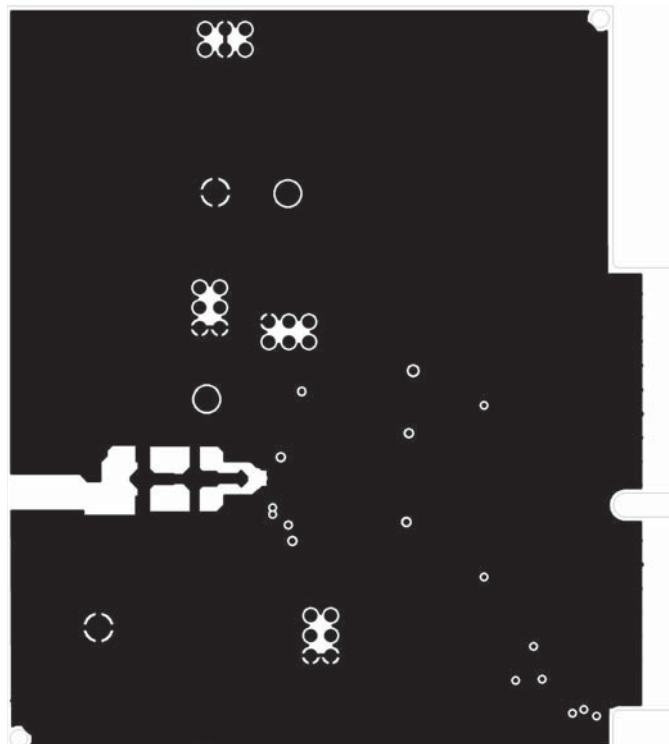
Heat Transfer

Most of the heat generated by the LTC2208 is transferred from the die through the bottom-side exposed pad. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. It is critical that the exposed pad and all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

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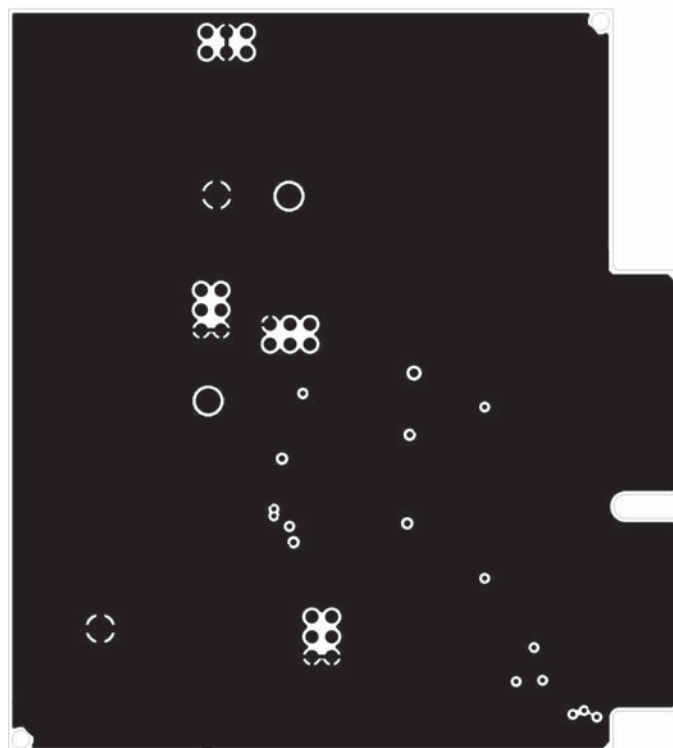


Layer 1 Component Side

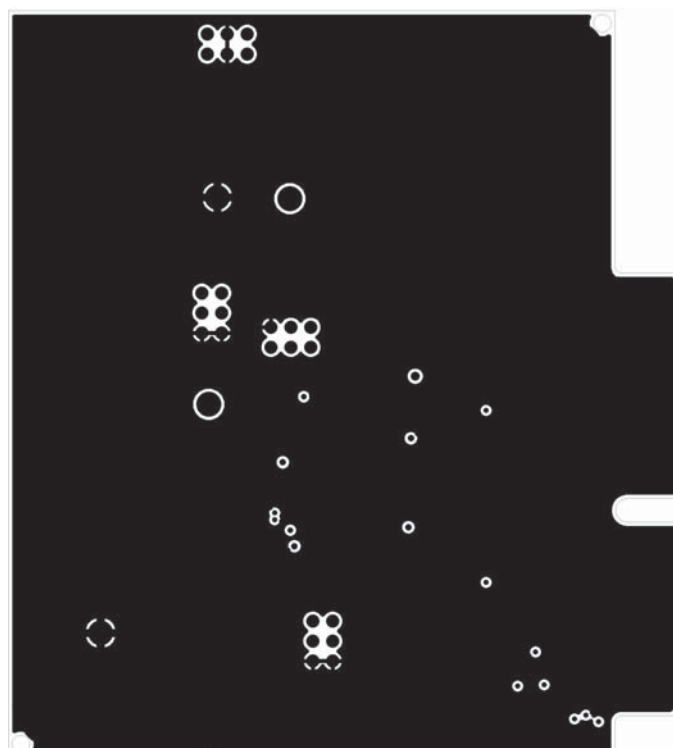


Layer 2 GND Plane

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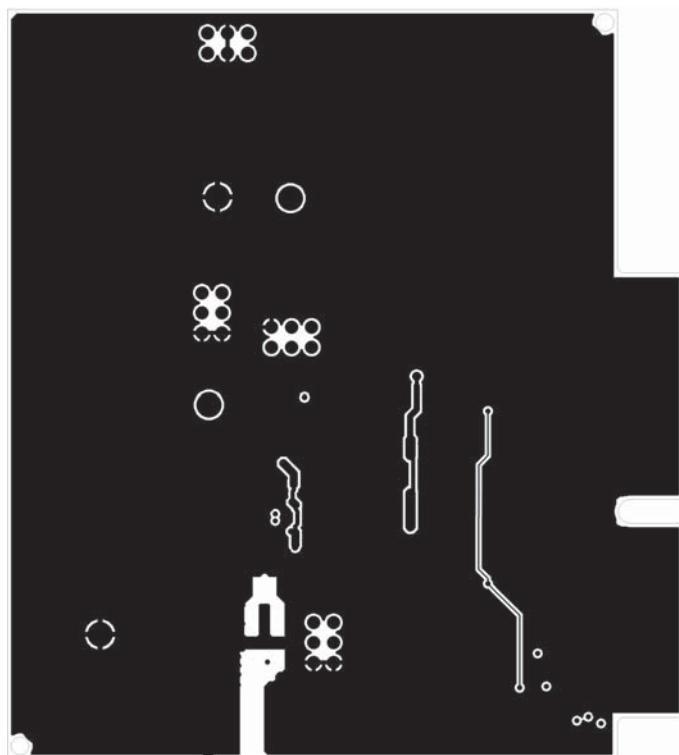


Layer 3 GND



Layer 4 GND

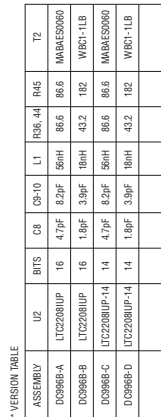
APPLICATIONS INFORMATION



Layer 5 GND

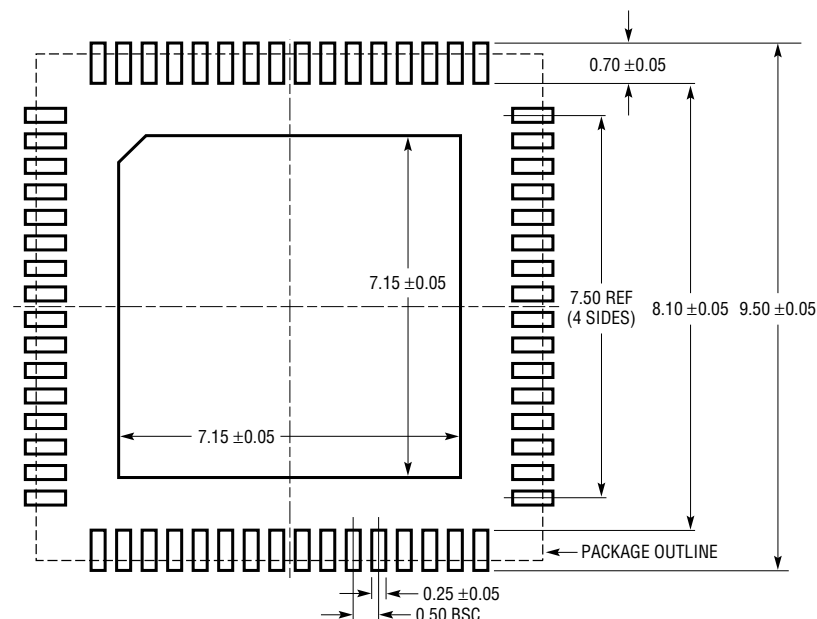


Layer 6 Bottom Side

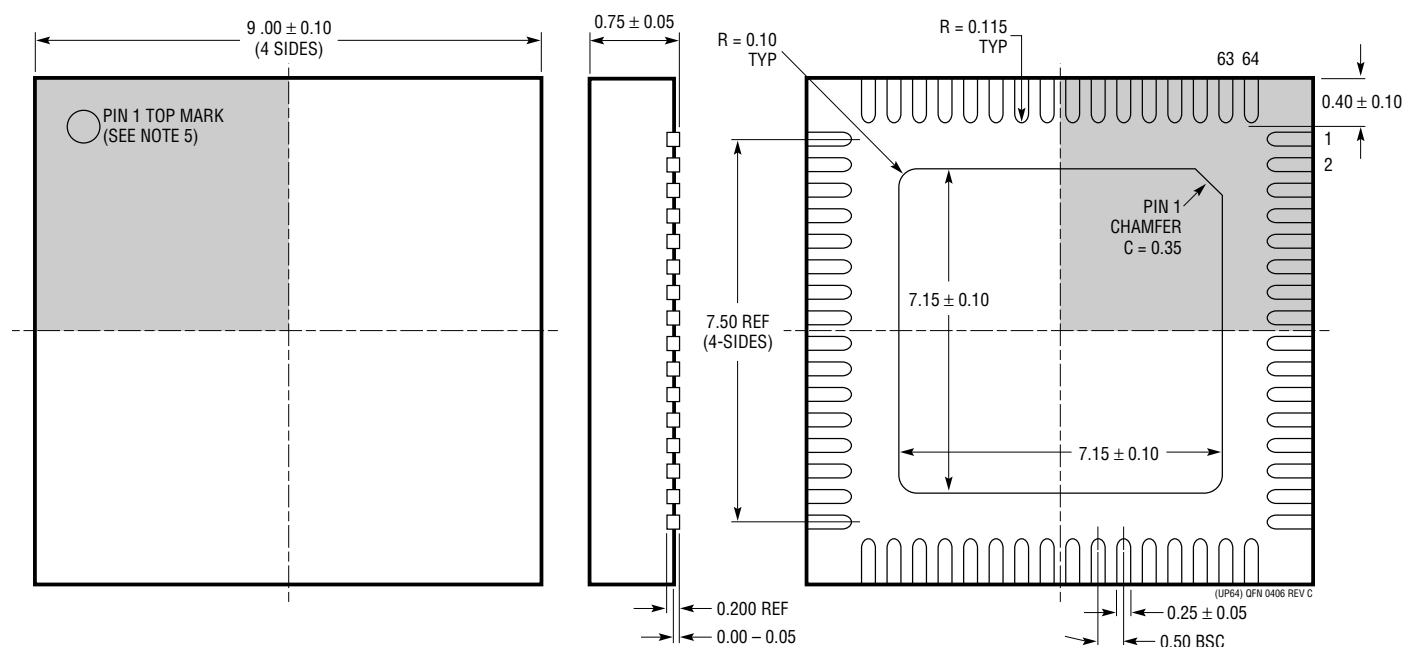


PACKAGE DESCRIPTION

UP Package
64-Lead Plastic QFN (9mm × 9mm)
 (Reference LTC DWG # 05-08-1705 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:

1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WNJR-5
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
6. DRAWING NOT TO SCALE

BOTTOM VIEW—EXPOSED PAD

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1747	12-Bit, 80Msps ADC	72dB SNR, 87dB SFDR, 48-Pin TSSOP Package
LTC1748	14-Bit, 80Msps ADC	76.3dB SNR, 90dB SFDR, 48-Pin TSSOP Package
LTC1749	12-Bit, 80Msps Wideband ADC	Up to 500MHz IF Undersampling, 87dB SFDR
LTC1750	14-Bit, 80Msps Wideband ADC	Up to 500MHz IF Undersampling, 90dB SFDR
LT1993	High Speed Differential Op Amp	600MHz BW, 75dBc Distortion at 70MHz
LTC2202	16-Bit, 10Msps ADC	150mW, 81.6dB SNR, 100dB SFDR
LTC2203	16-Bit, 25Msps ADC	230mW, 81.6dB SNR, 100dB SFDR
LTC2204	16-Bit, 40Msps ADC	470mW, 79dB SNR, 100dB SFDR
LTC2205	16-Bit, 65Msps ADC	530mW, 79dB SNR, 100dB SFDR
LTC2206	16-Bit, 80Msps ADC	725mW, 77.9dB SNR, 100dB SFDR
LTC2207	16-Bit, 105Msps ADC	900mW, 77.9dB SNR, 100dB SFDR
LTC2208	16-Bit, 130Msps ADC	1250mW, 77.7dB SNR, 100dB SFDR
LTC2220	12-Bit, 170Msps ADC	890mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2220-1	12-Bit, 185Msps ADC	910mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2249	14-Bit, 65Msps ADC	230mW, 73dB SNR, 5mm × 5mm QFN Package
LTC2250	10-Bit, 105Msps ADC	320mW, 61.6dB SNR, 5mm × 5mm QFN Package
LTC2251	10-Bit, 125Msps ADC	395mW, 61.6dB SNR, 5mm × 5mm QFN Package
LTC2252	12-Bit, 105Msps ADC	320mW, 70.2dB SNR, 5mm × 5mm QFN Package
LTC2253	12-Bit, 125Msps ADC	395mW, 70.2dB SNR, 5mm × 5mm QFN Package
LTC2254	14-Bit, 105Msps ADC	320mW, 72.5dB SNR, 5mm × 5mm QFN Package
LTC2255	14-Bit, 125Msps ADC	395mW, 72.4dB SNR, 5mm × 5mm QFN Package
LTC2299	Dual 14-Bit, 80Msps ADC	445mW, 73dB SNR, 9mm × 9mm QFN Package
LT5512	DC-3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 21dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	450MHz 1dB BW, 47dB OIP3, Digital Gain Control 10.5dB to 33dB in 1.5dB/Step
LT5522	600MHz to 2.7GHz High Linearity Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports