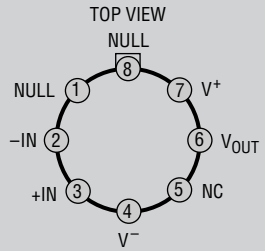
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 2) ..... Indefinite
Specified Temperature Range
LT1220C (Note 3) ..... 0°C to 70°C
LT1220M **(OBSOLETE)** ..... –55°C to 125°C
Operating Temperature Range
LT1220C ..... –40°C TO 85°C
LT1220M **(OBSOLETE)** ..... –55°C to 150°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Ceramic Package **(OBSOLETE)** ..... 175°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

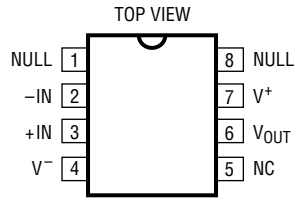
PACKAGE/ORDER INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN
T_{JMAX} = 175°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1220CH
LT1220MH

OBSOLETE PACKAGE
Consider the N8 or S8 Packages for Alternate Source



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N)

S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S)

J8 PACKAGE
8-LEAD CERAMIC DIP
T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J)

ORDER PART NUMBER
LT1220CN8
LT1220CS8
S8 PART MARKING
1220

ORDER PART NUMBER
LT1220MJ8

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)		0.5	1	mV
I_{OS}	Input Offset Current			100	300	nA
I_B	Input Bias Current			100	300	nA
e_n	Input Noise Voltage	f = 10kHz		17		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz		2		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V Differential	20	45 150		MΩ kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range (Positive) Input Voltage Range (Negative)		12	14 –13	 –12	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V	92	114		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	90	94		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±10V, R_L = 500Ω	20	50		V/mV
V_{OUT}	Output Swing	R_L = 500Ω	12	13		±V
I_{OUT}	Output Current	V_{OUT} = ±12V	24	26		mA
SR	Slew Rate	(Note 5)	200	250		V/µs
	Full Power Bandwidth	10V Peak (Note 6)		4		MHz
GBW	Gain-Bandwidth	f = 1MHz		45		MHz

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V		2.5		ns
	Overshoot	$A_V = 1$, 0.1V		5		%
	Propagation Delay	$A_V = 1$, 50% V_{IN} to 50% V_{OUT}, 0.1V		4.9		ns
t_s	Settling Time	10V Step, 0.1% 10V Step, 0.01%		75 95		ns ns
	Differential Gain	f = 3.58MHz, $R_L = 150\Omega$ (Note 7) f = 3.58MHz, R_L = 1k (Note 7)		0.10 0.02		% %
	Differential Phase	f = 3.58MHz, $R_L = 150\Omega$ (Note 7) f = 3.58MHz, R_L = 1k (Note 7)		0.20 0.03		DEG DEG
R_O	Output Resistance	$A_V = 1$, f = 1MHz		1		Ω
I_S	Supply Current			8	10.5	mA

The ● denotes the specifications which apply over the temperature range $0°C \le T_A \le 70°C$, otherwise specifications are at $T_A = 25°C$. $V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	●		0.5	3.5	mV
	Input V_{OS} Drift		●		20		µV/°C
I_{OS}	Input Offset Current		●		100	400	nA
I_B	Input Bias Current		●		100	400	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$	●	92	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	●	86	94		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	●	20	50		V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$	●	12	13		±V
I_{OUT}	Output Current	$V_{OUT} = \pm 12V$	●	24	26		mA
SR	Slew Rate	(Note 5)	●	180	250		V/µs
I_S	Supply Current		●		8	11	mA

The ● denotes the specifications which apply over the temperature range $-55°C \le T_A \le 125°C$, otherwise specifications are at $T_A = 25°C$. $V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	●		0.5	4	mV
	Input V_{OS} Drift		●		20		µV/°C
I_{OS}	Input Offset Current		●		100	800	nA
I_B	Input Bias Current		●		100	1000	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$	●	92	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	●	82	94		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	●	5	50		V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$ R_L = 1k	● ●	10 12	13 13		±V ±V
I_{OUT}	Output Current	$V_{OUT} = \pm 10V$ $V_{OUT} = \pm 12V$	● ●	20 12	26 13		mA mA
SR	Slew Rate	(Note 5)	●	130	250		V/µs
I_S	Supply Current		●		8	11	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: A heat sink may be required when the output is shorted indefinitely.

Note 3: Commercial parts are designed to operate over –40°C to 85°C, but are not tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C to 85°C are available on special request. Consult factory.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

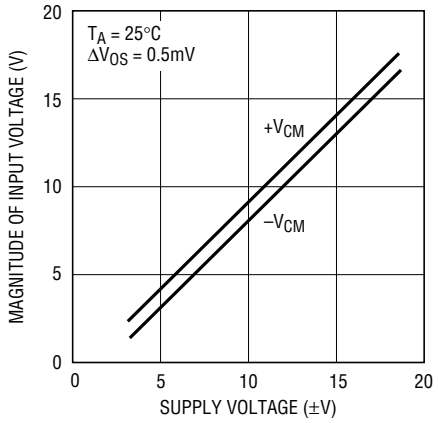
Note 5: Slew rate is measured between ±10V on an output swing of ±12V.

Note 6: FPBW = $SR/2\pi V_P$.

Note 7: Differential Gain and Phase are tested in $A_V = 2$ with five amps in series. Attenuators of 1/2 are used as loads (75Ω, 75Ω and 499Ω, 499Ω).

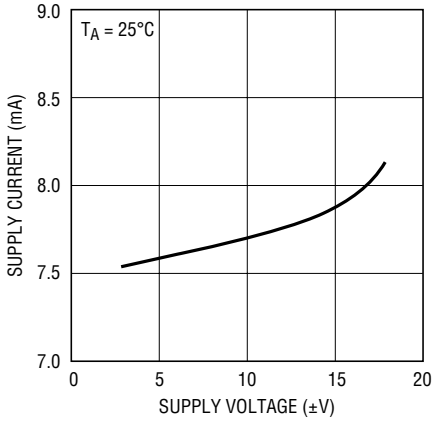
TYPICAL PERFORMANCE CHARACTERISTICS

Input Common Mode Range vs Supply Voltage



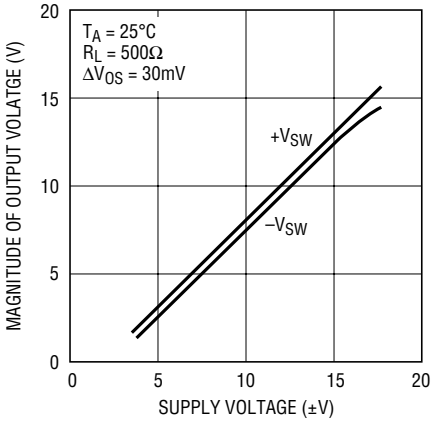
LT1220 • TPC01

Supply Current vs Supply Voltage and Temperature



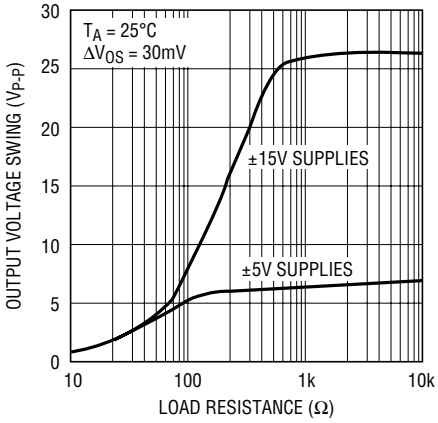
LT1220 • TPC02

Output Voltage Swing vs Supply Voltage



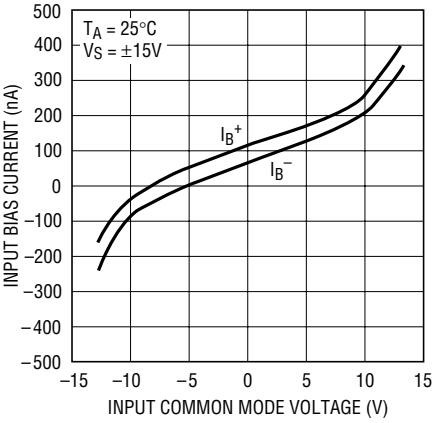
LT1220 • TPC03

Output Voltage Swing vs Resistive Load



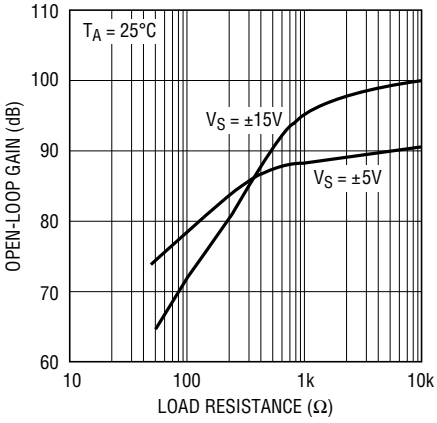
LT1220 • TPC04

Input Bias Current vs Input Common Mode Voltage



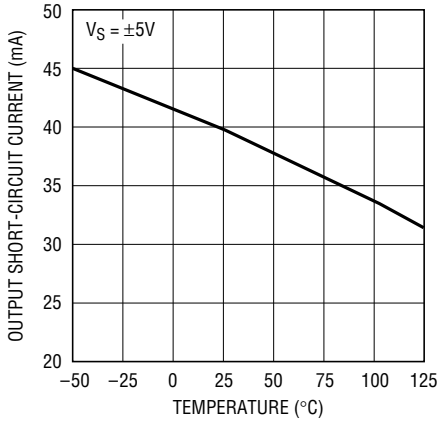
LT1220 • TPC05

Open-Loop Gain vs Resistive Load



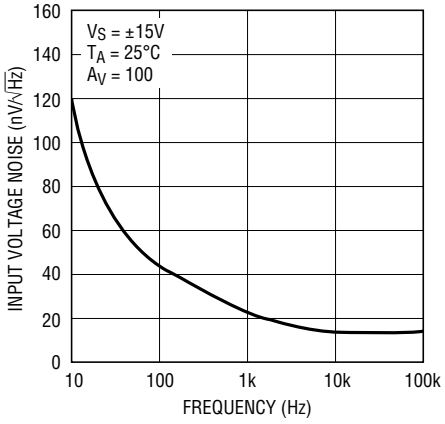
LT1220 • TPC06

Output Short-Circuit Current vs Temperature



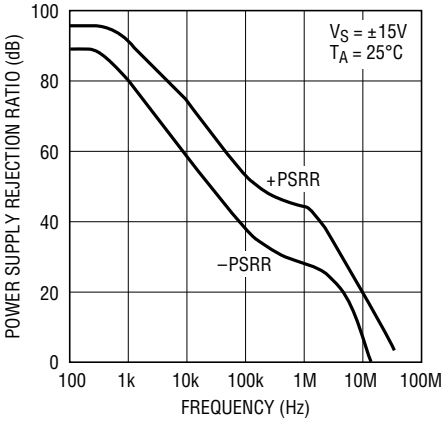
LT1220 • TPC07

Input Noise Spectral Density



LT1220 • TPC08

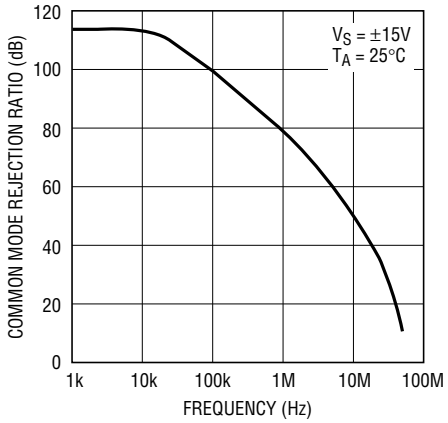
Power Supply Rejection Ratio vs Frequency



LT1220 • TPC09

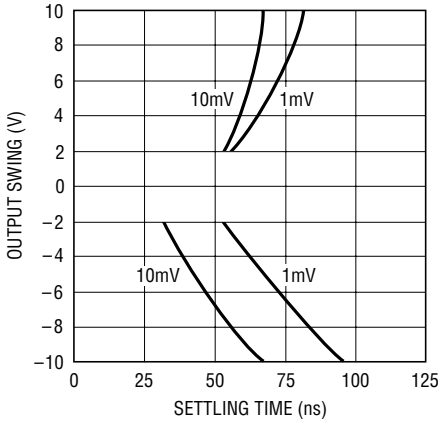
TYPICAL PERFORMANCE CHARACTERISTICS

Common Mode Rejection Ratio vs Frequency



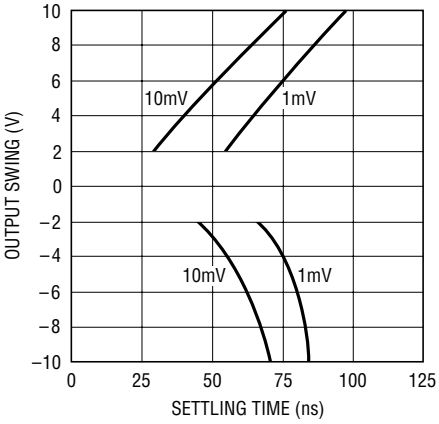
LT1220 • TPC10

Output Swing and Error vs Settling Time (Noninverting)



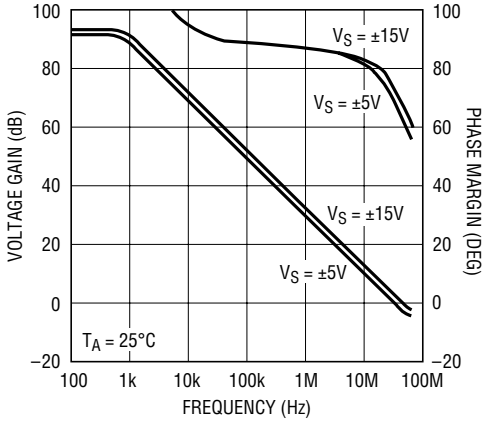
LT1220 • TPC11

Output Swing and Error vs Settling Time (Inverting)



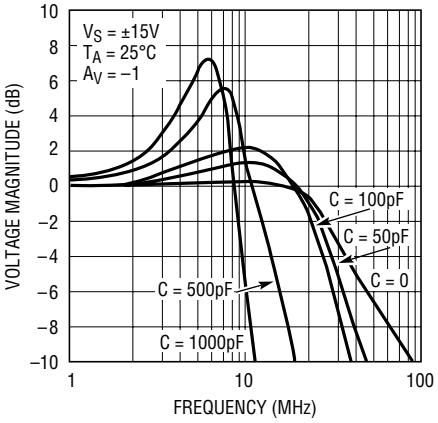
LT1220 • TPC12

Voltage Gain and Phase vs Frequency



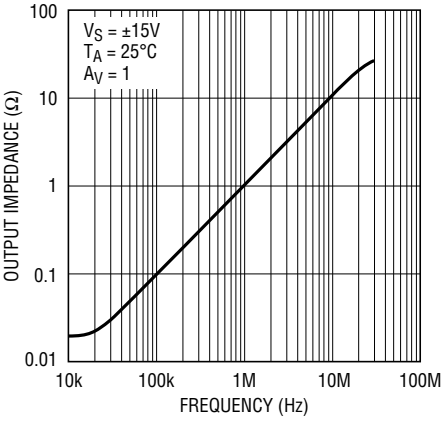
LT1220 • TPC13

Frequency Response vs Capacitive Load



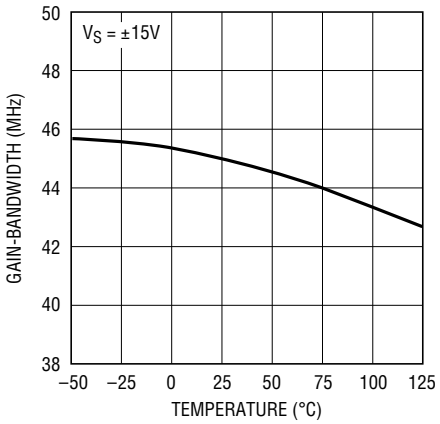
LT1220 • TPC14

Closed-Loop Output Impedance vs Frequency



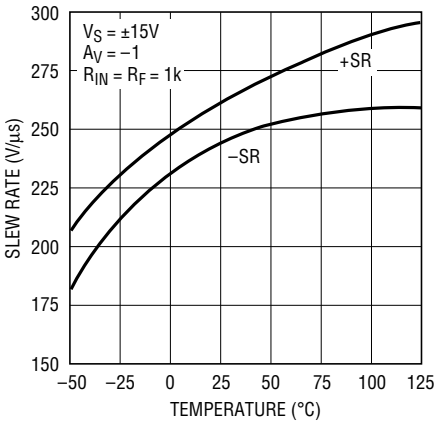
LT1220 • TPC15

Gain-Bandwidth vs Temperature



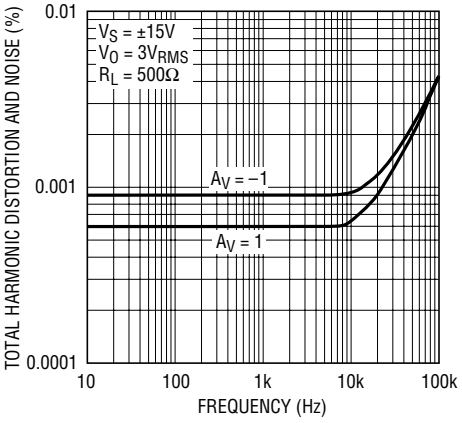
LT1220 • TPC16

Slew Rate vs Temperature



LT1220 • TPC24

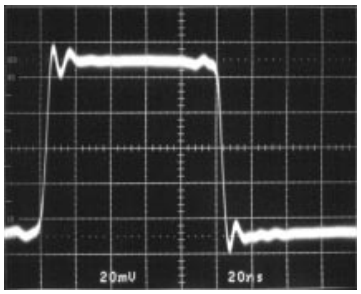
Total Harmonic Distortion vs Frequency



LT1220 • TPC18

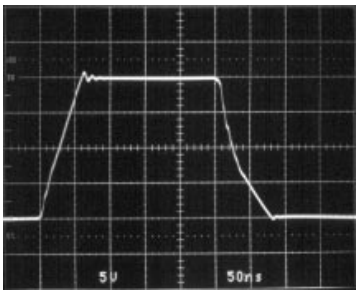
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal, $A_V = 1$



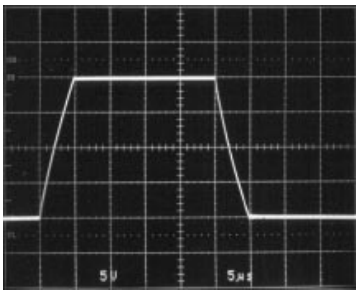
$R_G = 0$ $V_{IN} = 100mV$
$V_S = \pm15V$ $f = 5MHz$
LT1220 • TPC19

Large Signal, $A_V = 1$



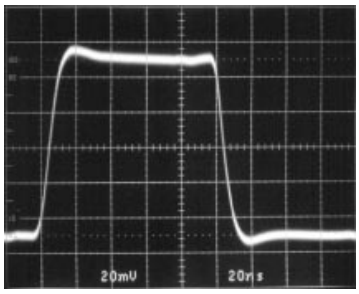
$R_G = 0$ $V_{IN} = 20V$
$V_S = \pm15V$ $f = 2MHz$
LT1220 • TPC20

Large Signal, $A_V = 1$, $C_L = 10,000pF$



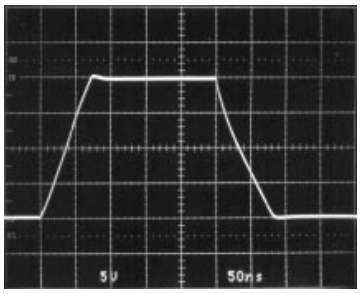
$R_G = 0$ $V_{IN} = 10V$
$V_S = \pm15V$ $f = 20kHz$
LT1220 • TPC21

Small Signal, $A_V = -1$



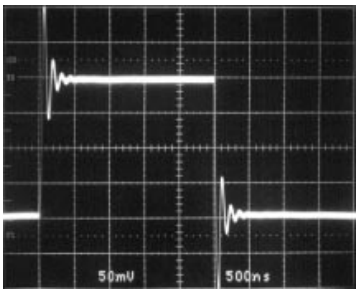
$R_F = R_G = 1k$ $V_{IN} = 100mV$
$V_S = \pm15V$ $f = 5MHz$
LT1220 • TPC22

Large Signal, $A_V = -1$



$R_F = R_G = 1k$ $V_{IN} = 20V$
$V_S = \pm15V$ $f = 2MHz$
LT1220 • TPC23

Small Signal, $A_V = -1$, $C_L = 1,000pF$

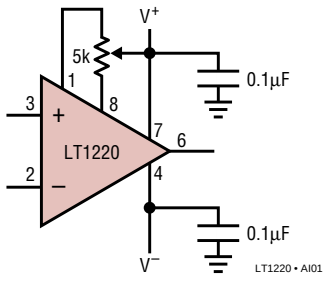


$R_F = R_G = 1k$ $V_{IN} = 200mV$
$V_S = \pm15V$ $f = 200kHz$
LT1220 • TPC24

APPLICATIONS INFORMATION

The LT1220 may be inserted directly into HA2505/15/25, HA2541/2/4, AD817, AD847, EL2020, EL2044 and LM6361 applications, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1220 is shown in the following figure.

Offset Nulling



Layout and Passive Components

The LT1220 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example, fast settling time) use a ground plane, short lead lengths and RF-quality bypass capacitors (0.01µF to 0.1µF). For high driver current applications use low ESR bypass capacitors (1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. Feedback resistors greater than 5k are not recommended because a pole is formed with the input capacitance which can cause peaking or oscillations.

APPLICATIONS INFORMATION

Input Considerations

Bias current cancellation circuitry is employed on the inputs of the LT1220 so the input bias current and input offset current have identical specifications. For this reason, matching the impedance on the inputs to reduce bias current errors is not necessary.

Capacitive Loading

The LT1220 is stable with capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease. There will be peaking in the frequency domain as shown in the curve of Frequency Response vs Capacitive Load. The small-signal transient response will have more overshoot as shown in the photo of the small-signal response with 1000pF load. The large-signal response with a 10,000pF load shows the output slew rate being limited to 4V/μs by the short-circuit current. The LT1220 can drive coaxial cable directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

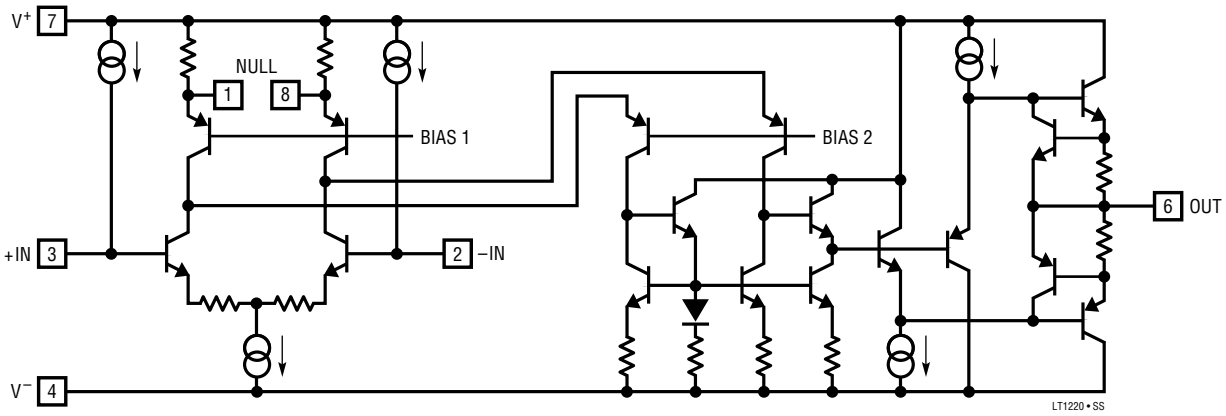
DAC Current-to-Voltage Amplifier

The high gain, low offset voltage, low input bias current, and fast settling of the LT1220 make it particularly useful as an I/V converter for current output DACs. A typical application is shown with a 565A type, 12-bit, 2mA full-scale output current DAC. The 5k resistor around the LT1220 is internal to the DAC and gives a 10V full-scale output voltage. A 5pF capacitor in parallel with the feedback resistor compensates for the DAC output capacitance and improves settling. The output of the LT1220 settles to 1/2LSB (1.2mV) in less than 300ns. The accuracy of this circuit is equal to:

$$V_{ERROR} = V_{OS} + (I_{OS} \bullet 5k\Omega) + (V_{OUT}/A_{VOL})$$

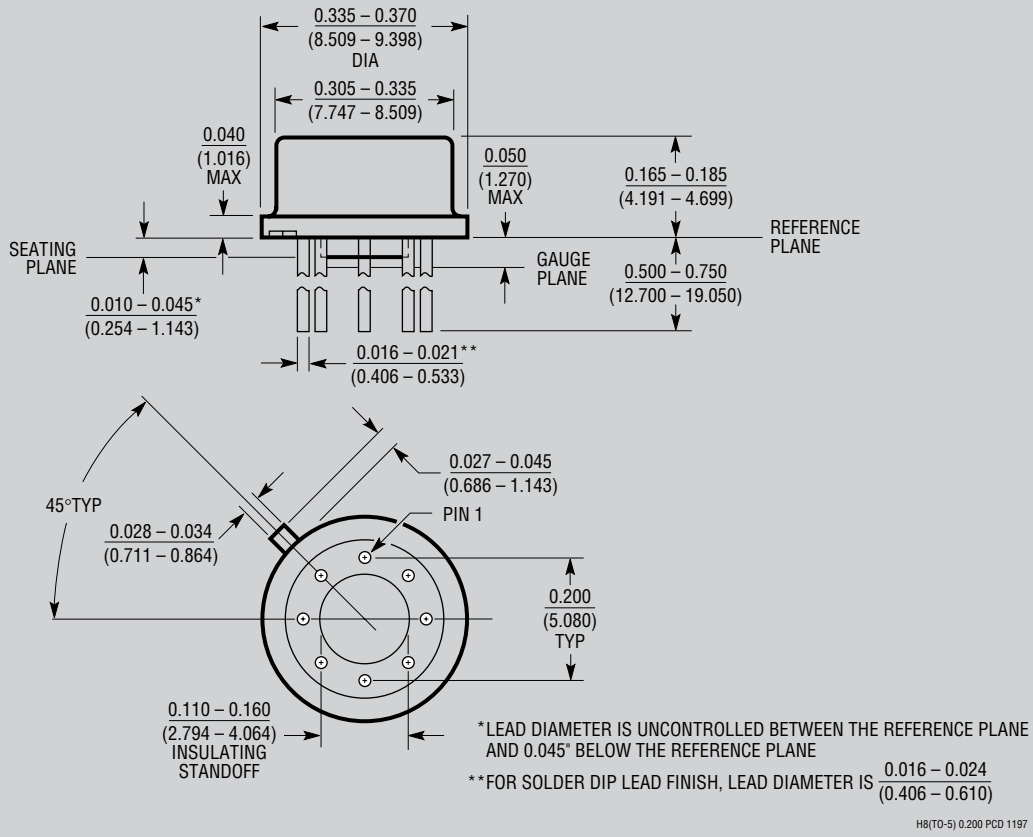
At room temperature the worst-case error is 3mV (1.2LSB). Typically the error is 1.2mV (1/2LSB). Over the commercial temperature range the worse-case error is 6mV (2.5LSB).

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.200 Inch PCD)
(Reference LTC DWG # 05-08-1320)



*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

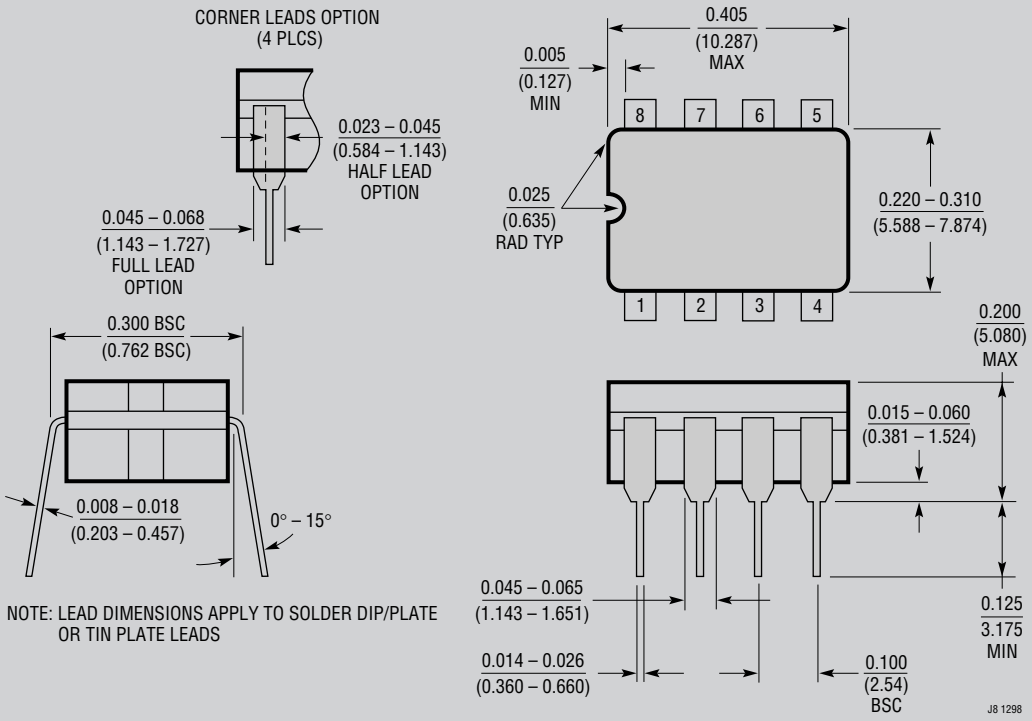
**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

H8(TO-5) 0.200 PCD 1197

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

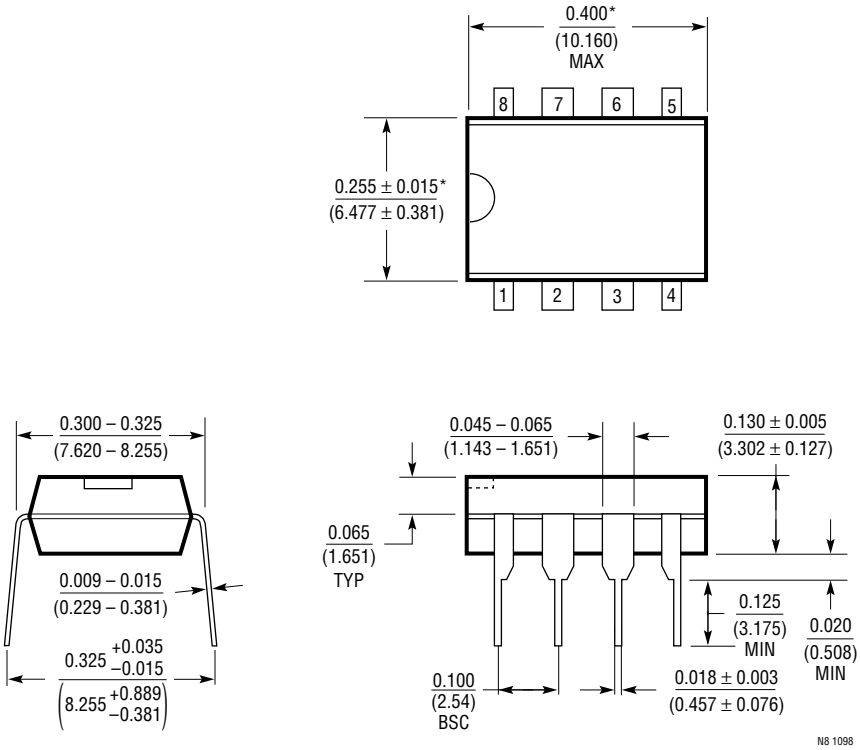
J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

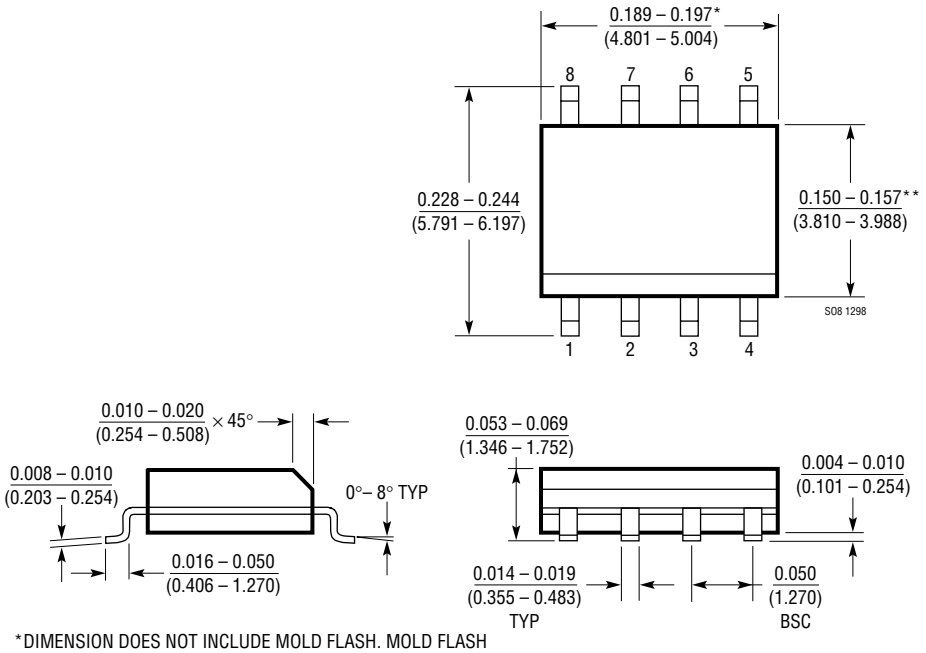
N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

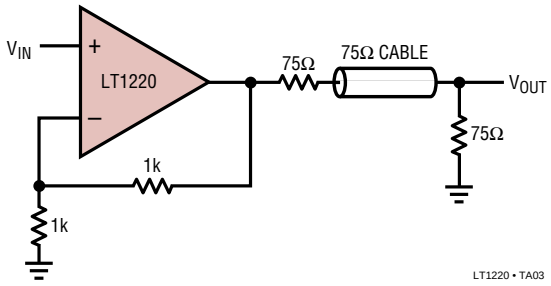


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

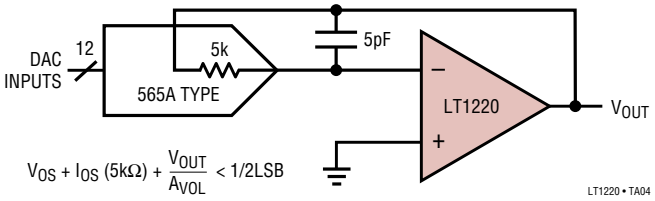
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATIONS

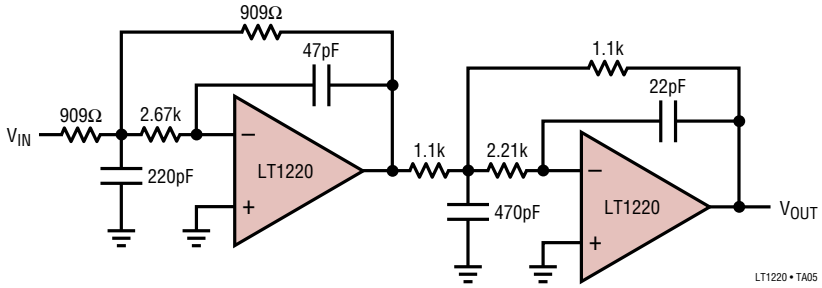
Cable Driver



DAC Current-to-Voltage Converter



1MHz, 4th Order Butterworth Filter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1221	150MHz, 250V/µs Amplifier	$A_V \geq 4$ Version of the LT1220
LT1222	500MHz, 200V/µs Amplifier	$A_V \geq 10$ Version of the LT1220

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