Absolute Maximum Ratings

IO Voltage Range Relative to GND .....-0.5V to +6V
IO Sink Current.....20mA
Operating Temperature Range .....-40°C to +85°C*
Storage Temperature Range.....-40°C to +50°C*

**Storage or operation above +50°C significantly reduces battery life.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{PUP} = +2.8V to +5.25V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Resistance	R_{PUP}	(Notes 1, 2)			2.2	kΩ
Input Capacitance	C_{IO}	(Notes 3, 4)		100	800	pF
Input Load Current	I_L	IO pin at V_{PUP} (Note 5)			10	µA
High-to-Low Switching Threshold (Notes 4, 6, 7, 8)	V_{TL}	V_{PUP} > 4.5V	1.14		2.70	V
			0.71		2.70	
Input Low Voltage	V_{IL}	(Notes 1, 6, 9)			0.30	V
Low-to-High Switching Threshold (Notes 4, 6, 7, 10)	V_{TH}	V_{PUP} > 4.5V	1.00		2.70	V
			0.66		2.70	
Output Low Voltage at 4mA	V_{OL}	(Notes 6, 11)			0.4	V
Recovery Time (Notes 1, 4)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Time-Slot Duration (Notes 1, 12)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	8			
IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE						
Reset Low Time (Notes 1,12)	t_{RSTL}	Standard speed, V_{PUP} > 4.5V	480		640	µs
		Standard speed	**540**		640	
		Overdrive speed, V_{PUP} > 4.5V	48		80	
		Overdrive speed	**58**		80	
Presence-Detect High Time (Note 12)	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	**1.1**		6	
Presence-Detect Low Time (Note 12)	t_{PDL}	Standard speed	60		**270**	µs
		Overdrive speed, V_{PUP} > 4.5V	**7.5**		24	
		Overdrive speed	**7.5**		**32**	
Presence-Detect Sample Time (Notes 1, 4)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		8.6	

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Notes 1, 12, 13)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed, V_{PUP} > 4.5V	6		**15**	
		Overdrive speed	**8.5**		**15**	
Write-One Low Time (Notes 1, 13)	t_{W1L}	Standard speed	5		15	µs
		Overdrive speed	1		2	
IO PIN: 1-Wire READ						
Read Low Time (Notes 1, 14)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read Sample Time (Notes 1, 14)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
REAL-TIME CLOCK						
Frequency Deviation	Δ_F	-5°C to +46°C	-48		+46	ppm
TEMPERATURE CONVERTER						
Tempcore Operating Range	T_{TC}		-40		+85	°C
Conversion Time	t_{CONV}		19		90	ms
Thermal Response Time Constant	τ_{RESP}	(Note 15)		130		s
Conversion Error (Notes 16, 17)	$\Delta\vartheta$	-40°C to < -30°C	-1.3		+1.3	°C
		-30°C to +70°C	-1.0		+1.0	
		> +70°C to +85°C	-1.3		+1.3	
Number of Conversions	N_{CONV}	(Notes 4, 18)	(See the lifetime graphs.)			—

Note 1: System requirement.

Note 2: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2480B may be required.

Note 3: Capacitance on IO could be 800pF when power is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5µs after V_{PUP} has been applied, the parasite capacitor does not affect normal communication.

Note 4: These values are derived from simulation across process, voltage, and temperature and are not production tested.

Note 5: Input load is to ground.

Note 6: All voltages are referenced to ground.

Note 7: V_{TL} and V_{TH} are functions of the internal supply voltage, which is a function of V_{PUP} and the 1-Wire recovery times. The V_{TH} and V_{TL} maximum specifications are valid at V_{PUP} = 5.25V. In any case, $V_{TL} < V_{TH} < V_{PUP}$.

Note 8: Voltage below which, during a falling edge of IO, a logic 0 is detected.

Note 9: The voltage on IO must be less than or equal to V_{ILMAX} whenever the master drives the line low.

Note 10: Voltage above which, during a rising edge on IO, a logic 1 is detected.

Note 11: The I-V characteristic is linear for voltages less than 1V.

Note 12: Numbers in **bold** are **not** in compliance with the published iButton device standards. See the *Comparison Table*.

Note 13: ε in Figure 15 represents the time required for the pullup circuitry to pull the voltage on the IO pin up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.

Note 14: δ in Figure 15 represents the time required for the pullup circuitry to pull the voltage on the IO pin up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

Note 15: This number was derived from a test conducted by Cemagref in Antony, France, in July 2000. http://www.cemagref.fr/English/index.htm Test Report No. E42

Note 16: Total accuracy is $\Delta\vartheta$ plus 0.25°C quantization due to the 0.5°C digital resolution of the device.

Electrical Characteristics (continued)

Note 17: **WARNING:** Maxim data-logger products are 100% tested and calibrated at time of manufacture to ensure that they meet all data sheet parameters, including temperature accuracy. As with any sensor-based product, user shall be responsible for occasionally rechecking the temperature accuracy of the product to ensure it is still operating properly. Furthermore, as with all products of this type, when deployed in the field and subjected to handling, harsh environments, or other hazards/use conditions, there may be some extremely small but nonzero logger failure rate. In applications where the failure of any logger is a concern, user shall assure that redundant (or other primary) methods of testing and determining the handling methods, quality, and fitness of the articles and products are implemented to further mitigate any risk.

Note 18: The number of temperature conversions (= samples) possible with the built-in energy source depends on the operating and storage temperature of the device. When not in use for a mission, the RTC oscillator should be turned off and the device should be stored at a temperature not exceeding +25°C. Under this condition the shelf life time is 10 years minimum.

Comparison Table

PARAMETER	LEGACY VALUES				DS1921G VALUES			
	STANDARD SPEED (µs)		OVERDRIVE SPEED (µs)		STANDARD SPEED (µs)		OVERDRIVE SPEED (µs)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (including t_{REC})	61	(undefined)	7	(undefined)	65*	(undefined)	8*	(undefined)
t_{RSTL}	480	(undefined)	48	80	**540**	640	**58**	80
t_{PDH}	15	60	2	6	15	60	**1.1**	6
t_{PDL}	60	240	8	24	60	**270**	**7.5**	**32**
t_{W0L}	60	120	6	16	60	120	**8.5**	**15**

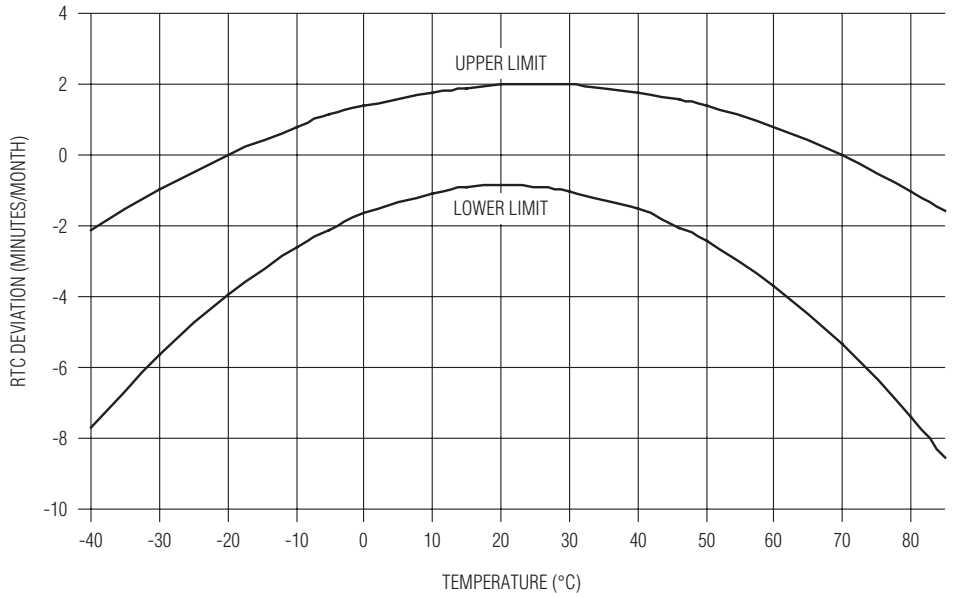
**Intentional change; longer recovery time between time slots.*

Note: *Numbers in* ***bold*** *are* ***not*** *in compliance with the published iButton device standards.*

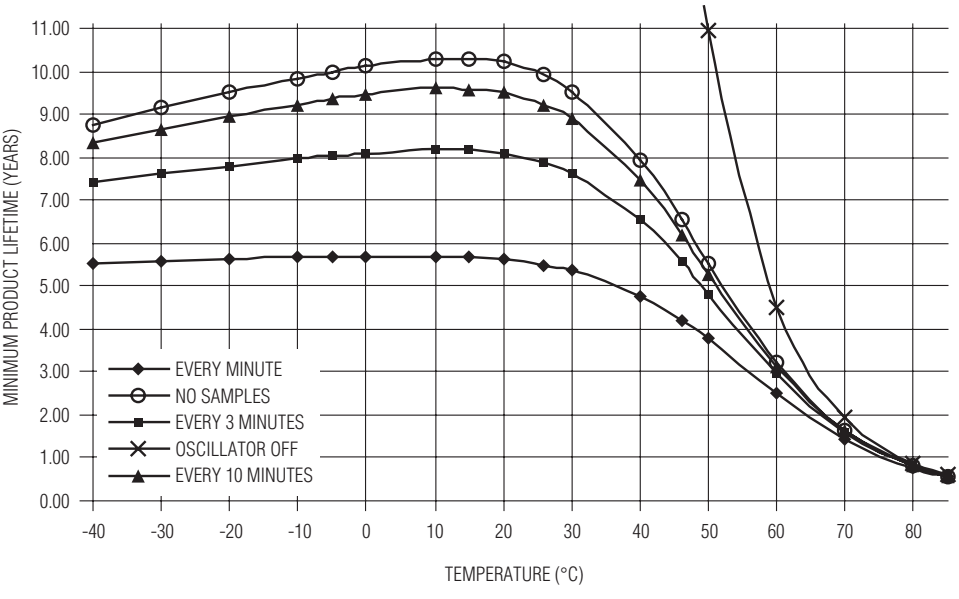
iButton Can Physical Specification

SIZE	See the *Package Information* section.
WEIGHT	Ca. 3.3g

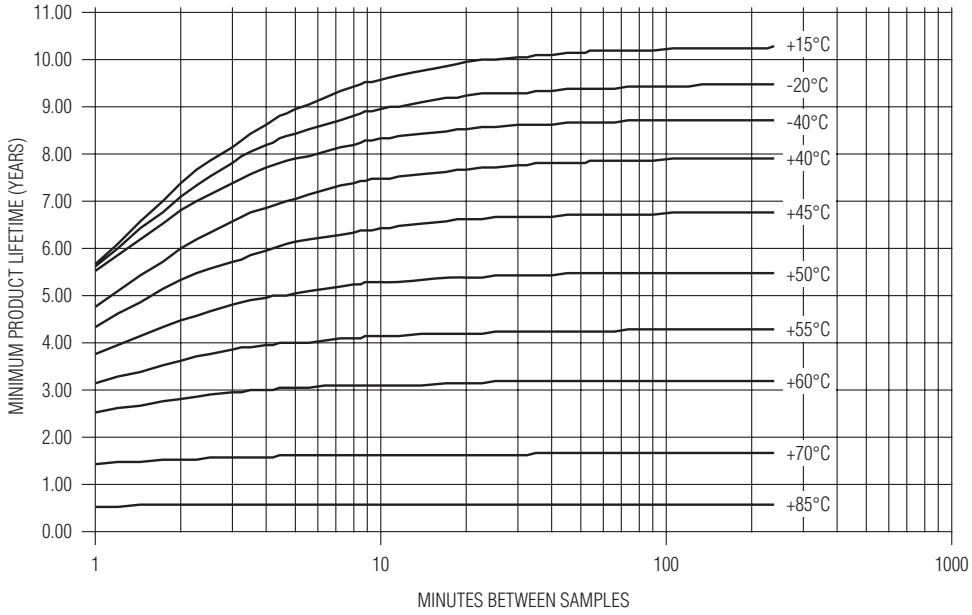
RTC Deviation vs. Temperature



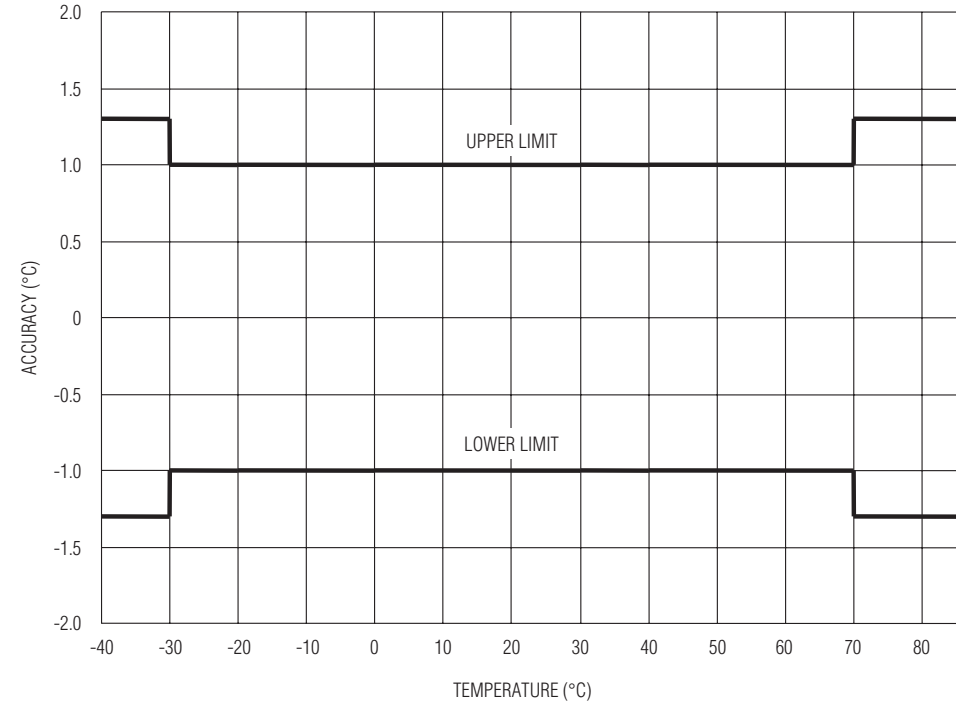
Minimum Product Lifetime vs. Temperature at Different Sample Rates



Minimum Product Lifetime vs. Sample Rate at Different Temperatures



Accuracy Limits



Detailed Description

The DS1921G is an ideal device to monitor the temperature of any object it is attached to or shipped with, such as perishable goods or containers of temperature-sensitive chemicals. The general-purpose battery-backed SRAM can store an electronic copy of shipping information, date of manufacture and other important data written as clear as well as encrypted files. Note that the initial sealing level of the DS1921G achieves IP56. Aging and use conditions can degrade the integrity of the seal over time, therefore, for applications with significant exposure to liquids, sprays, or other similar environments, it is recommended to place the Thermochron in the DS9107 capsule. The DS9107 provides a watertight enclosure that has been rated to IP68 (refer to Application Note 4126: *Understanding the IP (Ingress Protection) Ratings of iButton Data Loggers and Capsule*).

Overview

Figure 1 shows the relationships between the major control and memory sections of the DS1921G. The device has seven main data components: 64-bit lasered ROM; 256-bit scratchpad; 4096-bit general-purpose SRAM; 256-bit register page of timekeeping, control, and counter registers; 96 bytes of alarm timestamp and duration logging memory; 126 bytes of histogram memory; and 2048 bytes of data-log mem-

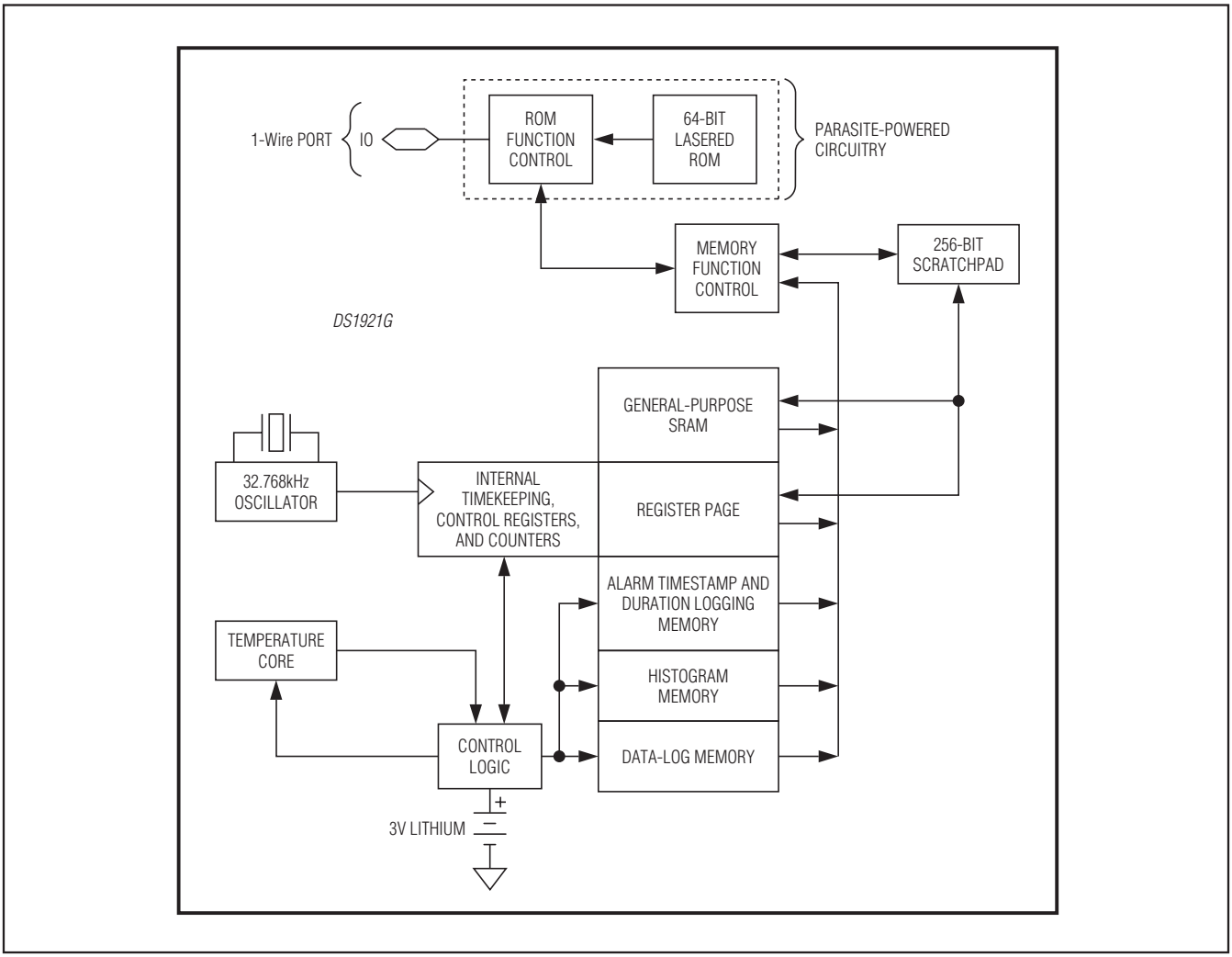


Figure 1. Block Diagram

ory. Except for the ROM and the scratchpad, all other memory is arranged in a single linear address space. All memory reserved for logging purposes, including counter registers and several other registers, is read-only for the user. The timekeeping and control registers are write protected while the device is programmed for a mission.

The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Conditional Search ROM, Skip ROM, Overdrive-Skip ROM, or Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters overdrive mode, where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 13. After a ROM function command is successfully executed, the memory functions become accessible and the master can provide any one of the seven available commands. The protocol for these memory function commands is described in Figure 10. **All data is read and written least significant bit first.**

Parasite Power

Figure 1 shows the parasite-powered circuitry. This circuitry "steals" power whenever the IO input is high. IO provides sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) By parasiting off this input, battery power is not consumed for 1-Wire ROM function commands, and 2) if the battery is exhausted for any reason, the ROM may still be read normally. The remaining circuitry of the DS1921G is solely operated by battery energy. As a consequence, if the battery is exhausted, all memory data is lost including the data of the last mission, and no new mission can be started. Refer to Application Note 5057: *OneWireViewer Tips and Tricks* for how to check the battery status.

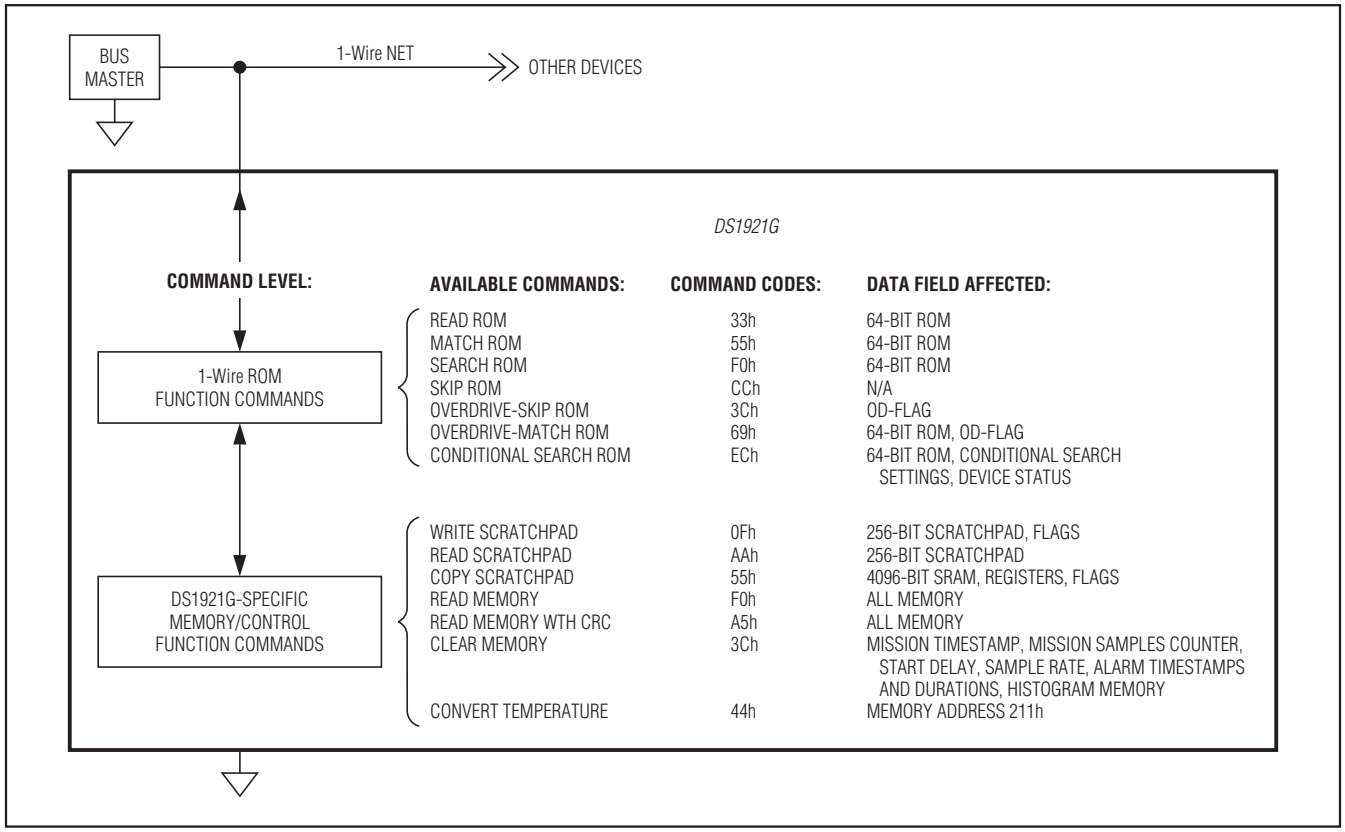


Figure 2. Hierarchical Structure for 1-Wire Protocol

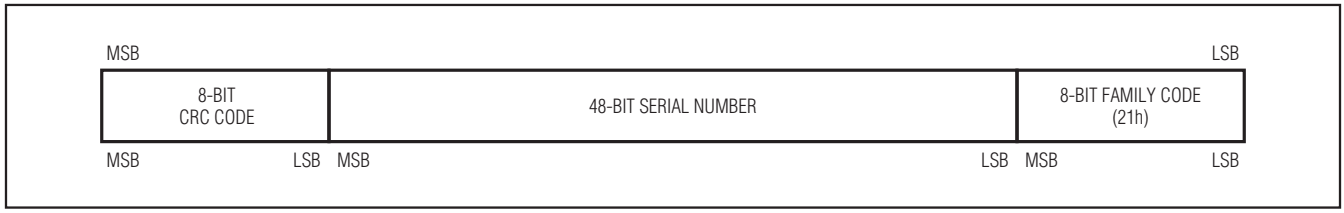


Figure 3. 64-Bit Lasered ROM

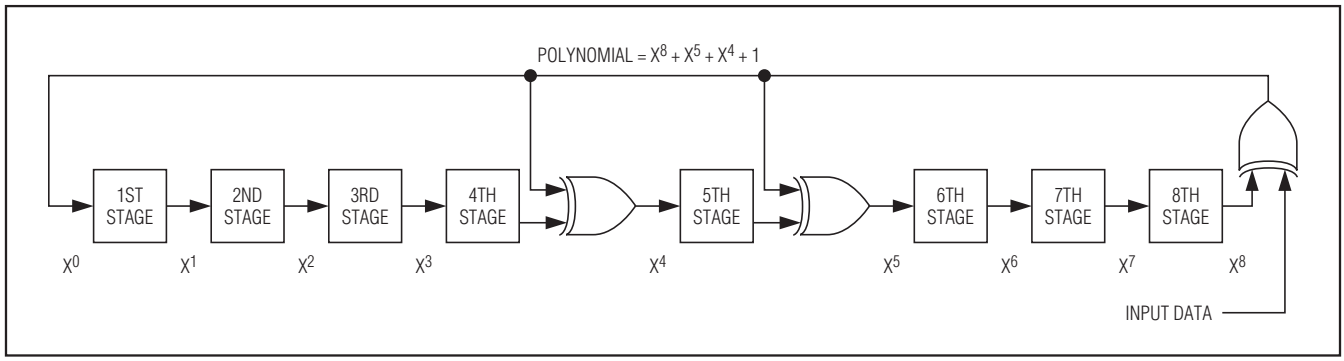


Figure 4. 1-Wire CRC Generator

64-Bit Lasered ROM

Each DS1921G contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits (see Figure 3 for details). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products*.

The Shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is then entered. After the 48th bit of the serial number has been entered, the Shift register contains the CRC value. Shifting in the 8 bits of CRC returns the Shift register to all zeros.

Memory

Figure 5 shows the DS1921G memory map. The 4096-bit general-purpose SRAM makes up pages 0 to 15. The timekeeping, control, and counter registers fill page 16, called register page (see Figure 6). Pages 17, 18, and 19 are assigned to storing the alarm timestamps and durations. The temperature histogram bins begin at page 64 and use up to four pages. The data-log memory covers pages 128 to 191. Memory pages 20 to 63, 68 to 127, and 192 to 255 are reserved for future extensions. The scratchpad is an additional page that acts as a buffer when writing to the SRAM or the register page. The memory pages 17 and higher are read only for the user. They are written to or erased solely under the supervision of the on-chip control logic.

ADDRESS	32-BYTE INTERMEDIATE STORAGE SCRATCHPAD	
0000h to 01FFh	**GENERAL-PURPOSE SRAM (16 PAGES)**	PAGES 0 to 15
0200h to 021Fh	**32-BYTE REGISTER PAGE**	PAGE 16
0220h to 027Fh	**ALARM TIMESTAMPS AND DURATIONS**	PAGES 17 to 19
0280h to 07FFh	(RESERVED FOR FUTURE EXTENSIONS)	PAGES 20 to 63
0800h to 087Fh	**TEMPERATURE HISTOGRAM MEMORY**	PAGES 64 to 67
0880h to 0FFFh	(RESERVED FOR FUTURE EXTENSIONS)	PAGES 68 to 127
1000h to 17FFh	**DATA-LOG MEMORY (64 PAGES)**	PAGES128 to 191
1800h to 1FFFh	(RESERVED FOR FUTURE EXTENSIONS)	PAGES 192 to 255

Figure 5. Memory Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	ACCESS*	
0200h	0	10 Seconds			Single Seconds				RTC Registers	R/W	R/W**
0201h	0	10 Minutes			Single Minutes						
0202h	0	12/24	20 Hour AM/PM	10 Hour	Single Hours						
0203h	0	0	0	0	0	Day of Week					
0204h	0	0	10 Date		Single Date						
0205h	CENT	0	0	10 Months	Single Months						
0206h	10 Years				Single Years						
0207h	MS	10 Seconds Alarm			Single Seconds Alarm				RTC Alarm Registers	R/W	R/W**
0208h	MM	10 Minutes Alarm			Single Minutes Alarm						
0209h	MH	12/24	20 Hour AM/PM Alarm	10 Hour Alarm	Single Hours Alarm						
020Ah	MD	0	0	0	0	Day of Week Alarm					
020Bh	Temperature Low Alarm Threshold								Temperature Alarms	R/W	R/W**
020Ch	Temperature High Alarm Threshold										
020Dh	Number of Minutes Between Temperature Conversions								Sample Rate	R/W	R**
020Eh	$\overline{EOSC}$	EMCLR	0	$\overline{EM}$	RO	TLS	THS	TAS	Control	R/W	R/W**
020Fh	(No function, reads 00h)								—	R	R**

**The left entry in the ACCESS column is valid between missions. The right entry shows the applicable access mode while a mission is in progress.*

***While a mission is in progress, these addresses can be read. The first attempt to write to these registers (even read-only ones), however, ends the mission and overwrites selected writable registers.*

Figure 6. Register Pages Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	ACCESS*	
0210h	(No function, reads 00h)								—	R	R**
0211h	Temperature Read-Out (Forced Conversion)								Temperature	R	R**
0212h	Low Byte								Mission Start Delay	R/W	R/W**
0213h	High Byte										
0214h	$\overline{TCB}$	MEMCLR	MIP	SIP	0	TLF	THF	TAF	Status	R/W	R/W
0215h	Minutes								Mission Timestamp	R	R
0216h	Hours										
0217h	Date										
0218h	Month										
0219h	Year										
021Ah	Low Byte								Mission Samples Counter	R	R
021Bh	Center Byte										
021Ch	High Byte										
021Dh	Low Byte								Device Samples Counter	R	R
021Eh	Center Byte										
021Fh	High Byte										

**The left entry in the ACCESS column is valid between missions. The right entry shows the applicable access mode while a mission is in progress.*

***While a mission is in progress, these addresses can be read. The first attempt to write to these registers (even read-only ones), however, ends the mission and overwrites selected writable registers.*

Figure 6. Register Pages Map (continued)

Detailed Register Descriptions

Timekeeping

The RTC/alarm and calendar information is accessed by reading/writing the appropriate bytes in the register page, address 0200h to 0206h. Note that some bits are set to 0. These bits always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the binary-coded decimal (BCD) format.

RTC/Calendar

The RTC of the DS1921G can run in either 12hr or 24hr mode. Bit 6 of the Hours register (address 0202h) is defined as the 12hr or 24hr mode select bit. When high, the 12hr mode is selected. In the 12hr mode, bit 5 is the AM/PM bit with logic 1 being PM. In the 24hr mode, bit 5 is the 20hr bit (20hr to 23hr).

To distinguish between the days of the week, the DS1921G includes a counter with a range from 1 to 7. The assignment of a counter value to the day of week is arbitrary. Typically, the number 1 is assigned to a Sunday (U.S. standard) or to a Monday (European standard).

The calendar logic is designed to automatically compensate for leap years. For every year value that is either 00 or a multiple of four, the device adds a 29th of February. This works correctly up to (but not including) the year 2100.

The DS1921G is Y2K compliant. Bit 7 (CENT) of the Months register at address 0205h serves as a century flag. When the Year register rolls over from 99 to 00, the century flag toggles. It is recommended to write the century bit to a 1 when setting the RTC to a time/date between the years 2000 and 2099.

RTC and RTC Alarm Registers Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0200h	0	10 Seconds			Single Seconds			
0201h	0	10 Minutes			Single Minutes			
0202h	0	12/24	20 Hour AM/PM	10 Hour	Single Hours			
0203h	0	0	0	0	0	Day of Week		
0204h	0	0	10 Date		Single Date			
0205h	CENT	0	0	10 Months	Single Months			
0206h	10 Years				Single Years			
0207h	MS	10 Seconds Alarm			Single Seconds Alarm			
0208h	MM	10 Minutes Alarm			Single Minutes Alarm			
0209h	MH	12/24	20 Hour AM/PM Alarm	10 Hour Alarm	Single Hours Alarm			
020Ah	MD	0	0	0	0	Day of Week Alarm		

RTC Alarm Control

ALARM REGISTER MASK BITS (BIT 7 OF 0207h TO 20Ah)				FUNCTION
MS	MM	MH	MD	
1	1	1	1	Alarm once per second.
0	1	1	1	Alarm when seconds match (once per minute).
0	0	1	1	Alarm when minutes and seconds match (once every hour).
0	0	0	1	Alarm when hours, minutes, and seconds match (once every day).
0	0	0	0	Alarm when day, hours, minutes, and seconds match (once every week).

RTC Alarms

The DS1921G also contains an RTC alarm function. The RTC Alarm registers are located in registers 0207h to 020Ah. The most significant bit of each of the alarm registers is a mask bit. When all the mask bits are logic 0, an alarm occurs once per week when the values stored in timekeeping registers 0200h to 0203h match the values stored in the RTC Alarm registers. Any alarm sets the timer alarm flag (TAF) in the device's Status register (address 214h). The bus master can set the search conditions in the Control register (address 20Eh) to identify devices with timer alarms by means of the conditional search function (see the *ROM Function Commands* section).

Temperature Alarm Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
020Bh	Temperature Low Alarm Threshold							
020Ch	Temperature High Alarm Threshold							

Sample Rate Register Map

ADDRRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
020Dh	Sample Rate							

Temperature Conversion

The DS1921G measures temperatures with a resolution of 0.5°C. Temperature values are represented in a single byte as an unsigned binary number, which translates into a theoretical range of 128°C. The range, however, has been limited to values from 0000 0000 (00h) through 1111 1010 (FAh). The codes 01h to F9h are considered valid temperature readings.

If a temperature conversion yields a temperature that is out of range, it is recorded as 00h (if too low) or FAh (if too high). Since out-of-range results are accumulated in histogram bins 0 and 62 (see the *Temperature Logging and Histogram* section), the data in these bins is of limited value. For this reason the specified temperature range of the DS1921G is considered to begin at code 04h and end at code F7h, which corresponds to histogram bins 1 to 61.

With T[7…0] representing the decimal equivalent of a temperature reading, the temperature value is calculated as

$$\vartheta(°C) = T[7…0]/2 - 40.0$$

This equation is valid for converting temperature readings stored in the data-log memory as well as for data read from the Forced Temperature Conversion Readout register (address 0211h).

To specify the temperature alarm thresholds, this equation needs to be resolved to

$$T[7…0] = 2 \times \vartheta(°C) + 80.0$$

A value of 23°C, for example, thus translates into 126 decimal or 7Eh. This corresponds to the binary patterns 0111 1110, which could be written to a Temperature Alarm register (address 020Bh and 020Ch, respectively).

Sample Rate

The content of the Sample Rate register (address 020Dh) determines how many minutes the temperature conversions are apart from each other during a mission. The sample rate can be any value from 1 to 255, coded as an unsigned 8-bit binary number. If the memory has been cleared (Status register bit MEMCLR = 1) and a mission is enabled (Control register bit $\overline{EM}$ = 0), writing a nonzero value to the Sample Rate register starts a mission. For a full description of the correct sequence of steps to start a temperature-logging mission, see the *Missioning* or *Mission Example: Prepare and Start a New Mission* sections.

Control Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
020Eh	$\overline{EOSC}$	EMCLR	0	$\overline{EM}$	RO	TLS	THS	TAS

Control Register

The DS1921G is set up for its operation by writing appropriate data to its special function registers that are located in the register page. Several functions that are controlled by a single bit only are combined into a single byte called the Control register (address 020Eh). This register can be read and written. If the device is programmed for a mission, writing to the Control register ends the mission and changes the register contents.

The functional assignments of the individual bits are explained below. Bit 5 has no function. It always reads 0 and cannot be written to 1.

Bit 7: Enable Oscillator ($\overline{EOSC}$). This bit controls the crystal oscillator of the RTC. When set to logic 0, the oscillator starts operation. When written to logic 1, the oscillator stops and the device is in a low-power data-retention mode. **This bit must be 0 for normal operation.** The RTC must have advanced at least 1 second before a Mission Start is accepted.

Bit 6: Memory Clear Enable (EMCLR). This bit needs to be set to logic 1 to enable the Clear Memory function, which is invoked as a memory function command. The timestamp, histogram memory as well as the Mission Timestamp, Mission Samples Counter, Mission Start Delay, and Sample Rate are cleared only if the Clear Memory command is issued **with the next access to the device**. The EMCLR bit returns to 0 as the next memory function command is executed.

Bit 4: Enable Mission ($\overline{EM}$). This bit controls whether the DS1921G begins a mission as soon as the sample rate is written. To enable the device for a mission, this bit must be 0.

Bit 3: Rollover Enable/Disable (RO). This bit controls whether the data-log memory is overwritten with new data or whether data logging is stopped once the memory is filled with data during a mission. Setting this bit to a 1 enables the rollover and data logging continues at the beginning, overwriting previously collected data. Clearing this bit to 0 disables the rollover and no further temperature values are stored in the data-log memory once it is filled with data. This does not stop the mission. The device continues measuring temperatures and updating the histogram and alarm timestamps and durations.

Bit 2: Temperature Low Alarm Search (TLS). If this bit is 1, the device responds to a Conditional Search ROM command if, during a mission, the temperature has reached or is lower than the Low Temperature Threshold stored at address 020Bh.

Bit 1: Temperature High Alarm Search (THS). If this bit is 1, the device responds to a Conditional Search ROM command if, during a mission, the temperature has reached or is higher than the High Temperature Threshold stored at address 020Ch.

Bit 0: Timer Alarm Search (TAS). If this bit is 1, the device responds to a Conditional Search ROM command if, during a mission, a timer alarm has occurred. Since a timer alarm cannot be disabled, the TAF flag usually reads 1 during a mission. Therefore, it is advisable to set the TAS bit to a 0, in most cases.

Mission Start Delay Counter

The content of the Mission Start Delay Counter register determines how many minutes the device waits before starting the logging process. The Mission Start Delay value is stored as an unsigned 16-bit integer number at addresses 0212h (low byte) and 0213h (high byte). The maximum delay is 65,535 minutes, equivalent to 45 days, 12 hours, and 15 minutes.

For a typical mission, the Mission Start Delay is 0. If a mission is too long for a single DS1921G to store all temperature readings at the selected sample rate, one can use several devices, staggering the Mission Start Delay to record the full period. In this case, the rollover enable (RO) bit in the Control register (address 020Eh) must be set to 0 to prevent overwriting of the recorded temperature log after the data-log memory is full. See the *Mission Start and Logging Process* section and Figure 11 for details.

Status Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0214h	$\overline{TCB}$	MEMCLR	MIP	SIP	0	TLF	THF	TAF

Status Register

The Status register holds device status information and alarm flags. The register is located at address 0214h. Writing to this register does not necessarily end a mission.

The functional assignments of the individual bits are explained below. The bits MIP, TLF, THF, and TAF can only be written to 0. All other bits are read-only. Bit 3 has no function.

Bit 7: Temperature Core Busy ($\overline{TCB}$). If this bit reads 0, the DS1921G is currently performing a temperature conversion. This temperature conversion is either self-initiated because of a mission being in progress or initiated by a command when a mission is not in progress. The $\overline{TCB}$ bit goes low just before a conversion starts and returns to high just after the result is latched into the Read-Out register at address 0211h.

Bit 6: Memory Cleared (MEMCLR). If this bit reads 1, the memory pages 17 and higher (alarm timestamps/durations, temperature histogram, excluding data-log memory), as well as the Mission Timestamp, Mission Samples Counter, Mission Start Delay, and Sample Rate have been cleared to 0 from executing a Clear Memory function command. The MEMCLR bit returns to 0 as soon as writing a nonzero value to the Sample Rate register starts a new mission, provided that the $\overline{EM}$ bit is also 0. **The memory has to be cleared in order for a mission to start.**

Bit 5: Mission in Progress (MIP). If this bit reads 1, the DS1921G has been set up for a mission and this mission is still in progress. A mission is started if the $\overline{EM}$ bit of the Control register (address 20Eh) is 0 and a nonzero value is written to the Sample Rate register, address 20Dh. The MIP bit returns from logic 1 to logic 0 when a mission is ended. A mission ends with the first write attempt (Copy Scratchpad command) to any register in the address range of 200h to 213h. Alternatively, a mission can be ended by directly writing to the Status register and setting the MIP bit to 0. The MIP bit cannot be set to 1 by writing to the Status register.

BIT 4: Sample in Progress (SIP). If this bit reads 1, the DS1921G is currently performing a temperature conversion as part of a mission in progress. The mission samples occur on the seconds rollover from 59 to 00. The SIP bit changes from 0 to 1 approximately 250ms before the actual temperature conversion begins allowing the circuitry of the chip to wake up. A temperature conversion including a wake-up phase takes maximum 875ms. During this time, read accesses to the memory pages 17 and higher are permissible but can reveal invalid data.

Bit 2: Temperature Low Flag (TLF). Logic 1 in the temperature low flag bit indicates that a temperature measurement during a mission revealed a temperature equal to or lower than the value in the Temperature Low Threshold register. The temperature low flag can be cleared at any time by writing this bit to 0. This flag must be cleared before starting a new mission.

Bit 1: Temperature High Flag (THF). Logic 1 in the temperature high flag bit indicates that a temperature measurement during a mission revealed a temperature equal to or higher than the value in the Temperature High Threshold register. The temperature high flag can be cleared at any time by writing this bit to 0. This flag must be cleared before starting a new mission.

Bit 0: Timer Alarm Flag (TAF). If this bit reads 1, a RTC alarm has occurred (see the *Timekeeping* section for details). The timer alarm flag can be cleared at any time by writing this bit to logic 0. Since the timer alarm cannot be disabled, the TAF flag usually reads 1 during a mission. This flag should be cleared before starting a new mission.

Mission Timestamp Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0215h	0	10 Minutes			Single Minutes			
0216h	0	12/24	20 Hour AM/PM	10 Hour	Single Hours			
0217h	0	0	10 Date		Single Date			
0218h	0	0	0	10 Months	Single Months			
0219h	10 Years				Single Years			

Mission Samples Counter Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
021Ah	Low Byte							
021Bh	Center Byte							
021Ch	High Byte							

Device Samples Counter Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
021Dh	Low Byte							
021Eh	Center Byte							
021Fh	High Byte							

Mission Timestamp

The Mission Timestamp register indicates the time and date of the first temperature conversion of a mission. Subsequent temperature conversions take place as many minutes apart from each other as specified by the value in the Sample Rate register. Mission samples occur on minute boundaries.

Mission Samples Counter

The Mission Samples Counter register indicates how many temperature measurements have taken place during the current mission in progress (if MIP = 1) or during the latest mission (if MIP = 0). The value is stored as an unsigned 24-bit integer number. This counter is reset through the Clear Memory command.

Device Samples Counter

The Device Samples Counter register indicates how many temperature measurements have taken place since the device was assembled at the factory. The value is stored as an unsigned, 24-bit integer number. The maximum number that can be represented in this format is 16,777,215, which is higher than the expected lifetime of the DS1921G. This counter cannot be reset under software control.

Temperature Logging and Histogram

Once set up for a mission, the DS1921G logs the temperature measurements simultaneously byte after byte in the data-log memory as well as in histogram form in the histogram memory. The data-log memory is able to store 2,048 temperature values measured at equidistant time points. The first temperature value of a mission is written to address location 1000h of the data-log memory, the second value to address location 1001h and so on. Knowing the starting time point (Mission Timestamp register), the interval between temperature measurements, the Mission Samples Counter register, and the rollover setting, one can reconstruct the time and date of each measurement stored in the data log.

There are two alternatives to the way the DS1921G behaves after the 2048 bytes of data-log memory is filled with data. With rollover disabled (RO = 0), the device fills the data-log memory with the first 2048 mission samples. Additional mission samples are not logged in the data-log, but the histogram and temperature alarm RAM continue to update. With rollover enabled (RO = 1), the data log wraps around and overwrites previous data starting at 1000h for the every 2049th mission sample. In this mode, the device stores the last 2048 mission samples.

TEMPERATURE READING	TEMPERATURE EQUIVALENT IN °C	HISTOGRAM BIN NUMBER	HISTOGRAM BIN ADDRESS
00h	-40.0 or lower	0	800h to 801h
01h	-39.5	0	800h to 801h
02h	-39.0	0	800h to 801h
03h	-38.5	0	800h to 801h
04h	-38.0	1	802h to 803h
05h	-37.5	1	802h to 803h
06h	-37.0	1	802h to 803h
07h	-36.5	1	802h to 803h
08h	-36.0	2	804h to 805h
…	…	…	…
F3h	+81.5	60	878h to 879h
F4h	+82.0	61	87Ah to 87Bh
F5h	+82.5	61	87Ah to 87Bh
F6h	+83.0	61	87Ah to 87Bh
F7h	+83.5	61	87Ah to 87Bh
F8h	+84.0	62	87Ch to 87Dh
F9h	+84.5	62	87Ch to 87Dh
FAh	+85.0 or higher	62	87Ch to 87Dh

Figure 7. Histogram Bin and Temperature Cross-Reference

For the temperature histogram, the DS1921G provides 63 bins that begin at memory address 0800h. Each bin consists of a 16-bit, nonrolling-over binary counter that is incremented each time a temperature value acquired during a mission falls into the range of the bin. The least significant byte of each bin is stored at the lower address. Bin 0 begins at memory address 0800h, bin 1 at 0802h, and so on up to 087Ch for bin 62, as shown in Figure 7. The number of the bin to be updated after a temperature conversion is determined by cutting off the two least significant bits of the binary temperature value. Out-of-range values are range locked and counted as 00h or FAh.

Since each data bin is 2 bytes, it can increment up to 65,535 times. Additional measurements for a bin that has already reached its maximum value are not counted; the bin counter remains at its maximum value. With the fastest sample rate of one sample every minute, a 2-byte bin is sufficient for up to 45 days if all temperature readings fall into the same bin.

Temperature Alarm Logging

For some applications it is essential to not only record temperature over time and the temperature histogram, but also record **when** exactly the temperature exceeded a predefined tolerance band and for **how long** the temperature stayed outside the desirable range. The DS1921G can log high and low durations. The tolerance band is specified by means of the Temperature Alarm Threshold registers, addresses 20Bh and 20Ch in the register page. One can set a high temperature and low temperature threshold. See the *Temperature Conversion* section for the data format the temperature has to be written in. As long as the temperature values stay within the tolerance band (i.e., are higher than the low threshold and lower than the high threshold), the DS1921G does not record any temperature alarm. If the temperature during a mission reaches or exceeds either threshold, the DS1921G generates an alarm and sets either the temperature high flag (THF) or the temperature low flag (TLF) in the Status register (address

ADDRESS	DESCRIPTION	ALARM EVENT
0220h	Mission Samples Counter, Low Byte	Low Alarm 1
0221h	Mission Samples Counter, Center Byte	
0222h	Mission Samples Counter, High Byte	
0223h	Alarm Duration Counter	
0224h to 0227h	Alarm Timestamp and Duration	Low Alarm 2
0228h to 024Fh	Alarm Timestamp and Durations	Low Alarms 3 to 12
0250h	Mission Samples Counter, Low Byte	High Alarm 1
0251h	Mission Samples Counter, Center Byte	
0252h	Mission Samples Counter, High Byte	
0253h	Alarm Duration Counter	
0254h to 0257h	Alarm Timestamp and Duration	High Alarm 2
0258h to 027Fh	Alarm Timestamp and Durations	High Alarms 3 to 12

Figure 8. Alarm Timestamps and Durations Address Map

214h). This way, if the search conditions (address 20Eh) are set accordingly, the master can quickly identify devices with temperature alarms by means of the conditional search function (see the *ROM Function Commands* section). The device also generates a timestamp of when the alarm occurred and begins recording the duration of the alarming temperature.

Timestamps and durations where the temperature leaves the tolerance band are stored in the address range 0220h to 027Fh, as shown in Figure 8. This allocation allows recording 24 individual alarm events and periods (12 periods for too hot and 12 for too cold). The date and time of each of these periods can be determined from the Mission Timestamp register and the time distance between each temperature reading.

The alarm timestamp is a copy of the Mission Samples Counter register when the alarm first occurred. The least significant byte is stored at the lower address. One address higher than the timestamp, the DS1921G maintains a 1-byte duration counter that stores the number of samples the temperature was found to be beyond the threshold. If this counter has reached its limit after 255 consecutive temperature readings and the temperature has not yet returned to within the tolerance band, the device issues another timestamp at the next higher alarm location and opens another counter to record the duration. If the temperature returns to normal before the counter has reached its limit, the duration counter of the particular timestamp does not increment any further. Should the temperature again cross this threshold, it is recorded at the next available alarm location. This algorithm is implemented for the low temperature thresholds as well as for the high temperature threshold.

Missioning

The typical task of the DS1921G is recording the temperature of a temperature-sensitive object. Before the device can perform this function, it needs to be configured. This procedure is called missioning.

First, the DS1921G must have its RTC set to a valid time and date. This reference time can be UTC (also called GMT, Greenwich Mean Time) or any other time standard that was chosen for the application. The clock must be running ($\overline{EOSC}$ = 0) for at least one second. Setting an RTC alarm is optional. The memory assigned to store the alarm timestamps and durations, temperature histogram, Mission Timestamp, Mission Samples Counter, Mission Start Delay, and Sample Rate must be cleared using the Clear Memory command. In case there were temperature alarms in the previous mission, the TLF and THF flags need to be cleared manually. To enable the device for a mission, the $\overline{EM}$ flag must be set to 0. These are general settings that have to be made regardless of the type of object to be monitored and the duration of the mission.

Next, the low temperature and high temperature thresholds that specify the temperature tolerance band must be defined. The *Temperature Conversion* section describes how to convert a temperature value into the binary code to be written to the threshold registers.

The state of the search condition bits in the Control register does not affect the mission. If multiple devices are connected to form a 1-Wire net, the setting of the search condition enables these devices to participate in the conditional search if certain events, such as timer or temperature alarms, have occurred. Details on the search conditions are found in the *ROM Function Commands* section and in the Control register description.

The setting of the rollover-enable bit (RO) and sample rate depends on the duration of the mission and the monitoring requirements. If the most recent temperature history is important, the rollover should be enabled (RO = 1). Otherwise, one should estimate the duration of the mission in minutes and divide the number by 2048 to calculate the value of the sample rate (number of minutes between temperature conversions). For example, if the estimated duration of a mission is 10 days (14,400min), then the 2048-byte capacity of the data-log memory would be sufficient to store a new value every 7min. If the DS1921G's data-log memory is not large enough to store all temperature readings, one can use several devices and set the Mission Start Delay to values that make the second device start recording as soon as the memory of the first device is full and so on. The RO bit needs to be set to 0 to disable rollover that would otherwise overwrite the recorded temperature log.

After the RO bit and the Mission Start Delay are set, the Sample Rate register is the last element of data that is written. The sample rate can be any value from 1 to 255, coded as an unsigned 8-bit binary number. As soon as the sample rate is written, the DS1921G sets the MIP flag and clears the MEMCLR flag. After as many minutes as specified by the Mission Start Delay are over, the device waits for the next minute boundary, then wakes up, copies the current time and date to the Mission Timestamp register, and makes the first temperature conversion of the mission. This increments both the Mission Samples Counter and Device Samples Counter. All subsequent temperature measurements are taken on minute boundaries specified by the value in the Sample Rate register. One can read the memory of the DS1921G to watch the mission as it progresses. Care should be taken to avoid memory access conflicts. See the *Memory Access Conflicts* section for details.

Address Registers and Transfer Status

Because of the serial data transfer, the DS1921G employs three address registers, called TA1, TA2, and E/S (Figure 9). Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is sent to the master upon a read command. Register E/S acts like a byte counter and transfer status register. It is used to verify data integrity with write commands. Therefore, the master has only read access to this register. The lower 5 bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF or partial byte flag, is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 is always a 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad where intermediate storage of data begins. This address is called byte offset. If the target address for a write command is 13Ch, for example, then the scratchpad stores incoming data beginning at the byte offset 1Ch and is full after only 4 bytes. The corresponding ending offset in this example is 1Fh. For the best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset is 0. Thus, the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1Fh. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the partial and overflow flag are a means to support the master checking the data integrity after a write command. The highest valued bit of the E/S register, called authorization accepted (AA), indicates that a valid copy command for the scratchpad has been received and executed. Writing data to the scratchpad clears this flag.

Writing with Verification

To write data to the DS1921G, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. In the next step, the master sends the Read Scratchpad command to read the scratchpad and to verify data integrity. As preamble to the scratchpad data, the DS1921G sends the requested target address TA1 and TA2 and the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the

BIT NUMBER	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ-ONLY)	AA	0	PF	E4	E3	E2	E1	E0

Figure 9. Address Registers

write command was not recognized by the device. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue verifying every data bit. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2, and E/S as the master has read them verifying the scratchpad. As soon as the DS1921G has received these bytes, it copies the data to the requested location beginning at the target address.

Memory/Control Function Commands

The *Memory/Control Function Flowchart* (Figure 10) describes the protocols necessary for accessing the memory and the special function registers of the DS1921G. An example on how to use these and other functions to set up the DS1921G for a mission is included in the *Mission Example: Prepare and Start a New Mission* section. The communication between master and DS1921G takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into the overdrive mode, the DS1921G assumes standard speed. Internal memory access during a mission has priority over external access through the 1-Wire interface. This affects the read memory commands described below. See the *Memory Access Conflicts* section for details.

Write Scratchpad [0Fh]

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset T[4:0]. The ending offset E[4:0] is the byte offset at which the master stops writing data. Only full data bytes are accepted. If the last data byte is incomplete, its content is ignored and the partial byte flag (PF) is set.

When executing the Write Scratchpad command, the CRC generator inside the DS1921G (see Figure 16) calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte sent by the master. This CRC is generated using the CRC-16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses TA1 and TA2 as supplied by the master, and all the data bytes. The master can end the Write Scratchpad command at any time. However, if the ending offset is 11111b, the master can send 16 read time slots and receive an inverted CRC-16 generated by the DS1921G.

Note: The range 200h to 213h of the register page is protected during a mission. See Figure 6 for the access type of the individual registers between and during missions.

Read Scratchpad [AAh]

This command is used to verify scratchpad data and target addresses. After issuing the Read Scratchpad command, the master begins reading. The first 2 bytes are the target address. The next byte is the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset T[4:0], as shown in Figure 9. Regardless of the actual ending offset, the master can read data until the end of the scratchpad after which it receives an inverted CRC-16 of the command code, target addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. After the CRC is read, the bus master reads logical "1"s from the DS1921G until a reset pulse is issued.

Copy Scratchpad [55h]

This command is used to copy data from the scratchpad to the writable memory sections. Applying a Copy Scratchpad command to the Sample Rate register can start a mission provided that several preconditions are met. See the *Mission Start and Logging Process* section and the flowchart in Figure 11 for details. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA flag is set and the copy begins. A pattern of alternating "1"s and "0"s is transmitted after the data has been copied until the master issues a reset pulse. While the copy is in progress, any attempt to reset the part is ignored. Copy typically takes 2µs per byte.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset is copied, starting at the target address. Anywhere from 1 to 32 bytes can be copied to memory with this command. The AA flag remains at logic 1 until it is cleared by the next Write Scratchpad command. Note that the Copy Scratchpad command, when applied to the address range 200h to 213h during a mission, ends the mission.

Read Memory [F0h]

The Read Memory command can be used to read the entire memory. After issuing the command, the master must provide the 2-byte target address. After the 2 bytes, the master reads data beginning from the target address and can continue until the end of memory, at which point logic "0"s are read. It is important to realize that the target address registers contain the address provided. The ending offset/data status byte is unaffected.

The hardware of the DS1921G provides a means to accomplish error-free writing to the memory section. To safeguard data in the 1-Wire environment when reading and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to verify if the received data is correct (refer to Application Note 114: *1-Wire File Structure* for the recommended file structure).

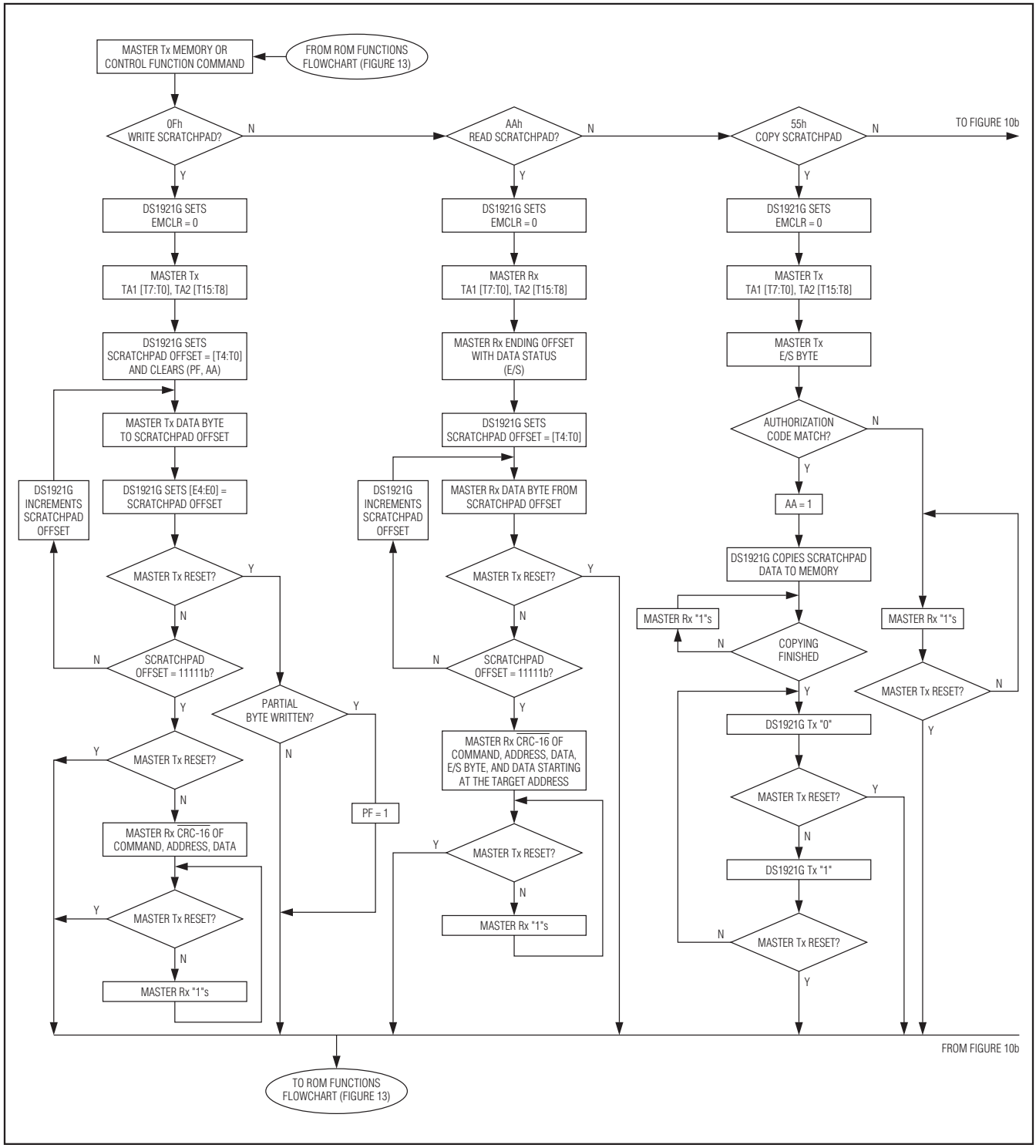


Figure 10a. Memory/Control Function Flowchart

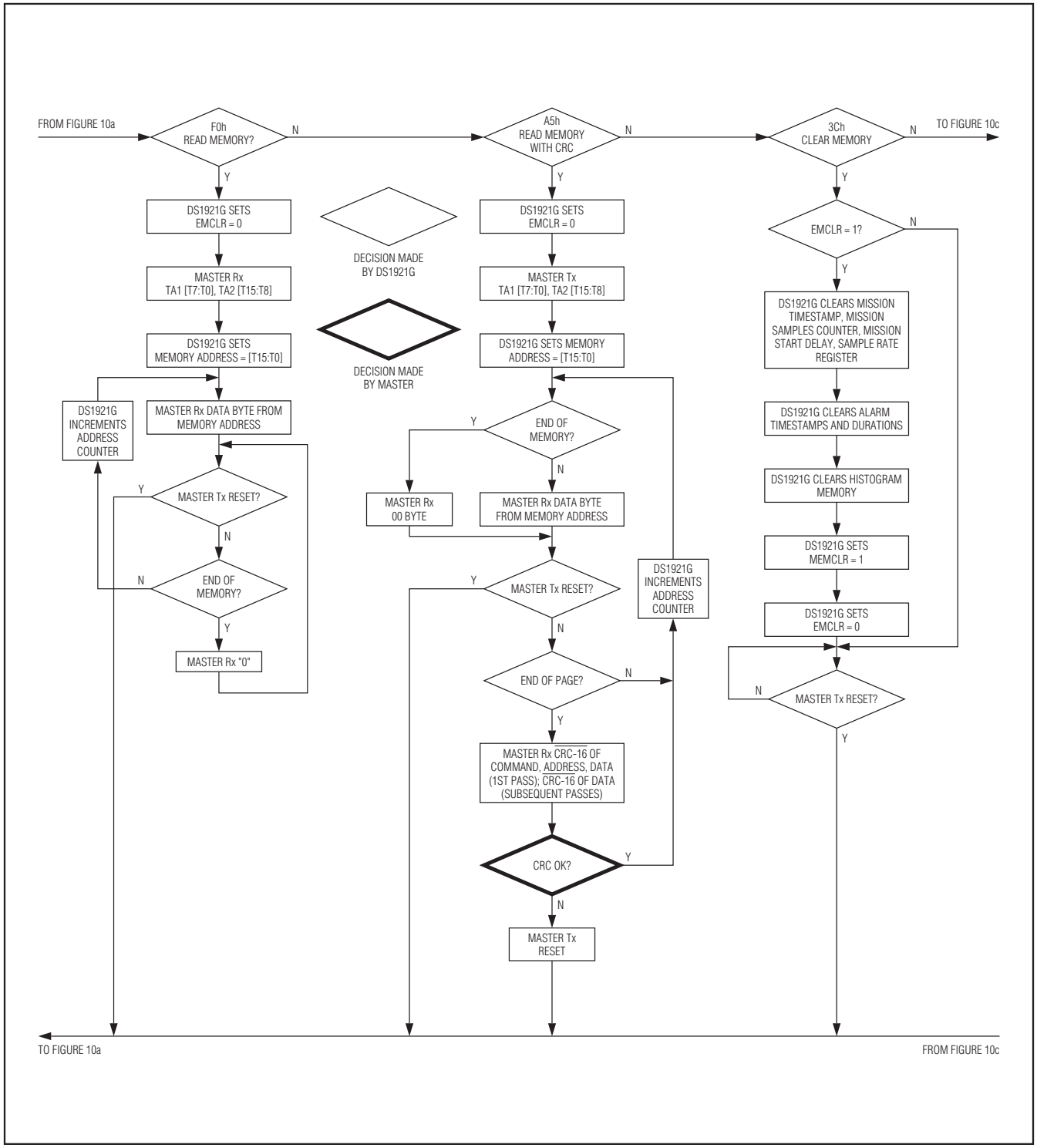


Figure 10b. Memory/Control Function Flowchart

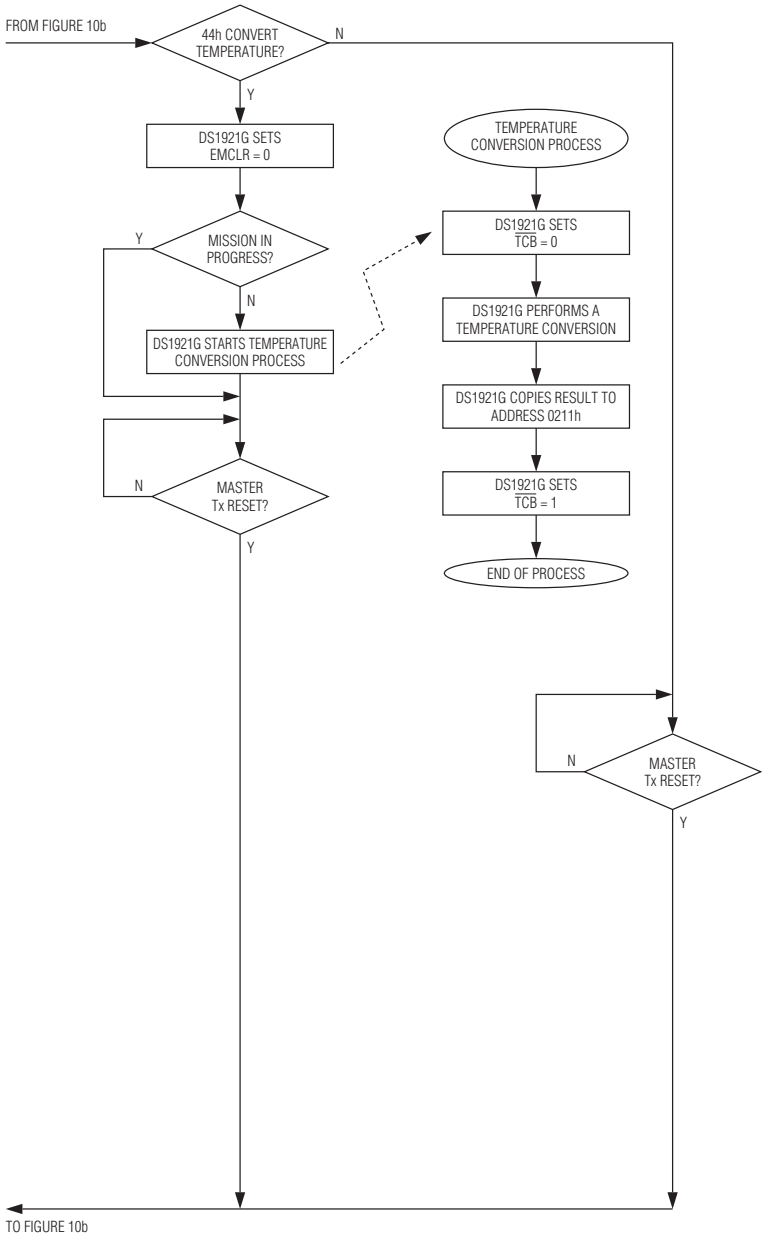


Figure 10c. Memory/Control Function Flowchart

Read Memory with CRC [A5h]

The Read Memory with CRC command is used to read memory data that cannot be packetized, such as the register page and the data recorded by the device during a mission. The command works the same way as the simple Read Memory command, except for the 16-bit CRC that the DS1921G generates and transmits following the last data byte of a memory page.

After having sent the command code of the Read Memory with CRC command, the bus master sends a 2-byte address (TA1 = T[7:0], TA2 = T[15:8]) that indicates a starting byte location. With the subsequent read-data time slots, the master receives data from the DS1921G starting at the initial address and continues until the end of a 32-byte page is reached. At that point the bus master sends 16 additional read-data time slots and receives an inverted 16-bit CRC. With subsequent read-data time slots the master receives data starting at the beginning of the next page followed again by the inverted CRC for that page. This sequence continues until the bus master resets the device.

With the initial pass through the Read Memory with CRC command flow, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator followed by the two address bytes and the contents of the data memory. Subsequent passes through the Read Memory with CRC command flow generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the contents of the data memory page. After the 16-bit CRC of the last page is read, the bus master receives logical “0”s from the DS1921G and inverted CRC-16s at page boundaries until a reset pulse is issued. The Read Memory with CRC command sequence can be ended at any point by issuing a reset pulse.

Clear Memory [3Ch]

The Clear Memory command is used to clear the Sample Rate, Mission Start Delay, Mission Timestamp, and Mission Samples Counter in the register page and the temperature alarm memory and the temperature histogram memory. These memory areas must be cleared for the device to be set up for another mission. The Clear Memory command does not clear the data-log memory or the temperature and timer alarm flags in the Status register. The RTC oscillator must be on and have counted at least 1s before issuing the command. For the Clear Memory command to function, the EMCLR bit in the Control register must be set to 1, and the Clear Memory command must be issued with the very next access to the device’s memory functions. Issuing any other memory function command resets the EMCLR bit. The Clear Memory process takes 500µs. When the command is completed the MEMCLR bit in the Status register reads 1 and the EMCLR bit is 0.

Convert Temperature [44h]

If a mission is not in progress (MIP = 0), the Convert Temperature command can be issued to measure the current temperature of the device. The result of the temperature conversion can be found at memory address 211h in the register page. This command takes maximum 90ms to complete. During this time the device remains fully accessible for memory/control and ROM function commands.

Mission Start and Logging Process

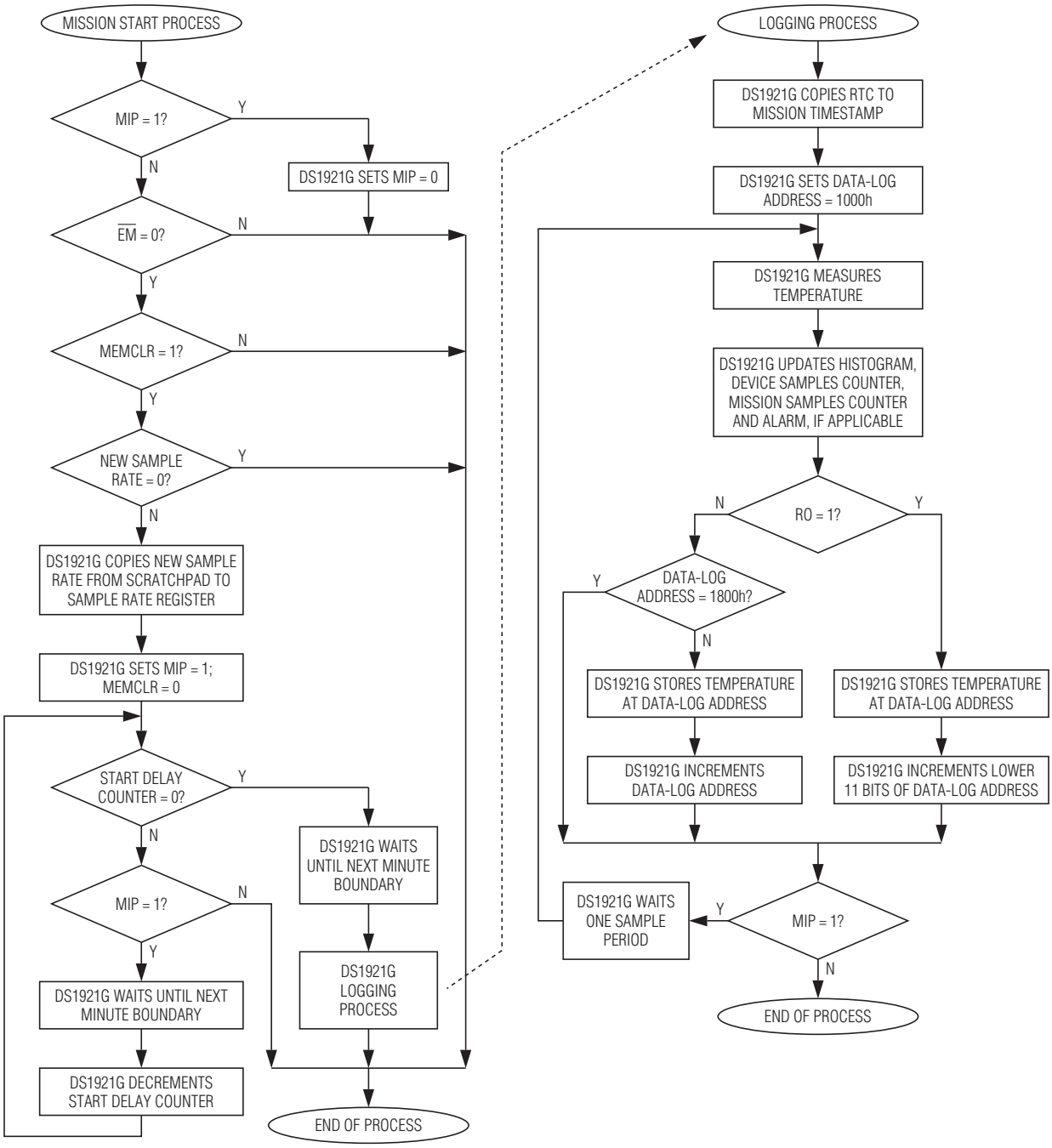
The DS1921G does not use a special command to start a mission. Instead, a mission is started by writing a nonzero value to the Sample Rate register using the Copy Scratchpad command. As shown in Figure 11, a new mission can only be started if the previous mission has been stopped (MIP = 0), the memory is cleared (MEMCLR = 1), and the mission is enabled ($\overline{EM}$ = 0). If the new sample rate is different from zero, the value is copied to the Sample Rate register. At the same time the MIP bit is set and the MEMCLR bit is cleared to indicate that the device is on a mission. Next, the Mission Start Delay Counter starts decrementing every minute until it is down to 0. Now the DS1921G waits until the next minute boundary and starts the logging process, which as its first action copies the applicable RTC registers to the Mission Timestamp register.

Stop Mission

The DS1921G does not have a special command to stop a mission. A mission can be stopped at any time by writing to any address in the range of 0200h to 0213h or by writing the MIP bit of the Status register at address 0214h to 0. Either approach involves the use of the Copy Scratchpad command. There is no need for the Mission Start Delay to expire before a mission can be stopped (see Figure 11).

Memory Access Conflicts

While a mission is in progress, a temperature sample is periodically taken and stored in the data-log, histogram, and potential alarm memory. This “internal activity” has priority over a Read Memory command’s or Read Memory with CRC command’s access to these pages. If a conflict occurs, the data read may be invalid, even if the CRC value matches the data. To ensure that the data read is valid, it is recommended to first read the SIP bit of the Status register. If the SIP bit is set, delay reading the data-log, histogram, and alarm memory until SIP is 0. The interference is more likely to be seen with a high sample rate (one sample every



NOTE: THE MISSION START PROCESS IS INVOKED WHEN THE COPY SCRATCHPAD COMMAND IS USED TO SET A NEW SAMPLE RATE BY WRITING TO THE SAMPLE RATE REGISTER AT ADDRESS 020Dh. ONE MINUTE AFTER THE START DELAY COUNTDOWN IS OVER, THE LOGGING PROCESS BEGINS AND THE MISSION START PROCESS ENDS.

Figure 11. Mission Start and Logging Process

minute). Since all mission samples occur on the seconds rollover (59 to 00), memory conflicts can be avoided by first reading the RTC seconds counter. For example, if it takes 2s to read the data log, then avoid starting the memory read if the seconds counter is 58, 59, or 00. Alternatively, one can read the affected memory section twice and accept the data only if both readings match. In any case, when writing driver software, it is important to know about the possibility of interference and to take measures to work around it.

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS1921G is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS1921G is open drain with an internal circuit equivalent to that shown in Figure 12.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At standard speed the 1-Wire bus has a maximum data rate of 16.3kbps. The speed can be boosted to 142kbps by activating the overdrive mode. The DS1921G is not guaranteed to be fully compliant to the iButton device standard. Its maximum data rate in standard speed is 15.4kbps and 125kbps in overdrive. The value of the pullup resistor primarily depends on the network size and load conditions. The DS1921G requires a pullup resistor of maximum 2.2kΩ at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **must** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus may be reset. Note that the DS1921G does not quite meet the full 16µs maximum low time of the normal 1-Wire bus overdrive timing. With the DS1921G the bus must be left low for no longer than 15µs at overdrive speed to ensure that no DS1921G on the 1-Wire bus performs a reset. The DS1921G communicates properly when used in conjunction with a DS2480B or DS2490 1-Wire driver and adapters that are based on these driver chips.

Transaction Sequence

The protocol for accessing the DS1921G through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory/Control Function Command
- Transaction/Data

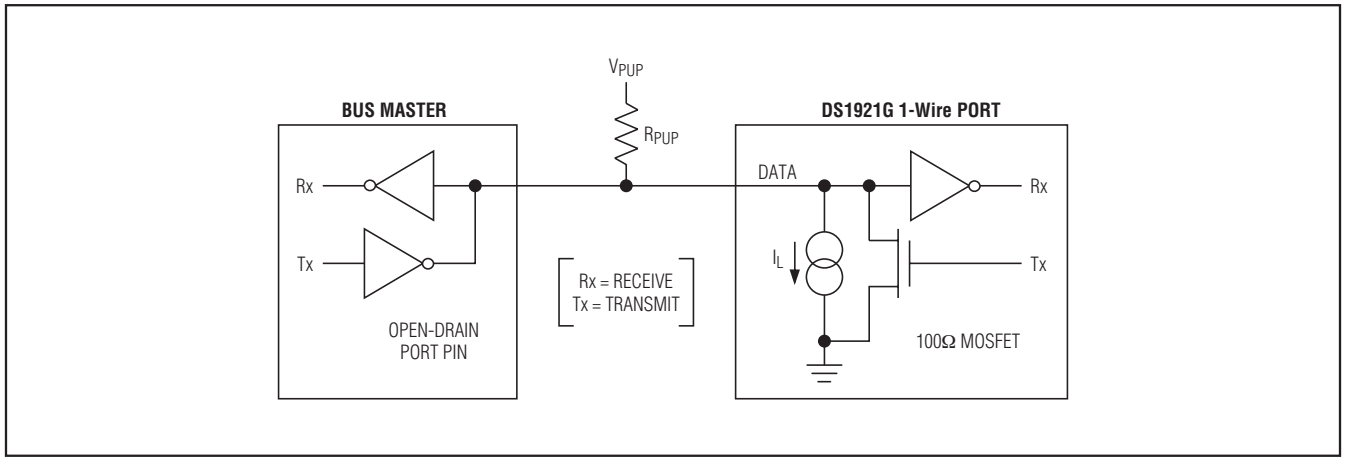


Figure 12. Hardware Configuration

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master, followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1921G is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

ROM Function Commands

Once the bus master has detected a presence, it can issue one of the seven ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (see the flowchart in Figure 13).

Read ROM [33h]

This command allows the bus master to read the DS1921G's 8-bit family code, unique 48-bit serial number and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1921G on a multidrop bus. Only the DS1921G that exactly matches the 64-bit ROM sequence responds to the memory function command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

Conditional Search ROM [ECh]

The Conditional Search ROM command operates similarly to the Search ROM command except that only devices fulfilling the specified condition participate in the search. The condition is specified by the bit functions TAS, THS, and TLS in the Control register, address 20Eh. The Conditional Search ROM provides an efficient means for the bus master to determine devices on a multidrop system that have to signal an important event, such as a temperature leaving the tolerance band. After each pass of the conditional search that successfully determined the 64-bit ROM code for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM command had been issued, since all other devices have dropped out of the search process and are waiting for a reset pulse.

For the conditional search, one can select any combination of the three search conditions by writing the associated bit to a logical 1. These bits correspond directly to the flags in the Status register of the device. If the flag in the Status register reads 1 **and** the corresponding bit in the Control register is a logical 1 too, the device responds to the Conditional Search ROM command. If more than one bit search condition is selected, the first event that occurs makes the device respond to the Conditional Search ROM command.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

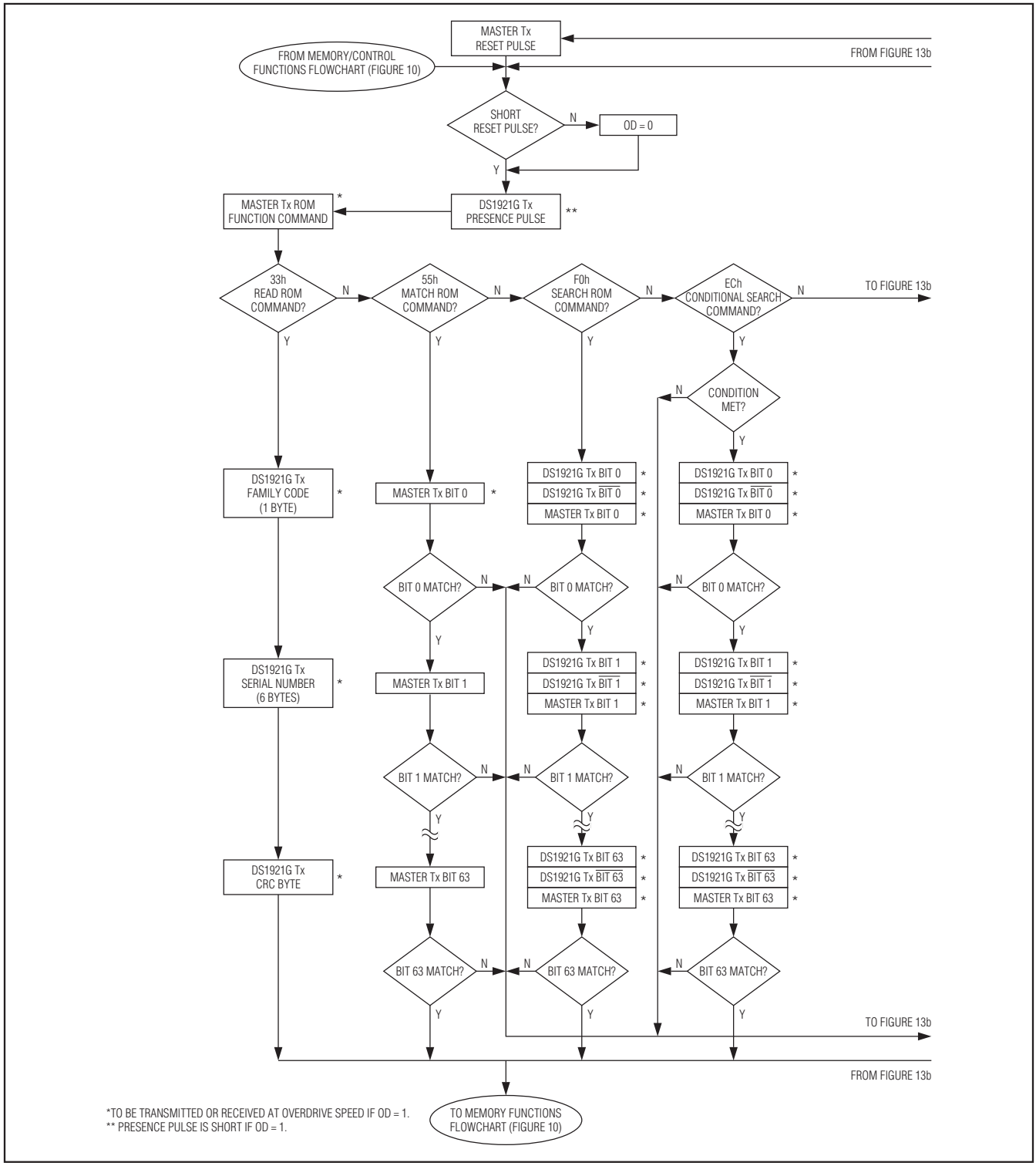


Figure 13a. ROM Functions Flowchart

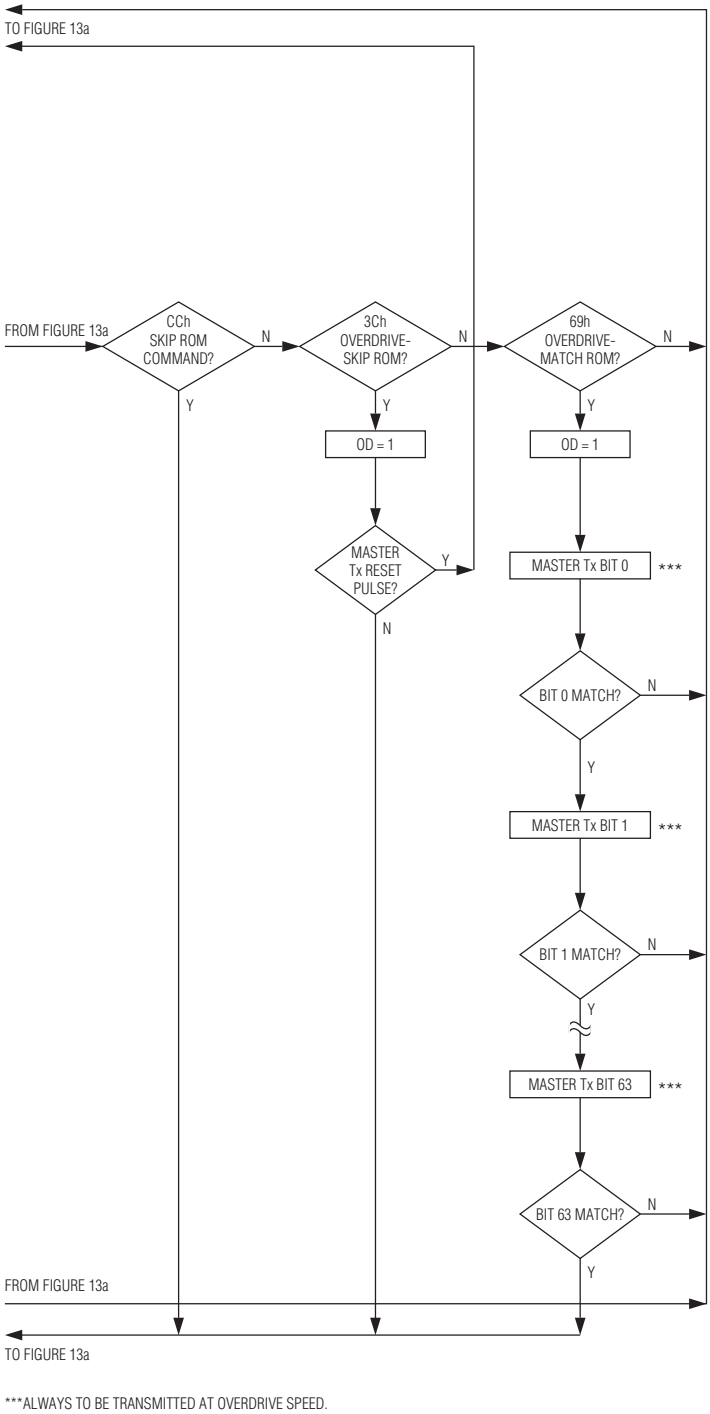


Figure 13b. ROM Functions Flowchart

Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory/control functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS1921G in the overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS1921G on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS1921G that exactly matches the 64-bit ROM sequence responds to the subsequent memory/control function command. Slaves already in overdrive mode from a previous Overdrive-Skip or successful Overdrive-Match ROM command remain in overdrive mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive-Match ROM command can be used with a single or multiple devices on the bus.

1-Wire Signaling

The DS1921G requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all these signals. The DS1921G can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the overdrive mode, the DS1921G communicates at standard speed. While in overdrive mode, the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 14 as “ε” and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS1921G when determining a logical level, but not for triggering any events.

The initialization sequence required to begin any communication with the DS1921G is shown in Figure 14. A reset pulse followed by a presence pulse indicates the DS1921G is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge.

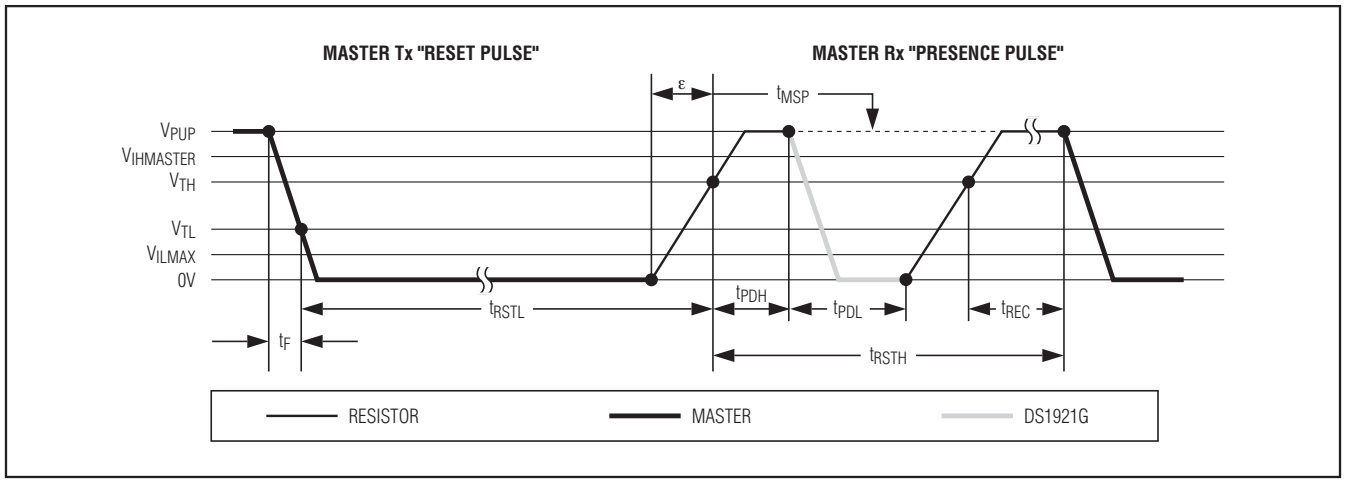


Figure 14. Intitialization Procedure: Reset and Presence Pulses

A t_{RSTL} duration of 480µs or longer exits the overdrive mode, returning the device to standard speed. If the DS1921G is in overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in overdrive mode.

After the bus master has released the line, it goes into receive mode (Rx). Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in case of a DS2480B driver, through active circuitry. When the threshold V_{TH} is crossed, the DS1921G waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS1921G is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

Read/Write Time Slots

Data communication with the DS1921G takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. The definitions of the write and read time slots are illustrated in Figure 15.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS1921G starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold after the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. The voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS1921G needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS1921G starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS1921G does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of $t_{RL} + \delta$ (rise time) on one side and the internal timing generator of the DS1921G on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For most reliable communication, t_{RL} should be as short as permissible and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS1921G to get ready for the next time slot.

CRC Generation

There are two different types of CRCs with the DS1921G. One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS1921G to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form. It is computed at the factory and lasered into the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC-16 polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used for error detection when reading data memory using the Read Memory with CRC command and for fast verification of a data transfer when writing to or reading from the scratchpad. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC-generator inside the DS1921G chip (Figure 16) calculates a new 16-bit CRC as shown in the command flowchart of Figure 10. The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to reread the portion of the data with the CRC error. With the initial pass through the Read Memory with CRC flowchart, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the 2 address bytes and the data bytes. Subsequent passes through the Read Memory with CRC flowchart generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes.

With the Write Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, and all the data bytes. The DS1921G transmits this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data can start at any location within the scratchpad.

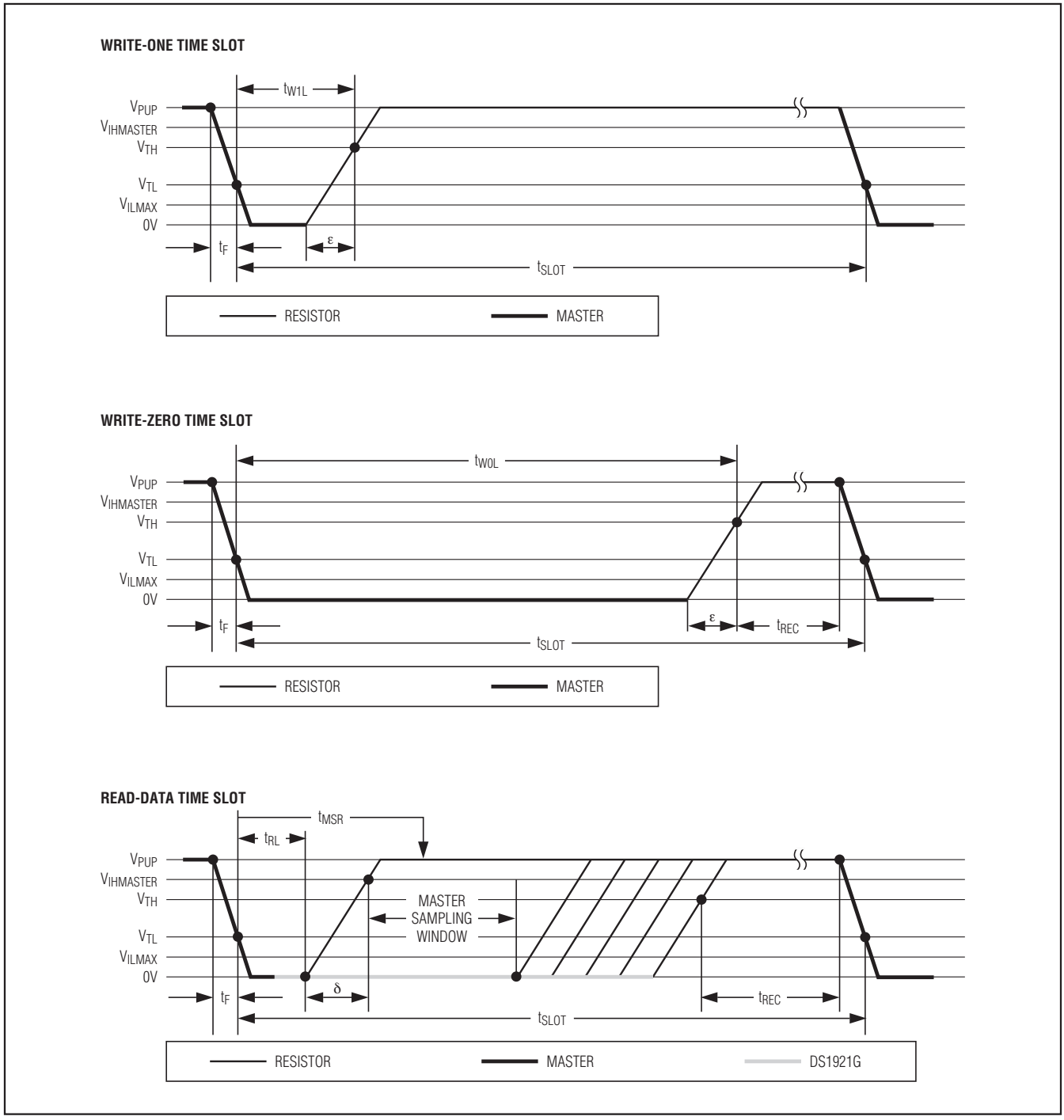


Figure 15. Read/Write Timing Diagram

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. The DS1921G transmits this CRC only if the reading continues through the end of the scratchpad, regardless of the actual ending offset. For more information on generating CRC values refer to Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products*.

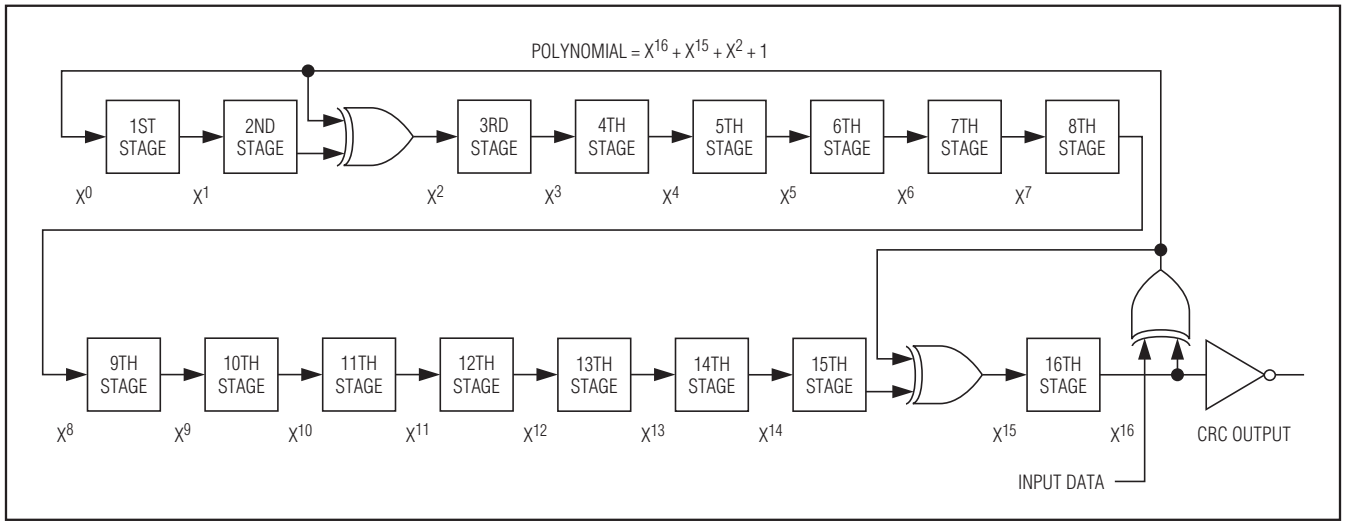


Figure 16. CRC-16 Hardware Description and Polynomial

Command-Specific 1-Wire Communication Protocol—Legend

SYMBOL	DESCRIPTION
RST	1-Wire reset pulse generated by master
PD	1-Wire presence pulse generated by slave
Select	Command and data to satisfy the ROM function protocol (Skip ROM, Search ROM, etc.)
WS	Command: “Write Scratchpad”
RS	Command: “Read Scratchpad”
CPS	Command: “Copy Scratchpad”
RM	Command: “Read Memory”
RMC	Command: “Read Memory with CRC”
CM	Command: “Clear Memory”
CT	Command: “Convert Temperature”
TA	Target Address TA1, TA2
TA-E/S	Target Address TA1, TA2 with E/S byte
<data to EOS>	Transfer of as many data bytes as are needed to reach the scratchpad offset 1Fh
<data to EOP>	Transfer of as many data bytes as are needed to reach the end of a memory page
<data to EOM>	Transfer of as many data bytes as are needed to reach the end of the data-log memory
<00 to EOP>	Transfer of as many 00h bytes as are needed to reach a memory page boundary
<32 bytes>	Transfer of 32 bytes

Command-Specific 1-Wire Communication Protocol—Legend (continued)

SYMBOL	DESCRIPTION
<data>	Transfer of an undetermined amount of data
$\overline{\text{CRC-16}}$	Transfer of an inverted CRC-16
FF loop	Indefinite loop where the master reads FFh bytes
AA loop	Indefinite loop where the master reads AAh bytes
Busy	Interval during Copy Scratchpad where the DS1921G does not respond. Any bits read during this time are logic 1.
00 loop	Indefinite loop where the master reads 00h bytes

Command-Specific 1-Wire Communication Protocol—Color Codes

Master-to-Slave	Slave-to-Master

1-Wire Communication Examples

Write Scratchpad, Reaching the End of the Scratchpad

RST	PD	Select	WS	TA	<data to EOS>	$\overline{\text{CRC-16}}$	FF loop

Write Scratchpad, Not Reaching the End of the Scratchpad

RST	PD	Select	WS	TA	<data>	RST	PD

Read Scratchpad

RST	PD	Select	RS	TA-E/S	<data to EOS>	$\overline{\text{CRC-16}}$	FF loop

Copy Scratchpad (Success)

RST	PD	Select	CPS	TA-E/S	Busy	AA loop

Copy Scratchpad (Invalid TA-E/S)

RST	PD	Select	CPS	TA-E/S	FF loop

Read Memory (Success)

RST	PD	Select	RM	TA	<data to EOM>	00 loop

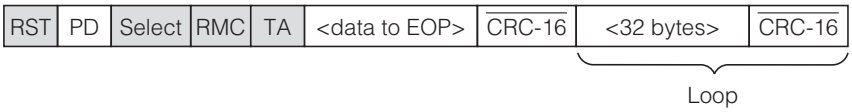
Read Memory (Invalid Address)

RST	PD	Select	RM	TA	00 loop

Reading reserved pages 20 through 63 or 68 through 127 or pages 192 and higher (beyond data-log memory) results in 00h bytes.

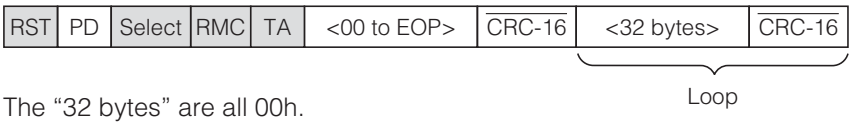
1-Wire Communication Examples (continued)

Read Memory with CRC (Success)



The “32 bytes” are either valid page data or 00h bytes when reading reserved pages 20 through 63 or 68 through 127 or pages 192 and higher (beyond data-log memory).

Read Memory with CRC (Invalid Address)



The “32 bytes” are all 00h.

Clear Memory

To verify success, read the Status register at address 0214h. If MEMCLR is 1, the command was executed successfully.

Convert Temperature

To read the result and to verify success, read the addresses 0211h (result) and the Device Samples Counter at address 021Dh to 021Fh. If the count has incremented, the command was executed successfully.

Mission Example: Prepare and *Start a New Mission*

Assumption: The previous mission has ended. To end an ongoing mission write the MIP bit in the Status register to 0.

The preparation of a DS1921G for a mission including the start of the mission requires up to four steps:

Step 1: Set the RTC (if it needs to be adjusted).

Step 2: Clear the data of the previous mission.

Step 3: Set the search condition and Mission Start Delay and clear the alarm flags.

Step 4: Set the temperature alarms and write the Sample Rate to start the mission.

Step 1: Set the RTC

Let the actual time be 15:30:00 hours on Monday, the 1st of April in 2002. This results in the following data to be written to the RTC registers:

ADDRESS	200h	201h	202h	203h	204h	205h	206h
DATA	00h	30h	15h	01h	81h	04h	02h

With only a single DS1921G connected to the bus master, the communication of step 1 is as follows:

MASTER MODE	DATA (LSB FIRST)	COMMENTS	
Tx	(Reset)	Reset pulse (480µs to 960µs)	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	0Fh	Issue Write Scratchpad command	
Tx	00h	TA1, beginning offset = 00h	
Tx	02h	TA2, address = 0200h	
Tx	<7 data bytes>	Write 7 bytes of data to scratchpad	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	AAh	Issue Read Scratchpad command	
Rx	00h	Read TA1, beginning offset = 00h	
Rx	02h	Read TA2, address = 0200h	
Rx	06h	Read E/S, ending offset = 6h, flags = 0h	
Rx	<7 data bytes>	Read scratchpad data and verify	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	55h	Issue Copy Scratchpad command	
Tx	00h	TA1	(AUTHORIZATION CODE)
Tx	02h	TA2	
Tx	06h	E/S	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	

Step 2: Clear the data of the previous mission

Set the EMCLR bit to 1, enable the RTC, and then execute the Clear Memory command. The RTC oscillator must be stable before the Clear Memory command is issued. Wait 500µs after issuing the Clear Memory command before proceeding to step 3. This results in the following data to be written to the Status register:

ADDRESS	20Eh
DATA	40h

With only a single DS1921G connected to the bus master, the communication of step 2 is as follows:

MASTER MODE	DATA (LSB FIRST)	COMMENTS	
Tx	(Reset)	Reset pulse (480µs to 960µs)	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	0Fh	Issue Write Scratchpad command	
Tx	0Eh	TA1, beginning offset = 0Eh	
Tx	02h	TA2, address = 020Eh	
Tx	40h	Write status byte to scratchpad	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	AAh	Issue Read Scratchpad command	
Rx	0Eh	Read TA1, beginning offset = 0Eh	
Rx	02h	Read TA2, address = 020Eh	
Rx	0Eh	Read E/S, ending offset = 0Eh, flags = 0h	
Rx	40h	Read scratchpad data and verify	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	55h	Issue Copy Scratchpad command	
Tx	0Eh	TA1	(AUTHORIZATION CODE)
Tx	02h	TA2	
Tx	0Eh	E/S	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	3Ch	Issue Clear Memory command	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	

Step 3: Set the search condition and Mission Start Delay and clear the alarm flags

In this example, the rollover is disabled and the search condition is set for a high temperature only. The mission is to start with a delay of 90min (005Ah) and the alarm flags TLF, THF, and TAF are cleared. This results in the following data to be written to the special function registers:

ADDRESS	20Eh	20Fh	210h	211h	212h	213h	214h
DATA	02h	00h*	00h*	00h*	5Ah	00h	00h

**Writing through address locations 20Fh to 211h is faster than accessing the Mission Start Delay register in a separate cycle. The write attempt has no effect on the contents of these registers.*

With only a single DS1921G connected to the bus master, the communication of step 3 is as follows:

MASTER MODE	DATA (LSB FIRST)	COMMENTS	
Tx	(Reset)	Reset Pulse (480µs to 960µs)	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	0Fh	Issue Write Scratchpad command	
Tx	0Eh	TA1, beginning offset = 0Eh	
Tx	02h	TA2, address = 020Eh	
Tx	<7 data bytes>	Write 7 bytes of data to scratchpad	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	AAh	Issue Read Scratchpad command	
Rx	0Eh	Read TA1, beginning offset = 0Eh	
Rx	02h	Read TA2, address = 020Eh	
Rx	14h	Read E/S, ending offset = 14h, flags = 0h	
Rx	<7 data bytes>	Read scratchpad data and verify	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	55h	Issue Copy Scratchpad command	
Tx	0Eh	TA1	(AUTHORIZATION CODE)
Tx	02h	TA2	
Tx	13h	E/S	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	

Step 4: Set the temperature alarms and write the Sample Rate to start the mission

In this example, the temperature alarms are set to -5°C for the low temperature threshold and 0°C for the high temperature threshold. The sample rate is once every 10min, allowing the mission to last up to 14 days. This results in the following data to be written to the special function registers:

ADDRESS	20Bh	20Ch	20Dh
DATA	46h	50h	0Ah

With only a single DS1921G connected to the bus master, the communication of step 4 is as follows:

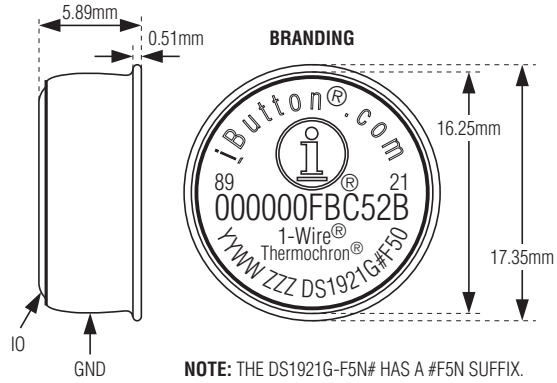
MASTER MODE	DATA (LSB FIRST)	COMMENTS	
Tx	(Reset)	Reset pulse (480µs to 960µs)	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	0Fh	Issue Write Scratchpad command	
Tx	0Bh	TA1, beginning offset = 0Bh	
Tx	02h	TA2, address = 020Bh	
Tx	<3 data bytes>	Write 3 bytes of data to scratchpad	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	AAh	Issue Read Scratchpad command	
Rx	0Bh	Read TA1, beginning offset = 0Bh	
Rx	02h	Read TA2, address = 020Bh	
Rx	0Dh	Read E/S, ending offset = 0Dh, flags = 0h	
Rx	<3 data bytes>	Read scratchpad data and verify	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue Skip ROM command	
Tx	55h	Issue Copy Scratchpad command	
Tx	0Bh	TA1	(AUTHORIZATION CODE)
Tx	02h	TA2	
Tx	0Dh	E/S	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	

If step 4 is successful, the MIP bit in the Status register is 1, the MEMCLR bit is 0, and the Mission Start Delay counts down.

Common iButton Device Features

- Rugged Chip-Based Data Carrier with Fast, Simple Access to Information
  - Digital Identification and Information by Momentary Contact
  - Unique Factory-Lasered 64-Bit Registration Number Ensures
- Error-Free Device Selection and Absolute Traceability Because No Two Parts Are Alike
  - Built-In Multidrop Controller for 1-Wire Net
  - Compactly Stores Information
  - Data Can Be Accessed While Affixed to an Object
  - Button Shape is Self-Aligning with Cup-Shaped Probes
  - Durable Stainless-Steel Case Engraved with Registration Number Withstands Harsh Environments
  - Easily Affixed with Self-Stick Adhesive Backing, Latched by Its Flange, or Locked with a Ring Pressed Onto Its Rim
  - Presence Detector Acknowledges When Reader First Applies Voltage

Pin Configuration



NOTE: THE DS1921G-F5N# HAS A #F5N SUFFIX.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
F5 Can	IB#5CP	21-0266	—

Revision History

REVISION DATE	DESCRIPTION	PAGES CHANGED
120407	Added bullet “Water resistant or waterproof if placed inside DS9107 iButton capsule (Exceeds Water Resistant 3 ATM requirements)”	1, 2
	Deleted “application pending” from UL bullet and safety statement	
	Added text to *Detailed Description* section: Note that the initial sealing level of DS1921G achieves IP56. Aging and use conditions can degrade the integrity of the seal over time, so for applications with significant exposure to liquids, sprays, or other similar environments, it is recommended to place the Thermochron in the DS9107 iButton capsule. The DS9107 provides a watertight enclosure that has been rated to IP68 (See **www.maximintegrated.com/AN4126**)	
4/09	Created newer template-style data sheet	All
4/10	Overdrive specifications for t_{RSTL}, t_{PDL}, and t_{W0L} split into range V_{PUP} > 4.5V and full range. New values for the full range	2–4
4/11	Updated UL certificate reference; deleted ε from the t_{W1L} specification in the *Electrical Characteristics* table; applied note 13 to the t_{W0L} specification in the *Electrical Characteristics* table; added more details to *Electrical Characteristics* table notes 7, 13, and 14	1, 3, 4
9/11	DS1921G-F5N# part number added to the *Ordering Information*; branding information updated in the *Pin Configuration*	1, 41
3/12	Added terminology updates for consistency with similar products; added more details to the *Parasite Power* section	1, 7, 8, 9, 14
6/13	Removed the UL 913 5th Ed. compliance statement from the *Common iButton Device Features* section and *iButton Can Physical Specification* table; reworded the *Electrical Characteristics* table Note 17	1, 4
11/13	Added the Busy state during Copy Scratchpad to the *Command-Specific 1-Wire Communication Protocol—Legend* and *1-Wire Communication Examples* sections	35
3/15	Updated *Benefits and Features* and *Common iButton Device Features* sections	1, 41

