

Vishay Siliconix

ORDERING INFORMATION						
TEMP. RANGE	PACKAGE	PART NUMBER				
-40 °C to 85 °C	miniQFN-10	DG2723DN-T1-E4				

TRUTH TABLE					
S+ (PIN 8)	S- (PIN 10)	FUNCTION			
X	0	D- = HSD1-			
Х	1 D- = HSD2-				
0	Х	D+ = HSD1+			
1	Х	D+ = HSD2+			

PIN DESCRIPTIONS					
PIN NAME DESCRIPTION					
S+	Select Input for D+				
S-	Select Input for D-				
HSD±, HSD2±, D±	Data Port				

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER		LIMIT	UNIT		
Reference to GND	V+	-0.3 to 6	V		
neierence to GND	S+, S-, D±, HSD1±, HSD2± a	-0.3 to (V+ + 0.3)	☐ °		
Current (Any Terminal except S+, S-, D±, HSD1±, HSD2±)		30			
Continuous Current (S+, S-, D±, HSD1±, HSD2±)		± 250	mA		
Peak Current (Pulsed at 1 ms, 10 % Duty Cycle)		± 500	\neg		
Storage Temperature (D Suffix)		-65 to 150	°C		
Power Dissipation (Packages) ^b	miniQFN-10 ^c	208	mW		
ESD (Human Body Model)		5	kV		
Latch-up (Current Injection)		500	mA		

Notes

- a. Signals on S+, S-, D±, HSD1±, HSD2± exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 2.6 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITIONS OTHERWISE UNLESS SPECIFIED	TEMP.a	LIMITS -40 °C to 85 °C			UNIT
	OTHERWISE UNLESS SPECIFIED			MIN. b	TYP. c	MAX. b	
Analog Switch							
Analog Signal Range ^d	V_{ANALOG}	R _{DS(on)}	Full	0	-	V+	V
On-Resistance	В	$V+ = 3 \text{ V}, I_{D\pm} = 8 \text{ mA}, V_{HSD1/2\pm} = 0.4 \text{ V}$	Room	-	5.5	8	
On-nesistance	R _{DS(on)}	$V + = 3 V$, $I_{D\pm} = 0 IIIA$, $V_{HSD1/2\pm} = 0.4 V$	Full	-	-	9	
On-Resistance Match ^d	ΔR_{ON}	$V+ = 3 \text{ V}, I_{D\pm} = 8 \text{ mA}, V_{HSD1/2\pm} = 0.4 \text{ V}$	Room	-	0.8	-	Ω
On-Resistance Resistance Flatness ^d	R _{ON} Flatness	$V+ = 3 \text{ V}, I_{D\pm} = 8 \text{ mA}, V_{HSD1/2\pm} = 0 \text{ V}, 1 \text{ V}$	Room	-	2	-	
Switch Off Leakage Current	I _(off)	$V+ = 4.3 \text{ V}, V_{HSD1/2\pm} = 0.3 \text{ V}, 3 \text{ V}, V_{D\pm} = 3 \text{ V}, 0.3 \text{ V}$	Full	-100	-	100	Λ
Channel On Leakage Current	I _(on)	$V+ = 4.3 \text{ V}, V_{\text{HSD1/2}\pm} = 0.3 \text{ V}, 4 \text{ V}, \ V_{\text{D}\pm} = 4 \text{ V}, 0.3 \text{ V}$	Full	-200	-	200	nA
Digital Control							
Innet Voltage High		V+ = 3 V to 3.6 V	Full	1.3	-	-	
Input Voltage High	V _{INH}	V+ = 4.3 V	Full	1.5	-	-	V
Input Voltage Low	V _{INL}	V+ = 3 V to 4.3 V	Full	-	-	0.5	
Input Capacitance	C _{IN}		Full	-	6.5	-	pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1	-	1	μΑ



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PARAMETER	SYMBOL	TEST CONDITIONS OTHERWISE UNLESS SPECIFIED	TEMP.a	LIMITS -40 °C to 85 °C			UNIT		
		OTHERWISE UNLESS SPECIFIED		MIN. b	TYP. c	MAX. b	1		
Dynamic Characteristics	Dynamic Characteristics								
Break-Before-Make Time ^{e, d}	t _{BBM}		Room	_	5	-	ns		
Break Before Wake Time	ввм		Full						
S-, S+ Turn-On Time ^{e, d}	t _{ON}	$V+ = 3 V$, $V_{D1/2\pm} = 1.5 V$, $R_L = 50 \Omega$,	Room		_	30			
3-, 3+ Tuni-On Time	^t ON	$C_L = 35 \text{ pF}$	Full	_	_	30			
S-, S+ Turn-Off Time ^{e, d}	t _{OFF}		Room	-	-	25			
3-, 3+ Tuni-On Time	OFF		Full						
Charge Injection ^d	Q_{INJ}	$C_L = 1 \text{ nF}, R_{GEN} = 0 \Omega, V_{GEN} = 0 V$		-	3 -	-	рC		
Off-Isolation ^d	OIRR	$V + = 3 V \text{ to } 3.6 V, R_L = 50 \Omega, C_L = 5 pF,$		-	-29	-	dB		
Crosstalk ^d	X _{TALK}	f = 240 MHz	- - - - - - -	-	-36	-	ub		
Bandwidth ^d	BW	$V+ = 3 V \text{ to } 3.6 V, C_L = 5 pF, R_L = 50 \Omega, -3 dB$		-	700	-	MHz		
Channel-Off Capacitance d	$C_{D1\pm (off)}$	V+ = 3.3 V, f = 1 MHz		-	2.5	-	pF		
Chamer-on Capacitance	$C_{D2\pm (off)}$			-	2.5	-			
Channel-On Capacitance d	$C_{D\pm (off)}$			-	2.5	-			
Onamiei-On Oapacitance	$C_{D\pm (on)}$	1		-	6.5	-			
Channel-to-Channel Skew ^d	t _{SK(O)}			-	50	-			
Skew Off Opposite Transitions of the Same Output ^d	t _{SK(p)}	$V+ = 3 V \text{ to } 3.6 \text{ V}, \text{ R}_{L} = 50 \Omega, \text{ C}_{L} = 5 \text{ pF}$	-	20	-	ps			
Total Jitter ^d	tJ			-	200	-			
Power Supply									
Power Supply Range	V+			2.6	-	5.5	V		
Power Supply Current	I+	V _{IN} = 0 V, or V+	Full	-	-	2	μΑ		

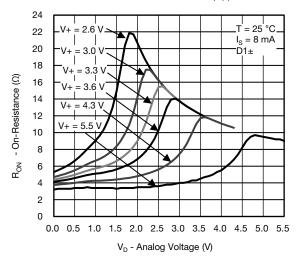
Notes

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, not subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Crosstalk measured between channels.

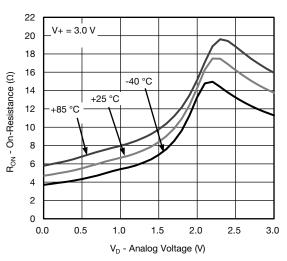
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



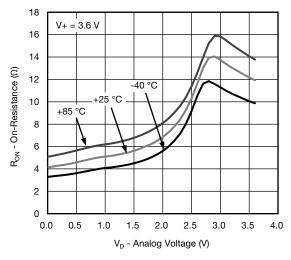
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



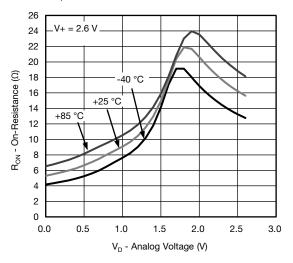
R_{ON} vs. V_D and Single Supply Voltage



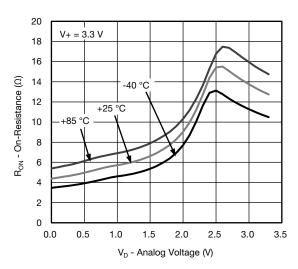
R_{ON} vs. Analog Voltage and Temperature



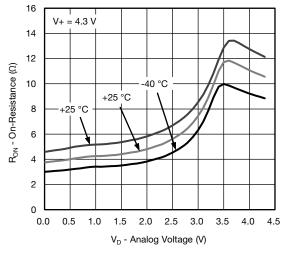
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature



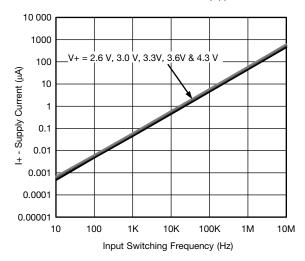
R_{ON} vs. Analog Voltage and Temperature



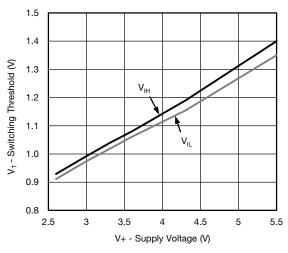
R_{ON} vs. Analog Voltage and Temperature



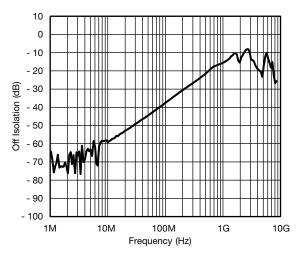
TYPICAL CHARACTERISTICS(T_A = 25 °C, unless otherwise noted)



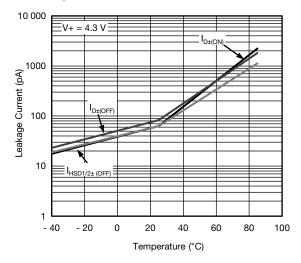
Supply Current vs. Input Switching Frequency



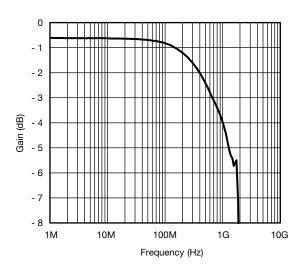
Switching Threshold vs. Supply Voltage



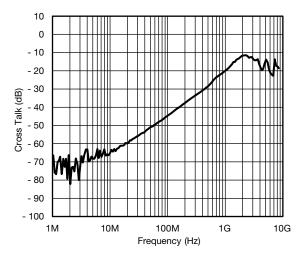
Off-Isolation, V+ = 3.3 V



Leakage Current vs. Temperature



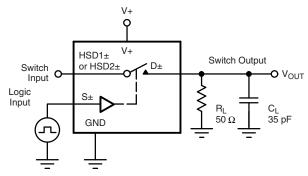
Gain vs. Frequency, V+ = 3.3 V



Crosstalk, V+ = 3.3 V

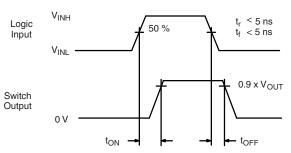


TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_{OUT} = D \pm \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch on Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time

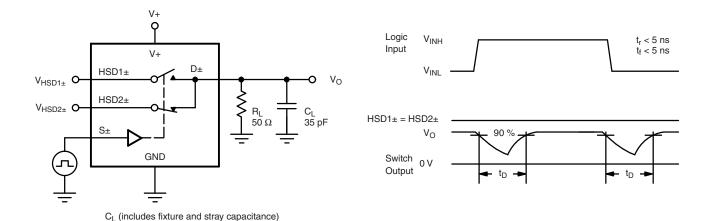


Fig. 2 - Break-Before-Make Interval

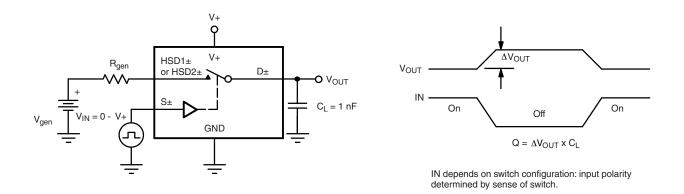


Fig. 3 - Charge Injection



TEST CIRCUITS

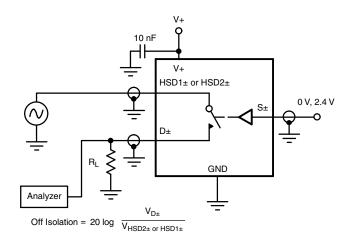


Fig. 4 - Off-Isolation

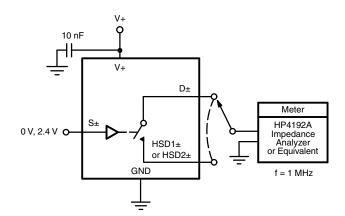


Fig. 5 - Channel Off/On Capacitance

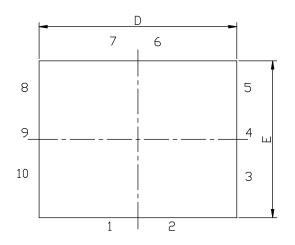
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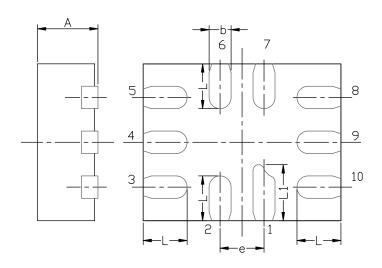


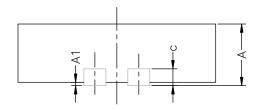
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MINI QFN-10L CASE OUTLINE







DIM		MILLIMETERS			INCHES			
DIM	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.		
Α	0.45	0.55	0.60	0.0177	0.0217	0.0236		
A1	0.00	-	0.05	0.000	-	0.002		
b	0.15	0.20	0.25	0.006	0.008	0.010		
С		0.150 or 0.127 REF ⁽¹⁾			0.006 or 0.005 REF ⁽¹)		
D	1.70	1.80	1.90	0.067 0.071 0.075				
E	1.30	1.40	1.50	0.051	0.055	0.059		
е		0.40 BSC			0.016 BSC			
L	0.35	0.40	0.45	0.014	0.016	0.018		
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217		

Note

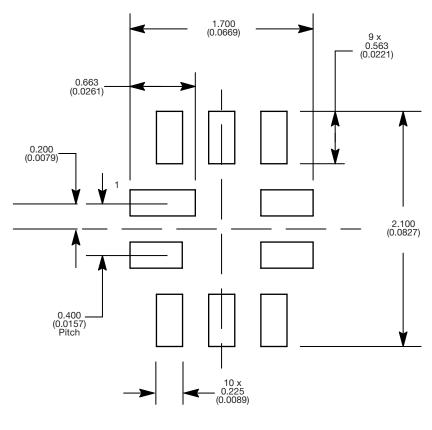
 $^{(1)}$ The dimension depends on the leadframe that assembly house used.

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RECOMMENDED MINIMUM PADS FOR MINI QFN 10L



Mounting Footprint Dimensions in mm (inch)

Document Number: 66554 Revision: 05-Mar-10

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