Contents

Pin Configuration

Figure 1. 48-pin TSOP I pinout (Front View) [1, 2]

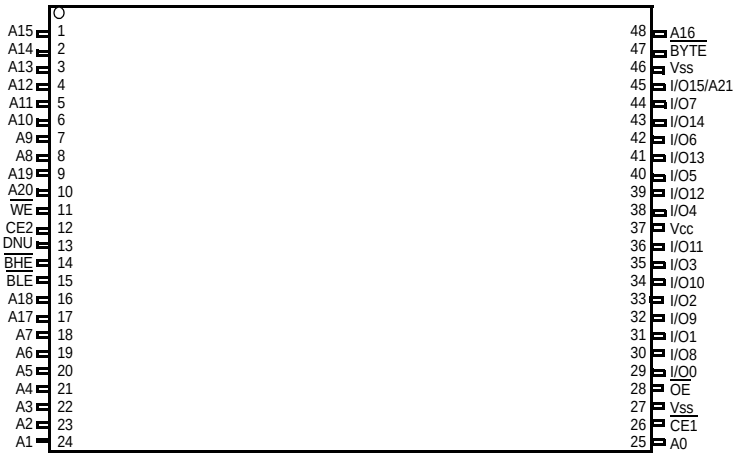
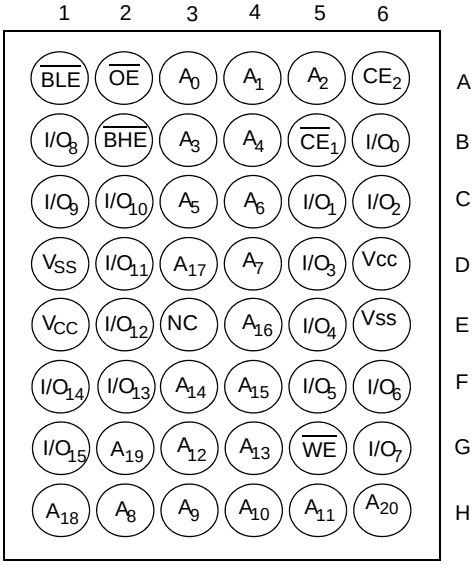


Figure 2. 48-ball FBGA pinout (Top View)



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ[3]	Max		Typ[3]	Max	Typ[3]	Max	Typ[3]	Max
CY62177EV18LL	1.65	1.8	2.25	70	4.5	5.5	35	45	3	25

Notes
1. DNU Pin# 13 needs to be left floating to ensure proper application.
2. The BYTE pin in the 48-TSOP I package has to be tied to V_{CC} to use the device as a 2 M × 16 SRAM. The 48-pin TSOP I package can also be used as a 4 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 4 M × 8 configuration, Pin 45 is A21, while BHE, BLE, and I/O_8 to I/O_{14} pins are not used.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.2 V to $V_{CC(max)}$ + 0.2 V

DC voltage applied to outputs in High Z state [4, 5] .....–0.2 V to $V_{CC(max)}$ + 0.2 V

DC input voltage [4, 5].....–0.2 V to $V_{CC(max)}$ + 0.2 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch up current .....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62177EV18LL	Industrial	–40 °C to +85 °C	1.65 V to 2.25 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		70 ns			Unit
				Min	Typ [7]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 1.65 V	1.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65 V	–	–	0.2	V
V_{IH}	Input HIGH voltage	V_{CC} = 1.65 V to 2.25 V		1.4	–	V_{CC} + 0.2 V	V
V_{IL}[8]	Input LOW voltage	V_{CC} = 1.65 V to 2.25 V		–0.2	–	0.4	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{Max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	35	45	mA
		f = 1 MHz		–	4.5	5.5	mA
I_{SB2} [9, 10]	Automatic CE power down current – CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	3	25	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
8. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7 V.
9. The $\overline{BYTE}$ pin in the 48-TSOP I package has to be tied to V_{CC} to use the device as a 2 M × 16 SRAM. The 48-TSOP I package can also be used as a 4 M × 8 SRAM by tying the $\overline{BYTE}$ signal to V_{SS}. In the 4 M × 8 configuration, Pin 45 is A21, while $\overline{BHE}$, $\overline{BLE}$, and I/O_8 to I/O_{14} pins are not used.
10. Chip enables ($\overline{CE_1}$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Parameter [11]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	15	pF
C_{OUT}	Output capacitance		15	pF

Thermal Resistance

Parameter [11]	Description	Test Conditions	FBGA	TSOPI	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	38.10	44.66	°C/W
Θ_{JC}	Thermal resistance (junction to case)		7.54	12.12	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms

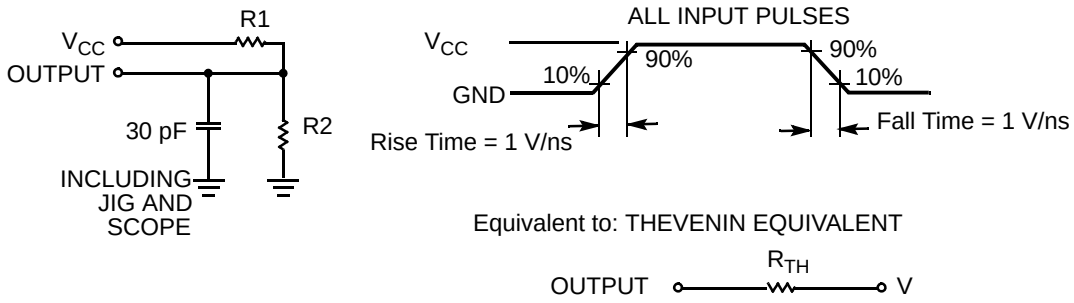


Table 1. AC Test Loads

Parameters	Value	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Note
11. Tested initially and after any design or process changes that may affect these parameters.

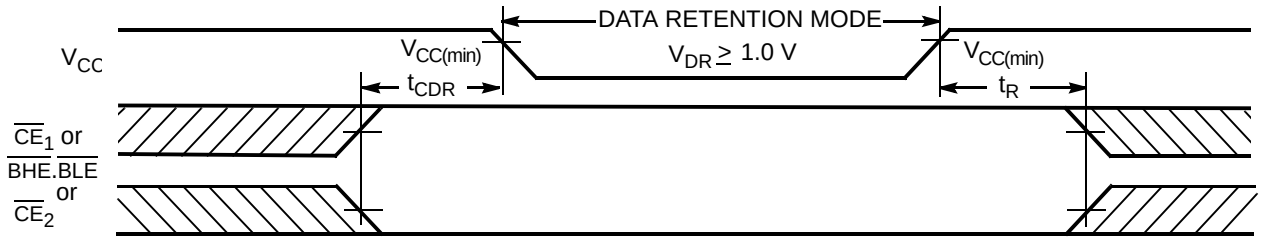
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [12]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} [13]	Data retention current	V_{CC} = 1.0 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	17	µA
t_{CDR} [14]	Chip deselect to data retention time		0	–	–	ns
t_R [15]	Operation recovery time		70	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform [16]



Notes

12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
13. Chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
16. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip is deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [17, 18]	Description	70 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	70	–	ns
t_{AA}	Address to data valid	–	70	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	70	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[19]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[19, 20]	–	25	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[19]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[19, 20]	–	25	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power down	–	70	ns
t_{DBE}	BLE/$\overline{BHE}$ LOW to data valid	–	70	ns
t_{LZBE}	BLE/$\overline{BHE}$ LOW to Low Z [19]	10	–	ns
t_{HZBE}	BLE/$\overline{BHE}$ HIGH to HIGH Z [19, 20]	–	25	ns
Write Cycle [21, 22]				
t_{WC}	Write cycle time	70	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	60	–	ns
t_{AW}	Address setup to write end	60	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	45	–	ns
t_{BW}	BLE/$\overline{BHE}$ LOW to write end	60	–	ns
t_{SD}	Data setup to write end	30	–	ns
t_{HD}	Data hold from Write End	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[19, 20]	–	25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[19]	10	–	ns

Notes

17. Test conditions for all parameters other than tristate parameters assume signal transition time of 1 V/ns, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Table 1 on page 5.
18. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
19. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
20. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
21. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled) [23, 24]

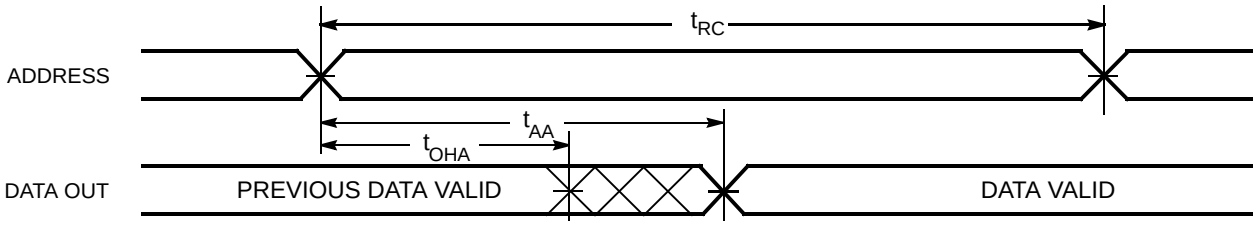
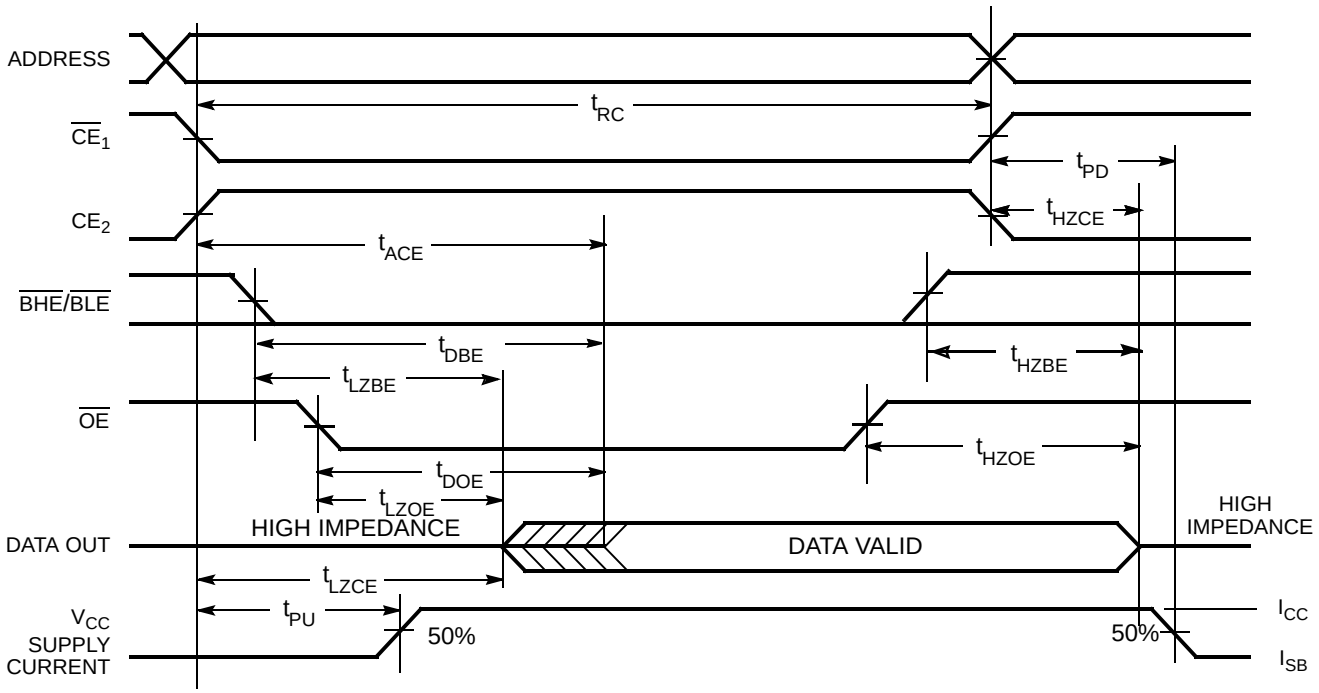


Figure 6. Read Cycle 2 ($\overline{OE}$ Controlled) [24, 25]



Notes
23. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}.
24. $\overline{WE}$ is HIGH for read cycle.
25. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms *(continued)*

Figure 7. Write Cycle 1 ($\overline{WE}$ Controlled) [26, 27, 28, 29]

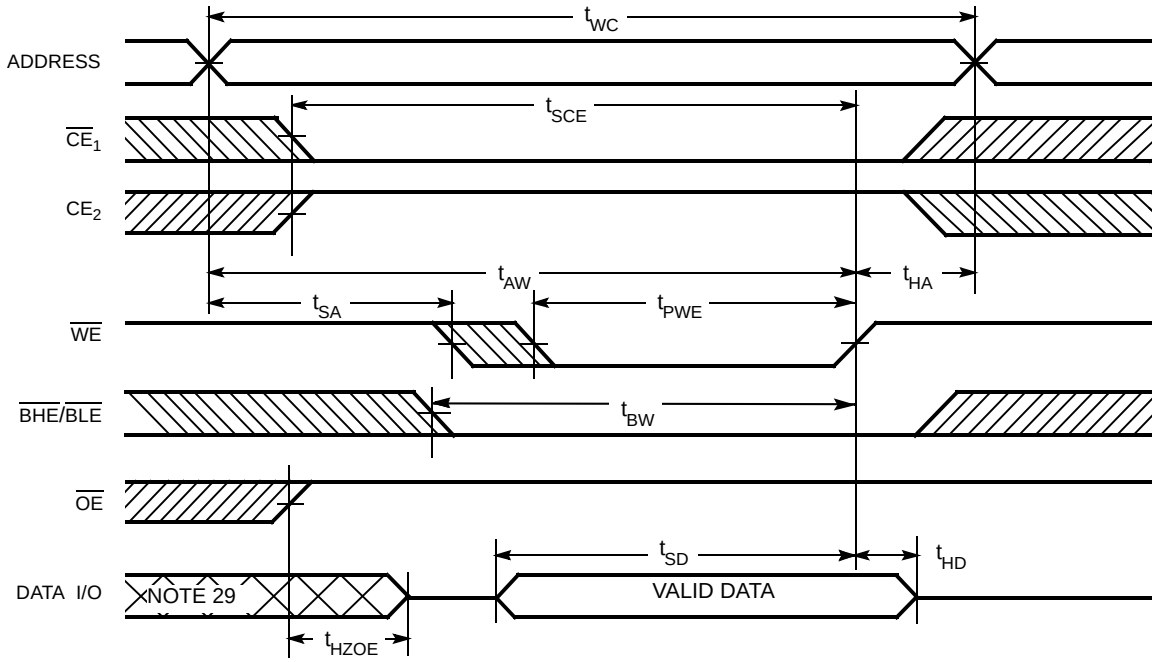
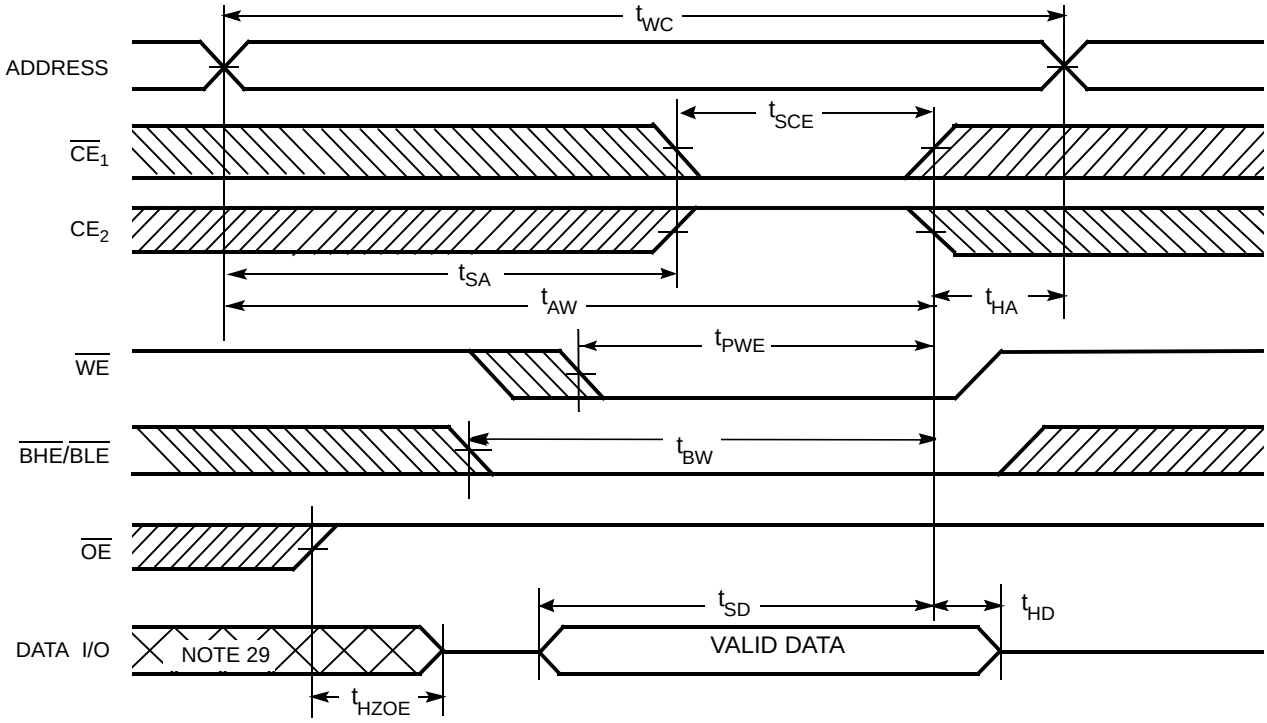


Figure 8. Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled) [26, 27, 28, 29]



Notes

26. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
27. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
28. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
29. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms *(continued)*

Figure 9. Write Cycle 3 (WE Controlled, OE LOW) [30, 31, 32]

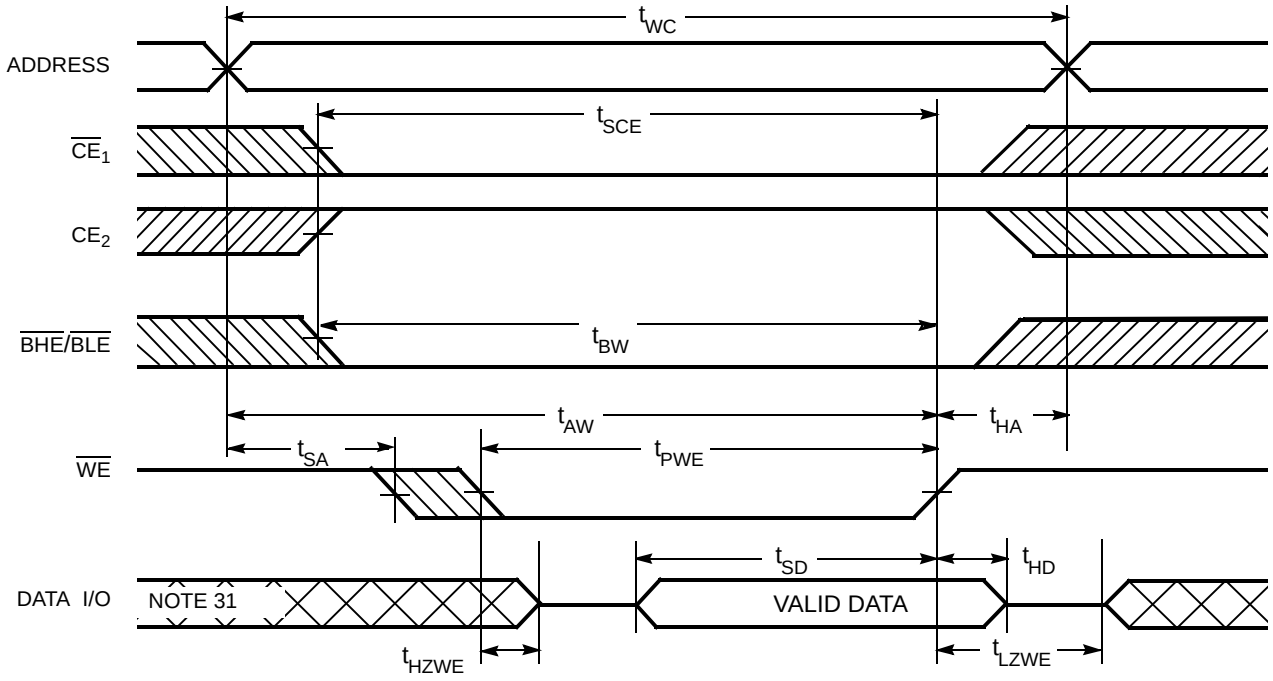
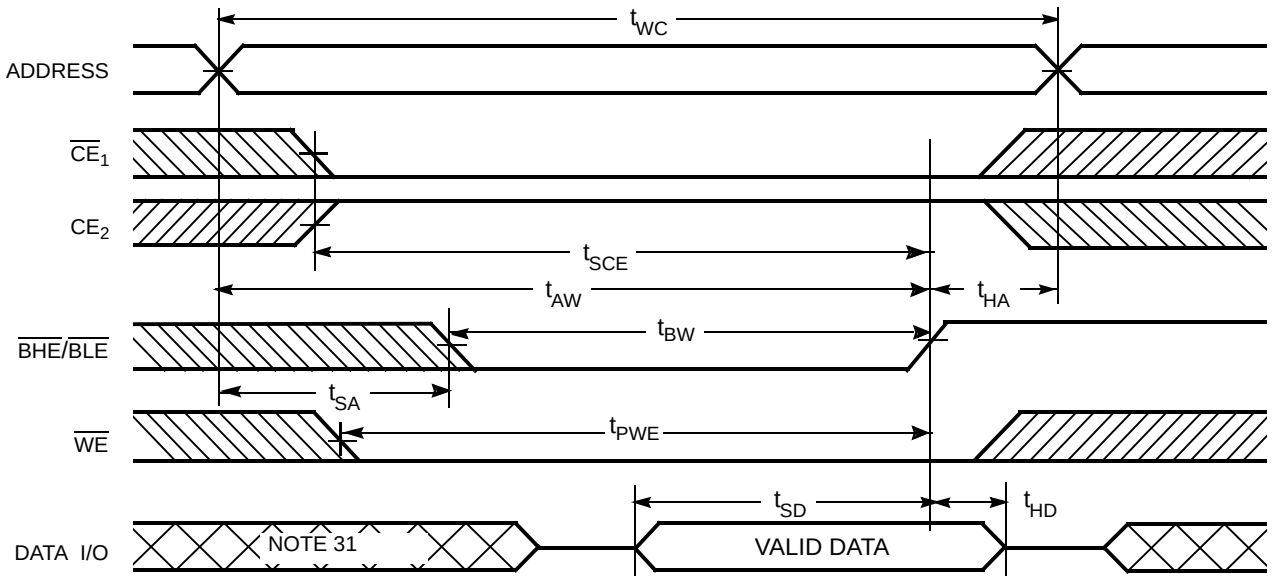


Figure 10. Write Cycle 4 (BHE/BLE Controlled, OE LOW) [30, 32]



Notes
30. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
31. During this period the I/Os are in output state and input signals should not be applied.
32. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X[33]	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X[33]	L	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X[33]	X[33]	X	X	H	H	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High Z (I/O_8–I/O_{15}); Data Out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High Z (I/O_8–I/O_{15}); Data In (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})

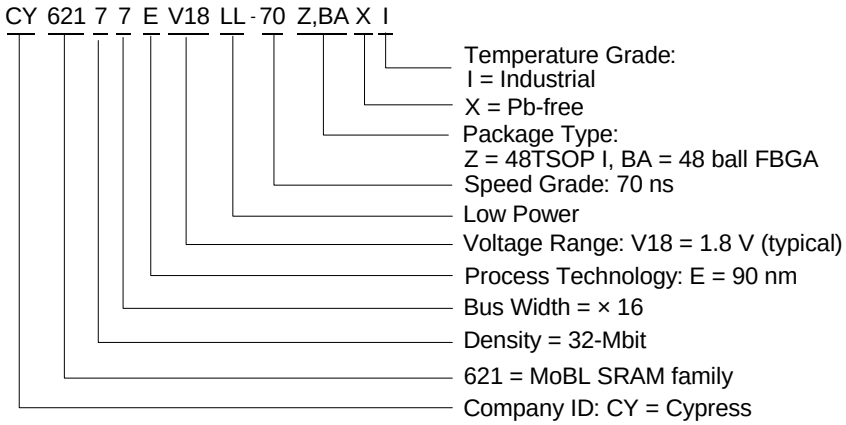
Note
33. The 'X' (Don't care) state for the chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62177EV18LL-70BAXI	51-85191	48 ball FBGA (8 × 9.5 × 1.2 mm) Pb-free	Industrial

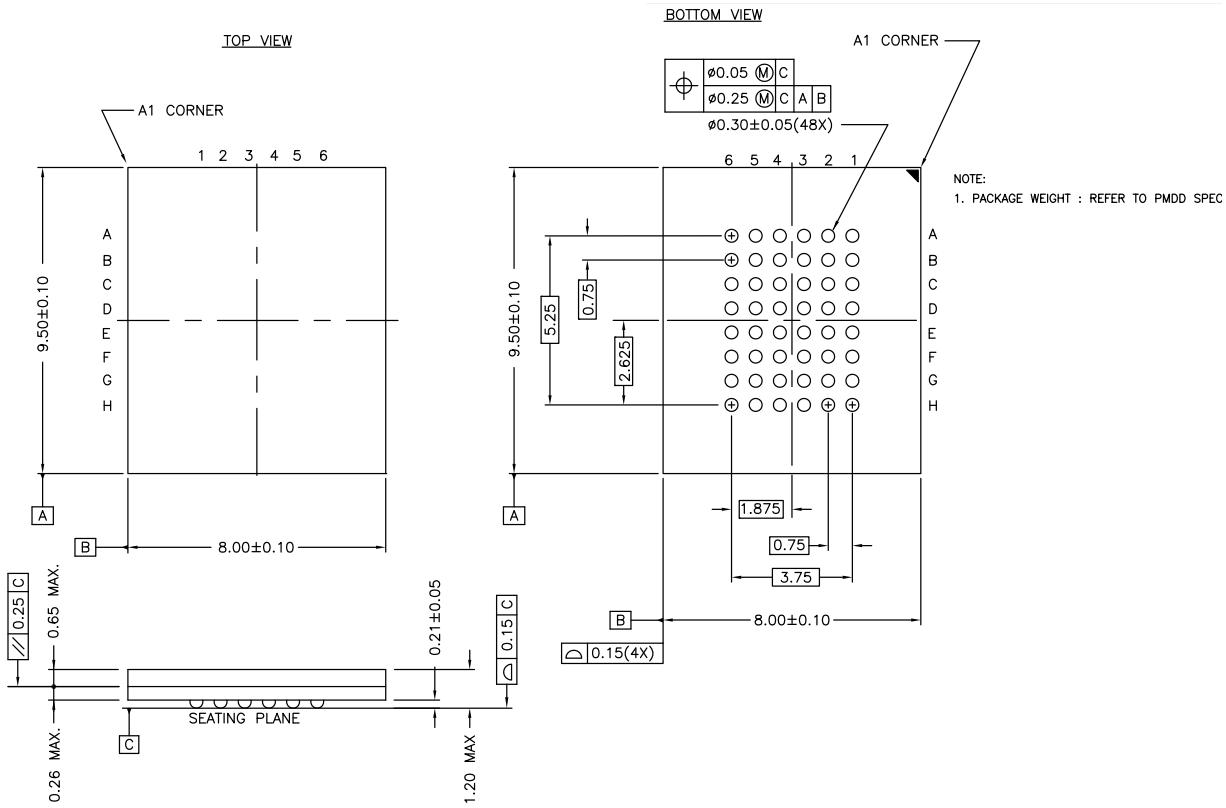
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

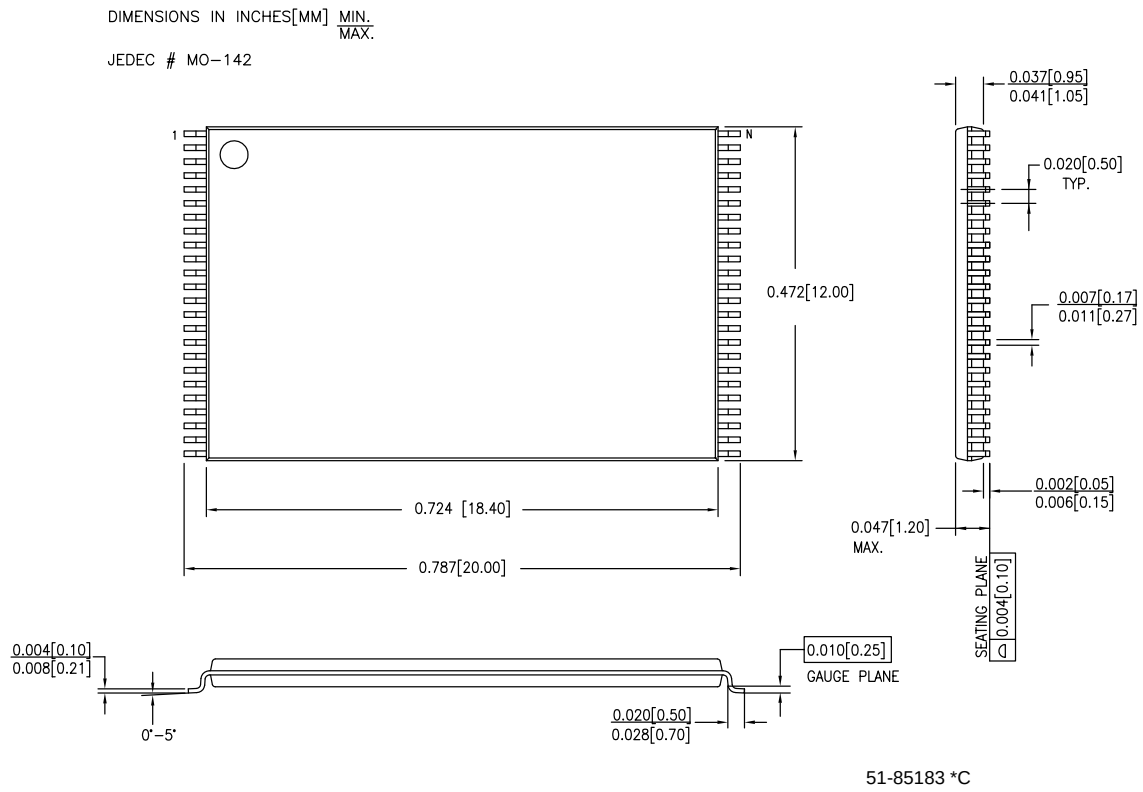
Figure 11. 48-ball FBGA (8 × 9.5 × 1.2 mm) Package Outline, 51-85191



51-85191 *C

Package Diagrams *(continued)*

Figure 12. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Package Outline, 51-85183



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY62177EV18 MoBL®, 32-Mbit (2 M × 16 / 4 M × 8) Static RAM Document Number: 001-76091				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3528465	AJU	02/17/2012	New data sheet.
*A	4116295	MEMJ	09/10/2013	Changed status from Preliminary to Final. Updated Features: Added 48-ball FBGA package related information. Updated Ordering Information (Updated part numbers). Updated Package Diagrams: spec 51-85191 – Changed revision from *B to *C. Updated in new template.
*B	4301112	NILE	03/07/2014	Updated Switching Characteristics: Added Note 18 and referred the same note in “Parameter” column. Completing Sunset Review.
*C	4571881	NILE	11/28/2014	Added related documentation hyperlink in page 1. Added Note 22 in Switching Characteristics. Added note reference 22 in the Switching Characteristics table. Added Note 32 in Switching Waveforms. Added note reference 32 in Figure 9.

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