

## Contents

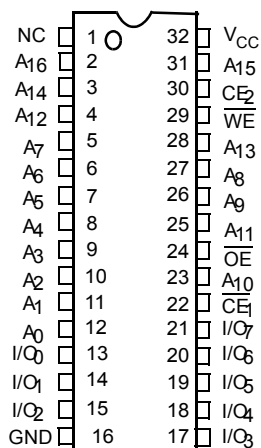
<b>Product Portfolio .....</b>	<b>3</b>	<b>Ordering Information .....</b>	<b>10</b>
<b>Pin Configuration .....</b>	<b>3</b>	Ordering Code Definitions .....	10
<b>Pin Definitions .....</b>	<b>3</b>	<b>Package Diagrams .....</b>	<b>11</b>
<b>Maximum Ratings .....</b>	<b>4</b>	<b>Acronyms .....</b>	<b>12</b>
<b>Operating Range .....</b>	<b>4</b>	<b>Document Conventions .....</b>	<b>12</b>
<b>Electrical Characteristics .....</b>	<b>4</b>	Units of Measure .....	12
<b>Capacitance .....</b>	<b>5</b>	<b>Document History Page .....</b>	<b>13</b>
<b>Thermal Resistance .....</b>	<b>5</b>	<b>Sales, Solutions, and Legal Information .....</b>	<b>14</b>
<b>AC Test Loads and Waveforms .....</b>	<b>5</b>	Worldwide Sales and Design Support .....	14
<b>Data Retention Waveform .....</b>	<b>6</b>	Products .....	14
<b>Data Retention Characteristics .....</b>	<b>6</b>	PSoC <sup>®</sup> Solutions .....	14
<b>Switching Characteristics .....</b>	<b>7</b>	Cypress Developer Community .....	14
<b>Switching Waveforms .....</b>	<b>8</b>	Technical Support .....	14
<b>Truth Table .....</b>	<b>10</b>		

## Product Portfolio

Product		V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation			
						Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
		Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY621282BN	Automotive-E	4.5	5.0	5.5	70	6	25	2.5	25

## Pin Configuration

Figure 1. 32-pin SOIC (Top View)



## Pin Definitions

I/O Type	Description
Input	<b>A<sub>0</sub>–A<sub>16</sub></b> . Address inputs
Input/output	<b>I/O<sub>0</sub>–I/O<sub>7</sub></b> . Data lines. Used as input or output lines depending on operation.
Input/control	<b>WE</b> . Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/control	<b>CE<sub>1</sub></b> . Chip Enable 1, Active LOW.
Input/control	<b>CE<sub>2</sub></b> . Chip Enable 2, Active HIGH.
Input/control	<b>OE</b> . Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
Ground	<b>GND</b> . Ground for the device.
Power supply	<b>V<sub>CC</sub></b> . Power supply for the device.

### Note

1. Typical values are included for reference only and are not tested or guaranteed. Typical values are measured at V<sub>CC</sub> = 5.0 V, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to relative GND<sup>[2]</sup> ..... -0.5 V to +7.0 V

DC voltage applied to outputs in High Z state <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[2, 3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Automotive-E	-40 °C to +125 °C	5 V ± 10%

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-70			Unit
			Min	Typ <sup>[4]</sup>	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = 4.5$ V, $I_{OH} = -1.0$ mA	2.4	—	—	V
		$V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA	3.95	—	—	
		$V_{CC} = 5$ V, $I_{OH} = -0.1$ mA	3.6	—	—	
		$V_{CC} = 4.5$ V, $I_{OH} = -0.1$ mA	3.25	—	—	
$V_{OL}$	Output LOW voltage	$V_{CC} = 4.5$ V, $I_{OL} = 2.1$ mA	—	—	0.4	V
$V_{IH}$	Input HIGH voltage		2.2	—	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage <sup>[2]</sup>		-0.3	—	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-10	—	+10	μA
$I_{OZ}$	Output leakage current	$GND \leq V_{IN} \leq V_{CC}$ , Output Disabled	-10	—	+10	μA
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{MAX} = 1/t_{RC}$	—	6	25	mA
		$f = 1$ MHz		2	12	
$I_{SB1}$	Automatic CE power-down current – TTL inputs	$V_{CC} = 5.5$ V, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	—	0.1	2	mA
$I_{SB2}$	Automatic CE power-down current – CMOS inputs	$V_{CC} = 5.5$ V, $\overline{CE}_1 \geq V_{CC} - 0.3$ V, or $CE_2 \leq 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V, or $V_{IN} \leq 0.3$ V, $f = 0$	—	2.5	25	μA

### Notes

2.  $V_{IL}$  (min.) = -2.0 V for pulse durations of less than 20 ns.

3. No input may exceed  $V_{CC} + 0.5$  V.

4. Typical values are included for reference only and are not tested or guaranteed. Typical values are measured at  $V_{CC} = 5.0$  V,  $T_A = 25$  °C.

## Capacitance

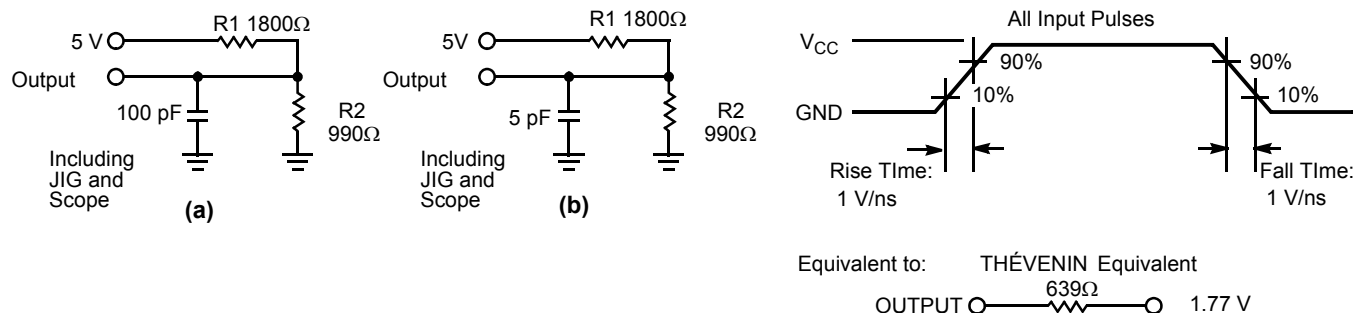
Parameter <sup>[5]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$	9	pF
$C_{OUT}$	Output capacitance		9	pF

## Thermal Resistance

Parameter <sup>[5]</sup>	Description	Test Conditions	32-pin SOIC	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	66.17	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		30.87	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

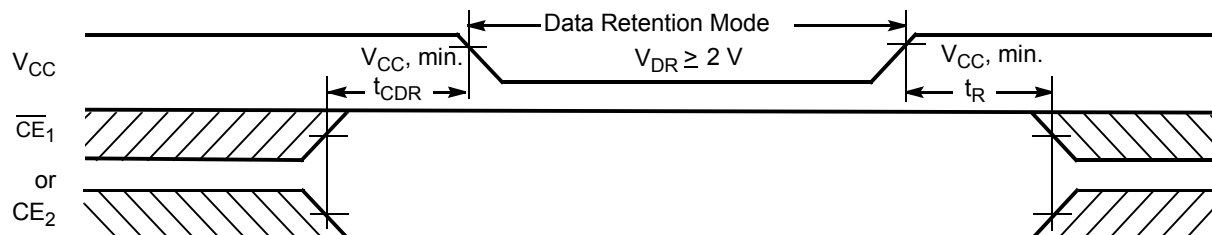


### Note

5. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Waveform

Figure 3. Data Retention Waveform



## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2.0	–	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $CE_1 \geq V_{CC} - 0.3\text{ V}$ , or $CE_2 \leq 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or, $V_{IN} \leq 0.3\text{ V}$	–	1.5	25	$\mu\text{A}$
$t_{CDR}$	Chip deselect to data retention time		0	–	–	ns
$t_R$	Operation recovery time		70	–	–	ns

## Switching Characteristics

Over the Operating Range

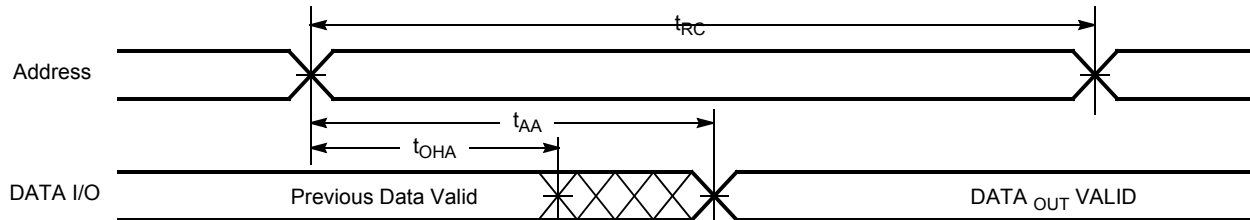
Parameter <sup>[6]</sup>	Description	CY621282BN-70		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	70	–	ns
t <sub>AA</sub>	Address to data valid	–	70	ns
t <sub>OHA</sub>	Data hold from address change	5	–	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW to data valid, CE <sub>2</sub> HIGH to data valid	–	70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	0	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup>	–	25	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW to Low Z, CE <sub>2</sub> HIGH to Low Z <sup>[7]</sup>	5	–	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH to High Z, CE <sub>2</sub> LOW to High Z <sup>[7, 8]</sup>	–	25	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW to Power-up, CE <sub>2</sub> HIGH to power-up	0	–	ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH to Power-down, CE <sub>2</sub> LOW to power-down	–	70	ns
Write Cycle <sup>[9, 10]</sup>				
t <sub>WC</sub>	Write cycle time	70	–	ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW to Write End, CE <sub>2</sub> HIGH to write end	60	–	ns
t <sub>AW</sub>	Address set-up to write end	60	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address set-up to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	50	–	ns
t <sub>SD</sub>	Data set-up to write end	30	–	ns
t <sub>HD</sub>	Data Hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	5	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>	–	25	ns

### Notes

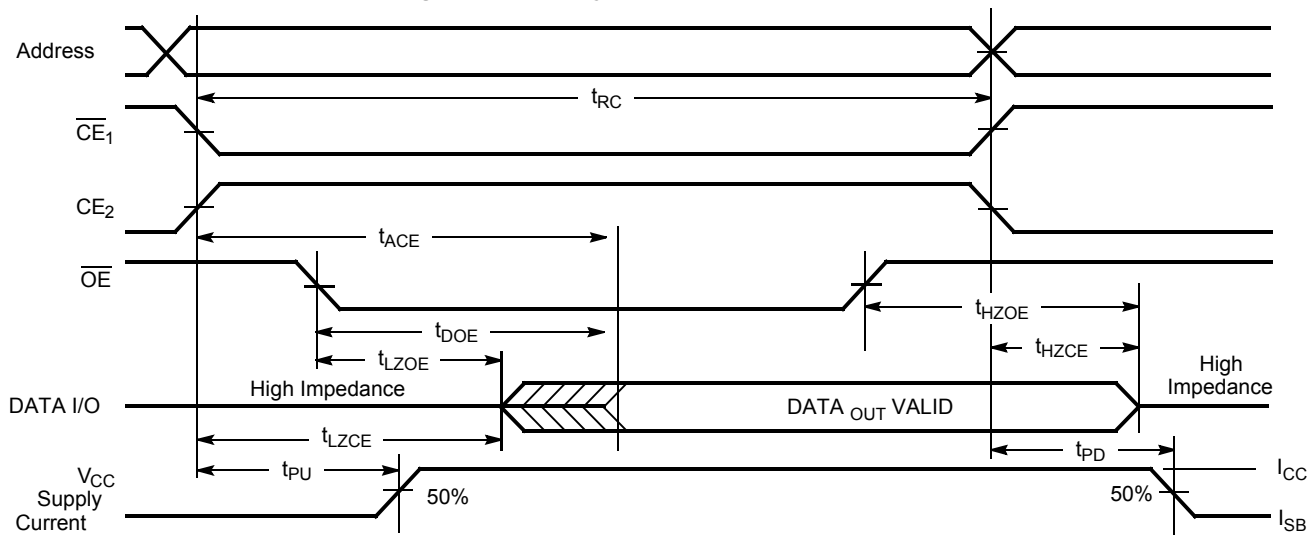
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 100-pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in (b) of [Figure 2 on page 5](#). Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle pulse width for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

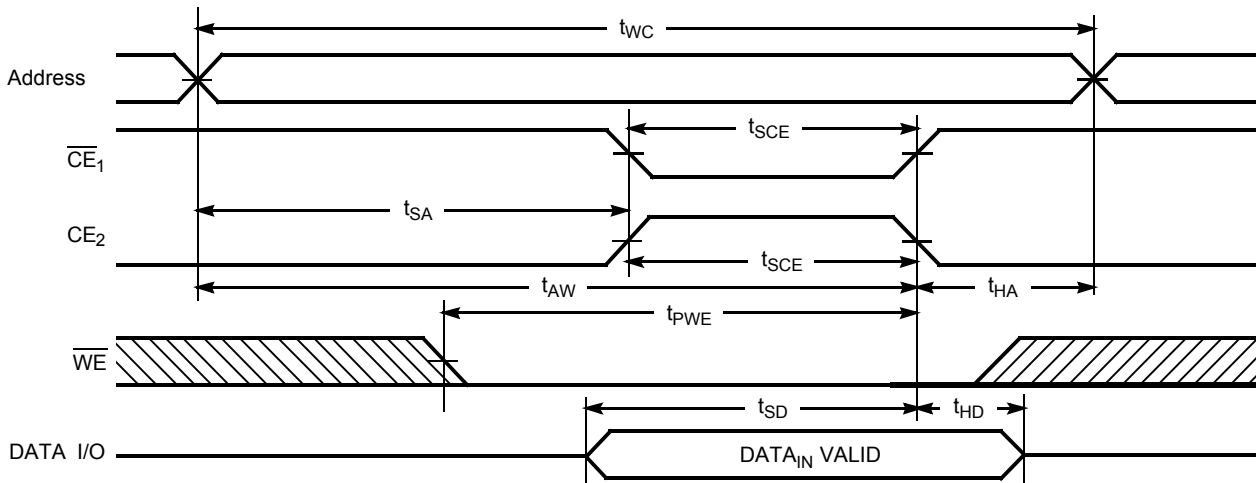
**Figure 4. Read Cycle No. 1** [11, 12]



**Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [12, 13]



**Figure 6. Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)** [14, 15]

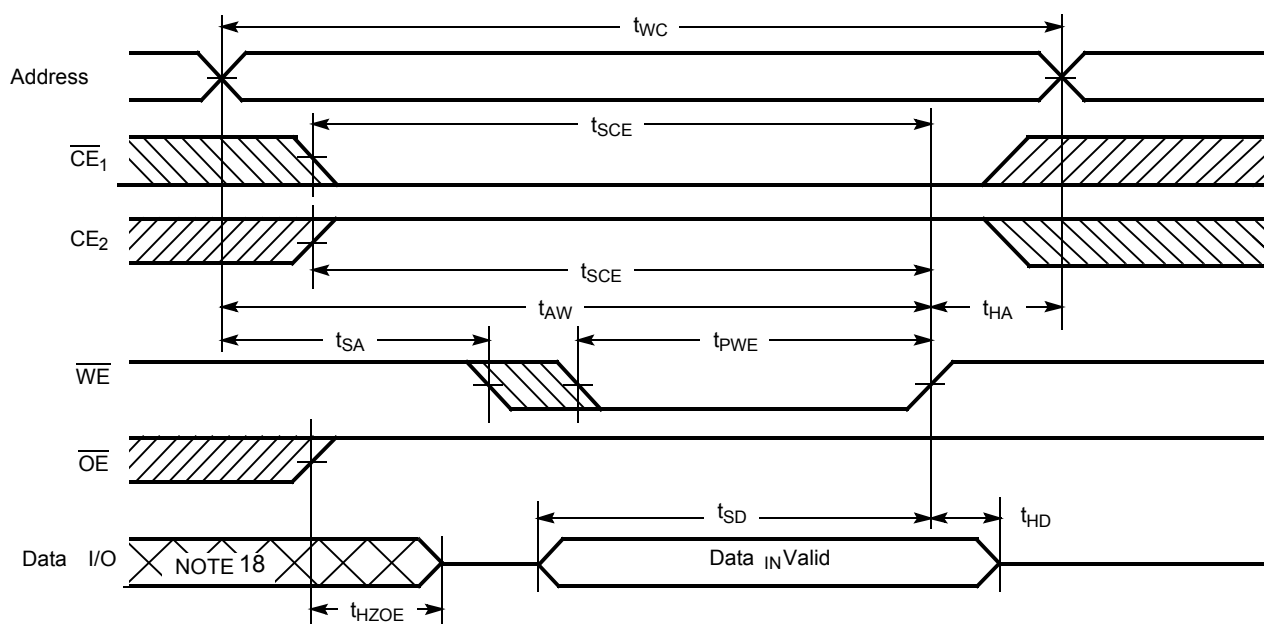


### Notes

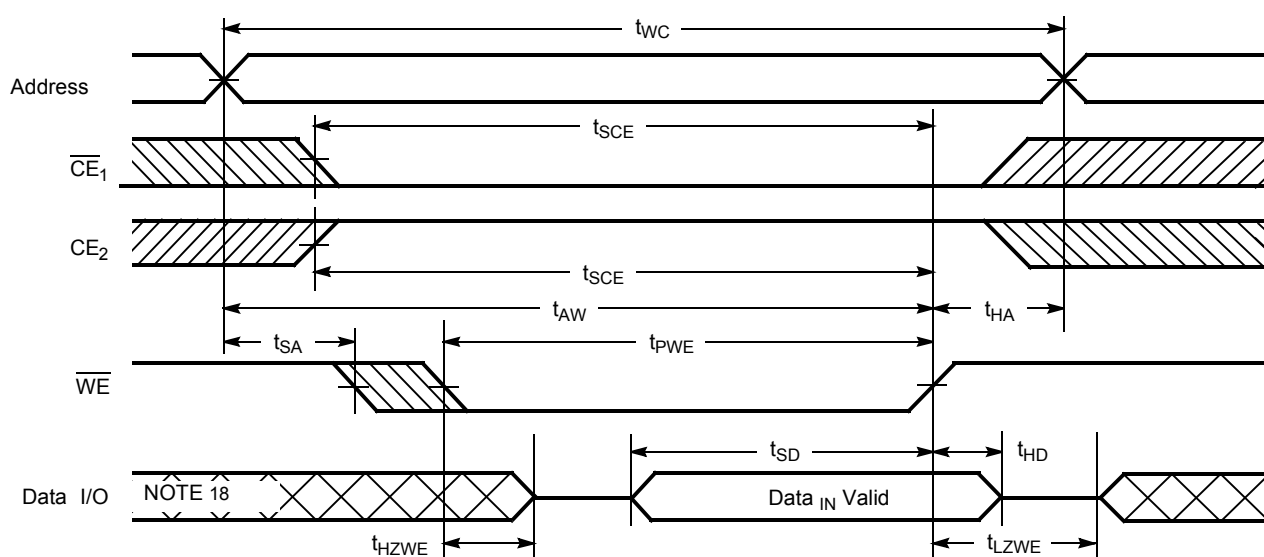
11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
15. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH during Write) [16, 17]**



**Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [16, 17, 19]**



### Notes

16. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
17. If  $\overline{CE}_1$  goes HIGH or  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
18. During this period the I/Os are in the output state and input signals should not be applied.
19. The minimum write cycle pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .



## Truth Table

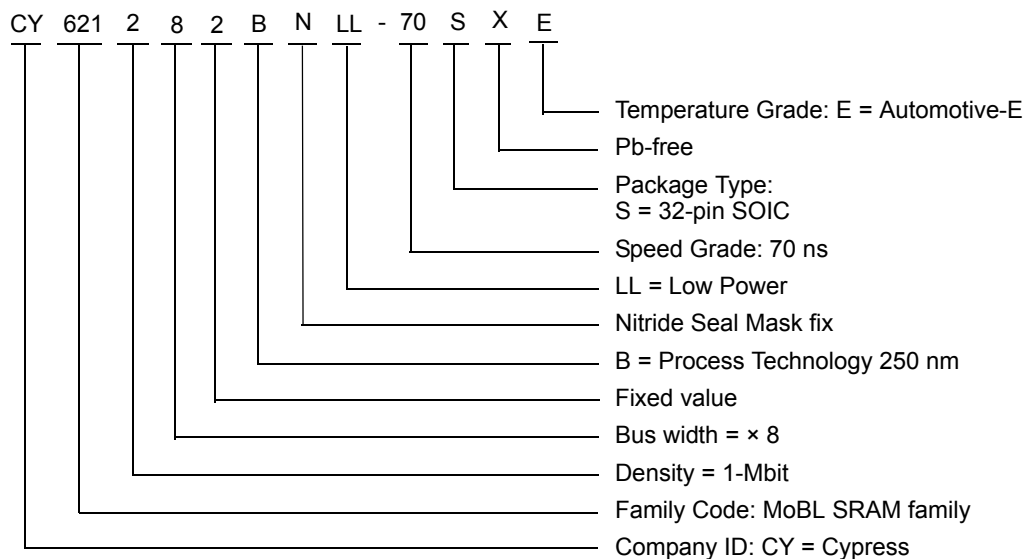
$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power-down	Standby ( $I_{SB}$ )
L	H	L	H	Data out	Read	Active ( $I_{CC}$ )
L	H	X	L	Data in	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, Outputs disabled	Active ( $I_{CC}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY621282BNLL-70SX E	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-E

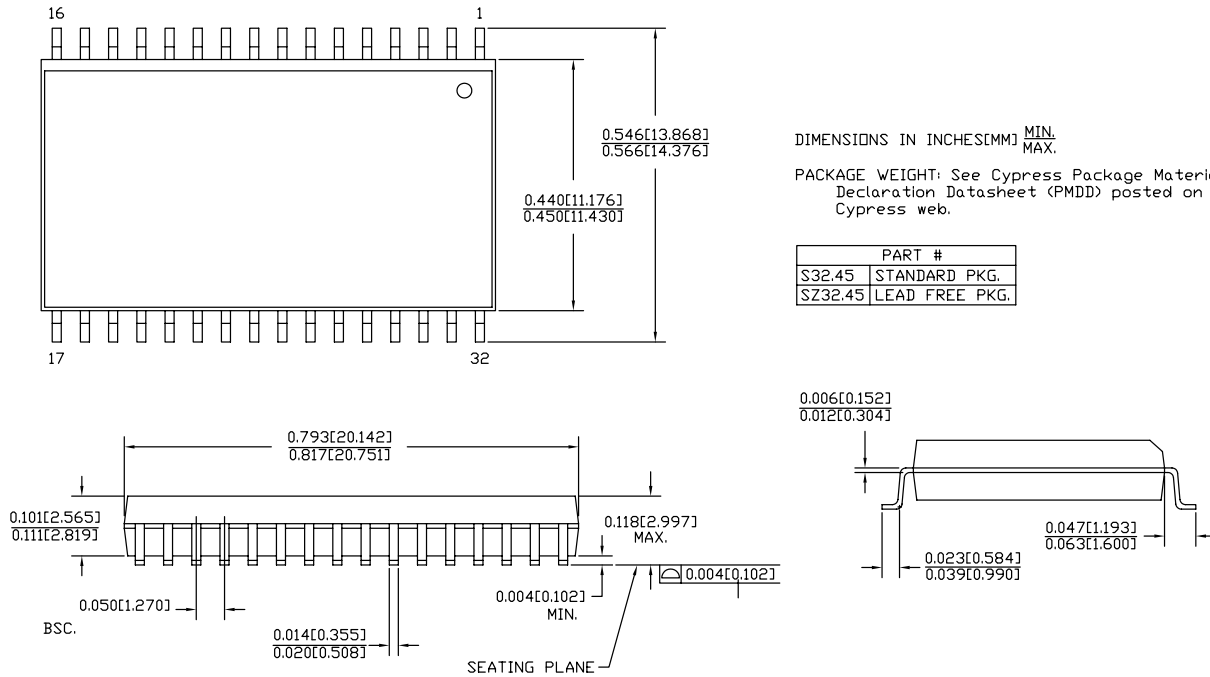
Please contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



## Package Diagrams

**Figure 9. 32-pin Molded SOIC (450 Mils) S32.45/SZ32.45, 51-85081**



51-85081 \*E

## Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

**Document Title: CY621282BN MoBL<sup>®</sup> Automotive, 1-Mbit (128 K × 8) Static RAM**  
**Document Number: 001-65526**

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	3115909	01/06/2011	RAME	New data sheet.
*A	3288690	06/21/2011	RAME	Updated <a href="#">Functional Description</a> : Removed the Note "For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <a href="http://www.cypress.com">http://www.cypress.com</a> website." and its reference. Updated to new template.
*B	3538379	03/05/2012	TAVA	Updated <a href="#">Electrical Characteristics</a> . Updated <a href="#">Switching Waveforms</a> . Updated <a href="#">Package Diagrams</a> .
*C	4703739	03/27/2015	MEMJ	Updated <a href="#">Switching Characteristics</a> : Added Note 10 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 19 and referred the same note in <a href="#">Figure 8</a> . Updated <a href="#">Package Diagrams</a> : spec 51-85081 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*D	4725832	04/15/2015	PSR	Updated <a href="#">Functional Description</a> : Added "For a complete list of related resources, <a href="#">click here</a> ." at the end.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

<a href="#">Automotive</a>	<a href="#">cypress.com/go/automotive</a>
<a href="#">Clocks &amp; Buffers</a>	<a href="#">cypress.com/go/clocks</a>
<a href="#">Interface</a>	<a href="#">cypress.com/go/interface</a>
<a href="#">Lighting &amp; Power Control</a>	<a href="#">cypress.com/go/powerpsoc</a>
<a href="#">Memory</a>	<a href="#">cypress.com/go/memory</a>
<a href="#">PSoC</a>	<a href="#">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="#">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="#">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="#">cypress.com/go/wireless</a>

#### PSoC<sup>®</sup> Solutions

[psoc.cypress.com/solutions](#)  
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2011-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.