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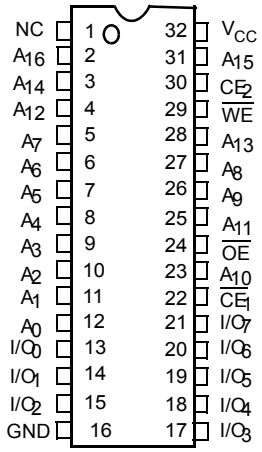
Product Portfolio

Product		V_{CC} Range (V)			Speed (ns)	Power Dissipation			
						Operating, I_{CC} (mA)		Standby, I_{SB2} (µA)	
		Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max
CY621282BN	Automotive-E	4.5	5.0	5.5	70	6	25	2.5	25

Pin Configuration

Figure 1. 32-pin SOIC (Top View)



Pin Definitions

I/O Type	Description
Input	**A_0–A_{16}**. Address inputs
Input/output	**I/O_0–I/O_7**. Data lines. Used as input or output lines depending on operation.
Input/control	**$\overline{WE}$**. Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/control	**$\overline{CE_1}$**. Chip Enable 1, Active LOW.
Input/control	**CE_2**. Chip Enable 2, Active HIGH.
Input/control	**$\overline{OE}$**. Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
Ground	**GND**. Ground for the device.
Power supply	**V_{CC}**. Power supply for the device.

Note
1. Typical values are included for reference only and are not tested or guaranteed. Typical values are measured at V_{CC} = 5.0 V, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[2] .....–0.5 V to +7.0 V

DC voltage applied to outputs in High Z state [2] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [2, 3] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive-E	–40 °C to +125 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-70			Unit
			Min	Typ [4]	Max	
V_{OH}	Output HIGH voltage	V_{CC} = 4.5 V, I_{OH} = –1.0 mA	2.4	–	–	V
		V_{CC} = 5.5 V, I_{OH} = –0.1 mA	3.95	–	–	
		V_{CC} = 5 V, I_{OH} = –0.1 mA	3.6	–	–	
		V_{CC} = 4.5 V, I_{OH} = –0.1 mA	3.25	–	–	
V_{OL}	Output LOW voltage	V_{CC} = 4.5 V, I_{OL} = 2.1 mA	–	–	0.4	V
V_{IH}	Input HIGH voltage		2.2	–	V_{CC}+ 0.3	V
V_{IL}	Input LOW voltage[2]		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}	–10	–	+10	µA
I_{OZ}	Output leakage current	GND ≤ V_{IN} ≤ V_{CC}, Output Disabled	–10	–	+10	µA
I_{CC}	V_{CC} operating supply current	f = f_{MAX} = 1/t_{RC}, V_{CC} = 5.5 V, I_{OUT} = 0 mA	–	6	25	mA
		f = 1 MHz, V_{CC} = 5.5 V, I_{OUT} = 0 mA		2	12	
I_{SB1}	Automatic CE power-down current – TTL inputs	V_{CC} = 5.5 V, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	0.1	2	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	V_{CC} = 5.5 V, $\overline{CE}_1$ ≥ V_{CC} – 0.3 V, or CE_2 ≤ 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	–	2.5	25	µA

Notes
2. V_{IL} (min.) = –2.0 V for pulse durations of less than 20 ns.
3. No input may exceed V_{CC} + 0.5 V.
4. Typical values are included for reference only and are not tested or guaranteed. Typical values are measured at V_{CC} = 5.0 V, T_A = 25 °C.

Capacitance

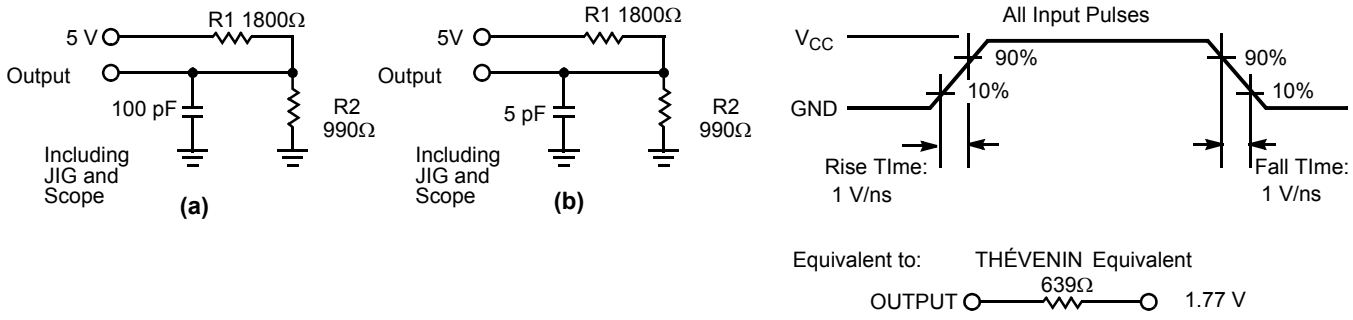
Parameter [5]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	9	pF
C_{OUT}	Output capacitance		9	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	32-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	66.17	°C/W
Θ_{JC}	Thermal resistance (junction to case)		30.87	°C/W

AC Test Loads and Waveforms

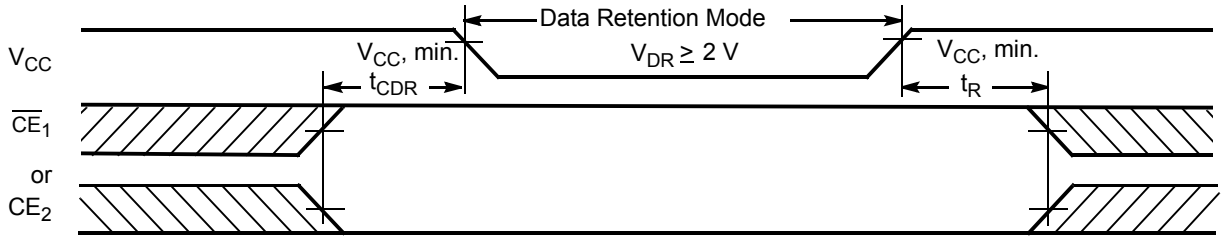
Figure 2. AC Test Loads and Waveforms



Note
5. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Waveform

Figure 3. Data Retention Waveform



Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ	Max	Unit
V_{DR}	V_{CC} for data retention			2.0	–	–	V
I_{CCDR}	Data retention current	$\overline{V_{CC}} = V_{DR} = 2.0$ V, $\overline{CE_1} \geq V_{CC} - 0.3$ V, or $CE_2 \leq 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or, $V_{IN} \leq 0.3$ V	Automotive-E	–	1.5	25	µA
t_{CDR}	Chip deselect to data retention time			0	–	–	ns
t_R	Operation recovery time			70	–	–	ns

Switching Characteristics

Over the Operating Range

Parameter [6]	Description	CY621282BN-70		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	70	–	ns
t_{AA}	Address to data valid	–	70	ns
t_{OHA}	Data hold from address change	5	–	ns
t_{ACE}	$\overline{CE}_1$ LOW to data valid, CE_2 HIGH to data valid	–	70	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [7]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [7, 8]	–	25	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z [7]	5	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z [7, 8]	–	25	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-up, CE_2 HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-down, CE_2 LOW to power-down	–	70	ns
Write Cycle [9, 10]				
t_{WC}	Write cycle time	70	–	ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to write end	60	–	ns
t_{AW}	Address set-up to write end	60	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	50	–	ns
t_{SD}	Data set-up to write end	30	–	ns
t_{HD}	Data Hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [7]	5	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [7, 8]	–	25	ns

Notes

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (b) of Figure 2 on page 5. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 [11, 12]

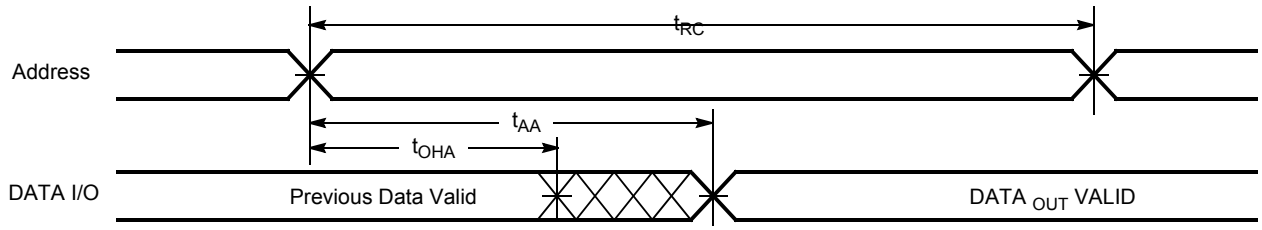


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]

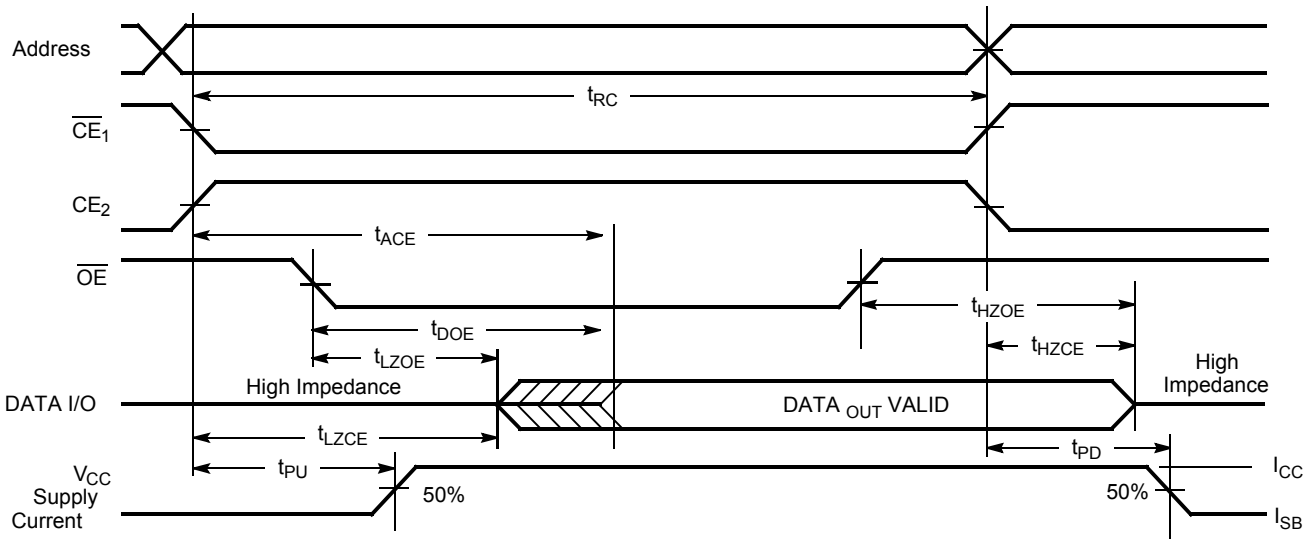
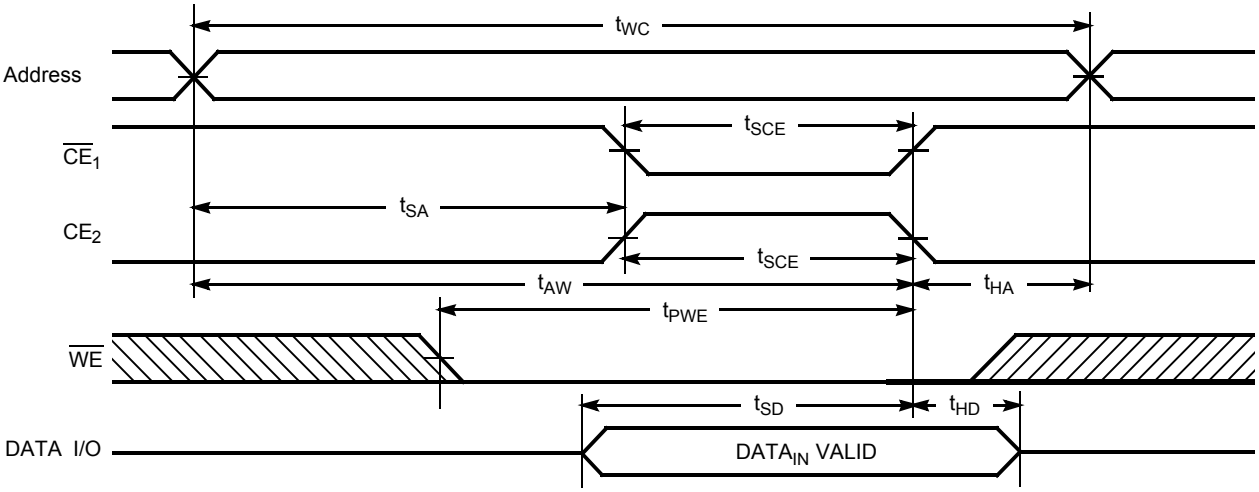


Figure 6. Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled) [14, 15]



Notes
11. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH during Write) [16, 17]

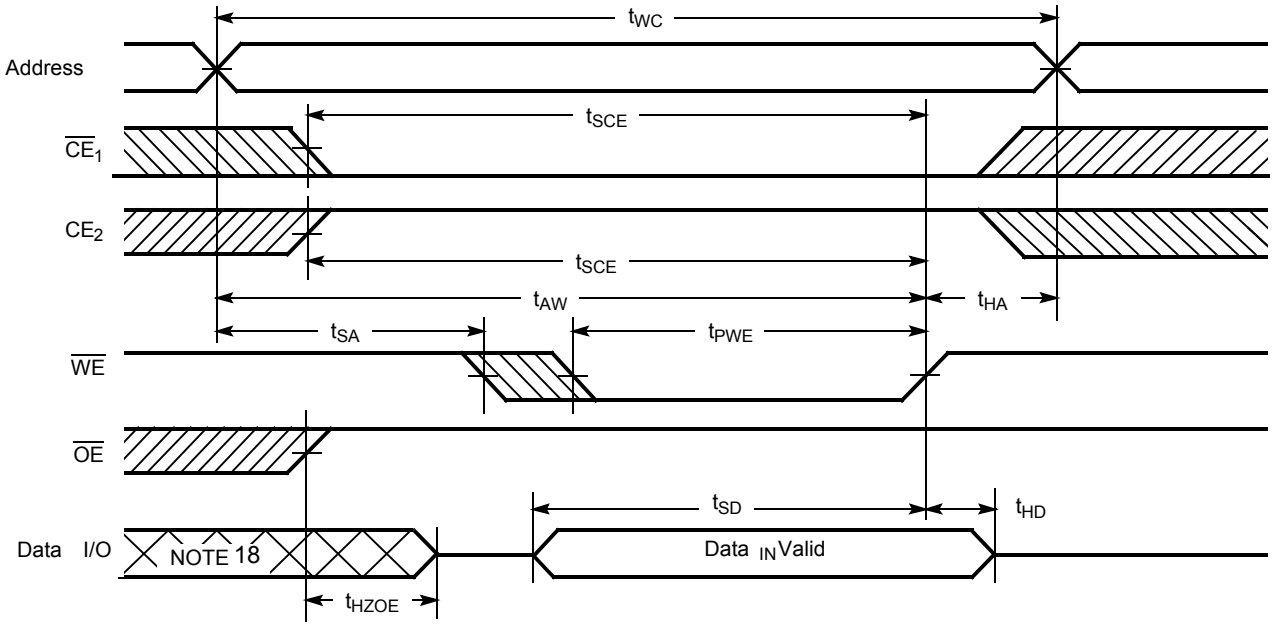
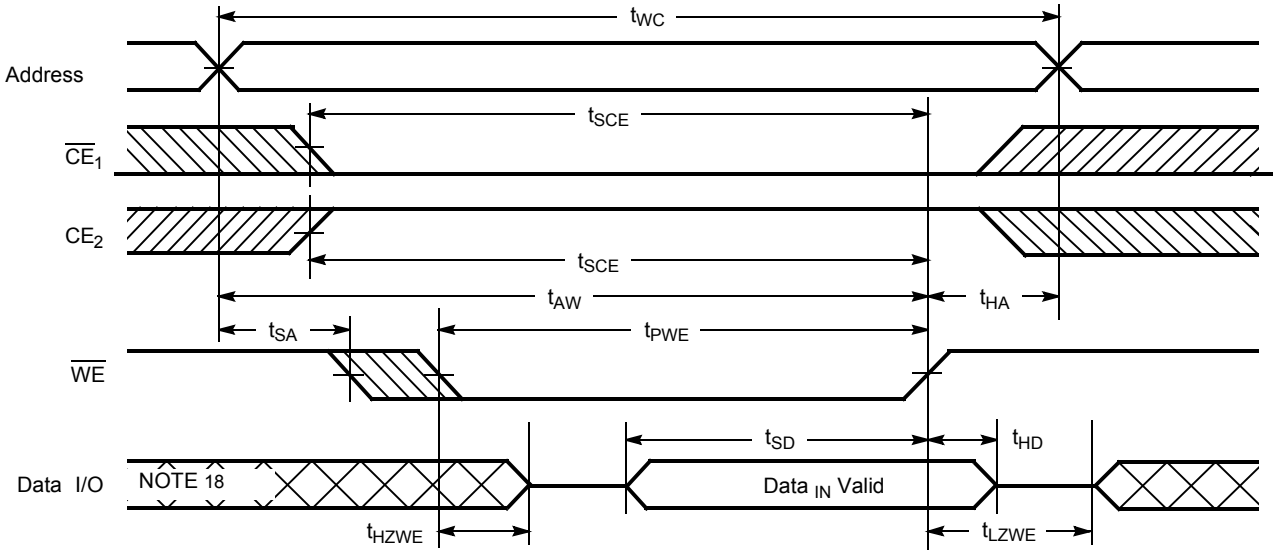


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [16, 17, 19]



Notes
16. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
17. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
18. During this period the I/Os are in the output state and input signals should not be applied.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

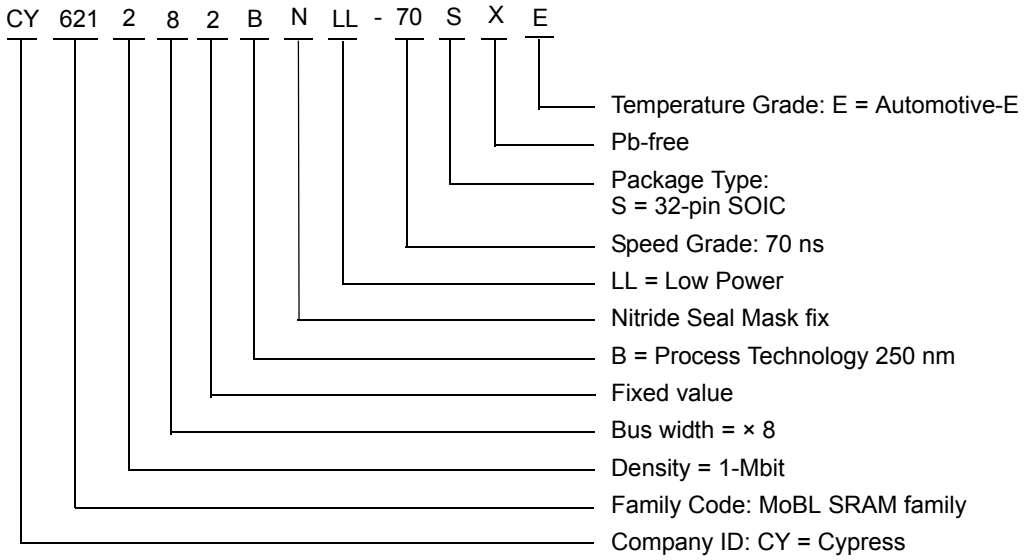
$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I_{SB})
X	L	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	H	Data out	Read	Active (I_{CC})
L	H	X	L	Data in	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY621282BNLL-70SXE	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-E

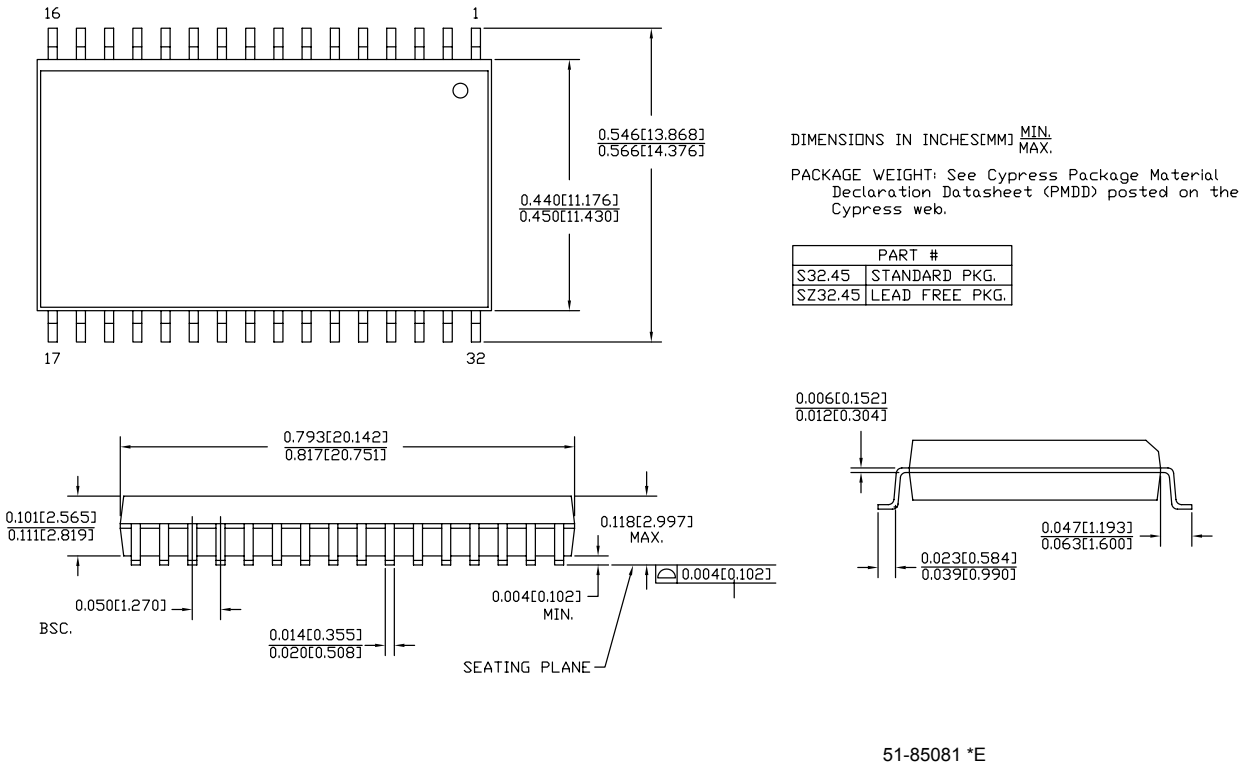
Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 9. 32-pin Molded SOIC (450 Mils) S32.45/SZ32.45, 51-85081



51-85081 *E

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY621282BN MoBL® Automotive, 1-Mbit (128 K × 8) Static RAM Document Number: 001-65526				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	3115909	01/06/2011	RAME	New data sheet.
*A	3288690	06/21/2011	RAME	Updated Functional Description: Removed the Note “For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com website.” and its reference. Updated to new template.
*B	3538379	03/05/2012	TAVA	Updated Electrical Characteristics. Updated Switching Waveforms. Updated Package Diagrams.
*C	4703739	03/27/2015	MEMJ	Updated Switching Characteristics: Added Note 10 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 19 and referred the same note in Figure 8. Updated Package Diagrams: spec 51-85081 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*D	4725832	04/15/2015	PSR	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end.

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