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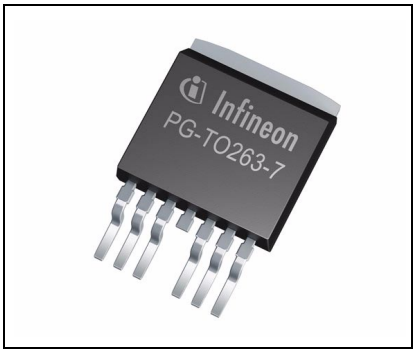
1 Overview



PG-TO263-7-8

Application

- All types of resistive, inductive and capacitive loads
- Replaces electromechanical relays and fuses
- Most suitable for applications with high current loads, such as heating system, main switch for power distribution and for switching single loads
- PWM application with low frequencies

Features

- One channel device
- Low Stand-by current
- Wide input voltage range (can be driven by logic levels 3.3V and 5V as well as directly by V_S)
- Electrostatic discharge protection (ESD)
- Optimized Electromagnetic Compatibility (EMC)
- Logic ground independent from load ground
- Very low leakage current on OUT pin
- Compatible to cranking pulse requirement (test pulse 4 of ISO7637 and cold start pulse in LV124)
- Embedded diagnostic functions
- Embedded protection functions
- Green Product (RoHS compliant)
- AEC Qualified

Description

The BTS50010-1TAC is a 1.0mΩ single channel Smart High-Side Power Switch, embedded in a PG-TO-263-7-8 package, providing protective functions and diagnosis. It contains Infineon® Reversave. The power transistor is built by a N-channel power MOSFET with charge pump. It is specially designed to drive high current loads up to 80A, for applications like switched battery couplings, power distribution switches, heaters, glow plugs, in the harsh automotive environment.

Type	Package	Marking
BTS50010-1TAC	PG-TO-263-7-8	S50010C

Table 1 Product Summary

Parameter	Symbol	Values
Operating voltage range	$V_{S(OP)}$	8 V … 18 V
Extended supply voltage contain dynamic undervoltage capability	$V_{S\ (DYN)}$	3.2 V … 28 V
Maximum on-state resistance at T_j = 150 °C	$R_{DS(ON)}$	2 mΩ
Minimum nominal load current	$I_{L\ (nom)}$	40 A
Typical current sense ratio	dk_{ILIS}	51500
Minimum short circuit current threshold	$I_{L\ (OVL)}$	150 A
Maximum stand-by current for the whole device with load at T_A=T_J= 85°C	$I_{S\ (OFF)}$	18 µA
Maximum reverse battery voltage at T_A = 25°C for 2 min	$-V_{S(REV)}$	16 V

Embedded Diagnostic Functions

- Proportional load current sense
- Short circuit / Overtemperature detection
- Latched status signal after short circuit or overtemperature detection

Embedded Protection Functions

- Infineon® Reversave: Reverse battery protection by self turn ON of power MOSFET
- Infineon® Inversave: Inverse operation robustness capability
- Secure load turn-OFF while device loss of GND connection
- Overtemperature protection with latch
- Short circuit protection with latch
- Overvoltage protection with external components
- Enhanced short circuit operation
- Infineon® SMART CLAMPING

2 Block Diagram

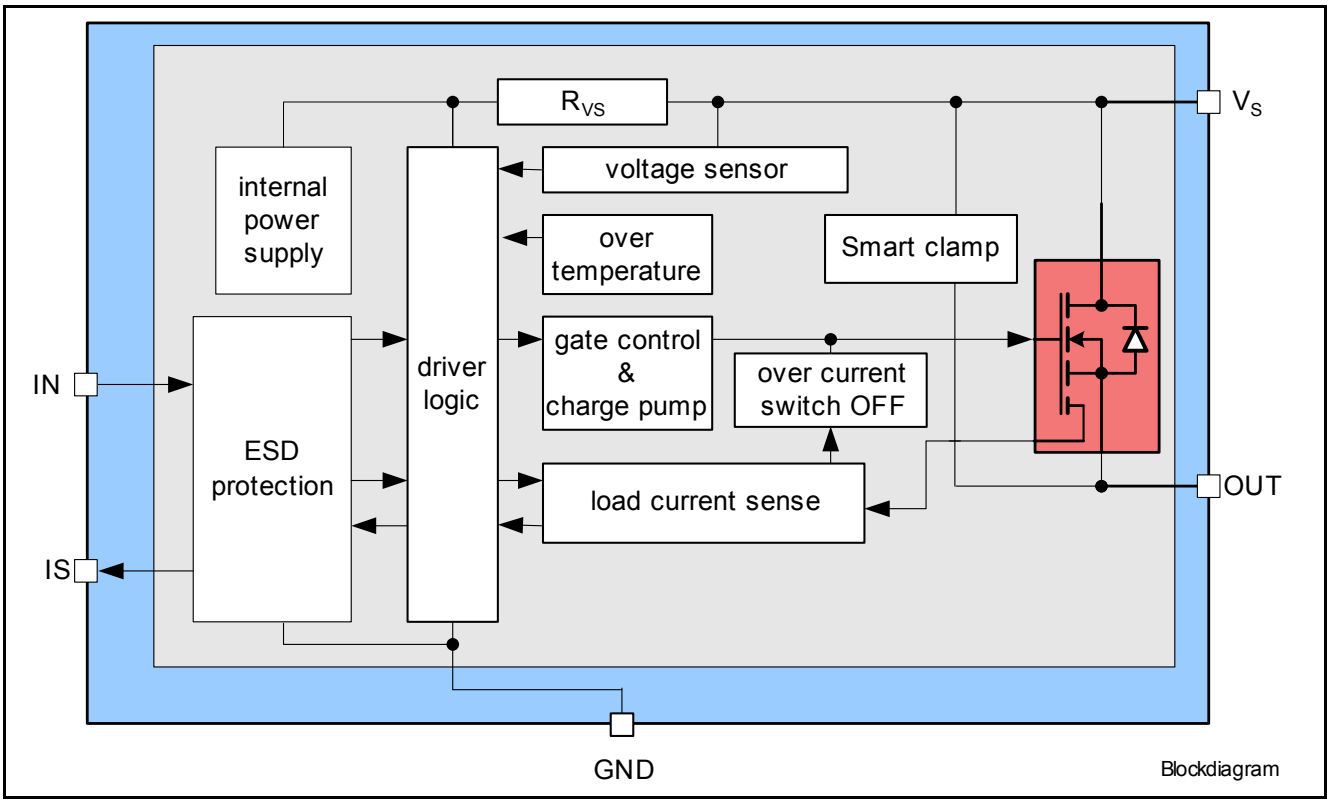


Figure 1 Block Diagram for the BTS50010-1TAC

3 Pin Configuration

3.1 Pin Assignment

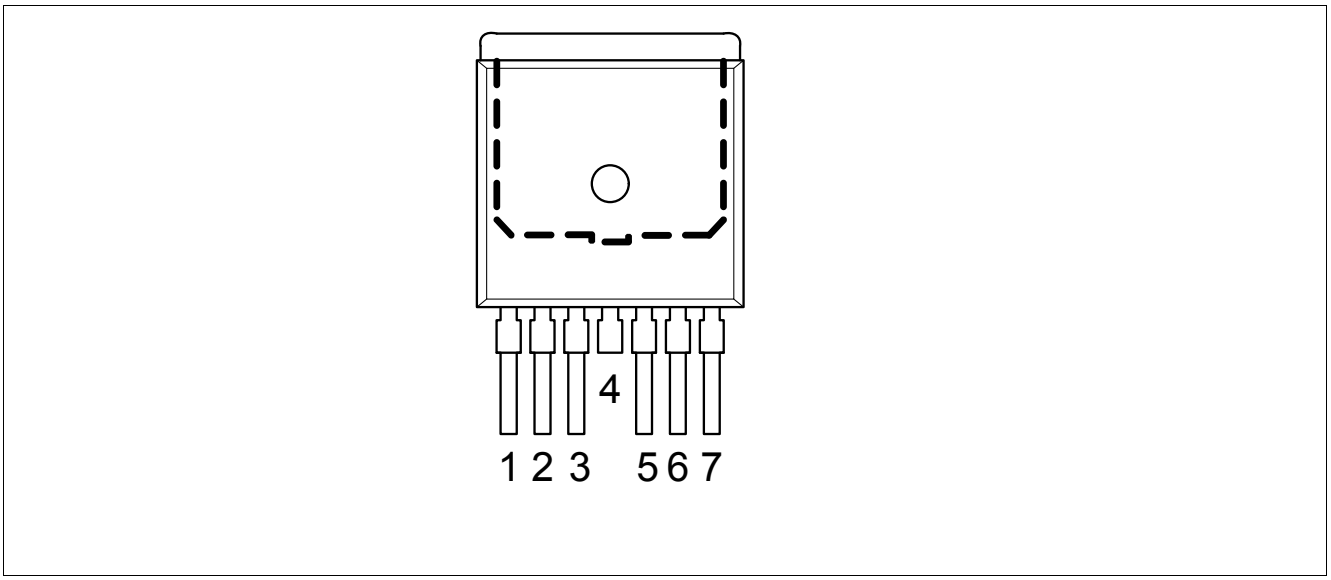


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**GrouND;** Ground connection
2	IN	**INput;** Input signal for channel activation. HIGH active
3	IS	**Sense;** Provides signal for diagnosis
4, Cooling tab	VS	**Supply Voltage;** Battery voltage
5, 6, 7	OUT	**OUTput;** Protected high side power output[1)]

1) All output pins are internally connected and they also have to be connected together on the PCB. Not shorting all outputs on PCB will considerably increase the ON-state resistance and decrease the current sense / overcurrent tripping accuracy. PCB traces have to be designed to withstand the maximum current.

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this datasheet, with associated convention for positive values.

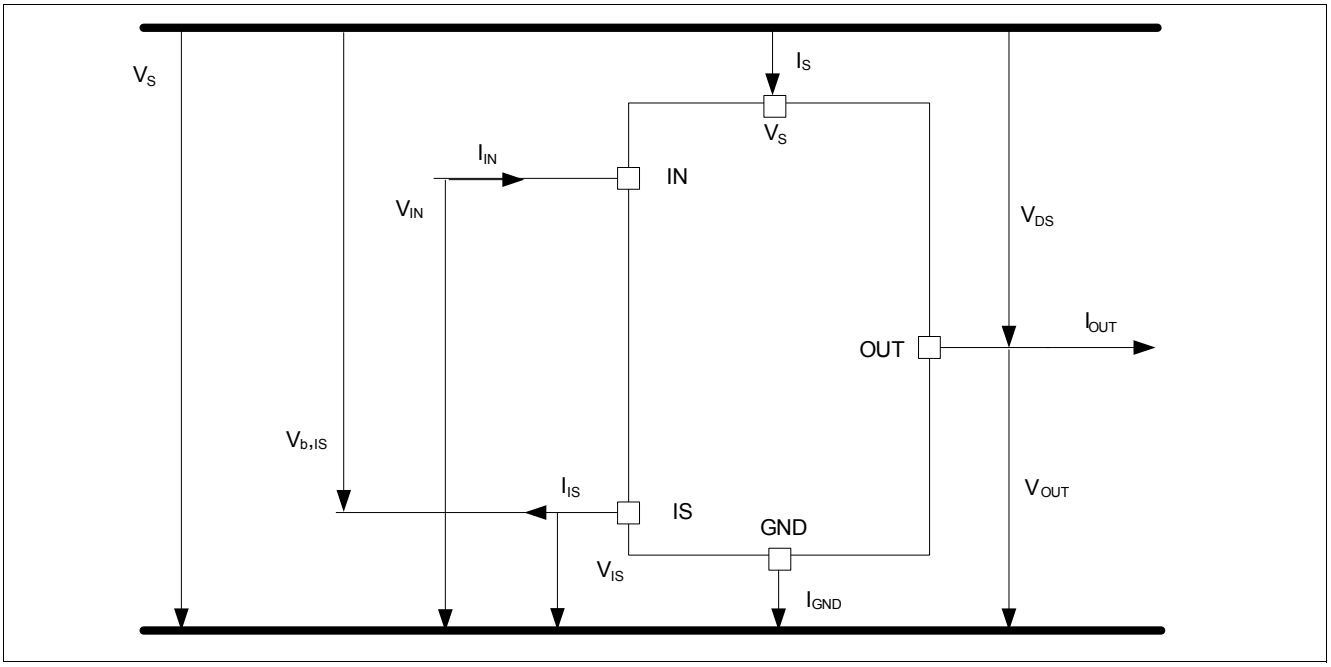


Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_j = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply Voltage	V_S	-0.3	–	28	V	–	4.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	16	V	[2)] t < 2 min T_A = 25°C $R_L \geq 0.5\Omega$	4.1.2
Supply voltage for load dump protection	$V_{S(LD)}$	–	–	45	V	[3)] R_I = 2Ω R_L = 2.2Ω R_{IS} = 1kΩ R_{IN} = 4.7kΩ	4.1.5
Short circuit capability							
Supply voltage for short circuit protection	$V_{S(SC)}$	5	–	20	V	[4)] R_{ECU} = 20mΩ L_{ECU} = 1µH R_{cable} = 6mΩ/m L_{cable} = 1µH/m l = 0 to 5m *R*, *C* as shown in **Figure 51** See **Chapter 5.3**	4.1.3
Short circuit is permanent: IN pin toggles short circuit (SC type 1)	n_{RSC1}	–	–	100k (Grade D)	–	[5)]	4.1.4
GND pin							
Current through ground pin	I_{GND}	-15 –[6)]	– –	10[7)] 15	mA	– $t \leq$ 2 min	4.1.6
Input Pin							
Voltage at IN pin	V_{IN}	-0.3	–	V_S	V	–	4.1.7
Current through IN pin	I_{IN}	-5 -5	– –	5 50[6)]	mA	– $t \leq$ 2 min	4.1.8
Maximum retry cycle rate in fault condition	f_{fault}	–	–	1	Hz	–	4.1.9
Sense Pin							
Voltage at IS pin	V_{IS}	-0.3	–	V_S	V	–	4.1.10
Current through IS pin	I_{IS}	-15 –[6)]	– –	10[7)] 15	mA	– $t \leq$ 2 min	4.1.11

Table 2 Absolute Maximum Ratings (cont'd)[1)]

T_j = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power Stage							
Maximum energy dissipation by switching off inductive load Single pulse over lifetime	E_{AS}	–	–	470	mJ	V_S = 13.5V $I_L = I_{L(NOM)}$ = 40A $T_{J(0)} \leq$ 150°C See **Figure 5**	4.1.12
Maximum energy dissipation Repetitive pulse	E_{AR}	–	–	200	mJ	[8)] V_S = 13.5V $I_L = I_{L(NOM)}$ = 40A $T_{J(0)} \leq$ 105°C See **Figure 5**	4.1.13
Maximum energy dissipation Repetitive pulse	$E_{AR(OVL)}$	–	–	200	mJ	[8)] V_S = 13.5V I_L = 80A $T_{J(0)} \leq$ 105°C See **Figure 5**	4.1.14
Average power dissipation	P_{TOT}	–	–	200	W	T_C = -40°C to 150°C	4.1.15
Voltage at OUT Pin	V_{OUT}	-64	–	–	V	–	4.1.21
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	4.1.16
Dynamic temperature increase while switching	ΔT_J	–	–	60	K	See **Chapter 5.3**	4.1.17
Storage Temperature	T_{STG}	-55	–	150	°C	–	4.1.18
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	HBM[9)]	4.1.19
ESD susceptibility OUT Pin vs. GND / V_S	V_{ESD}	-4	–	4	kV	HBM[9)]	4.1.20

1) Not subject to production test, specified by design.
2) The device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection.
3) $V_{S(LD)}$ is setup without DUT connected to the generator per ISO 7637-1.
4) In accordance to AEC Q100-012
5) In accordance to AEC Q100-012. Test aborted after 100,000 cycles. Short circuit conditions deviating from AEC Q100-012 may influence the specified short circuit cycle number in the datasheet.
6) The total reverse current (sum of I_{GND}, I_{IS} and $-I_{IN}$) is limited by $-V_{S(REV)\_max}$ and R_{VS}.
7) $T_C \leq$ 125°C
8) Equivalent to short circuit test AEC Q100-012: Grade A (for cycles > 1 Mio., parameter deviations are possible; Test aborted after 10 Mio. Cycles without fails)
9) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

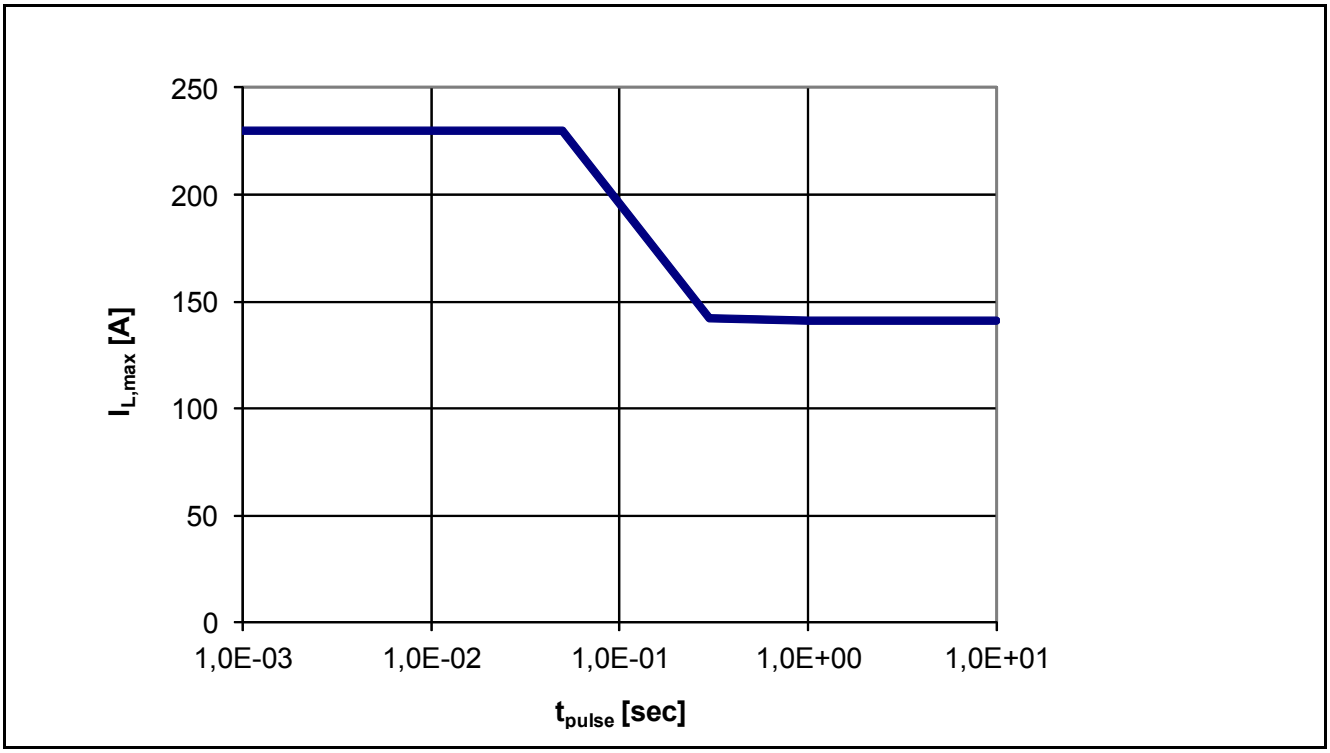


Figure 4 Maximum Single Pulse Current vs. Pulse Time, $T_J \leq 150°C$, $T_{amb} = 85°C$

Above diagram shows the maximum single pulse current that can be driven for a given pulse time t_{pulse}. The maximum reachable current may be smaller depending on the current limitation level. Pulse time may be limited due to thermal protection of the device.

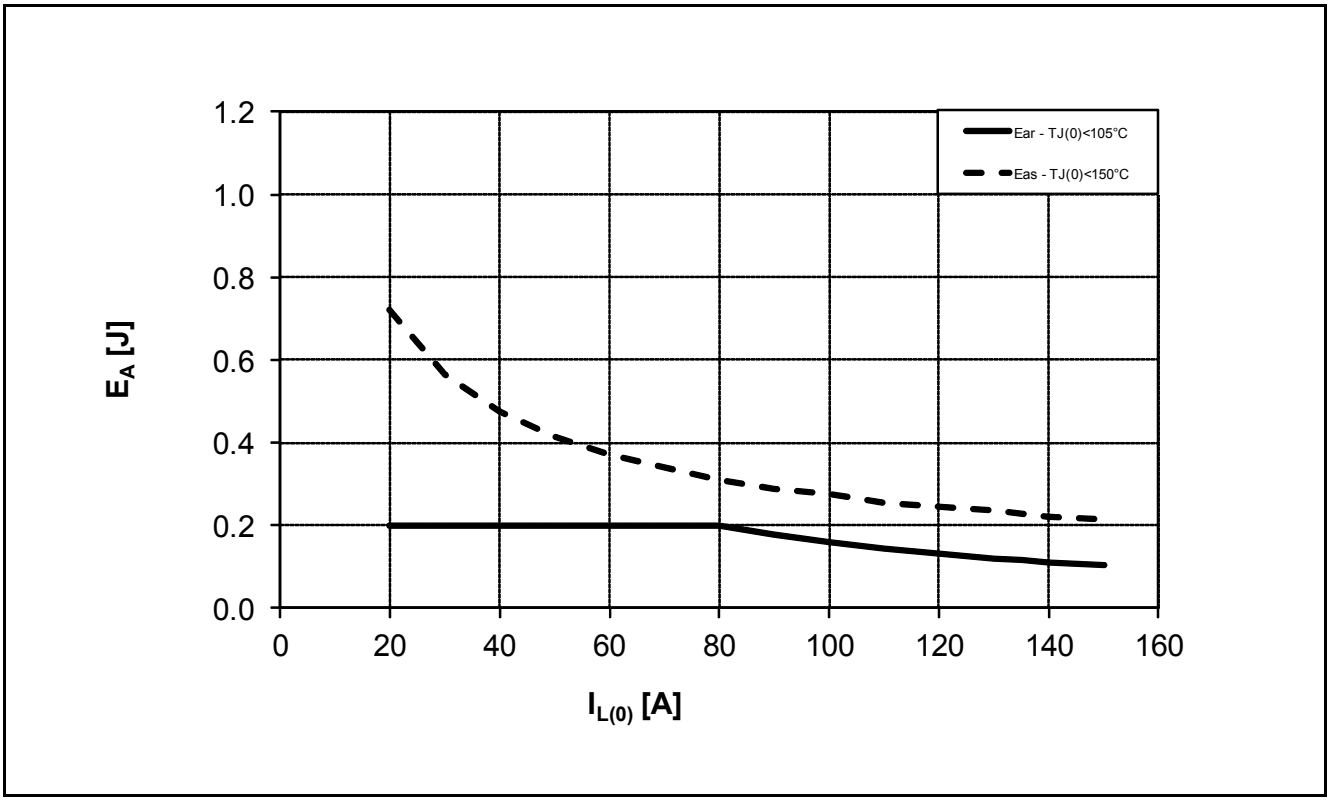


Figure 5 Maximum Energy Dissipation for Inductive Switch OFF, E_A vs Load Current

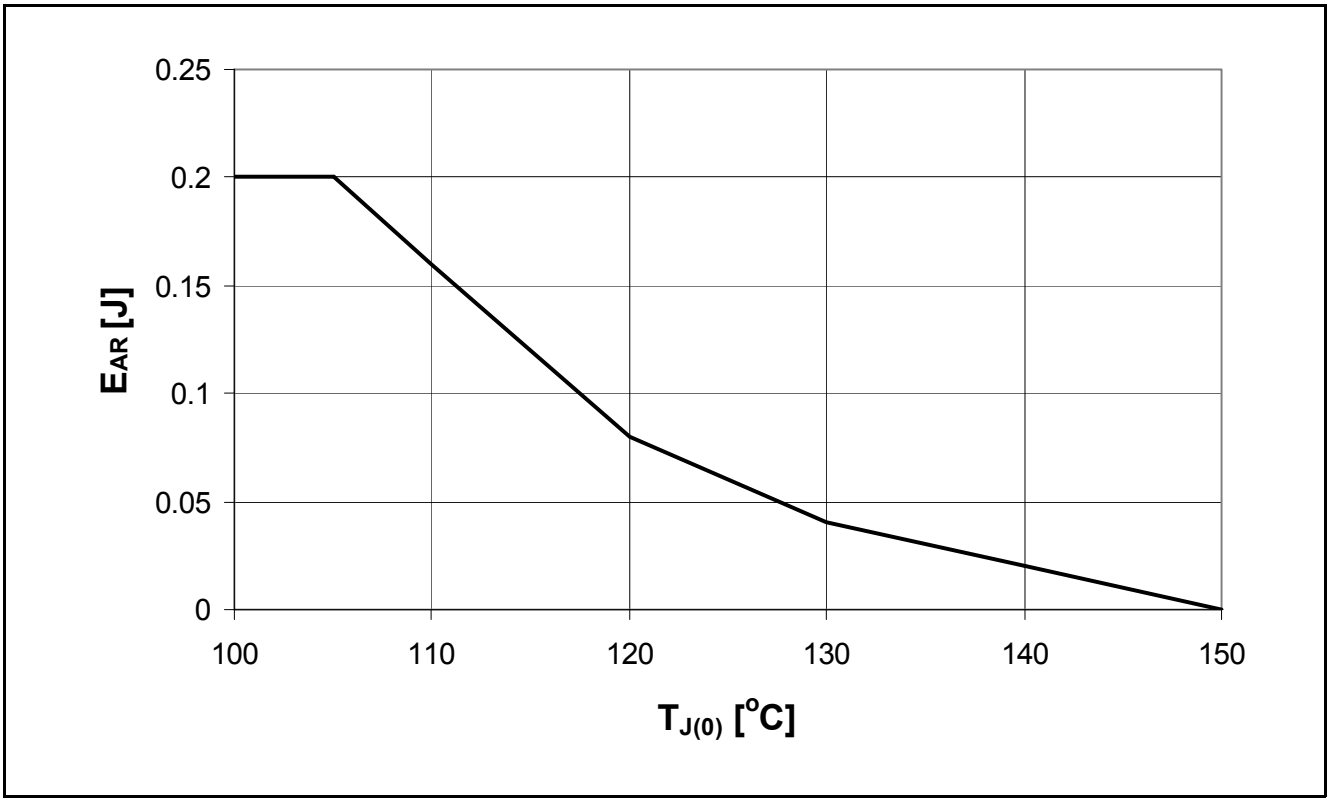


Figure 6 **Maximum Energy Dissipation Repetitive Pulse for Inductive Switch OFF vs Junction Temperature starting Point for Load Currents from 20A to 80A**

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	$V_{S(OP)}$	8	–	18	V	–	4.2.1
Extended operating voltage	$V_{S(OP\_EXT)}$	5.3	–	28	V	1) $V_{IN} \geq$ 2.2V $I_L \leq I_{L(NOM)}$ $T_J \leq$ 25°C Parameter deviations possible	4.2.2
		5.5	–	28	V	1) $V_{IN} \geq$ 2.2V $I_L \leq I_{L(NOM)}$ T_J = 150°C Parameter deviations possible	
Extended operating voltage contain short dynamic undervoltage capability	$V_{S(DYN)}$	3.2 2)	–	28	V	1) acc. to ISO7637	4.2.3
Undervoltage turn OFF voltage	$V_{S(UV\_OFF)}$	–	–	4.5	V	1) $V_{IN} \geq$ 2.2V R_L = 270Ω V_S decreasing See **Figure 19**	4.2.4
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	500 1)	–	mV	R_L = 270Ω See **Figure 19**	4.2.6
Slewrate at OUT	dV_{DS}/dt	–	–	10 1)	V/µs	$\|V_{DS}\|$ < 3V See **Chapter 5.1.4**	4.2.7

1) Not subject to production test. Specified by design

2) T_A = 25°C; R_L = 0.5Ω; pulse duration 6ms; cranking capability is depending on load and must be verified under application conditions

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	0.5	K/W	1)	4.3.1
Junction to Ambient	$R_{thJA(2s2p)}$	–	19	–	K/W	1)2)	4.3.2
Junction to Ambient	R_{thJA}	–	70	–	K/W	1)3)	4.3.3

1) Not subject to production test, specified by design.

2)Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 ×1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. T_A=25°C. Device is dissipating 2W power.

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 1 inner copper layers 1× 70µm Cu. T_A=25°C. Device is dissipating 2W power.

Figure 7 is showing the typical thermal impedance of BTS50010-1TAC mounted according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 1s0p and 2s2p boards.

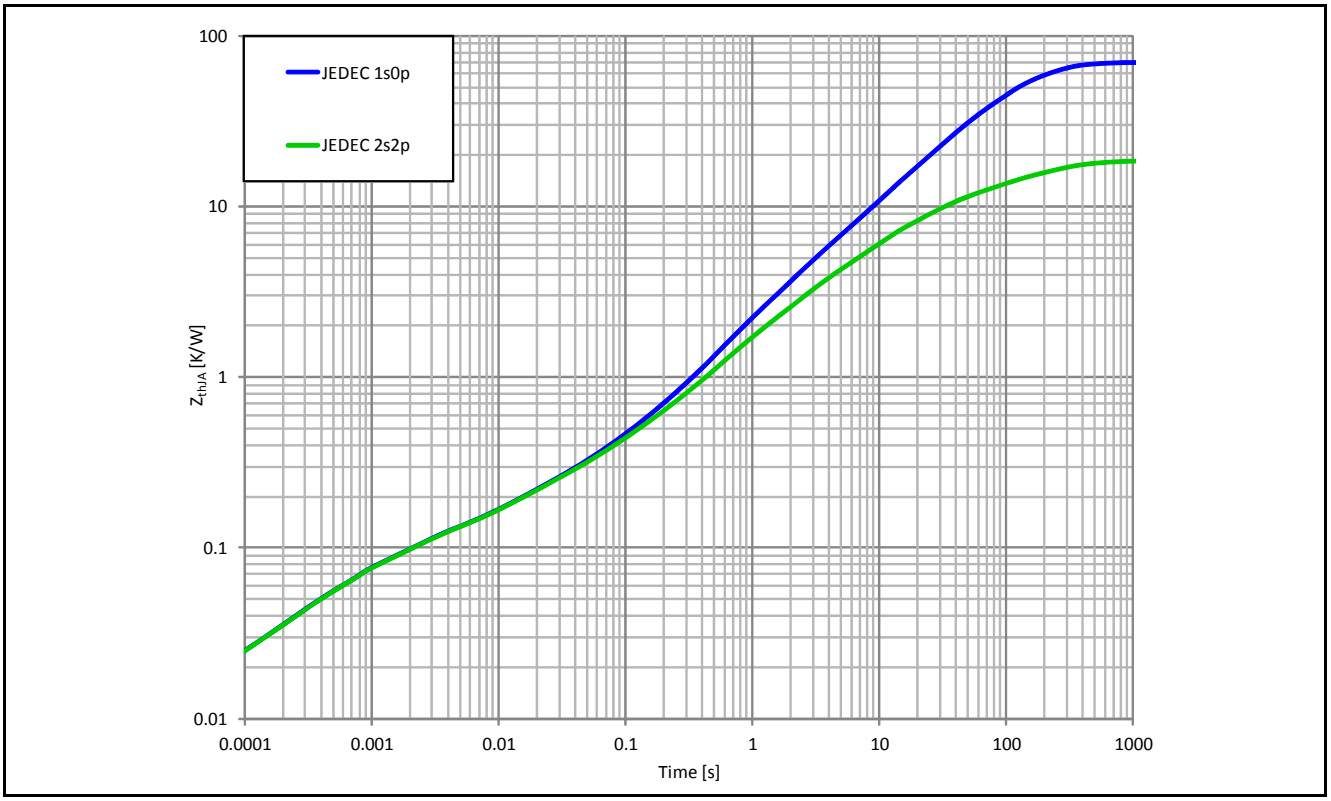


Figure 7 Typical Transient Thermal Impedance $Z_{th(JA)}$=f(time) for Different PCB Conditions

5 Functional Description

5.1 Power Stage

The power stage is built by a N-channel power MOSFET (DMOS) with charge pump.

5.1.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J. **Figure 31** shows the dependencies in terms of temperature and supply voltage, for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 5.3.5**.

A HIGH signal (see **Chapter 5.2**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.1.2 Switching a Resistive Load

Figure 8 shows the typical timing when switching a resistive load. The power stage has a defined switching behavior. Defined slew rates results in lowest EMC emission at minimum switching losses.

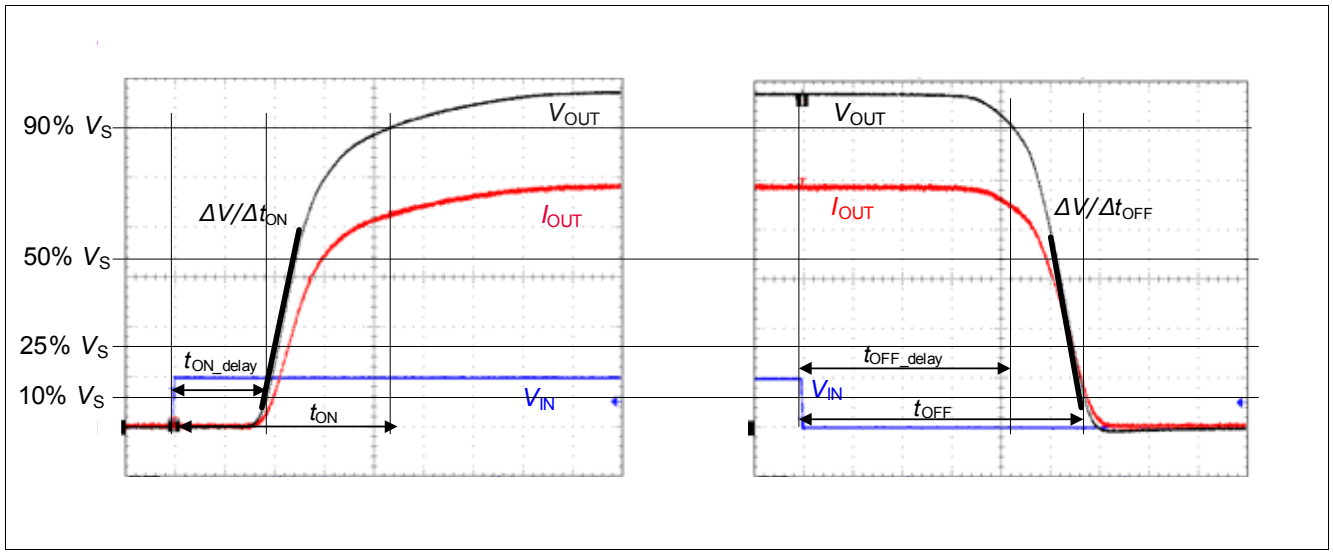


Figure 8 Switching a Resistive Load Timing

5.1.3 Switching an Inductive Load

5.1.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a Infineon® SMART CLAMPING mechanism implemented that keeps negative output voltage to a certain level (V_S - $V_{DS(CL)}$). Please refer to **Figure 9** and **Figure 10** for details. Nevertheless, the maximum allowed load inductance remains limited.

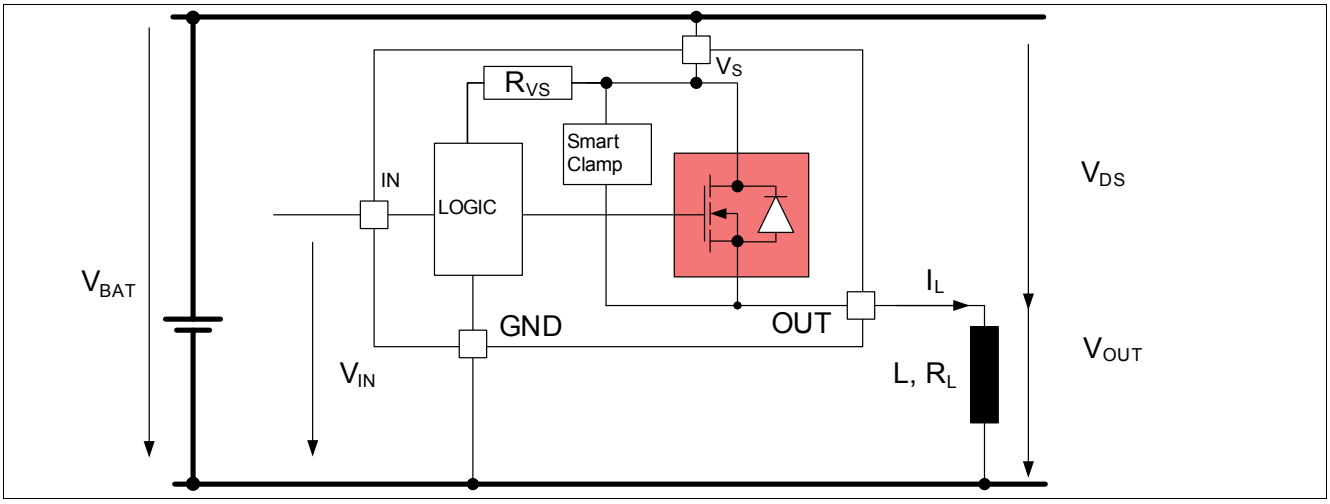


Figure 9 Output Clamp

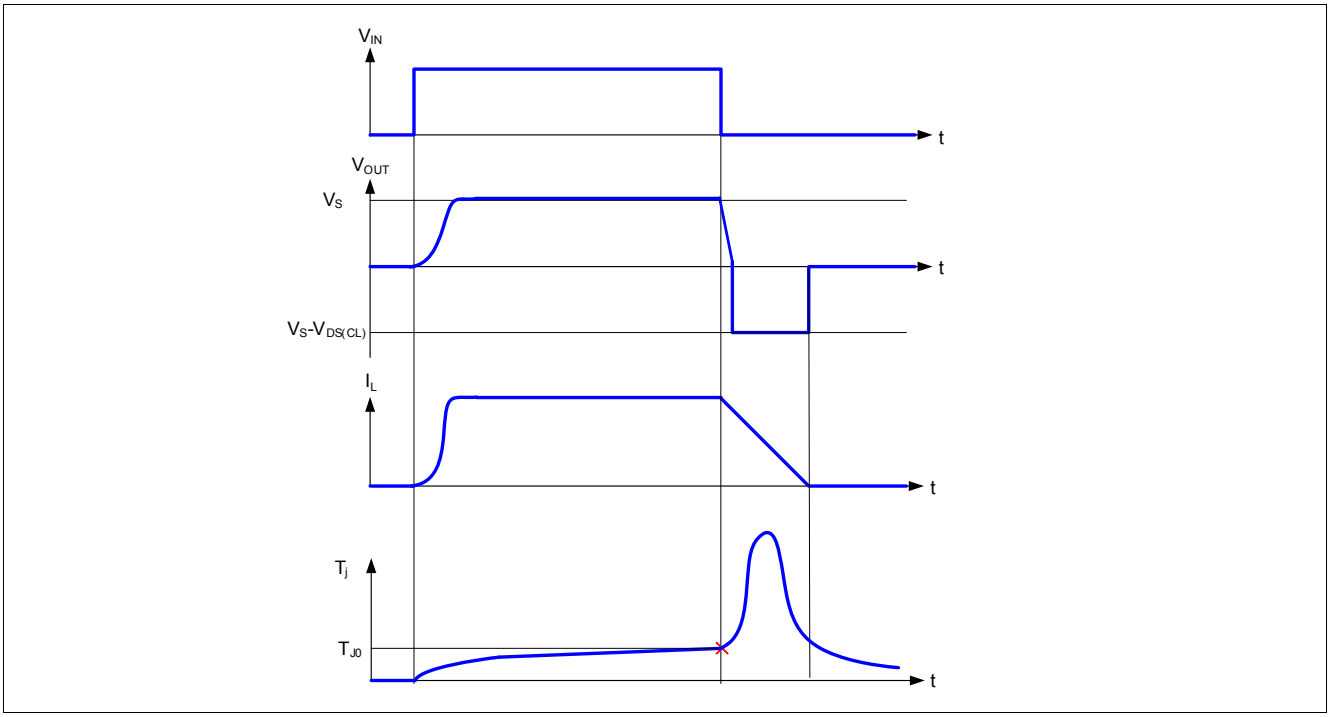


Figure 10 Switching an Inductance

The BTS50010-1TAC provides Infineon® SMART CLAMPING functionality. To increase the energy capability for single operation, the clamp voltage $V_{DS(CL)}$ increases over the junction temperature T_J and load current I_L. Refer to **Figure 39**.

5.1.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTS50010-1TAC. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(CL)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(CL)}}\right) + I_L \right] \quad (1)$$

Following equation simplifies under the assumption of R_L = 0Ω.

$$E = \frac{1}{2} \times L \times I_L^{\,2} \times \left(1 - \frac{V_S}{V_S - V_{DS(CL)}}\right) \quad (2)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 5** for the maximum allowed energy dissipation as function of the load current.

5.1.4 Inverse Current Capability

In case of inverse current, meaning a voltage $V_{OUT(INV)}$ at the output higher than the supply voltage V_S, a current $I_{L(INV)}$ will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 11**). In case the IN pin is HIGH, the power DMOS is already activated and keeps ON. In case, the input goes from “L” to “H”, the DMOS will be activated. Under inverse condition, the device is not overtemperature / overload protected. The IS pin is high impedance. Due to the limited speed of INV comparator, the output voltage slope needs to be limited.

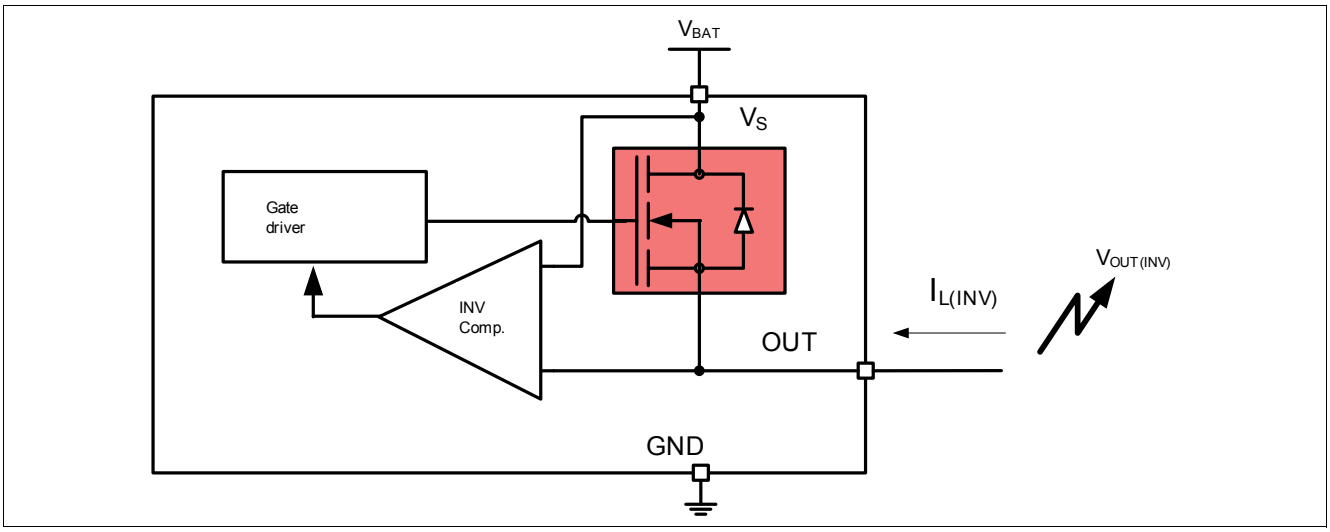


Figure 11 Inverse Current Circuitry

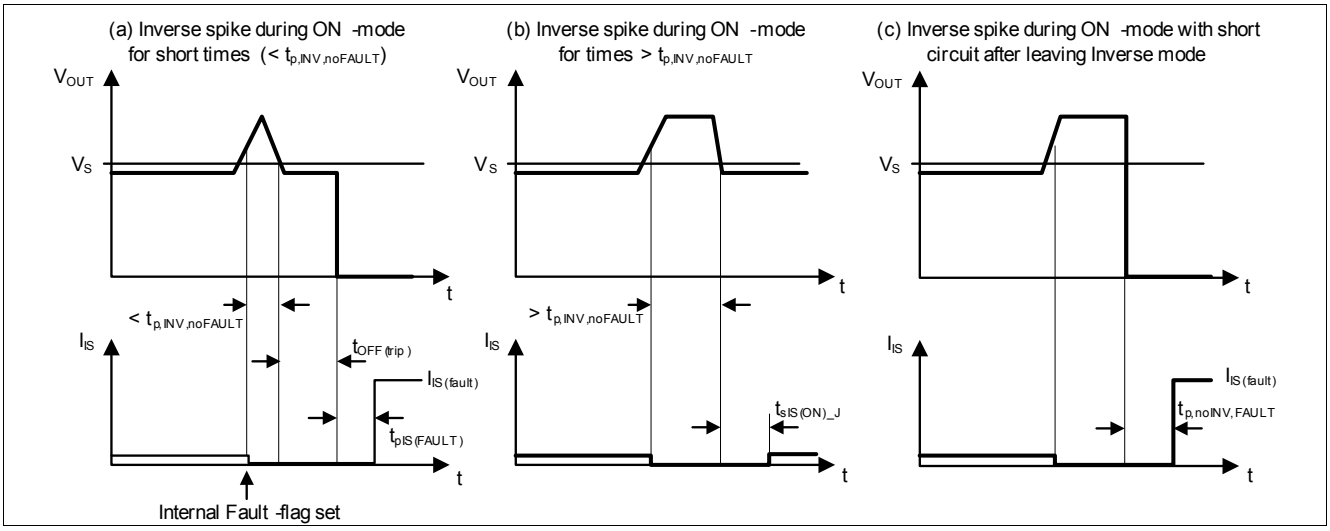


Figure 12 Inverse Behavior - Timing Diagram

5.1.5 PWM Switching

For PWM switching application, a $t_{IN(RESETDELAY)}$ parameter should be respected by defining the maximum PWM frequency (see **Figure 22**). The average power over time must be below the specified value (see paramater 4.1.15) and is defined as (see **Figure 13**):

P_{TOT} = (switching_ON_energy + switching_OFF_energy + $I_L^2 * R_{DS(ON)} * t_{DC}$) / period

For system with PWM switching, the maximum retry cycle (f_{fault}) under fault condition should not be exceeded.

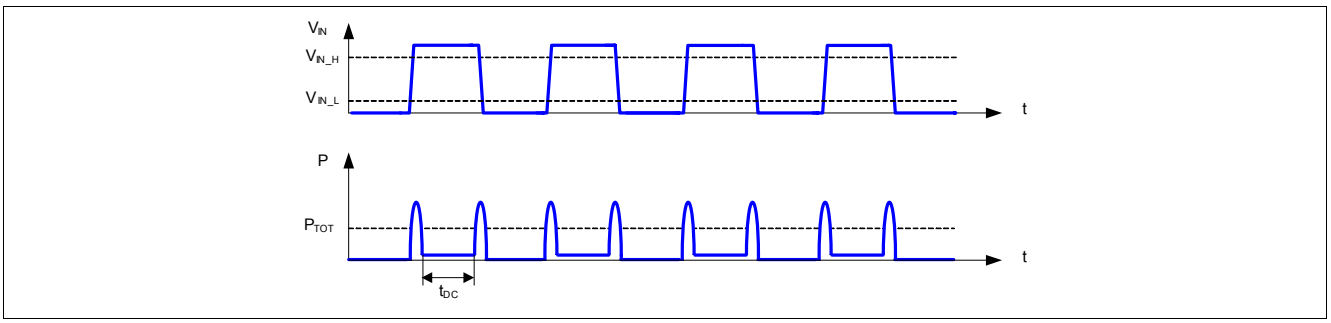


Figure 13 Switching in PWM

5.2 Input Pins

5.2.1 Input Circuitry

The input circuitry is compatible with 3.3V and 5V microcontrollers or can be directly driven by V_S. The concept of the input pin is to react to voltage threshold. With the Schmitt trigger, the output is either ON or OFF. **Figure 14** shows the electrical equivalent input circuitry.

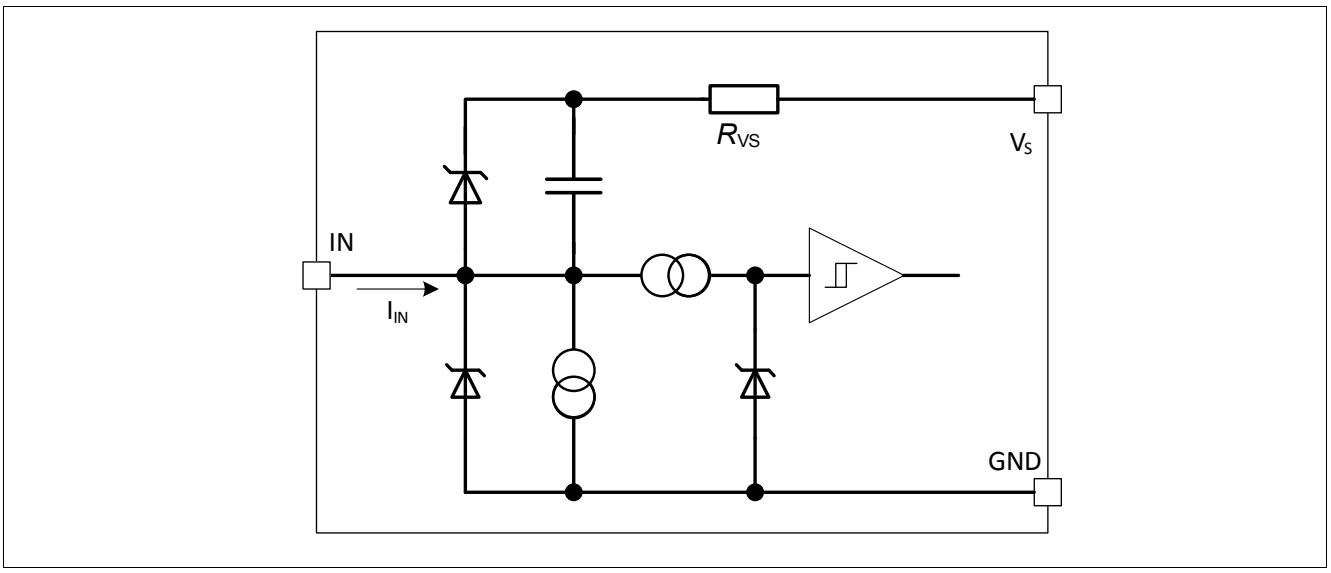


Figure 14 Input Pin Circuitry

5.2.2 Input Pin Voltage

The IN uses a comparator with hysteresis. The switching ON / OFF takes place in a defined region, set by the threshold $V_{IN(L)}$ Max and $V_{IN(H)}$ Min. The exact value where ON and OFF take place depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, an hysteresis is implemented. This ensures immunity to noise.

5.3 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed neither for continuous nor for repetitive operation.

Figure 15 describes the typical functionality of the diagnosis and protection block.

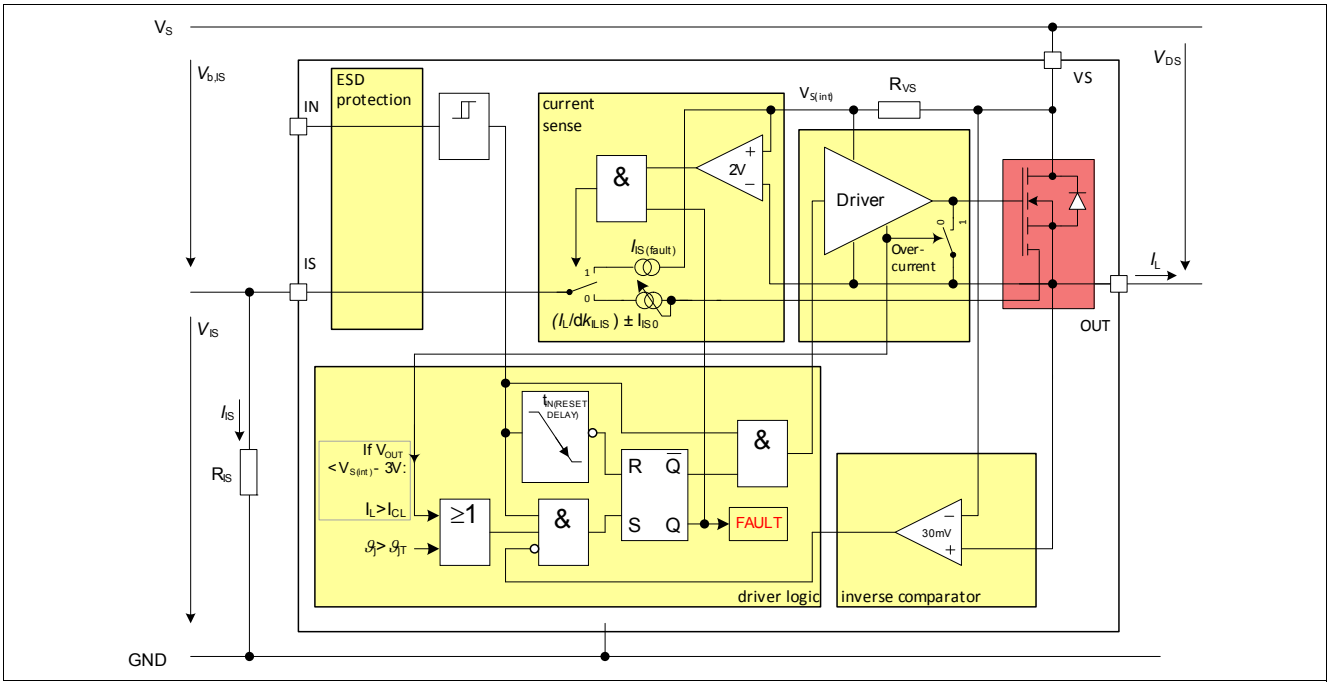


Figure 15 Diagram of Diagnosis & Protection Block

5.3.1 Loss of Ground Protection

In case of loss of module or device ground, where the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pin. It is recommended to use input resistors between the microcontroller and the BTS50010-1TAC to ensure switching OFF of channel. In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 16** sketches the situation.

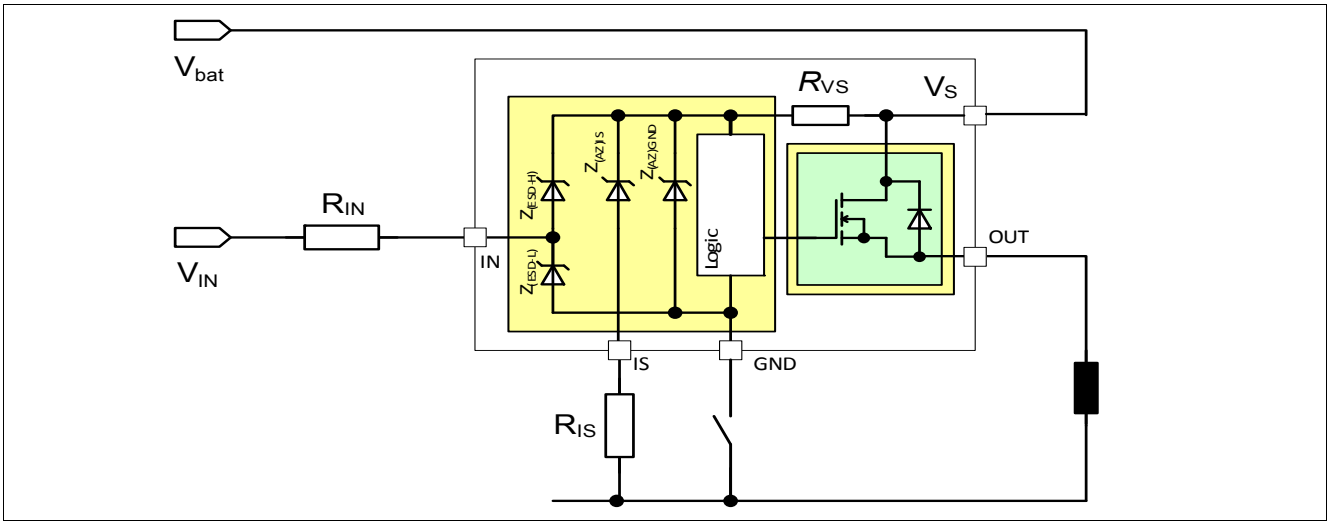


Figure 16 Loss of Ground Protection with External Components

5.3.2 Protection during Loss of Load or Loss of V_S Condition

In case of loss of load with charged primary inductances the maximum supply voltage has to be limited. It is recommended to use a Z-diode, a varistor or V_S clamping power switches with connected loads in parallel. The voltage must be limited according to the minimum value of the parameter 6.1.33 indicated in **Table 6**.

In case of loss of V_S connection with charged inductive loads, a current path with sufficient load current capability has to be provided, to demagnetize the charged inductances. It is recommended to protect the device using a zener diode together with a diode (V_{Z1} + V_{D1} < 16V), as shown in **Figure 17**.

For a proper restart of the device after loss of V_S, the input voltage must be applied delayed to the supply voltage. This can be realized by an capacitor between IN and GND (see **Figure 51**).

For higher clamp voltages, currents through all pins have to be limited according to the maximum ratings. Please see **Figure 17** and **Figure 18** for details.

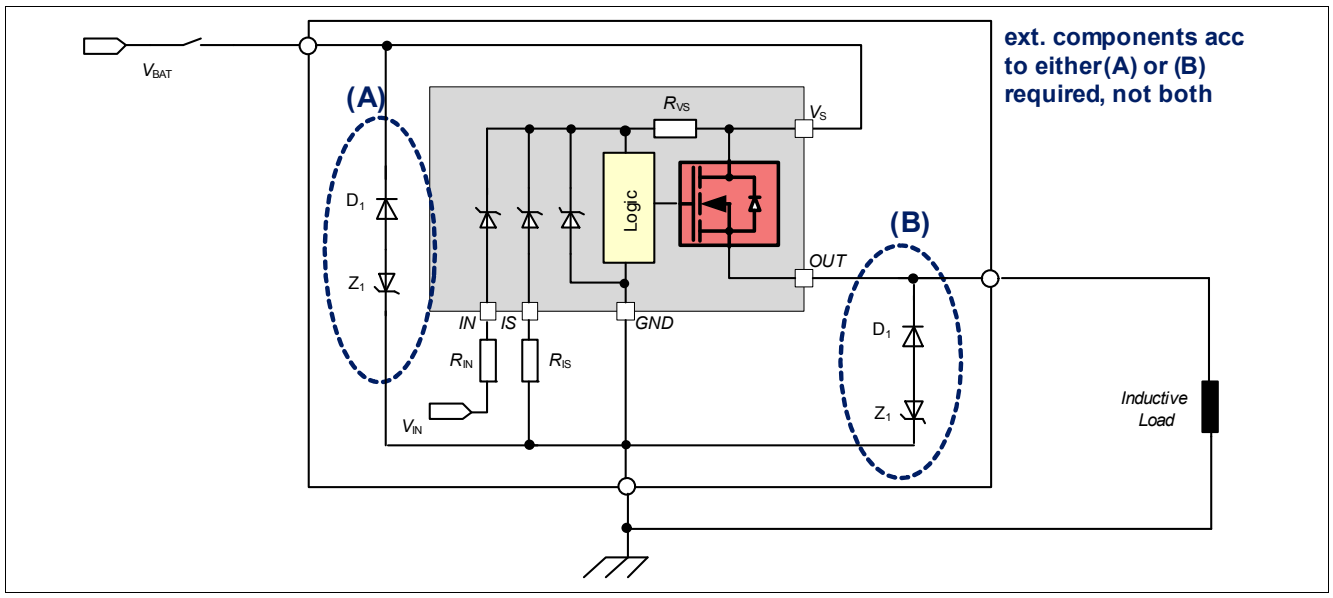


Figure 17 Loss of V_S

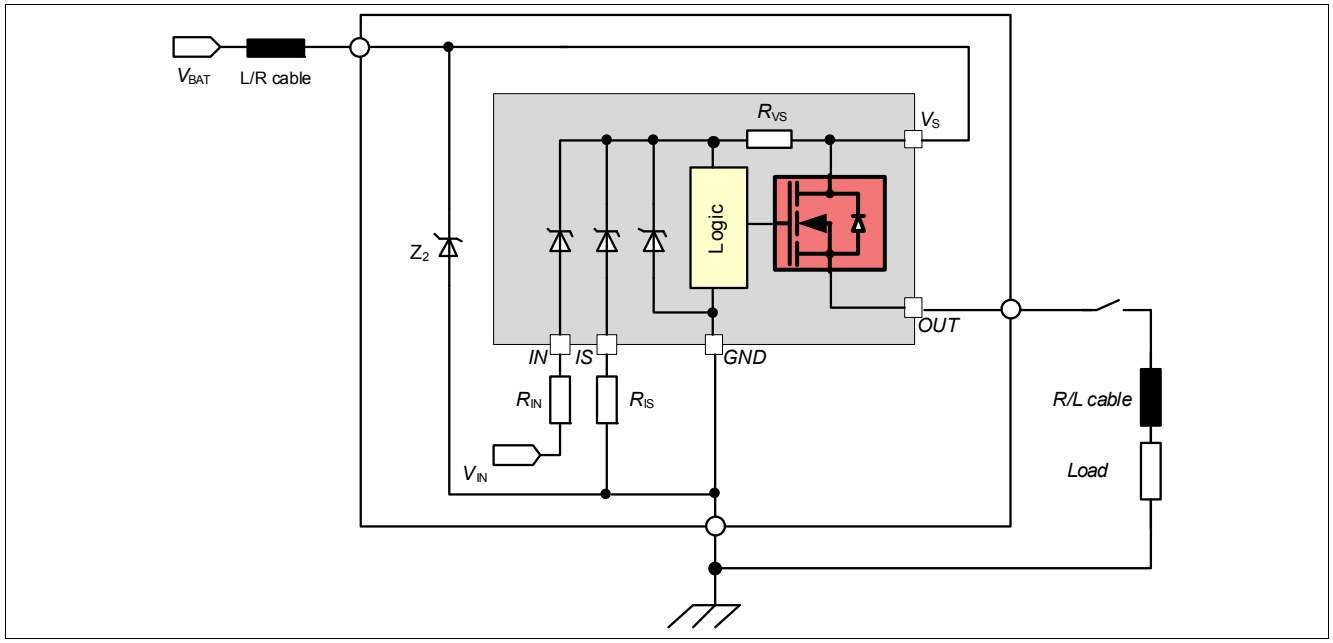


Figure 18 Loss of Load

5.3.3 Undervoltage Behavior

If the supply voltage is in the area below $V_{S(UV\_OFF)}$, the device is OFF (turns OFF). As soon as the supply voltage is above $V_{S(OP\_EXT)\_min}$, the device will switch ON again. **Figure 19** sketches the undervoltage behavior.

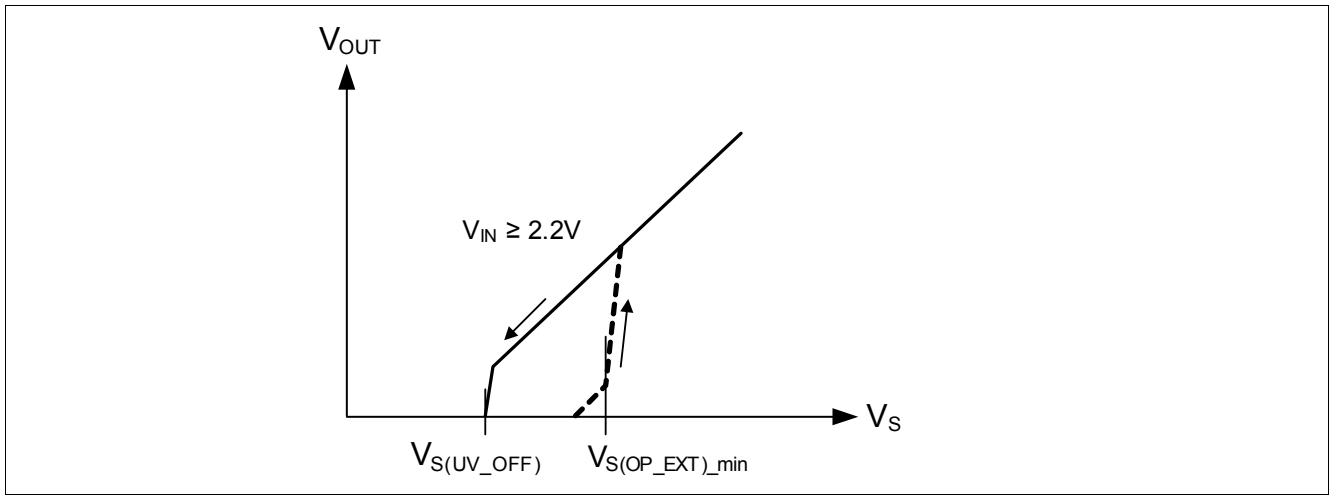


Figure 19 Undervoltage Behavior

5.3.4 Overvoltage Protection

In the case $V_{S(SC)\_max} < V_S < V_{DS(CL)}$, the ouput transistor is still operational and follows the input. Parameters are no longer warranted and lifetime is reduced compared to normal mode. This specially impacts the short circuit robustness, as well as the maximum energy E_{AS} & E_{AR} the device can handle.

The BTS50010-1TAC provides Infineon® SMART CLAMPING functionality, which suppresses non nominal over voltages by actively clamping the overvoltage across the power stage and the load. This is achieved by controlling the clamp voltage $V_{DS(CL)}$ depending on the junction temperature T_J and the load current I_L (see **Figure 20** for details).

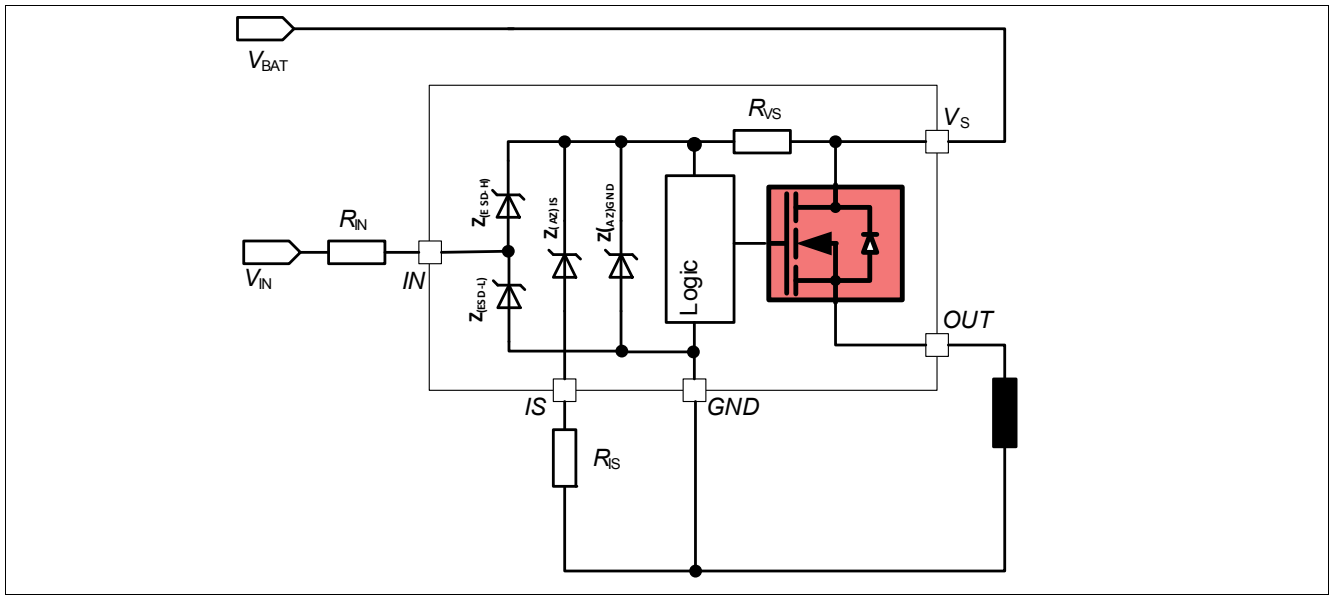


Figure 20 Overvoltage Protection with External Components

5.3.5 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power DMOS causes power dissipation. To limit the risk of overtemperature, the device provides Infineon® Reversave function. The power in this intrinsic body diode is limited by turning the DMOS ON. The DMOS resistance is then equal to $R_{DS(ON)\_REV}$.

Additonally, the current into the logic has to be limited. The device includes a R_{VS} resistor which limits the current in the diodes. To avoid overcurrent in the R_{VS} resistor, it is nevertheless recommended to use a R_{IN} resistor. Please refer to maximum current described in **Chapter 4.1**. **Figure 21** shows a typical application. R_{SENSE} is used to limit the current in the sense transistor which behaves as a diode.

The recommended typical values for R_{IN} is 4.7kΩ and for R_{SENSE} 1kΩ.

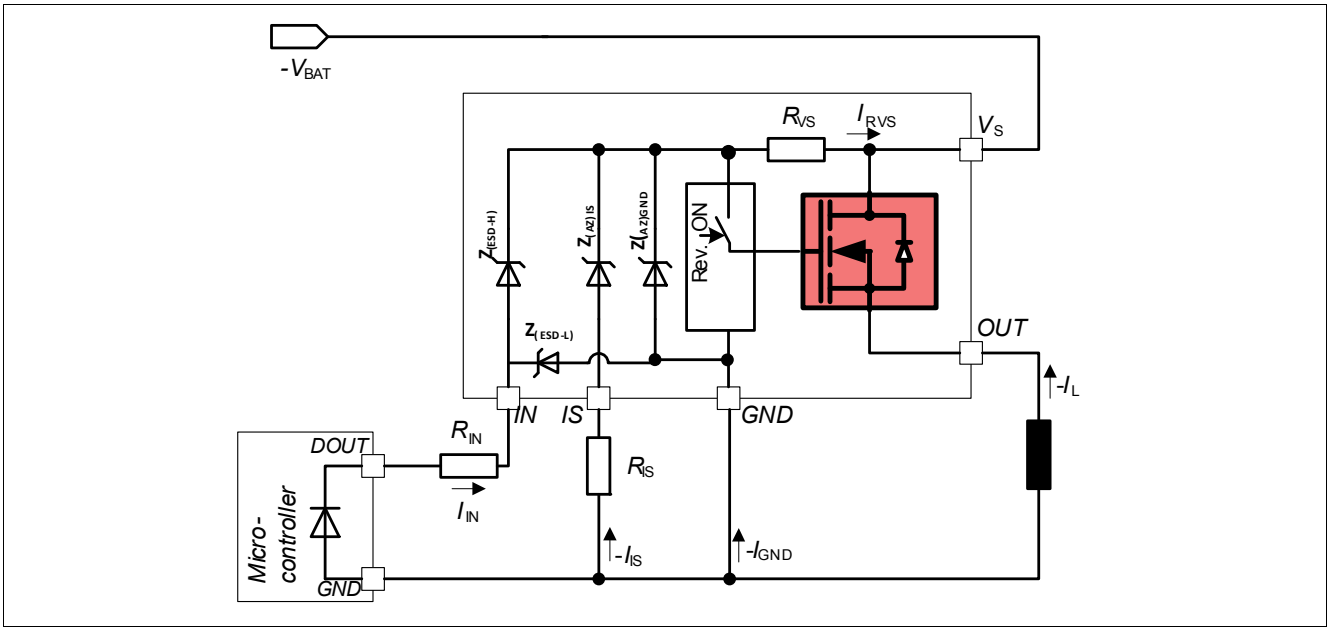


Figure 21 Reverse Polarity Protection with External Components

5.3.6 Overload Protection

In case of overload, high inrush current or short circuit to ground, the BTS50010-1TAC offers several protection mechanisms. Any protective switch OFF latches the output. To restart the device, it is necessary to set IN=LOW for $t > t_{IN(RESETDELAY)}$. This behavior is known as latch behavior. **Figure 22** gives a sketch of the situation.

5.3.6.1 Activation of the Switch into Short Circuit (Short circuit Type 1)

When the switch is activated into short circuit, the current will raise until reaching the $I_{L(TRIP)}$ value. After $t_{OFF(TRIP)}$, the device will turn OFF and latches until the IN pin is set to low for $t > t_{IN(RESETDELAY)}$. An undervoltage shutdown will not reset the latched fault overcurrent. For overload (short circuit or overtemperature), the maximum retry cycle (f_{fault}) under fault condition must be considered.

5.3.6.2 Short Circuit Appearance when the Device is already ON (Short circuit Type 2)

When the device is in ON state and a short circuit to ground appears at the output (SC2) with a overcurrent higher than $I_{L(TRIP)}$ for a time longer than $t_{OFF(TRIP)}$, the device automatically turns OFF and latches until the IN pin is set to low for $t > t_{IN(RESETDELAY)}$. An undervoltage shutdown will not reset the latched fault overcurrent.

5.3.7 Temperature Limitation in the Power DMOS

The BTS50010-1TAC incorporates an abolute ($T_{J(TRIP)}$) temperature sensor. Activation of the sensor will cause an overheated channel to switch OFF to prevent destruction. The device restarts when the IN pin is toggled and the temperature has decreased below $T_{J(TRIP)}$ - $\Delta T_{J(TRIP)}$. An undervoltage shutdown will not reset the fault over temperature.

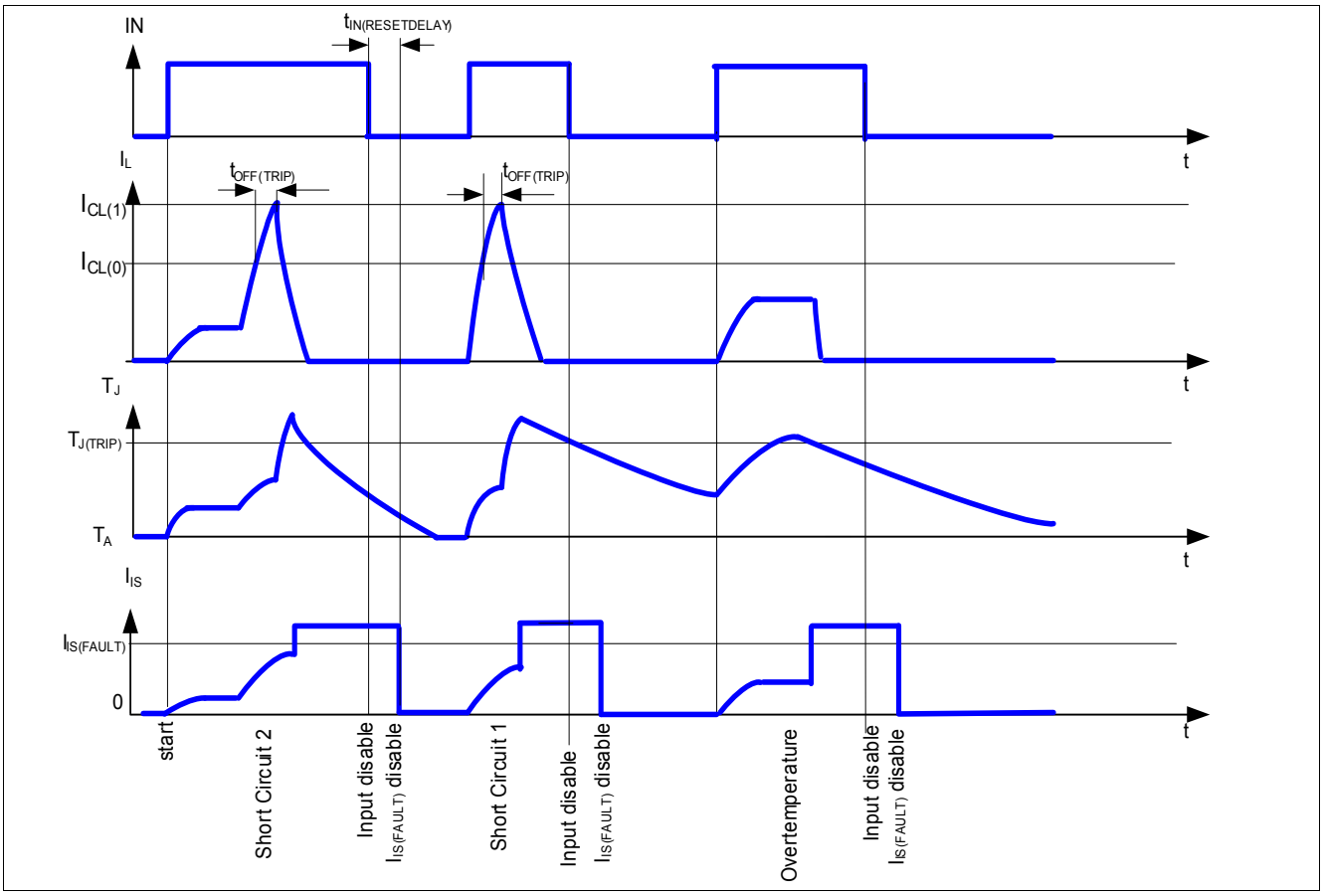


Figure 22 Overload Protection

The current sense exact signal timing can be found in the **Chapter 5.4**. It is represented here only for device's behavior understanding.

5.4 Diagnostic Functions

For diagnosis purposes, the BTS50010-1TAC provides a combination of digital and analog signal at pin IS.

5.4.1 IS Pin

The BTS50010-1TAC provides an enhanced current sense signal called I_{IS} at pin IS. As long as no “hard” failure mode occurs (short curcuit to GND / overcurrent / overtemperature) and the condition $V_{IS} \leq V_{OUT}$ - 5V is fulfilled, a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_S$) is provided. The complete IS pin and diagnostic mechanism is described in **Figure 23**. The accuracy of the sense current depends on temperature and load current. In case of failure, a fixed $I_{IS(FAULT)}$ is provided. In order to enable the fault current reporting, the condition V_S - V_{OUT} > 2V must be fulfilled. In order to get the fault current in the specified range, the condition V_S - $V_{IS} \geq$ 5V must be fulfilled.

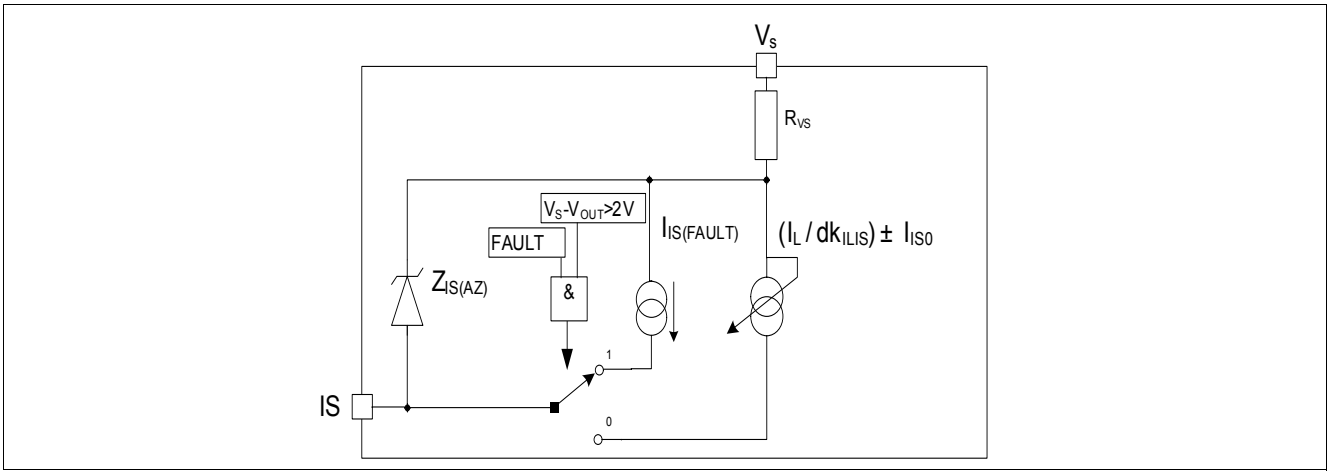


Figure 23 Diagnostic Block Diagram

5.4.2 SENSE Signal in Different Operation Mode

Table 5 Sense Signal, Function of Operation Mode[1)]

Operation mode	Input Level	Output Level V_{OUT}	Diagnostic Output (IS)[2)]
Normal operation	LOW (OFF)	~ GND	$I_{IS(OFF)}$
Short circuit to GND		GND	Z
Overtemperature		Z	Z
Short circuit to VS		V_S	Z
Open Load		Z	Z
Inverse current		> V_S	Z
Normal operation	HIGH (ON)	~ V_S	$I_{IS} = (I_L / dk_{ILIS}) \pm I_{IS0}$
Overcurrent condition		< V_S	$I_{IS} = (I_L / dk_{ILIS}) \pm I_{IS0}...I_{IS(FAULT)}$
Short circuit to GND		~ GND	$I_{IS(FAULT)}$
Overtemperature $T_{J(TRIP)}$ event		Z	$I_{IS(FAULT)}$
Short circuit to VS		V_S	$I_{IS} = 0 ... (I_L / dk_{ILIS}) \pm I_{IS0}$
Open Load		~ V_S	I_{IS0}
Inverse current		> V_S	Z

1) Z = High Impedance

2) See **Chapter 5.4.3** for Current Sense Range and Improved Current Sense Accuracy

5.4.3 SENSE Signal in the Nominal Current Range

Figure 24 and **Figure 25** show the current sense as function of the load current in the power DMOS. Usually, a pull-down resistor R_{IS} is connected to the current sense pin IS. A typical value is 1kΩ. The dotted curve represents the typical sense current, assuming a typical dk_{ILIS} factor value. The range between the two solid curves shows the sense accuracy the device is able to provide, at a defined current.

$$I_{IS} = \frac{I_L}{dk_{ILIS}} \pm I_{IS0} \qquad with(I_{IS} \geq 0) \tag{3}$$

Where the definition of dk_{ILIS} is:

$$dk_{ILIS} = \frac{I_{L4} - I_{L1}}{I_{IS4} - I_{IS1}} \tag{4}$$

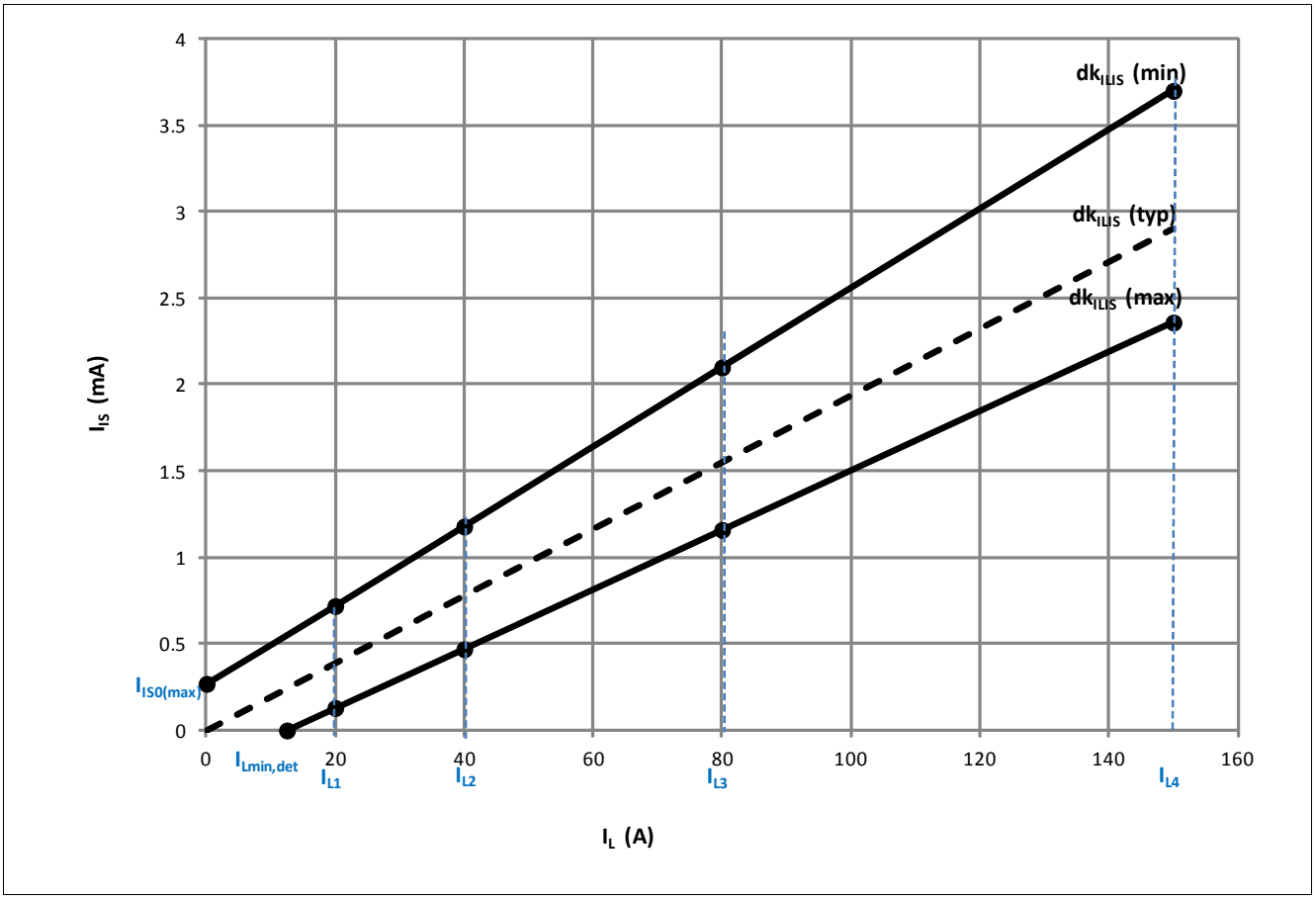


Figure 24 Current Sense for Nominal and Overload Condition

5.4.3.1 SENSE Signal Variation and Calibration

In some application, an enhanced accuracy is required around the device nominal current range $I_{L(NOM)}$. To achieve this accuracy requirement, a calibration on the application is possible. After two points calibration, the BTS50010-1TAC will have a limited I_{IS} value spread at different load currents and temperature conditions. The I_{IS}

variation can be described with the parameters $\Delta(dk_{ILIS(cal)})$ and the α_{IS0}. The blue solid line in **Figure 25** is the current sense ratio after the two point calibration. The slope of this line is defined as follow:

$$\frac{1}{dk_{KILIS(cal)}} = \frac{I_{S(cal)2} - I_{S(cal)1}}{I_{L(cal)2} - I_{L(cal)1}} \quad (5)$$

The bluish in area in **Figure 25** is the range where the current sense ratio can vary after performing the calibration. The accuracy of the load current sensing is improved and, given a sense current value I_{IS}(measured in the application), the load current can be calculated as follow:

$$I_L = dk_{ILIS(cal)} \cdot \left(1 + \frac{\Delta(dk_{ILIS(cal)})}{100}\right) \cdot \left(I_{IS} - \frac{I_{IS0(cal)}}{1 + \alpha_{IS0}(T_x - T_{cal})}\right) \quad (6)$$

where $dk_{ILIS(cal)}$ is the current sense ratio measured after two-points calibration (defined in **Equation (5)**), $I_{IS0(cal)}$ is the current sense offset (calculated after two points calibration, see **Equation (7)**), T_x is the operating temperature, and T_{cal} is temperature at which the calibration is performed (25°C). The **Equation (6)** actually provides two values for load current, considering that $\Delta(dk_{ILIS(cal)})$ can be both positive and negative (see parameter 6.1.47 in **Table 6**).

$$I_{IS0(cal)} = I_{S(cal)1} - \frac{I_{L(cal)1}}{dk_{ILIS(cal)}} = I_{S(cal)2} - \frac{I_{L(cal)2}}{dk_{ILIS(cal)}} \quad (7)$$

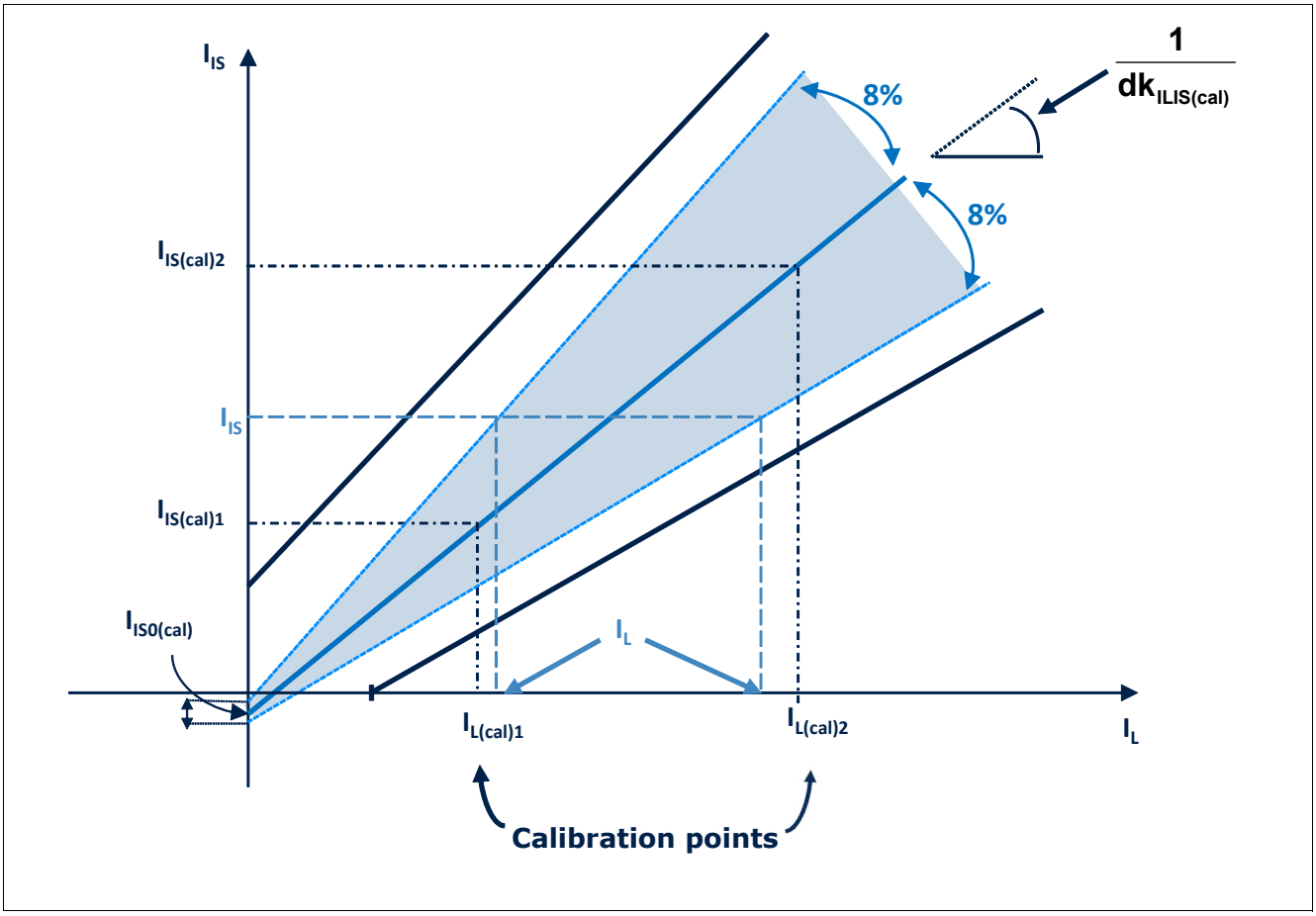


Figure 25 Improved Current Sense Accuracy after 2-Points Calibration

5.4.3.2 SENSE Signal Timing

Figure 26 shows the timing during settling and disabling of the sense.

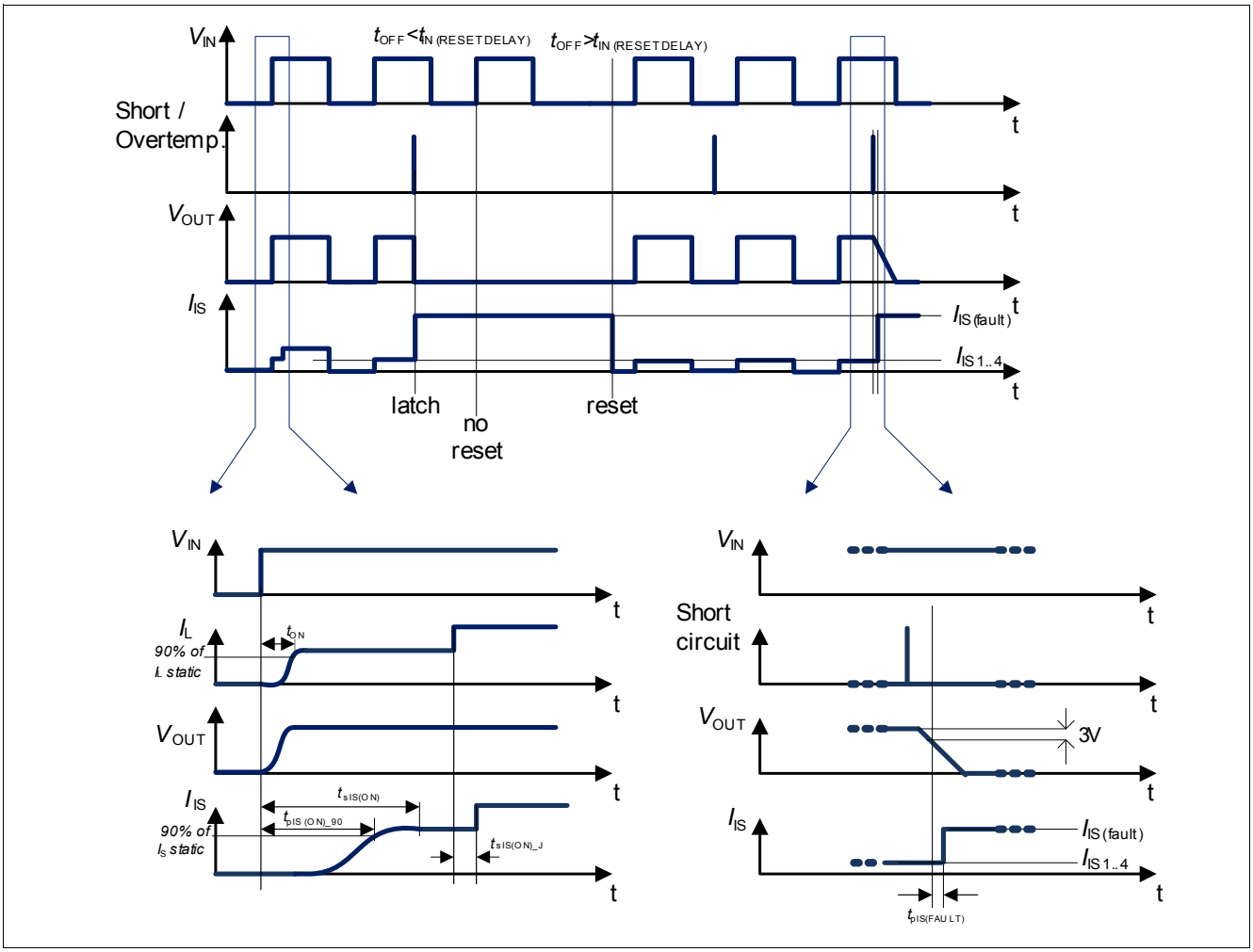


Figure 26 Fault Acknowledgement

5.4.3.3 SENSE Signal in Case of Short Circuit to V_S

In case of a short circuit between OUT and VS pin, a major part of the load current will flow through the short circuit. As a result, a lower current compared to the nominal operation will flow through the DMOS of the BTS50010-1TAC, which can be recognized at the current sense signal.

5.4.3.4 SENSE Signal in Case of Over Load

An over load condition is defined by a current flowing out of the DMOS reaching the current over load I_{CL} or the junction temperature reaches the thermal shutdown temperature $T_{J(TRIP)}$. Please refer to **Chapter 5.3.6** for details. In that case, the SENSE signal will be in the range of $I_{IS(FAULT)}$ when the IN pin stays HIGH.

This is a device with latch function. The state of the device will remain and the sense signal will remain on $I_{IS(FAULT)}$ until a reset signal comes from the IN pin. For example, when a thermal shutdown happened, even the over temperature condition was disappeared, the DMOS can only be reactivated when a reset signal is send to the IN pin.

6 Electrical characteristics BTS50010-1TAC

6.1 Electrical Characteristics Table

Table 6 Electrical Characteristics: BTS50010-1TAC

V_S = 8 V to 18 V, T_j = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Operating and Standby Currents							
Operating current (channel active)	I_{GND}	–	1.2	3	mA	$V_{IN} \geq$ 2.2V	6.1.1
Standby current for whole device with load at ambient	$I_{S(OFF)}$	–	7	18	µA	1) V_S = 18V V_{OUT} = 0V $V_{IN} \leq$ 0.8V $T_J \leq$ 85°C See **Figure 27** See **Figure 28**	6.1.2
Maximum standby current for whole device with load at max junction	$I_{S(OFF)}$	–	30	1000	µA	V_S = 18V V_{OUT} = 0V $V_{IN} \leq$ 0.8V $T_J \leq$ 150°C See **Figure 27** See **Figure 28**	6.1.3
Power Stage							
ON state resistance in forward condition	$R_{DS(ON)}$	–	1.4	2.0	mΩ	I_L = 150A $V_{IN} \geq$ 2.2V T_J = 150°C See **Figure 31**	6.1.4
ON state resistance in forward condition, Low battery voltage	$R_{DS(ON)}$	–	3.5	7.0	mΩ	I_L = 20A $V_{IN} \geq$ 2.2V V_S = 5.5V T_J = 150°C See **Figure 31**	6.1.5
ON state resistance in forward condition	$R_{DS(ON)}$	–	1.0	–	mΩ	1) I_L = 150A $V_{IN} \geq$ 2.2V T_J = 25°C See **Figure 31**	6.1.6
ON state resistance in inverse condition	$R_{DS(ON)\_INV}$	–	1.4	2.1	mΩ	I_L = -150A $V_{IN} \geq$ 2.2V T_J = 150°C See **Figure 11**	6.1.7
ON state resistance in inverse condition	$R_{DS(ON)\_INV}$	–	1.0	–	mΩ	1) I_L = -150A $V_{IN} \geq$ 2.2V T_J = 25°C See **Figure 11**	6.1.8

Table 6 Electrical Characteristics: BTS50010-1TAC (cont'd)

V_S = 8 V to 18 V, T_j = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal load current	$I_{L(NOM)}$	40	48	–	A	T_A = 85°C[2)] $T_J \leq$ 150°C	6.1.9
Drain to source smart clamp voltage $V_{DS(CL)} = V_S - V_{OUT}$	$V_{DS(CL)}$	28	–	56	V	I_{DS} = 50mA T_J = 25°C See **Figure 39**	6.1.11
Drain to source smart clamp voltage $V_{DS(CL)} = V_S - V_{OUT}$	$V_{DS(CL)}$	30	–	60	V	I_{DS} = 50mA T_J = 150°C See **Figure 39**	6.1.12
Output leakage current at ambient	$I_{L(OFF)}$	–	3	15	µA	[1)] $V_{IN} \leq$ 0.8V V_{OUT} = 0V $T_J \leq$ 85°C	6.1.13
Output leakage current at max junction temperature	$I_{L(OFF)}$	–	30	1000	µA	$V_{IN} \leq$ 0.8V V_{OUT} = 0V T_J = 150°C	6.1.14
Turn ON Slew rate V_{OUT} = 25% to 50% V_S	dV/dt_{ON}	0.05	0.23	0.5	V/µs	R_L = 0.5Ω V_S = 13.5V See **Figure 8** See **Figure 33** See **Figure 34** See **Figure 35** See **Figure 36**	6.1.15
Turn OFF Slew rate V_{OUT} = 50% to 25% V_S	$-dV/dt_{OFF}$	0.04	0.25	0.55	V/µs		6.1.16
Turn ON time to V_{OUT} = 90% V_S	t_{ON}	–	220	700	µs		6.1.17
Turn OFF time to V_{OUT} = 10% V_S	t_{OFF}	–	300	730	µs		6.1.18
Turn ON time to V_{OUT} = 10% V_S	t_{ON_delay}	–	80	150	µs		6.1.19
Turn OFF time to V_{OUT} = 90% V_S	t_{OFF_delay}	–	230	520	µs		6.1.20
Switch ON energy	E_{ON}	–	7	–	mJ	[1)] R_L = 0.5Ω V_S = 13.5V See **Figure 37**	6.1.21
Switch OFF energy	E_{OFF}	–	5	–	mJ	[1)] R_L = 0.5Ω V_S = 13.5V See **Figure 38**	6.1.22

Table 6 Electrical Characteristics: BTS50010-1TAC (cont'd)

V_S = 8 V to 18 V, T_j = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Pin							
LOW level input voltage	$V_{IN(L)}$	–	–	0.8	V	See **Figure 41**	6.1.23
HIGH level input voltage	$V_{IN(H)}$	2.2	–	–	V	See **Figure 42**	6.1.24
Input voltage hysteresis	$V_{IN(HYS)}$	–	200	–	mV	1)	6.1.25
LOW level input current	$I_{IN(L)}$	8	–	–	µA	V_{IN} = 0.8V	6.1.26
HIGH level input current	$I_{IN(H)}$	–	–	80	µA	$V_{IN} \geq$ 2.2V	6.1.27
Protection: Loss of ground							
Output leakage current while module GND disconnected	$I_{OUT(GND\_M)}$	0	30	1000	µA	1)3) V_S = 18V V_{OUT} = 0V IS & IN pins open GND pin open T_J = 150°C See **Figure 16**	6.1.28
Output leakage current while device GND disconnected	$I_{OUT(GND)}$	0	30	1000	µA	V_S = 18V GND pin open $V_{IN} \geq$ 2.2V 1kΩ pull down from IS to GND 4.7kΩ to IN pin T_J = 150°C See **Figure 16** See **Figure 43**	6.1.29
Protection: Reverse polarity							
ON state resistance in Infineon® Reversave	$R_{DS(ON)\_REV}$	–	–	2.2	mΩ	V_S = 0V V_{GND} = V_{IN} =16V I_L = -20A T_J = 150°C See **Figure 21**	6.1.30
ON state resistance in Infineon® Reversave	$R_{DS(ON)\_REV}$	–	1.0	–	mΩ	1) V_S = 0V V_{GND} = V_{IN} =16V I_L = -20A T_J = 25°C See **Figure 46**	6.1.31
Integrated resistor	R_{VS}	–	60	90	Ω	T_J = 25°C	6.1.32

Table 6 Electrical Characteristics: BTS50010-1TAC (cont'd)

V_S = 8 V to 18 V, T_j = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Protection: Overvoltage							
Overvoltage protection GND pin to V_S	$V_{S(AZ)\_GND}$	64	70	80	V	See **Figure 20** See **Figure 40**	6.1.33
Overvoltage protection IS pin to V_S	$V_{S(AZ)\_IS}$	64	70	80	V	GND and IN pin open See **Figure 20** See **Figure 40**	6.1.34
Protection: Overload							
Current trip detection level	$I_{CL(0)}$	150	190	–	A	V_S = 13.5V, static T_J = 150°C See **Figure 22**	6.1.35
	$I_{CL(0)}$	160	200	–	A	V_S = 13.5V, static T_J = -40...25°C See **Figure 22**	
Current trip maximum level	$I_{CL(1)}$	–	220	270	A	[1] V_S = 13.5V dI_L/dt = 1A/µs See **Figure 44**	
Overload shutdown delay time	$t_{OFF(TRIP)}$	–	12	–	µs	[1]	6.1.36
Thermal shutdown temperature	$T_{J(TRIP)}$	150	170[1]	200[1]	°C	See **Figure 22**	6.1.37
Thermal shutdown hysteresis	$\Delta T_{J(TRIP)}$	–	10	–	K	[1]	6.1.38
Diagnostic Function: Sense pin							
Sense signal current in fault condition	$I_{IS(FAULT)}$	4	6	8	mA	V_{IN} = 4.5V V_S - $V_{IS} \geq$ 5V	6.1.40
Diagnostic Function: Current sense ratio signal in the nominal area, stable current load condition							
Current sense differential ratio	dk_{ILIS}	43700	51500	58200	–	I_L = 150A I_{L1} = 20A See **Equation (4)**	6.1.41
Current sense $I_L = I_{L0}$ = 50mA	I_{IS0}	–	1	270	µA	$V_{IN} \geq$ 2.2V V_S - $V_{IS} \geq$ 5V T_J = -40°C See **Figure 24**	6.1.42
		–	1	205	µA	$V_{IN} \geq$ 2.2V V_S - $V_{IS} \geq$ 5V $T_J \geq$ 25°C See **Figure 24**	
Current sense $I_L = I_{L1}$ = 20A	I_{IS1}	130	390	720	µA	$V_{IN} \geq$ 2.2V V_S - $V_{IS} \geq$ 5V See **Figure 24**	6.1.43
Current sense $I_L = I_{L2}$ = 40A	I_{IS2}	470	780	1180	µA		6.1.44

Table 6 Electrical Characteristics: BTS50010-1TAC (cont'd)

V_S = 8 V to 18 V, T_j = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at V_S = 13.5V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current sense $I_L = I_{L3}$ = 80A	I_{IS3}	1.16	1.55	2.10	mA		6.1.45
Current sense $I_L = I_{L4}$ = 150A	I_{IS4}	2.36	2.90	3.70	mA		6.1.46
Current sense ratio spread over temperature and repetitive pulse operation after 2-points calibration	$\Delta(dk_{ILIS(cal)})$	–	±8	–	%	1)See **Figure 25**	6.1.47
Temperature coefficient for $I_{IS0(cal)}$	α_{IS0}	–	3.8	–	‰/K	1)see **Equation (6)** and **Equation (7)**	6.1.54
Diagnostic Function: Diagnostic timing in normal condition							
Current sense propagation time until 90% of I_{IS} stable after positive input slope on IN pin	$t_{pIS(ON)\_90}$	0	–	750	µs	$V_{IN} \geq$ 2.2V V_S = 13.5V R_L = 0.5Ω See **Figure 26**	6.1.48
Current sense settling time to I_{IS} stable after positive input slope on IN pin	$t_{sIS(ON)}$	–	–	3000	µs	$V_{IN} \geq$ 2.2V V_S = 13.5V R_L = 0.5Ω See **Figure 26**	6.1.49
I_{IS} leakage current when IN disabled	$I_{IS(OFF)}$	0	0.05	1	µA	$V_{IN} \leq$ 0.8V R_{IS} =1kΩ	6.1.50
Current sense propagation time after load jump during ON condition	$t_{sIS(ON)\_J}$	–	350	–	µs	1)$V_{IN} \geq$ 2.2V dI_L/dt = 0.4A/µs	6.1.51
Diagnostic Function: Diagnostic timing in overload condition							
Current sense propagation time for short circuit detection	$t_{pIS(FAULT)}$	0	–	100	µs	1)$V_{IN} \geq$ 2.2V from V_{OUT}= V_S-3V to $I_{IS(FAULT)\_min}$ See **Figure 26**	6.1.52
Delay time to reset fault signal at IS pin after turning OFF V_{IN}	$t_{IN(RESETDELAY)}$	250	1000	1500	µs	1)	6.1.53
Timing: Inverse Behavior							
Propagation time from $V_{OUT} > V_S$ to fault disable	$t_{p,INV,noFAULT}$	–	4	–	µs	1)See **Figure 12**	6.1.55
Propagation time from $V_{OUT} < V_S$ to fault enable	$t_{p,noINV,FAULT}$	–	10	–	µs	1)See **Figure 12**	6.1.56

1) Not subject to production test, specified by design
2) Value is calculated from the parameters typ. $R_{thJA(2s2p)}$, with 65K temperature increase, typ. and max. $R_{DS(ON)}$
3) All pins are disconnected except V_S and OUT

6.2 General Product Characteristics

Typical Performance Characteristics

Figure 27 Standby Current for Whole Device with Load, $I_{S(OFF)}$ = f(V_S, T_J)

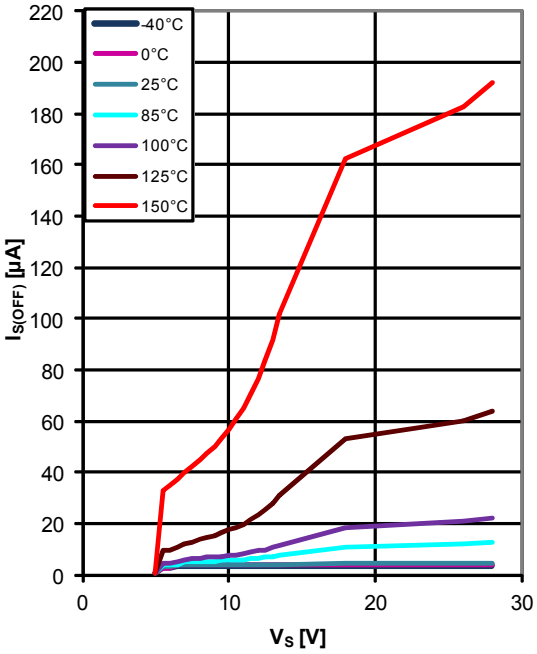


Figure 28 Standby Current for Whole Device with Load, $I_{S(OFF)}$ = f(T_J) at V_S = 13.5V

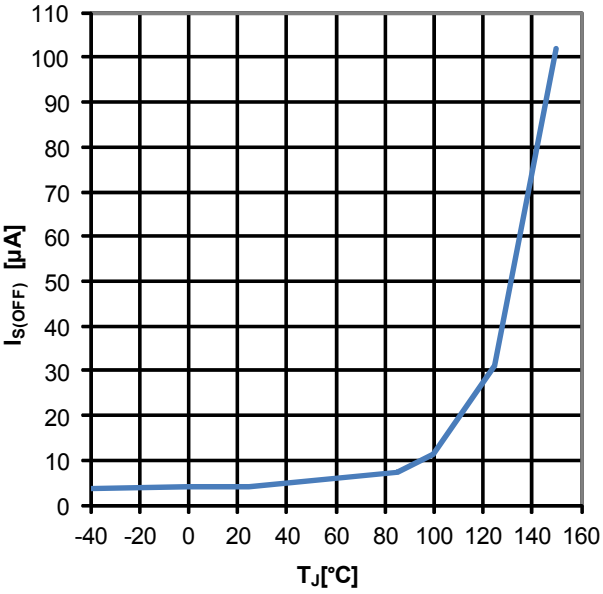


Figure 29 GND Leakage Current $I_{GND(OFF)}$ = f(V_S, T_J)

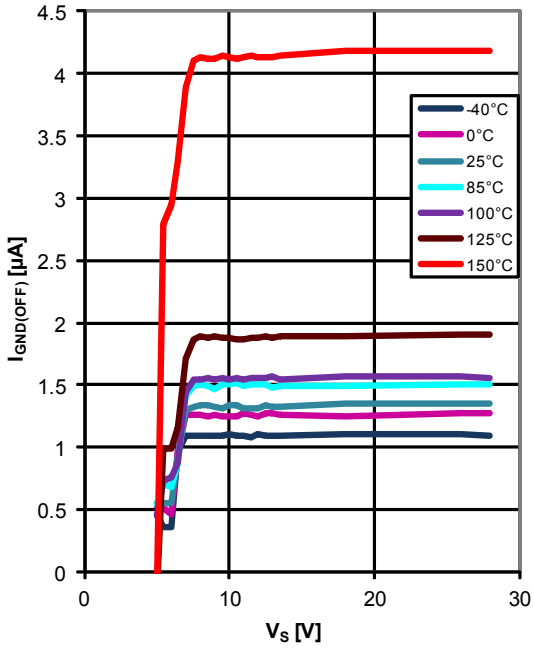


Figure 30 GND Leakage Current $I_{GND(OFF)}$ = f(T_J) at V_S = 13.5V

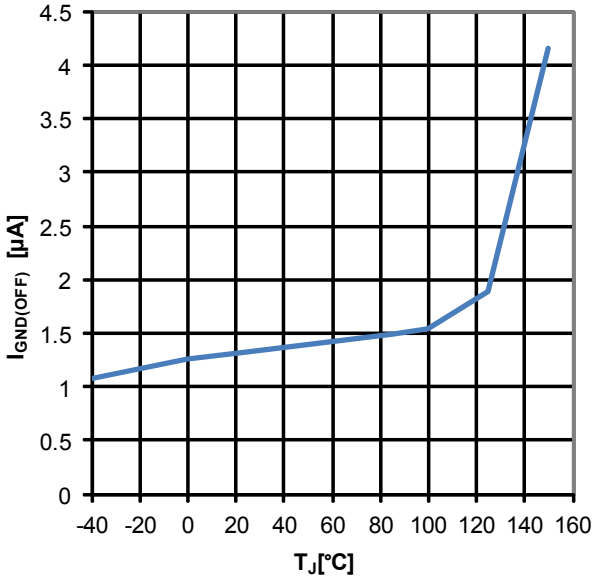


Figure 31 ON State Resistance
$R_{DS(ON)} = f(V_S, T_J), I_L = 20A \ldots 150A$

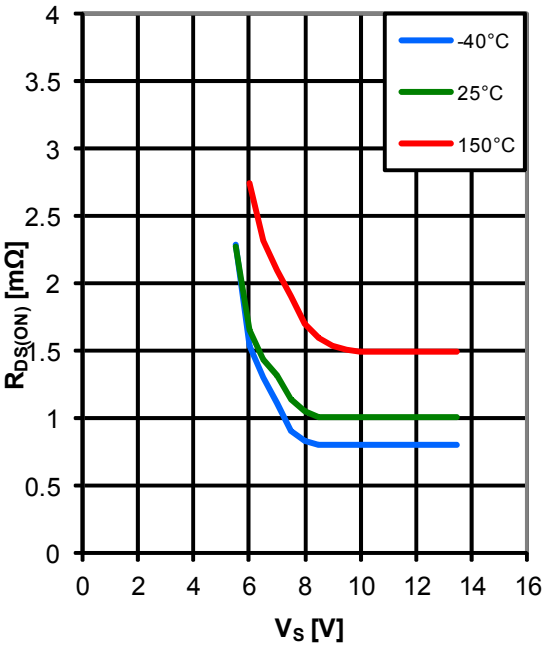


Figure 32 ON State Resistance
$R_{DS(ON)} = f(T_J), V_S = 13.5V, I_L = 20A...150A$

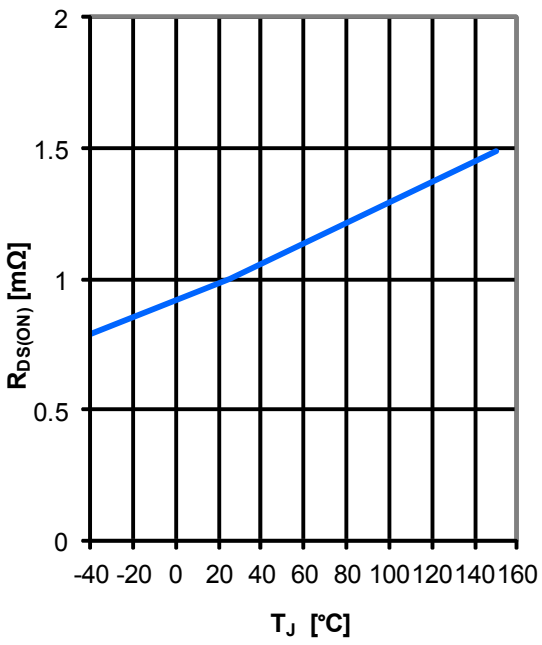


Figure 33 Turn ON Time
$t_{ON} = f(V_S, T_J), R_L = 0.5\Omega$

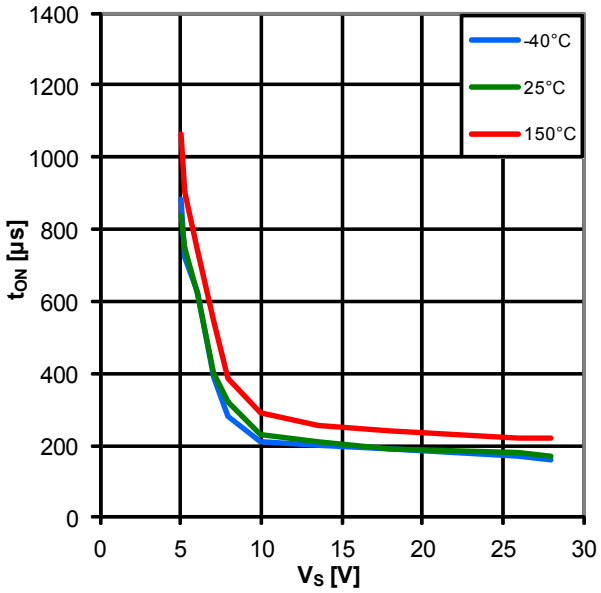


Figure 34 Turn OFF Time
$t_{OFF} = f(V_S, T_J), R_L = 0.5\Omega$

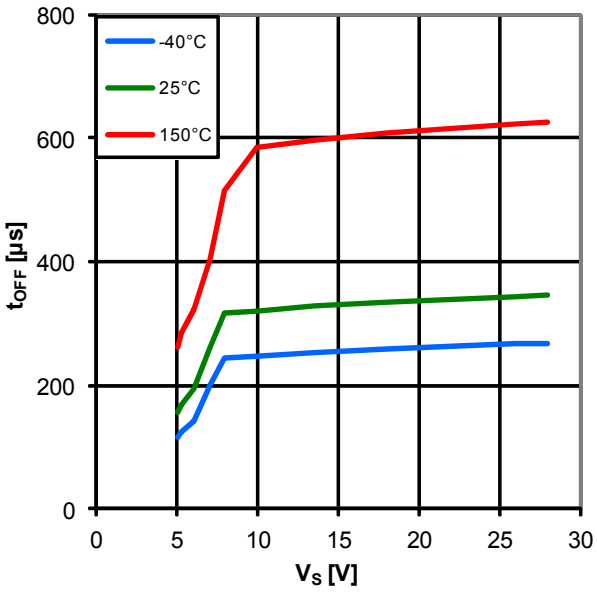


Figure 35 Slew Rate at Turn ON
dV / t_{ON} = f(V_S, T_J), R_L = 0.5Ω

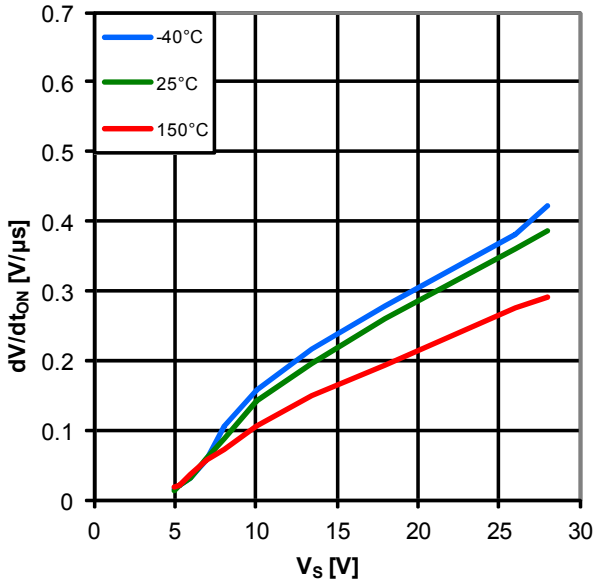


Figure 36 Slew Rate at Turn OFF
dV / t_{OFF} = f(V_S, T_J), R_L = 0.5Ω

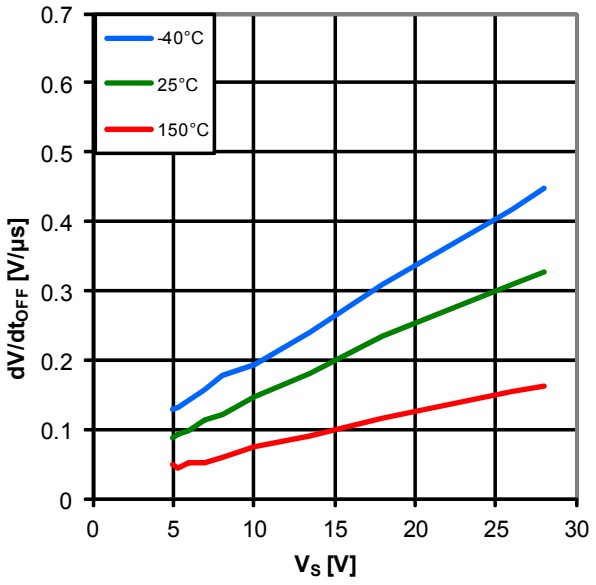


Figure 37 Switch ON Energy
E_{ON} = f(V_S, T_J), R_L = 0.5Ω

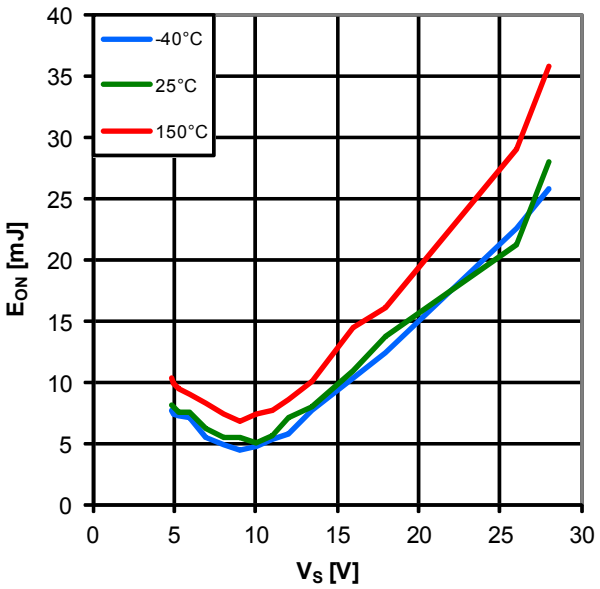


Figure 38 Switch OFF Energy
E_{OFF} = f(V_S, T_J), R_L = 0.5Ω

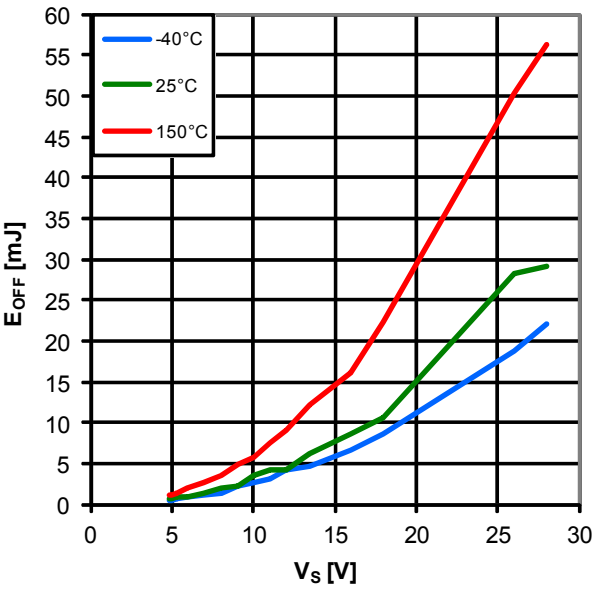


Figure 39 Drain to Source Clamp Voltage
$V_{DS(CL)}$ = f(T_J), I_L = 50mA

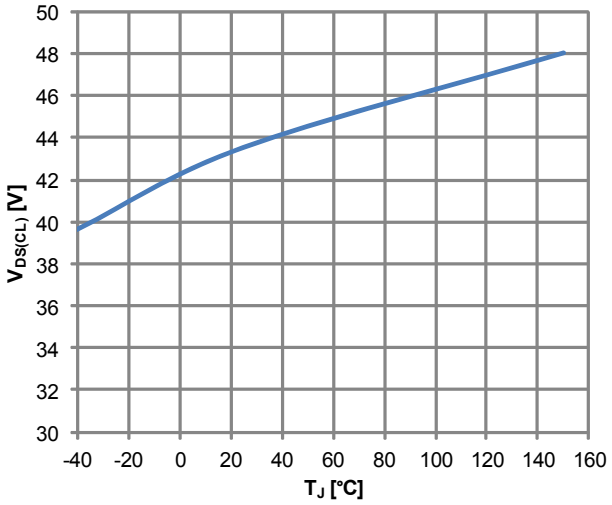


Figure 40 Overvoltage Protection
$V_{S(AZ)\_GND}$ = f(T_J), $V_{S(AZ)\_IS}$ = f(T_J)

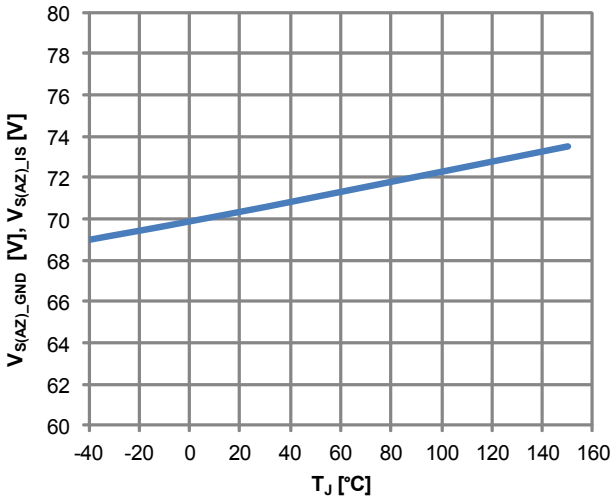


Figure 41 LOW Level Input Voltage
$V_{IN(L)}$ = f(V_S, T_J)

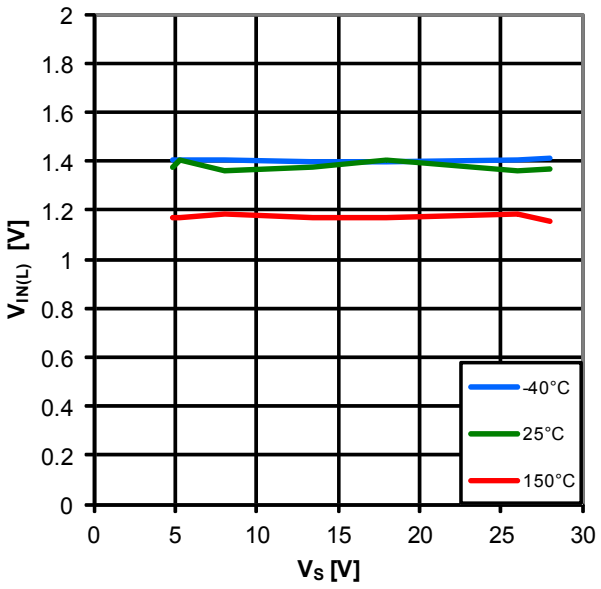


Figure 42 HIGH Level Input Voltage
$V_{IN(H)}$ = f(V_S, T_J)

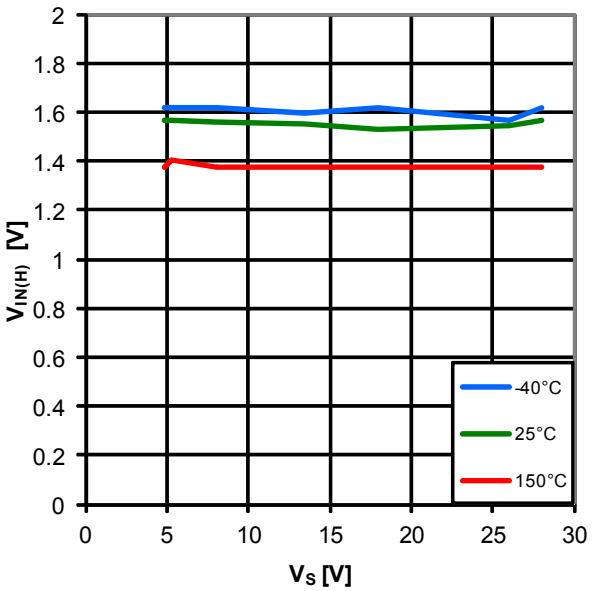


Figure 43 Output Leakage Current while Device GND Disconnected, $I_{OUT(GND)}$ = f(V_S, T_J)

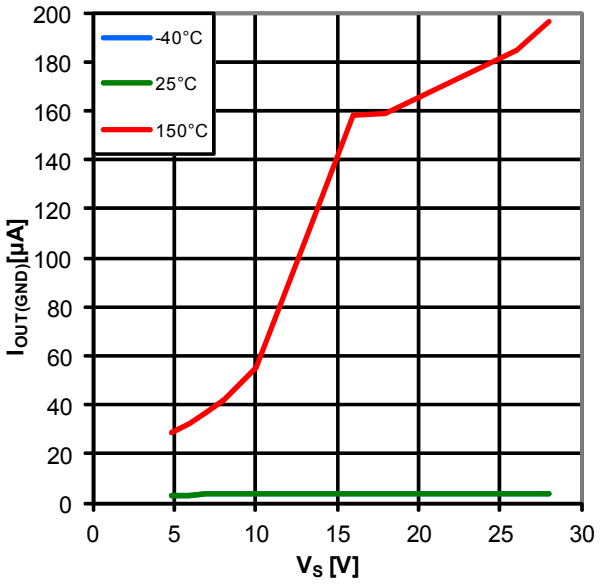


Figure 44 Overload Detection Current $I_{CL(1)}$ = f(dI_L/dt, T_J), V_S = 13.5V

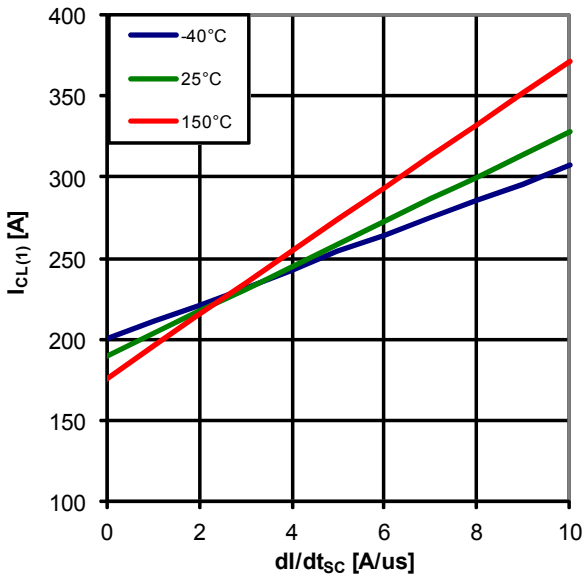


Figure 45 Resistance in Reversave $R_{DS(ON)\_REV}$ = f(V_S, T_J), I_L = -150A

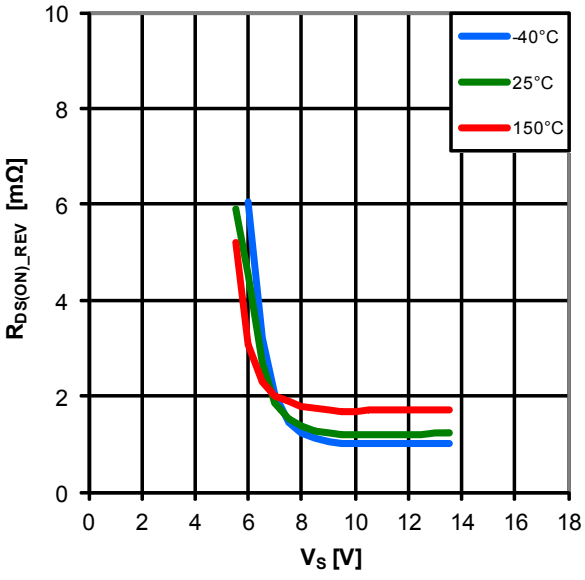


Figure 46 Resistance in Reversave $R_{DS(ON)\_REV}$ = f(V_S, T_J), I_L = -20A

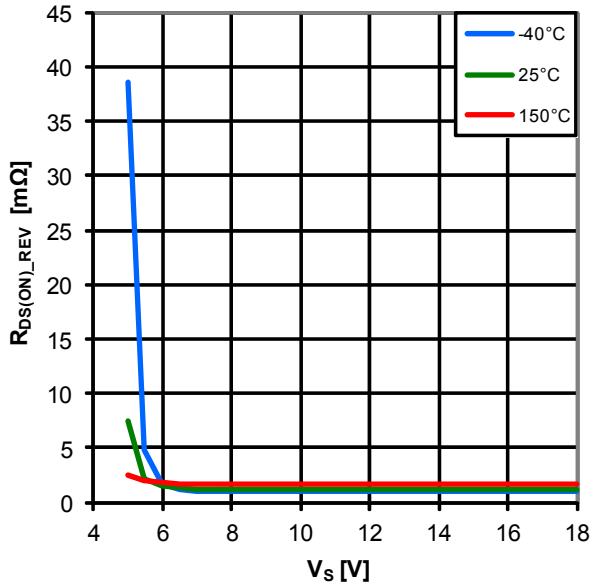


Figure 47 Input Current I_{IN} = f(T_J)
V_S = 13.5V; $V_{IN(L)}$ = 0.8V; $V_{IN(H)}$ = 5.0V

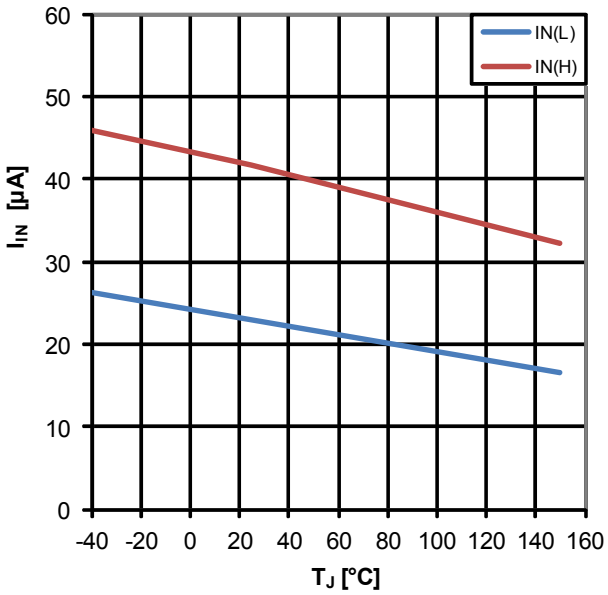


Figure 48 Input Current I_{IN} = f(V_{IN}, T_J)
V_S =13.5V

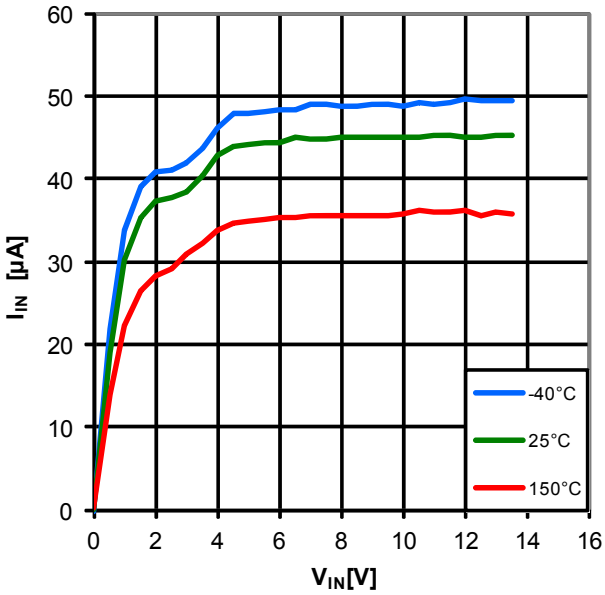
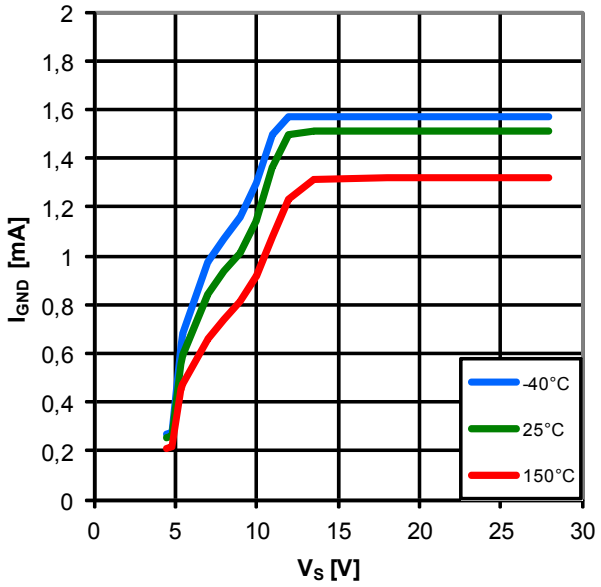


Figure 49 GND current I_{GND} = f(V_S, T_J)
V_{IN} = 2.2V



7 Package Outlines

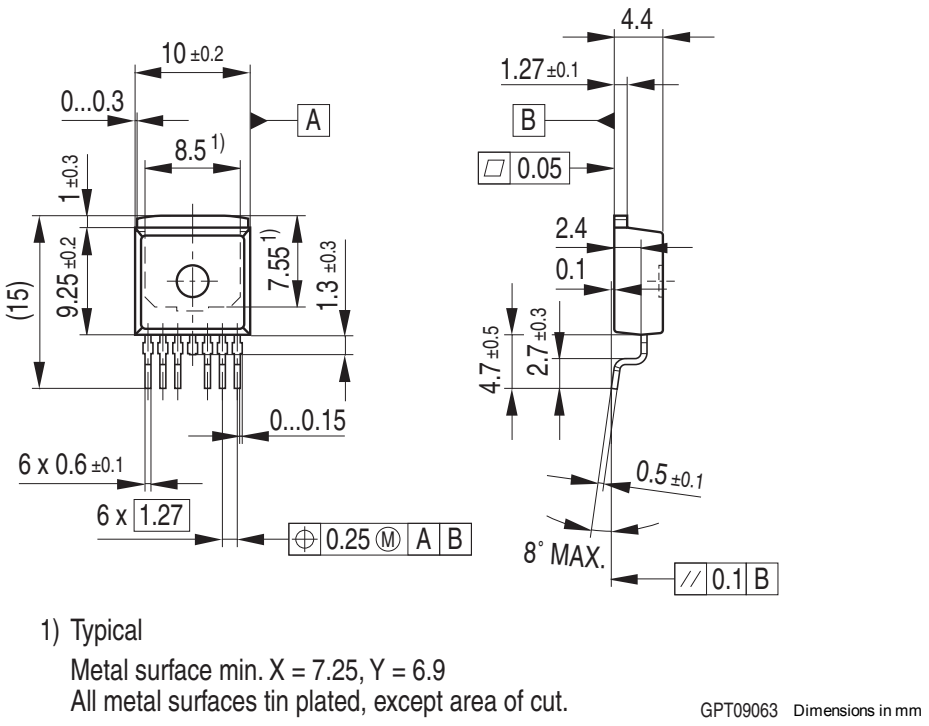


Figure 50 PG-TO-263-7-8 (RoHS-Compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

8 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

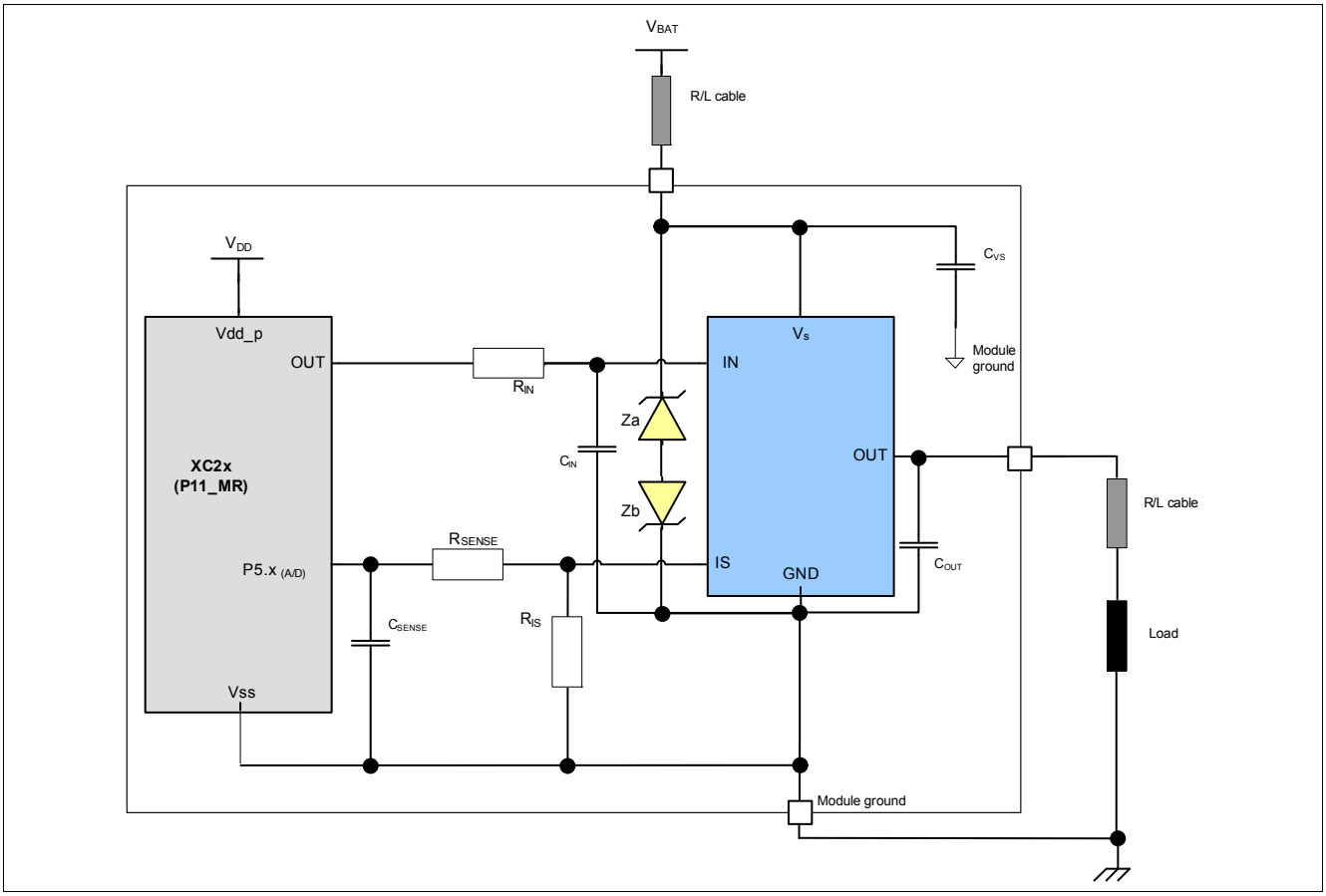


Figure 51 Application Diagram with BTS50010-1TAC

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 7 Bill of material

Reference	Value	Purpose
R_{IN}	4.7kΩ	Protection of the microcontroller during overvoltage, reverse polarity allows BTS50010-1TAC channels OFF during loss of ground
R_{IS}	1kΩ	Sense resistor
R_{SENSE}	4.7kΩ	Protection of the microcontroller during overvoltage Protection of the BTS50010-1TAC during reverse polarity
Z_a	Zener diode	Protection of the BTS50010-1TAC during loss of load with primary charged inductance, see **Chapter 5.3.2**
Z_b	Zener diode	Protection of the BTS50010-1TAC during loss of battery or against huge negative pulse at OUT (like ISO pulse 1), see **Chapter 5.3.2**
C_{SENSE}	10nF	Sense signal filtering
C_{VS}	100nF	Improved EMC behavior (in layout, pls. place close to the pins)

Table 7 Bill of material

Reference	Value	Purpose
C_{OUT}	10nF	Improved EMC behavior (in layout, pls. place close to the pins)
C_{IN}	150nF	BTS50010-1TAC tends to latched switch-off due to short negative transients on supply pin; C_{IN} automatically resets the device

8.1 Further Application Information

- Please contact us for information regarding the pin FMEA
- For further information you may contact **http://www.infineon.com/**

9 Revision History

Revision	Date	Changes
1.0	2014-01-28	Document release

Edition 2014-01-28

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