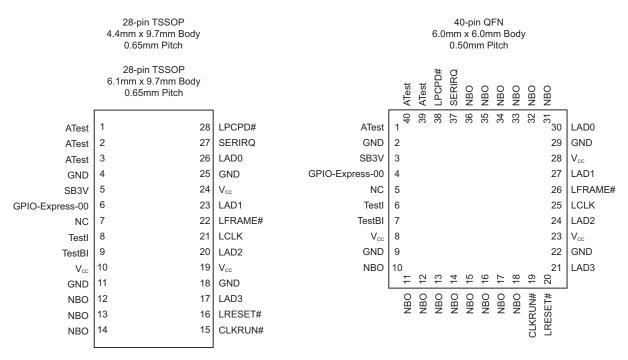
1. Pin Configurations and Pinouts

Table 1-1. Pin Configurations

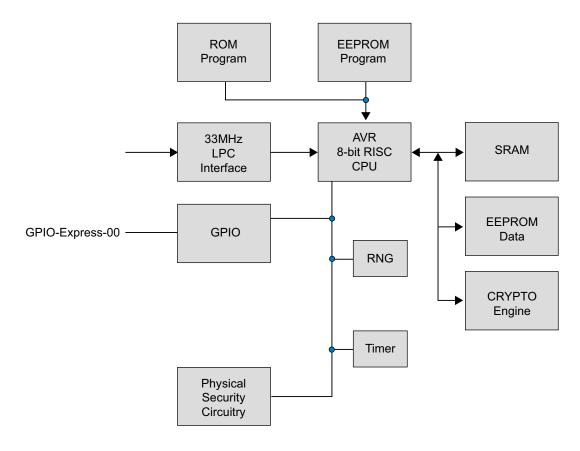
Pin name	Function		
V _{CC}	3.3V Supply Voltage		
SB3V	Standby 3.3V Supply Voltage		
GND	Ground		
LRESET#	PCI Reset Input Active Low		
LAD0	LPC Command, Address, Data Line Input/Output		
LAD1	LPC Command, Address, Data Line Input/Output		
LAD2	LPC Command, Address, Data Line Input/Output		
LAD3	LPC Command, Address, Data Line Input/Output		
LCLK	33MHz PCI Clock Input		
LFRAME#	LPC FRAME Input		
CLKRUN#	PCI Clock Run Input/Output		
LPCPD#	LPC Power-Down Input		
SERIRQ	Serialized Interrupt Request Input/Output		
GPIO-Express-00	GPIO assigned to TPM_NV_INDEX_GPIO_00		
Testl	Test Input (Disabled)		
TestBI	Test Input (Disabled)		
ATest	Atmel Test Pin		
NC	No Connect		
NBO	Not Bounded Out		

Table 1-2. Pinouts





2. Block Diagram



The TPM includes a hardware random number generator, including a FIPS-approved Pseudo Random Number Generator that is used for key generation and TCG protocol functions. The RNG is also available to the system to generate random numbers that may be needed during normal operation.

The chip uses a dynamic internal memory management scheme to store multiple RSA keys. Other than the standard TCG commands (TPM_FlushSpecific, TPM_Loadkey2), no system intervention is required to manage this internal key cache.

The TPM is offered to OEM and ODM manufacturers as a turnkey solution, including the firmware integrated on the chip. In addition, Atmel provides the necessary device driver software for integration into certain operating systems, along with BIOS drivers. Atmel will also provide manufacturing support software for use by OEMs and ODMs during initialization and verification of the TPM during board assembly.

Full documentation for TCG primitives can be found in the TCG TPM Main Specification, Parts 1 to 3, on the TCG Web site located at https://www.trustedcomputinggroup.org. TPM features specific to PC Client platforms are specified in the "TCG PC Client Specific TPM Interface Specification, Version 1.2", also available on the TCG web site. Implementation guidance for 32-bit PC platforms is outlined in the "TCG PC Client Specific Implementation Specification for Conventional BIOS for TCG Version 1.2", also available on the TCG website.



3. Ordering Information

Atmel Ordering Code	Package		Operating Range
AT97SC3204 ⁽¹⁾	28X1 (28-pin thin TSSOP)	Lead-free, RoHS	Commercial (0°C to 70°C)
AT97SC3204 ⁽¹⁾	40ML1 (40-pin QFN)	Leau-liee, Rons	Industrial (-40°C to 85°C)

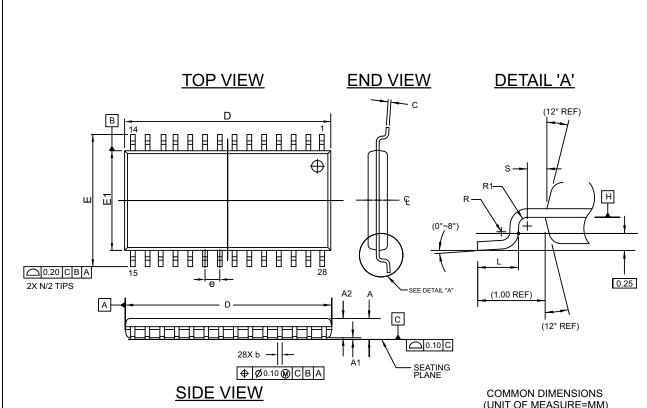
Note: 1. Please see the AT97SC3204 datasheet addendum for the complete catalog number ordering code.

	Package Type
28X1	28-lead, 4.4mm body width, Plastic Thin Shrink Small Outline (thin TSSOP)
40ML1	40-pad 6.0 x 6.0x0.9mm body, 0.50mm pitch, Very-thin Quad Flat No Lead (VQFN)



4. Package Drawings

4.1 28X1 — 28-lead Thin TSSOP



Note:

- 1. Refer to JEDEC drawing MO-153, variation AE
- Dimension D does not include mold flash, protrusions or gate burrs. Mold flash,protrusions or gate burrs shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
- 3. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.

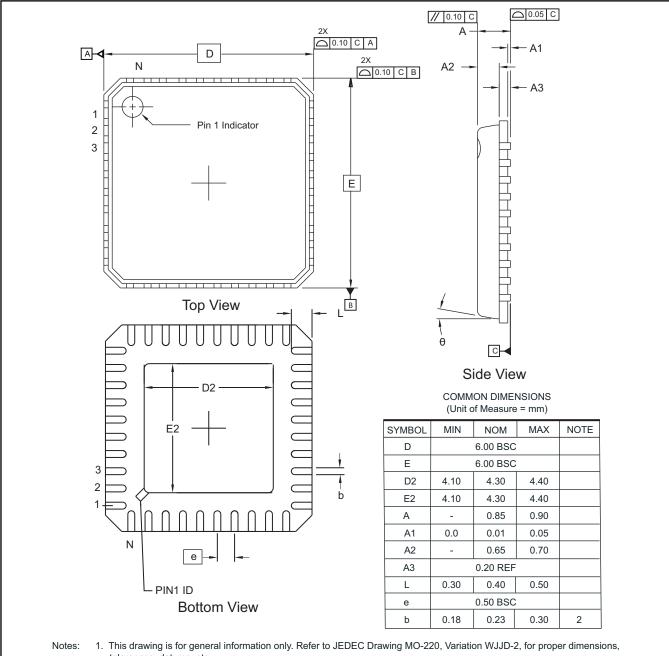
(UNIT OF MEASURE=MM)				
SYMBOL	MIN	NOM	MAX	NOTE
Α	-	-	1.10	
A1	0.05	-	0.15	
A2	0.85	0.90	0.95	
b	0.19	-	0.30	2
С	0.09	-	0.20	
D	9.60	9.70	9.80	1
Е	6.40BSC			
E1	4.30	4.40	4.50	1
е		0.65 BSC		
L	0.45	0.60	0.75	
R	0.09	-	-	
R1	0.09	-	-	
S	0.20	-	-	

7/8/2011

Atmel	TITLE	GPC	DRAWING NO.	REV.	
Package Drawing Contact: packagedrawings@atmel.com	28X1, 28-lead, 4.4mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	TFL	28X1	Α	



40ML1 — 40-pad VQFN 4.2



- tolerances, datums, etc.
- 2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

09/23/11

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Package Drawing Contact: packagedrawings@atmel.com 40ML1, 40-pad 6.0 x 6.0x0.9 mm Body, 0.50 mm pitch, Very-Thin Quad Flat No Lead Package (VQFN) Punched

GPC	DRAWING NO.	REV.
ZJI	40ML1	D



5. Revision History

Doc. Rev.	Date	Comments
5295ES	03/2013	Removed bullet from features: 2048-bit RSA® sign in 200ms. Updated footers and disclaimer page.
5295DS	12/2012	Changed GPIO6 to GPIO-Express-00. Updated package drawings 28A3 and 40ML1. Updated package drawing 28A1 to 28X1. Updated template and Atmel logos.
5295CS	03/2011	Corrected header and footers.
5295BS	10/2010	Added Industrial Grade support detail.
5295AS	01/2008	Initial document release.





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