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REVISION HISTORY

10/2017—Rev. 0 to Rev. A

Changes to Ordering Guide ... 15

5/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{EN} = 24 V, V_{OUT} = 3.3 V, typical values are at T_A = 25°C, and minimum/maximum limits are guaranteed for T_J = −40°C to +125°C, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 1.

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE SUPPLY RANGE	V_{IN}		4.5		60	V
QUIESCENT CURRENT						
Sleep Mode	I_{Q_SLEEP}	Between switching cycles, FB > V_{FB_RISING}		12	23	µA
Active	I_{Q_ACTIVE}	During switching cycle, FB < $V_{FB\_FALLING}$		140	165	µA
Shutdown Current	$I_{Q\_SHUTDOWN}$	V_{EN} = 0 V, T_J = −40°C to +85°C		0.8	4	µA
UNDERVOLTAGE LOCKOUT (UVLO)						
VIN UVLO Rising Threshold	V_{UVLO_RISING}		4.3	4.4	4.5	V
VIN UVLO Falling Threshold	$V_{UVLO\_FALLING}$		4.1	4.2	4.3	V
SOFT START (SS)						
SS Pin Current	I_{SS}	V_{SS} = 0 V	0.75	1	1.25	µA
PRECISION ENABLE LOGIC/SHUTDOWN						
EN Pin Voltage Range	V_{EN}		0		60	V
EN Threshold Rising	V_{EN_RISING}		0.95	1	1.05	V
EN Hysteresis	V_{EN_HYS}			50		mV
EN Pin Leakage Current	$I_{EN\_LEAKAGE}$	V_{IN} = V_{EN} = 60 V		0.1	0.5	µA
Shutdown Threshold	$V_{EN\_SHUTDOWN}$		0.35	0.57	0.7	V
FEEDBACK						
Adjustable Output Voltage Range	V_{OUT}		0.8		V_{IN}	V
FB Falling Threshold	$V_{FB\_FALLING}$	Adjustable output voltage model	0.792	0.800	0.808	V
		Fixed 3.3 V output voltage model	3.267	3.300	3.333	V
		Fixed 5.0 V output voltage model	4.950	5.000	5.050	V
FB Rising Threshold	V_{FB_RISING}	Adjustable output voltage model	0.794	0.803	0.812	V
		Fixed 3.3 V output voltage model	3.284	3.317	3.349	V
		Fixed 5.0 V output voltage model	4.975	5.025	5.075	V
FB Pin Current	I_{FB}	Adjustable output voltage models		0.005	0.1	µA
		Fixed output voltage models		1.15	1.5	µA
SWITCH (SW) PARAMETERS						
On Resistance						
Positive Metal Oxide Semiconductor (PMOS)	R_{DSON_P}	I_{SW} = 50 mA		4	8	Ω
Negative Metal Oxide Semiconductor (NMOS)	R_{DSON_N}	I_{SW} = 50 mA		2	4	Ω
Leakage Current						
PMOS		V_{SW} = 0 V			1	µA
NMOS		V_{SW} = 24 V			1	µA
Discharge Resistor		EN = 0 V		100		kΩ
INDUCTOR CURRENT LIMIT						
ITH Threshold Voltage	V_{ITH}		0.967	1	1.018	V
Peak Current Limit	I_{PEAK}	R_{ITH} = 0 Ω, at power-up	126	140	154	mA
		R_{ITH} = open, at power-up	45	50	55	mA
Minimum PMOS on Time	$t_{PMOS\ (MIN)}$	I_{SW} = 20 mA, R_{ITH} = open		35		ns
POWER GOOD (PG)						
PG Pin Voltage Range	V_{PG}		0		60	V
PG Pin Pull-Down Resistance	R_{PG}			1.0	1.5	kΩ
Rising Threshold	V_{PG_RISING}	Adjustable output voltage model		0.740	0.760	V
		Fixed 3.3 V output voltage model		3.053	3.135	V
		Fixed 5.0 V output voltage model		4.625	4.750	V

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hysteresis	V_{PG_HYS}	Adjustable output voltage model		40		mV
		Fixed 3.3 V output voltage model		165		mV
		Fixed 5.0 V output voltage model		250		mV
Leakage Current	$I_{PG\_LEAKAGE}$	V_{PG} = 24 V		0.06	0.5	µA
THERMAL SHUTDOWN						
Rising Threshold	T_{SHDN}			150		°C
Hysteresis	T_{HYS}			15		°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN, PG, to AGND, PGND	−0.3 V to +61 V
FB to AGND, PGND	−0.3 V to +5.5 V
SW to AGND, PGND	−0.3 V to V_{IN} + 0.3 V
ITH, SS to AGND, PGND	−0.3 V to +4 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

For additional information on thermal resistance, refer to Application Note AN-000, *Thermal Characteristics of IC Assembly*.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
8-Lead LFCSP	62.7	33.60	°C/W

θ_{JA} and Ψ_{JB} and are modeled using a standard 4-layer JEDEC printed circuit board (PCB) (2S2P) with the exposed pad soldered to the board with a 2 × 2 array of thermal vias and still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

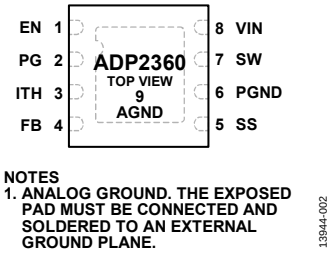

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input. This pin enables control for the ADP2360 with precision thresholds.
2	PG	Power-Good Output. This pin is an open-drain, power-good indicator.
3	ITH	I_{PEAK} Threshold Programming Pin. Connect a resistor to ground to adjust the I_{PEAK} level in the application.
4	FB	Output Voltage Feedback Input. Use this pin to set the output voltage.
5	SS	Soft Start. Connect a capacitor from SS to AGND to adjust the soft start time of the device.
6	PGND	Power Ground. NMOS power device and driver ground connection.
7	SW	Switch Node. This pin is the drain of the power NMOS and power PMOS devices.
8	VIN	Input Voltage. An input capacitor must be placed between this pin and PGND.
9	AGND (EPAD)	Analog Ground. The exposed pad must be connected and soldered to an external ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

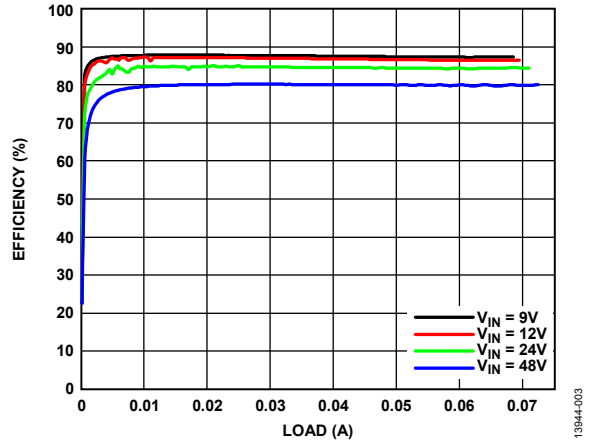

Figure 3. Efficiency vs. Load, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, T_A = 25°C

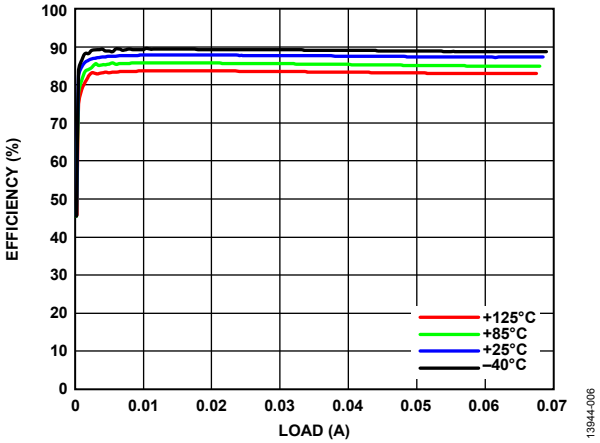

Figure 6. Efficiency vs. Load over Temperature, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω

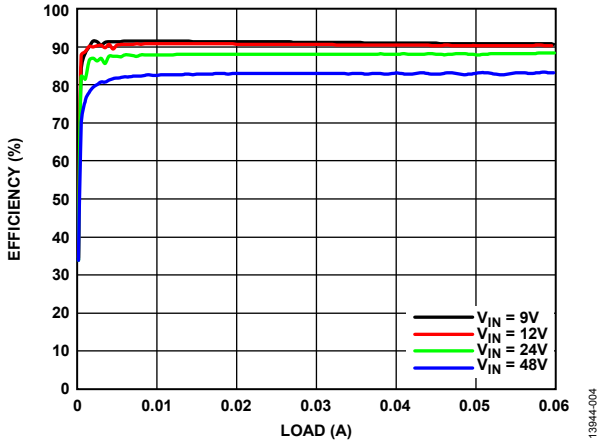

Figure 4. Efficiency vs. Load, V_{OUT} = 5 V Fixed, R_{ITH} = 0 Ω, T_A = 25°C

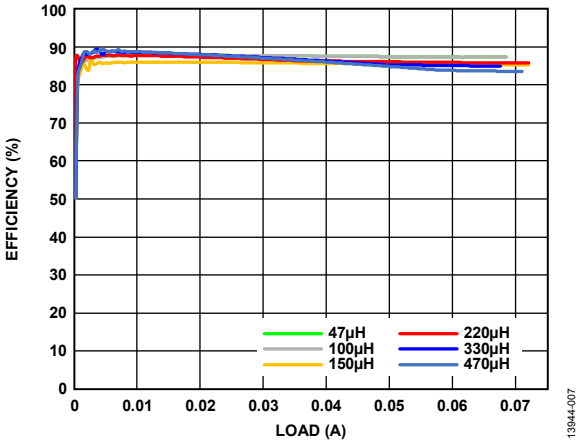

Figure 7. Efficiency vs. Load over Inductor Size, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, T_A = 25°C

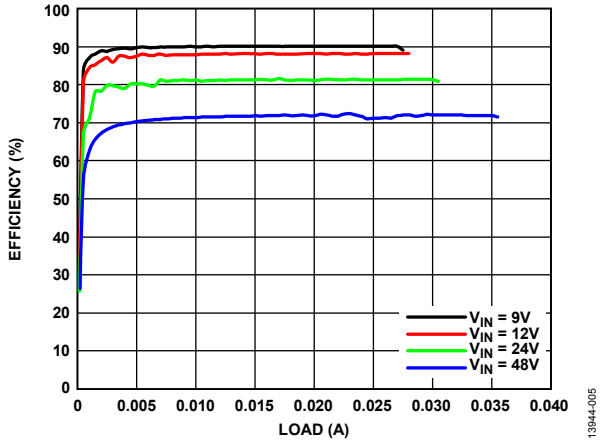

Figure 5. Efficiency vs. Load, V_{OUT} = 3.3 V Fixed, R_{ITH} = Open, T_A = 25°C

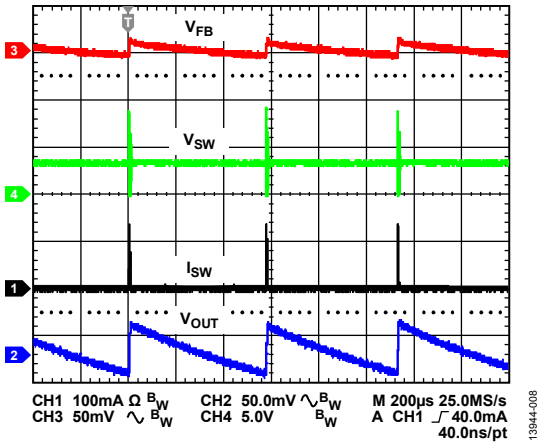

Figure 8. Switching Waveforms, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load = 1 mA

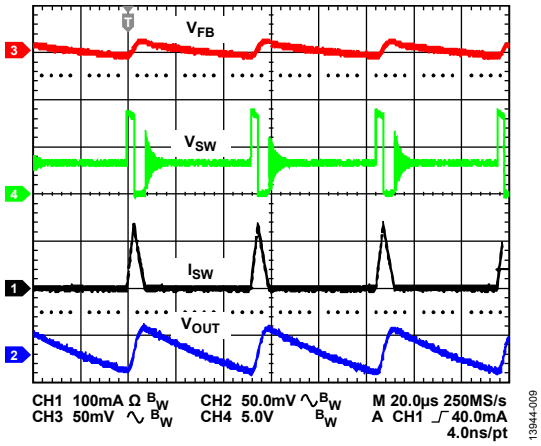

Figure 9. Switching Waveforms, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load = 10 mA

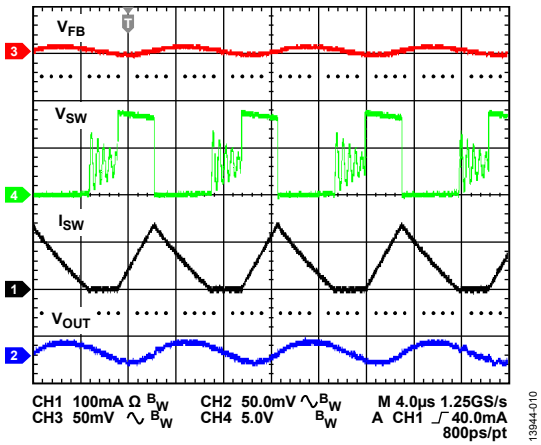

Figure 10. Switching Waveforms, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load = 50 mA

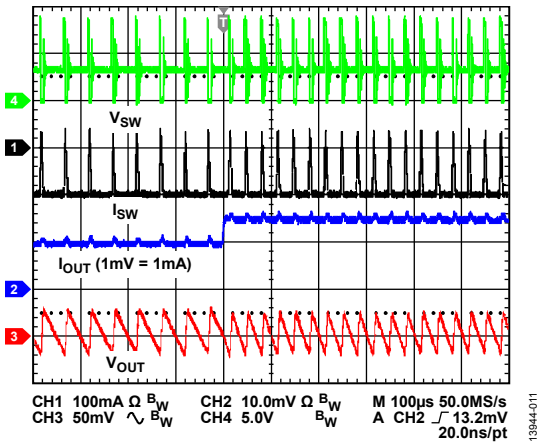

Figure 11. Load Transient, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load Step 10 mA to 15 mA

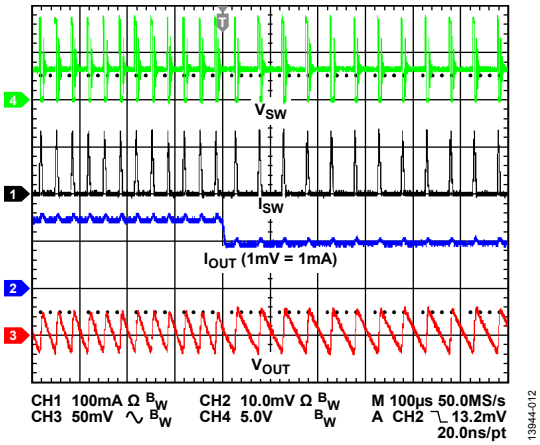

Figure 12. Load Transient, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load Step 15 mA to 10 mA

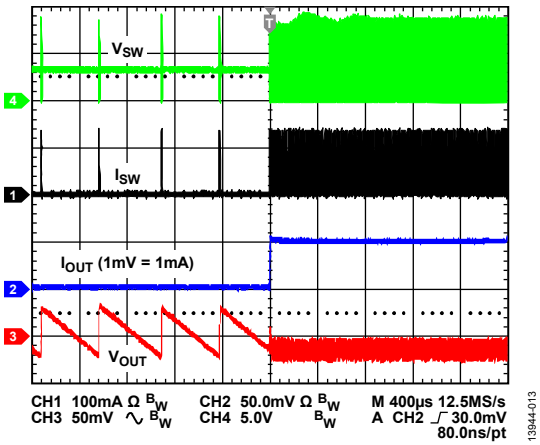

Figure 13. Load Transient, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load Step 1 mA to 50 mA

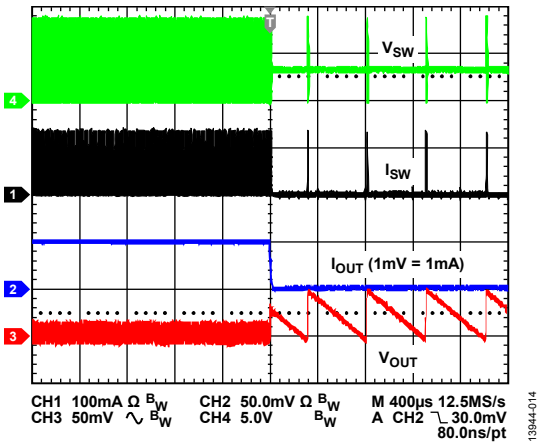

Figure 14. Load Transient, V_{IN} = 9 V, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load Step 50 mA to 1 mA

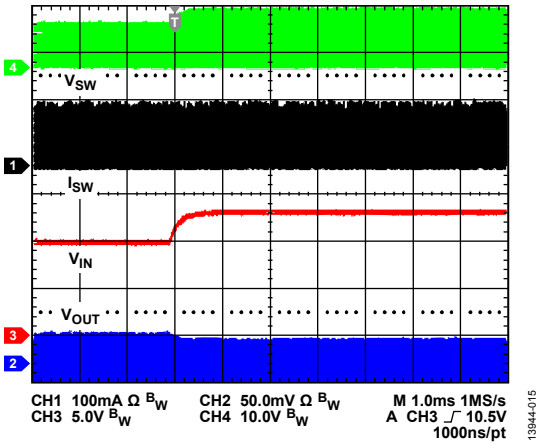

Figure 15. Line Transient, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load = 10 mA Line Step 9 V to 12 V

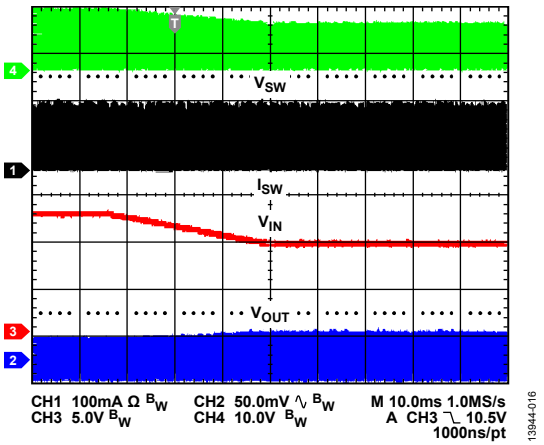

Figure 16. Line Transient, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load = 10 mA Line Step 12 V to 9 V

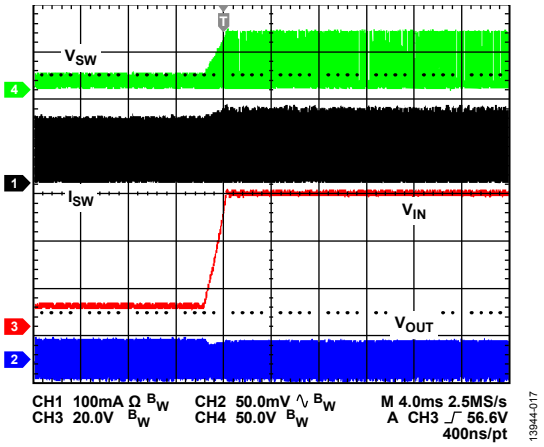

Figure 17. Line Transient, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load = 10 mA Line Step 12 V to 60 V

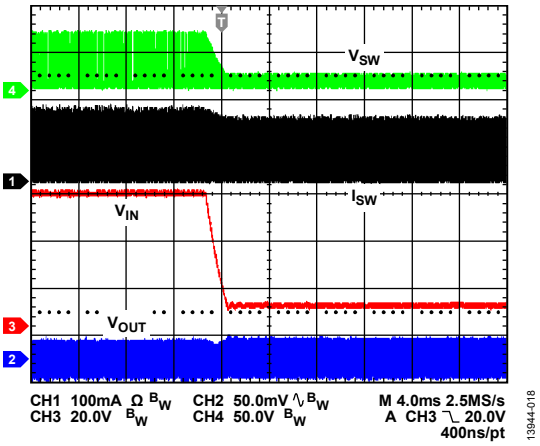

Figure 18. Line Transient, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load = 10 mA Line Step 60 V to 12 V

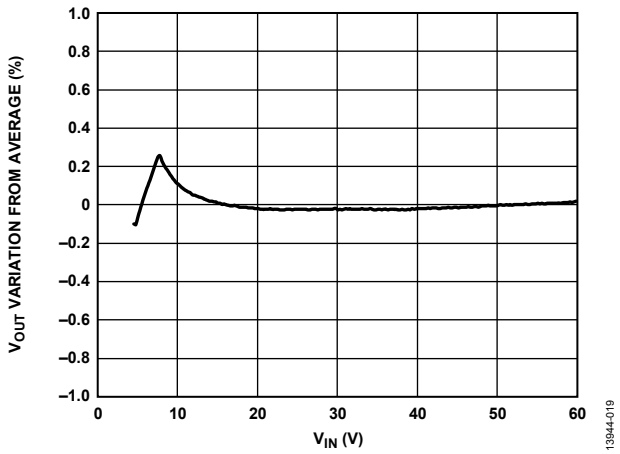

Figure 19. Line Regulation, V_{OUT} = 3.3 V Fixed, R_{ITH} = 0 Ω, Load = 10 mA

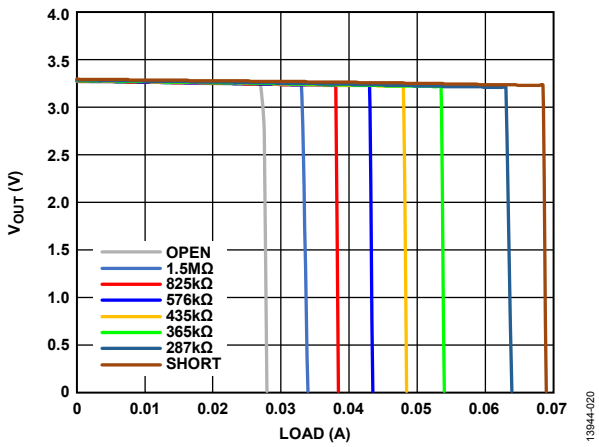

Figure 20. Load Current Capability, V_{OUT} vs. Load for Various R_{ITH} Values, V_{IN} = 9 V (V_{OUT} Drops to 0 V when Current Limit Reached)

THEORY OF OPERATION

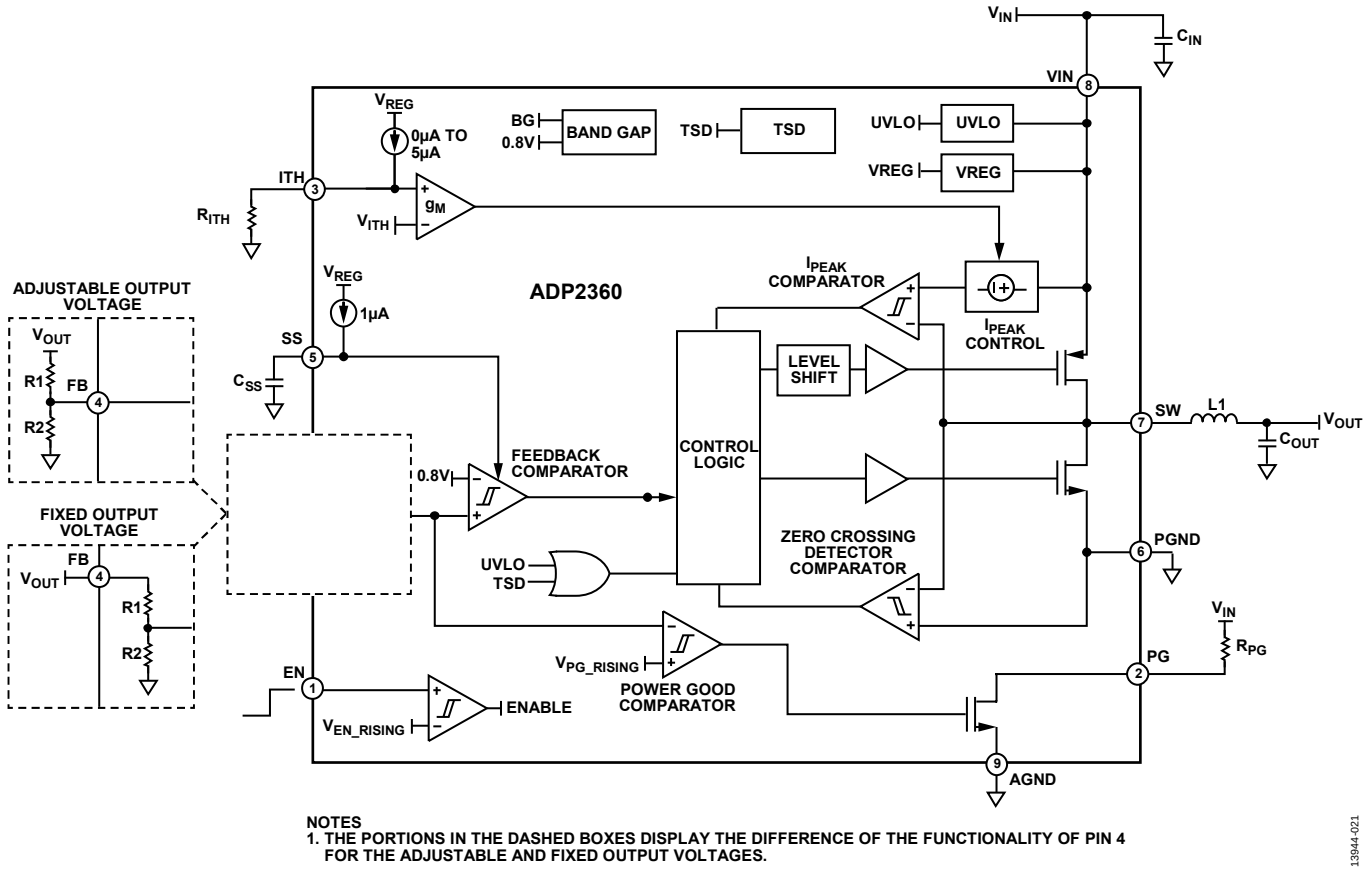

Figure 21. Block Diagram

OVERVIEW

The ADP2360 is a high efficiency, high input voltage, DCM synchronous, step-down, dc-to-dc switching regulator.

The ADP2360 uses a single-pulse PFM architecture with adjustable I_{PEAK} control to adjust the frequency variation within the application and to minimize the input and output ripple.

The ADP2360 further offers a power-good (PG) pin with an open-drain output signal to indicate when the output voltage is stable. Other key features include 100% duty cycle operation, precision enable control, external soft start control, undervoltage lockout, and thermal shutdown.

CONTROL SCHEME

The ADP2360 uses a single-pulse, peak current PFM control scheme. A switching cycle is started when the FB pin voltage, V_{FB}, is less than the $V_{FB\_FALLING}$ threshold, and the PMOS is turned on. While the PMOS is on, the current through the inductor increases to charge the output capacitor (C_{OUT}) and store energy in the inductor. The current through the inductor continues to increase until it reaches the IPEAK programmed via the ITH pin. When I_{PEAK} is reached, or if the V_{FB} voltage rises above V_{FB_RISING}, the PMOS turns off.

When the PMOS turns off, the NMOS turns on, reducing the energy stored in the inductor until the inductor current reaches zero. At this point, the NMOS also turns off.

When both the NMOS and PMOS are off, the ADP2360 enters into sleep mode. During this phase of operation, the stored energy in C_{OUT} delivers the load current, and thus V_{OUT} and V_{FB} decrease. When V_{FB} drops below the $V_{FB\_FALLING}$ threshold, another switching cycle begins.

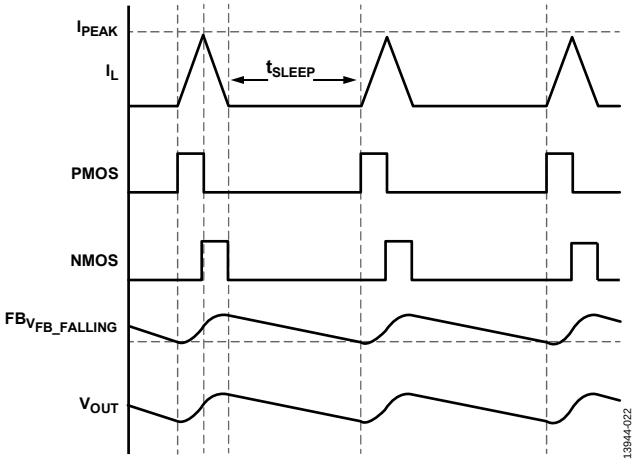

Figure 22. Control Scheme Typical Waveforms

100% Duty Cycle

Because the PMOS turns off only if the peak current is reached or if the feedback voltage exceeds V_{FB_RISING}, the ADP2360 seamlessly operates up to 100% duty cycle. This situation arises when the input and output voltage are nearly equal. If the input voltage drops below the output voltage, the output is maintained with a small voltage drop across the PMOS device. When operating in 100% duty cycle, the output current limit is approximately equal to I_{PEAK}. Steps must be taken to ensure that the load does not exceed 50% of I_{PEAK} to avoid the current limit when the input voltage rises above the output voltage.

Adjustable Peak Current Threshold (ITH)

The control method of the ADP2360 means that the maximum output current is slightly less than half of I_{PEAK}. This peak current value is resistor programmable with R_{ITH}.

The I_{PEAK} value set by R_{ITH} on the ITH pin is determined at startup and is reset only if the device is disabled and reenabled using the EN pin or a VIN power cycle.

DEVICE FEATURES

Fixed and Adjustable Output Models

Both fixed and adjustable output models are available. The fixed output models provide the feedback resistors internally.

Shutdown/Precision Enable

The EN pin of the ADP2360 tolerates the full supply voltage range and provides three states of operation for the device: shutdown, sleep, and active. When the EN pin voltage (V_{EN}) is less than $V_{EN\_SHUTDOWN}$, the ADP2360 is in shutdown mode and the VIN supply current is at the lowest value ($I_{Q\_SHUTDOWN}$).

When V_{EN} rises above $V_{EN\_SHUTDOWN}$ but is below V_{EN_RISING}, some internal circuitry is enabled and the device is in standby mode. This circuitry enables the references that provide the precision enable threshold.

The precision enable turns on the regulator when the EN pin voltage rises above V_{EN_RISING} and returns to standby mode when the voltage falls below $V_{EN\_RISING} - V_{EN\_HYS}$.

Soft Start

When the ADP2360 is enabled, an internal current source supplies current (I_{SS}) to the soft start capacitor (C_{SS}) until it reaches approximately 1 V at startup. During this time, V_{SS} replaces the internal feedback reference for the feedback comparator. This reference rises at the same rate as V_{SS} to the 0.8 V regulation level. After V_{SS} reaches 0.8 V, the feedback voltage reference is switched to an 0.8 V internal reference. When V_{SS} reaches approximately 1 V, the SS pin is connected to an internal pull-down resistor and discharged to 0 V. See Figure 23 for a diagram showing the soft start time period and the behavior of the SS pin.

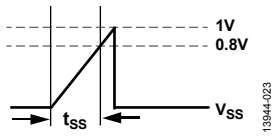

Figure 23. Soft Start Voltage Time Period

Calculate the soft start time using the following equation:

$$t_{SS} = \frac{C_{SS} \times 0.8\ \text{V}}{I_{SS}} \quad (1)$$

When the ADP2360 is disabled via the EN pin, a UVLO event, or a TSD event, the SS pin is reset. When the device is enabled or the condition causing the UVLO or TSD event is removed, the full soft start sequence occurs.

Thermal Shutdown (TSD)

The ADP2360 includes an internal TSD protection circuit. If the junction temperature exceeds T_{SHDN}, the TSD disables switching and reduces the power dissipation in the device. While in thermal shutdown, the power PMOS and NMOS devices are turned off and the soft start capacitor, C_{SS}, is discharged to AGND. When the junction temperature decreases to $T_{SHDN} - T_{HYS}$, the ADP2360 initiates a soft start and resumes switching to regulate the output voltage.

Undervoltage Lockout (UVLO)

The ADP2360 has an internal UVLO on the VIN pin. If the input voltage is falls below the $V_{UVLO\_FALLING}$ threshold, the ADP2360 is disabled. The ADP2360 does not resume operation until the input voltage rises above the V_{UVLO_RISING} threshold.

Power Good

The ADP2360 has an active high, internal, open-drain, 60 V, NMOS device connected to the power-good pin (PG) that is used as a flag to indicate the status of the output voltage. To configure the PG output, connect a pull-up resistor from PG to an external voltage rail. An internal current limit prevents damage to this pin.

When the feedback pin voltage (V_{FB}) is less than V_{PG_RISING}, the open-drain NMOS is on, and PG is pulled to ground. When the internal feedback voltage exceeds V_{PG_RISING}, the open-drain NMOS turns off.

The PG pin has hysteresis to prevent glitching. The NMOS remains off until the internal feedback voltage falls below the $V_{PG\_FALLING}$ threshold.

If EN is low or a TSD or UVLO event occurs, an internal discharge resistor is internally connected from the SW node to PGND. This resistor pulls the output voltage to ground when the regulator is disabled, even when there is no load on the output.

APPLICATIONS INFORMATION

Compatible components for the step-down application circuits in Figure 24 and Figure 25 are identified using the guidelines in this section.

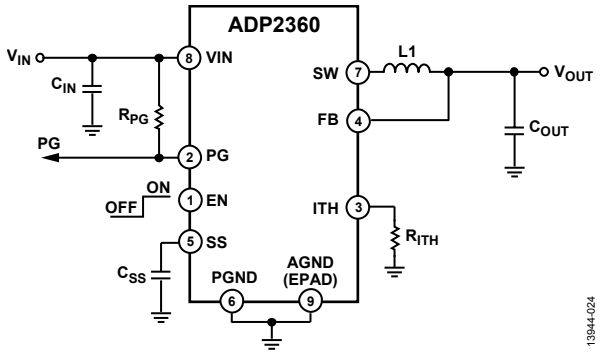

Figure 24. Typical Application Circuit Fixed Output Voltage

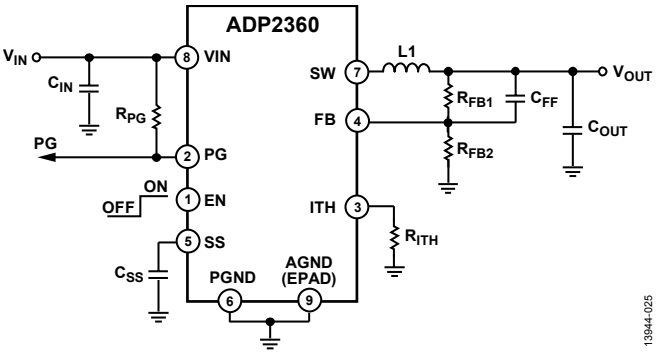

Figure 25. Typical Application Circuit Adjustable Output Voltage

SETTING THE OUTPUT VOLTAGE

The ADP2360 is available with 3.3 V and 5.0 V fixed output voltage options. For the fixed options, an internal resistive feedback divider sets the output voltage and no external resistors are necessary, as shown in Figure 24.

The ADP2360 is also available with an adjustable output voltage and can be configured for output voltages between 0.8 V and V_{IN}. Use the following equation to determine R_{FB1} and R_{FB2} for the desired V_{OUT}:

$$V_{OUT} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \times V_{FB\_FALLING} \quad (2)$$

When using an external resistor divider, the optional feedforward capacitor C_{FF} may be placed across R_{FB1}.

INPUT CAPACITOR SELECTION

An input capacitor must be placed between the VIN pin and PGND. Ceramic capacitors greater than or equal to 4.7 µF are recommended. The input capacitor reduces the input voltage ripple caused by the switching current. Place the input capacitor as close as possible to the VIN pin to reduce input voltage spikes. The voltage rating of the input capacitor must be greater than the maximum input voltage.

ESTIMATING THE SWITCHING FREQUENCY

The ADP2360 switching frequency (f_{SW}) can be estimated with the following equation:

$$f_{SW} \approx \frac{2 \times (V_{IN} - V_{OUT}) \times D \times I_{OUT}}{L \times I_{PEAK}{}^2} \quad (3)$$

where the duty cycle, D, is approximated by

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Note that the switching frequency changes in direct proportion to the output current. The maximum frequency can be controlled by the inductor value and the peak current control resistor R_{ITH}.

SETTING THE PEAK INDUCTOR CURRENT

The control method of the ADP2360 means that the maximum output current is slightly less than half of I_{PEAK}. The peak current limit must be programmed to at least twice the desired maximum output current.

The value of the selected I_{PEAK} current in the ADP2360 application affects the efficiency, switching frequency, and output voltage ripple. Larger I_{PEAK} values tend to give improved efficiency. Using a smaller I_{PEAK} value gives a higher switching frequency and reduced output voltage ripple.

The desired peak current limit (I_{PEAK}) is programmed to a discrete value between 50 mA and 140 mA with an external resistor from ITH to AGND. This external resistor, R_{ITH}, is chosen using the values in Table 5.

Table 5. Peak Inductor Current Settings

R_{ITH} (kΩ)	I_{PEAK} (mA)
Open	50
1500	60
825	70
576	80
453	90
365	100
287	120
0	140

The values given in Table 5 correspond to standard 1% E96 resistor values. A 1% tolerance resistor of the specified value must be used to ensure the correct I_{PEAK} value is selected. The I_{PEAK} value set by R_{ITH} on the ITH pin is determined upon startup and is reset only if the device is disabled and reenabled using the EN pin or a VIN power cycle.

INDUCTOR SELECTION

The value of the selected inductor in the ADP2360 application affects the efficiency, switching frequency, and output voltage ripple. Larger value inductors tend to give improved efficiency although for a given package size, the increased DCR and core losses eventually dominate. Using a smaller value inductor gives a higher switching frequency and reduced output voltage ripple, but may decrease the overall efficiency due to increased switching losses.

The ADP2360 is designed with an adjustable I_{PEAK} current limit that allows the designer to optimize the efficiency for the application operating conditions and reduce the required inductor size. Inductors in the 100 µH to 600 µH range are recommended.

Take care to select a compatible inductor with a sufficient current rating, saturation current, and low dc resistance. The current rating of the inductor must be greater than the maximum I_{PEAK} current limit set by the ITH pin, as specified in Table 1.

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects the output voltage ripple according to the following equation:

$$\Delta V_{OUT} = \frac{I_{OUT}}{C_{OUT} \times f_{SW}} \quad (5)$$

The ADP2360 is designed for operation with ceramic capacitors, because these have a small footprint and low equivalent series resistance (ESR) values, giving the lowest output voltage ripple. An output capacitance of 10 µF is suggested for most applications. This value can be increased to reduce output voltage ripple.

DESIGN OPTIMIZATION

For designs where the highest efficiency is desired, set the I_{PEAK} level to the maximum and use a high value low dc resistance inductor (330 µH to 470µH are recommended). These choices lead to a larger output voltage ripple that may be reduced with a larger value, low ESR output capacitor.

For designs where the highest switching frequency is desired, set I_{PEAK} to just above double the required maximum output current. Use a 100 µH inductor with low dc resistance.

For designs where the lowest ripple is desired, set I_{PEAK} to just above double the required maximum output current. Use a 100 µH inductor with low dc resistance and a large value, low ESR output capacitor.

RECOMMENDED COMPONENTS

The components specified in Table 6 are recommended for operation across the full input voltage range. All typical performance characteristic data was measured using these components and the adjustable voltage option of the ADP2360 with appropriately chosen feedback resistors to select the required output voltage.

Table 6. Recommended Components

Component	Value	Part Number	Manufacturer
COUT	10 µF, 50 V	GRM32ER71H106KA12L	Murata
L1	100 µH	744043101	Würth
CIN	10 µF, 100 V	C5750X7S2A106M230KB	TDK
CFF	10 pF, 50 V	GRM1885C1H100JA01D	Murata

PCB LAYOUT CONSIDERATIONS

For high efficiency, good regulation, and stability with the ADP2360, a well designed PCB is required. Poor layout can affect the ADP2360 buck performance, causing electromagnetic interference (EMI), poor electromagnetic compatibility (EMC), ground bounce, and voltage losses.

Use the following guidelines when designing PCBs:

- Keep the low ESR input and output capacitors, C_{IN} and C_{OUT}, and the inductor, L1, as close as possible to the ADP2360. Avoid long trace lengths from the device to the capacitors that add series inductance and may cause EMI issues or increased ripple.
- Keep R_{FB1}, R_{FB2}, and C_{FF} as close as possible to the FB pin.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Keep high current traces as short and as wide as possible.
- Avoid routing high impedance traces near any node connected to SW or near the inductor to prevent radiated noise injection.
- Use a ground plane with several vias connected to the component side ground to reduce noise interference on sensitive circuit nodes.
- Be aware that traces may carry up to 60 V and leave adequate separation between traces where necessary.
- Because up to 60 V may be present between the EPAD and device pins, the EPAD must be solder mask defined and reduced slightly in size to prevent the risk of bridging if the device is misaligned. To help ensure alignment during reflow processes, traces must exit the pads perpendicular to the device edge as shown in Figure 26. See the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, for further guidance on layout, footprint, and manufacturing.

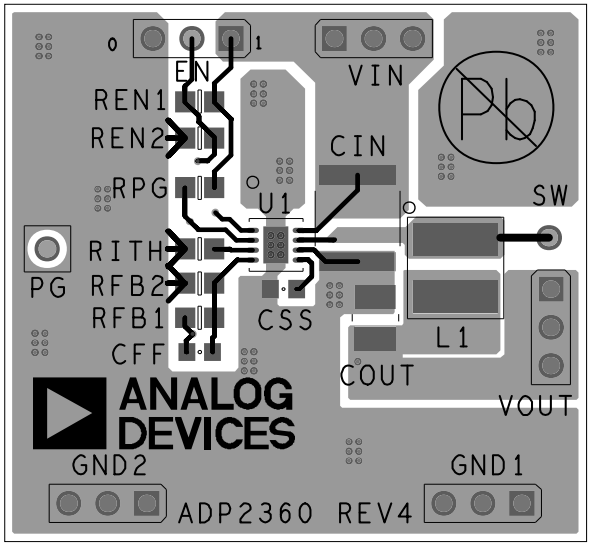

Figure 26. PCB Layout, Top

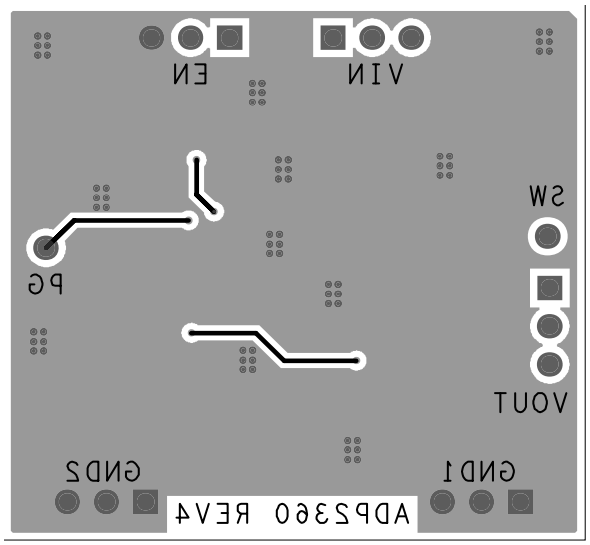

Figure 27. PCB Layout, Bottom

OUTLINE DIMENSIONS

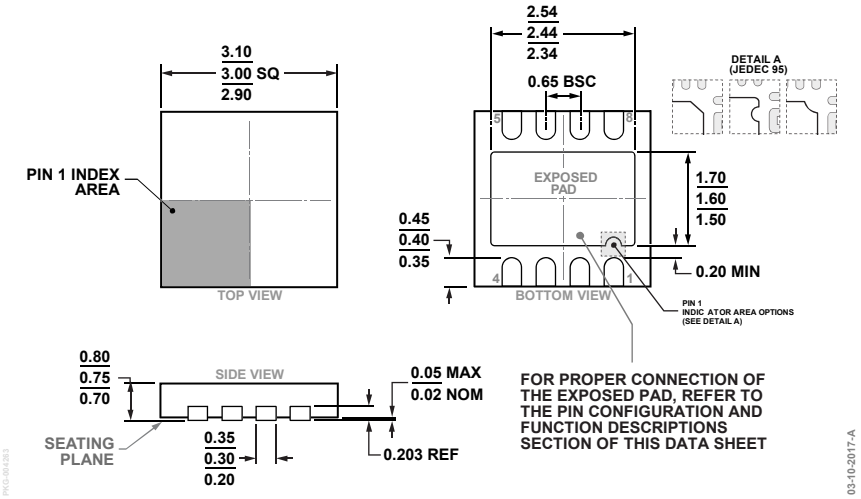

Figure 28. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-19)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Output Voltage	Temperature Range	Package Description	Package Option	Branding
ADP2360ACPZ-R7	0.8 V to V_{IN} adjustable	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-19	LTK
ADP2360ACPZ-3.3-R7	3.3 V fixed	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-19	LTH
ADP2360ACPZ-5.0-R7	5.0 V fixed	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-19	LTJ
ADP2360CP-EVALZ	0.8 V to V_{IN} adjustable		Evaluation Board		

[1] Z = RoHS Compliant Part.

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