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## **REVISION HISTORY**

9/15—Rev. 0 to Rev. A	
Change to Table 7	8
Updated Outline Dimensions	18

7/09—Revision 0: Initial Version

## **SPECIFICATIONS**

## ±5 V DUAL SUPPLY

 $V_{\text{DD}}$  = +5 V  $\pm$  10%,  $V_{\text{SS}}$  = -5 V  $\pm$  10%, GND = 0 V, unless otherwise noted.

#### Table 1.

Parameter25°C+85°C+125°CUnitTest Conditions/CommentsANALOG SWITCH Analog Signal Range $V_{DD}$ to $V_{SS}$ $V$ $V_{DD}$ to $V_{SS}$ $V$ On Resistance (R_{ON})4.5 $\Omega$ typ $V_{S} = \pm 4.5$ V, $I_{S} = -10$ mA; see Figure 25578 $\Omega$ max $V_{DD} = \pm 4.5$ V, $V_{SS} = \pm 4.5$ VOn-Resistance Match Between Channels ( $\Delta R_{ON}$ )0.12 $\Omega$ typ $V_{S} = \pm 4.5$ V, $I_{S} = -10$ mA0.250.30.35 $\Omega$ max $V_{S} = \pm 4.5$ V, $I_{S} = -10$ mA	
ANALOG SWITCH       V       V         Analog Signal Range       V       V         On Resistance (RoN)       4.5 $\Omega$ typ       Vs = ±4.5 V, Is = -10 mA; see Figure 25         5       7       8 $\Omega$ max       VDD = ±4.5 V, Vs = ±4.5 V         On-Resistance Match Between Channels ( $\Delta$ RoN)       0.12 $\Omega$ typ       Vs = ±4.5 V, Is = -10 mA         0.25       0.3       0.35 $\Omega$ max	
Analog Signal Range $V_{DD}$ to $V_{SS}$ $V$ On Resistance (R_{ON})       4.5 $\Omega$ typ $V_s = \pm 4.5$ V, $I_s = -10$ mA; see Figure 25         5       7       8 $\Omega$ max $V_{DD} = \pm 4.5$ V, $V_{SS} = \pm 4.5$ V         On-Resistance Match Between Channels ( $\Delta R_{ON}$ )       0.12 $\Omega$ typ $V_s = \pm 4.5$ V, $I_s = -10$ mA         0.25       0.3       0.35 $\Omega$ max	
On Resistance ( $R_{ON}$ )       4.5 $\Omega$ typ $V_s = \pm 4.5$ V, $I_s = -10$ mA; see Figure 25         5       7       8 $\Omega$ max $V_{DD} = \pm 4.5$ V, $V_{SS} = \pm 4.5$ V         On-Resistance Match Between Channels ( $\Delta R_{ON}$ )       0.12 $\Omega$ typ $V_s = \pm 4.5$ V, $I_s = -10$ mA         0.25       0.3       0.35 $\Omega$ max $V_s = \pm 4.5$ V, $I_s = -10$ mA	
Signal       Signal $\Omega$ max $V_{DD} = \pm 4.5$ V, $V_{SS} = \pm 4.5$ V         On-Resistance Match Between Channels ( $\Delta R_{ON}$ )       0.12 $\Omega$ typ $V_S = \pm 4.5$ V, $V_S = -10$ mA         0.25       0.3       0.35 $\Omega$ max	
On-Resistance Match Between Channels ( $\Delta R_{ON}$ ) 0.12 $\Omega$ typ Vs = ±4.5 V, ls = -10 mA	
0.25 0.3 0.35 O max	
0125 013 0135 1211104	
On-Resistance Flatness (R <sub>FLAT(ON)</sub> ) 1 $\Omega$ typ V <sub>S</sub> = ±4.5 V, I <sub>S</sub> = -10 mA	
1.3 1.7 2 Ω max	
LEAKAGE CURRENTS $V_{DD} = +5.5 \text{ V}, V_{SS} = -5.5 \text{ V}$	
Source Off Leakage, I <sub>s</sub> (Off) $\pm 0.02$ nA typ $V_s = \pm 4.5$ V, $V_D = \mp 4.5$ V; see Figure 26	
+0.1 +0.5 +3 nA max	
Drain Off Leakage $\ln (Off)$ $\pm 0.03$ $\ln A typ = 1.4 \pm 0.04$	
$V_s = \pm 4.5 \text{ V}, V_D = \pm 4.5 \text{ V}; \text{ see Figure 26}$	
ADG1608 ±0.15 ±2 ±14 nA max	
ADG1609 ±0.15 ±1 ±7 nA max	
Channel On Leakage, $I_D$ , $I_S$ (On) $\pm 0.03$ nA typ $V_S = V_D = \pm 4.5$ V; see Figure 27	
±0.15 ±2 ±14 nA max	
DIGITAL INPUTS	
Input High Voltage, VINH 2.0 V min	
Input Low Voltage, V <sub>INL</sub> 0.8 V max	
Input Current, $I_{INL}$ or $I_{INH}$ $\pm 1$ nA typ $V_{IN} = V_{GND}$ or $V_{DD}$	
±0.1 μA max	
Digital Input Capacitance, C <sub>IN</sub> 4 pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>	
Transition Time, $t_{\text{TRANSITION}}$ 150 ns typ $R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$	
182 230 258 ns max V <sub>s</sub> = 2.5 V; see Figure 28	
$t_{ON}$ (EN) 106 ns typ $R_L = 300 \Omega$ , $C_L = 35 pF$	
132 150 160 ns max V <sub>s</sub> = 2.5 V; see Figure 30	
$t_{OFF}$ (EN) 113 ns typ $R_L = 300 \Omega, C_L = 35 pF$	
144 178 202 ns max Vs = 2.5 V; see Figure 30	
Break-Before-Make Time Delay, t <sub>D</sub> 47 ns typ $R_L = 300 \Omega$ , $C_L = 35 pF$	
30 ns min $V_{S1} = V_{S2} = 2.5$ V; see Figure 29	
Charge Injection 24 pC typ $V_s = 0 V$ , $R_s = 0 \Omega$ , $C_L = 1 nF$ ; see Figure 31	
Off Isolation $-64$ dB typ $R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1$ MHz; see Figure 32	
Channel-to-Channel Crosstalk $-64$ dB typ $R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 34	
Total Harmonic Distortion + Noise (THD + N) 0.04 $\%$ typ $R_L = 110 \Omega$ , $V_S = 5 V p$ -p, $f = 20$ Hz to 20 kHz; see Figure 3	igure 35
-3 dB Bandwidth $R_L = 50 \Omega$ , $C_L = 5 pF$ ; see Figure 33	5
ADG1608 40 MHz typ	
ADG1609 71 MHz typ	
C <sub>s</sub> (Off) 20 $pF typ$ V <sub>s</sub> = 0 V, f = 1 MHz	
$C_{D}$ (Off)	
ADG1608 120 $pE typ V_s = 0 V_s f = 1 MHz$	
ADG1609 61 $pE typ V = 0 V f = 1 MHz$	
ADG1608 $153$ $pE typ V f = 1 MHz$	
ADG1609 85 PE typ V = 0 V = 1 MHz	
POWER REQUIREMENTS $V_{DD} = +5.5 V V_{CS} = -5.5 V$	
$l_{DD}$ 0.001 $\mu A typ$ Digital inputs = 0 V or V_{DD}	
$V_{DD}/V_{SS}$ $\pm 3.3/\pm 8$ V min/max	

<sup>1</sup> Guaranteed by design, but not subject to production test.

### **12 V SINGLE SUPPLY**

 $V_{\text{DD}}$  = 12 V  $\pm$  10%,  $V_{\text{SS}}$  = 0 V, GND = 0 V, unless otherwise noted.

#### Table 2.

Paramotor	25%	-40°C to -40°C to 25°C +85°C +125°C Unit Test Conditions/Co		Test Conditions/Comments	
	23 C	703 C	+125 C	onit	
Analog Signal Range			0 V to V <sub>DD</sub>	V	
On Resistance (R <sub>ON</sub> )	4			Ωtyp	$V_s = 0 V$ to 10 V, $I_s = -10 mA$ ; see Figure 25
	4.5	6.5	7.5	Ωmax	$V_{DD} = 10.8 \text{ V}, V_{SS} = 0 \text{ V}$
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.12			Ωtyp	$V_{s} = 10 V, I_{s} = -10 mA$
	0.25	0.3	0.35	Ωmax	
On-Resistance Flatness (R <sub>FLAT(ON)</sub> )	0.9			Ωtyp	$V_{s} = 0 V$ to 10 V, $I_{s} = -10 mA$
	1.2	1.6	1.9	Ωmax	
LEAKAGE CURRENTS					$V_{DD} = 13.2 \text{ V}, V_{SS} = 0 \text{ V}$
Source Off Leakage, I₅ (Off)	±0.02			nA typ	$V_{s} = 1 \text{ V}/10 \text{ V}, V_{D} = 10 \text{ V}/1 \text{ V};$ see Figure 26
	±0.1	±0.5	±3	nA max	
Drain Off Leakage, I <sub>D</sub> (Off)	±0.03			nA typ	$V_{s} = 1 \text{ V}/10 \text{ V}, V_{D} = 10 \text{ V}/1 \text{ V};$ see Figure 26
ADG1608	±0.15	±2	±14	nA max	
ADG1609	±0.15	±1	±7	nA max	
Channel On Leakage, I <sub>D</sub> , I <sub>S</sub> (On)	±0.03			nA typ	$V_s = V_D = 1 V$ or 10 V; see Figure 27
	±0.15	±2	±14	nA max	
DIGITAL INPUTS					
Input High Voltage, V <sub>INH</sub>			2.0	V min	
Input Low Voltage, VINL			0.8	V max	
Input Current, I <sub>INL</sub> or I <sub>INH</sub>	±1			nA typ	$V_{IN} = V_{GND} \text{ or } V_{DD}$
			±0.1	μA max	
Digital Input Capacitance, C <sub>IN</sub>	4			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
Transition Time, t <sub>TRANSITION</sub>	113			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	141	172	196	ns max	Vs = 8 V; see Figure 28
t <sub>on</sub> (EN)	80			ns typ	$R_L = 300 \Omega$ , $C_L = 35 pF$
	94	101	110	ns max	V <sub>s</sub> = 8 V; see Figure 30
t <sub>off</sub> (EN)	77			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	93	117	140	ns max	V <sub>s</sub> = 8 V; see Figure 30
Break-Before-Make Time Delay, t <sub>D</sub>	47			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
			30	ns min	$V_{S1} = V_{S2} = 8 V$ ; see Figure 29
Charge Injection	29			pC typ	$V_s = 6 V$ , $R_s = 0 \Omega$ , $C_L = 1 nF$ ; see Figure 31
Off Isolation	-64			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 32
Channel-to-Channel Crosstalk	-64			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 1 MHz$ ; see Figure 34
Total Harmonic Distortion + Noise (THD + N)	0.04			% typ	$R_L = 110 \Omega$ , $V_S = 5 V p$ -p, $f = 20 Hz$ to 20 kHz; see Figure 35
–3 dB Bandwidth					$R_L = 50 \Omega$ , $C_L = 5 pF$ ; see Figure 33
ADG1608	40			MHz typ	
ADG1609	78			MHz typ	
C <sub>s</sub> (Off)	19			pF typ	$V_s = 6 V$ , $f = 1 MHz$
C <sub>D</sub> (Off)					
ADG1608	117			pF typ	$V_s = 6 V$ , $f = 1 MHz$
ADG1609	59			pF typ	$V_{s} = 6 V, f = 1 MHz$
C <sub>D</sub> , C <sub>S</sub> (On)					
ADG1608	149			pF typ	$V_s = 6 V$ , $f = 1 MHz$
ADG1609	84			pF typ	$V_s = 6 V$ , $f = 1 MHz$
POWER REQUIREMENTS					V <sub>DD</sub> = 12 V
I <sub>DD</sub>	0.001			μA typ	Digital inputs = $0 V \text{ or } V_{DD}$
			1.0	µA max	
ADG1608	300			µA typ	Digital inputs = 5 V
			480	µA max	
ADG1609	225			µA typ	Digital inputs = 5 V
			360	µA max	
V <sub>DD</sub>			3.3/16	V min/max	

<sup>1</sup> Guaranteed by design, but not subject to production test.

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## **5 V SINGLE SUPPLY**

 $V_{\text{DD}}$  = 5 V  $\pm$  10%,  $V_{\text{SS}}$  = 0 V, GND = 0 V, unless otherwise noted.

### Table 3.

		–40°Cto	–40°C to		
Parameter	25°C	+85°C	+125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$0 V to V_{DD}$	V	
On Resistance (R <sub>ON</sub> )	8.5			Ωtyp	$V_s = 0 V$ to 4.5 V, $I_s = -10 mA$ ; see Figure 25
	10	12.5	14	Ωmax	$V_{DD} = 4.5 V, V_{SS} = 0 V$
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.15			Ωtyp	$V_s = 0 V$ to 4.5 V, $I_s = -10 mA$
	0.3	0.35	0.4	Ωmax	
On-Resistance Flatness (R <sub>FLAT(ON</sub> ))	1.7			Ωtyp	$V_s = 0 V$ to 4.5 V, $I_s = -10 mA$
	2.3	2.7	3	Ωmax	
LEAKAGE CURRENTS					$V_{DD} = 5.5 \text{ V}, V_{SS} = 0 \text{ V}$
Source Off Leakage, Is (Off)	±0.01			nA typ	$V_{\text{S}}$ = 1 V/4.5 V, $V_{\text{D}}$ = 4.5 V/1 V; see Figure 26
	±0.1	±0.5	±3	nA max	
Drain Off Leakage, I <sub>D</sub> (Off)	±0.01			nA typ	$V_{\text{S}}$ = 1 V/4.5 V, $V_{\text{D}}$ = 4.5 V/1 V; see Figure 26
ADG1608	±0.15	±2	±14	nA max	
ADG1609	±0.15	±1	±7	nA max	
Channel On Leakage, I <sub>D</sub> , I <sub>s</sub> (On)	±0.01			nA typ	$V_s = V_D = 1 V \text{ or } 4.5 V$ ; see Figure 27
	±0.15	±2	±14	nA max	
DIGITAL INPUTS					
Input High Voltage, VINH			2.0	V min	
Input Low Voltage, VINL			0.8	V max	
Input Current, IINL or IINH	±1			nA typ	$V_{IN} = V_{GND} \text{ or } V_{DD}$
			±0.1	µA max	
Digital Input Capacitance, C <sub>IN</sub>	4			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
Transition Time, transition	193			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	251	301	339	ns max	$V_s = 2.5 V$ ; see Figure 28
t <sub>on</sub> (EN)	115			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	152	171	184	ns max	$V_s = 2.5 V$ ; see Figure 30
t <sub>off</sub> (EN)	140			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	184	225	259	ns max	$V_s = 2.5 V$ ; see Figure 30
Break-Before-Make Time Delay, t <sub>D</sub>	66			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
			37	ns min	$V_{S1} = V_{S2} = 2.5 V$ ; see Figure 29
Charge Injection	11			pC typ	$V_s = 2.5 V$ , $R_s = 0 \Omega$ , $C_L = 1 nF$ ; see Figure 31
Off Isolation	-64			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 100 kHz$ ; see Figure 32
Channel-to-Channel Crosstalk	-64			dB typ	$R_{L} = 50 \Omega, C_{L} = 5 pF, f = 100 kHz; see Figure 34$
Total Harmonic Distortion + Noise (THD + N)	0.3			% typ	$R_{L} = 110 \Omega$ , f = 20 Hz to 20 kHz, V <sub>5</sub> = 3.5 V p-p; see Figure 35
–3 dB Bandwidth					$R_L = 50 \Omega$ , $C_L = 5 pF$ ; see Figure 33
ADG1608	37			MHz typ	
ADG1609	72			MHz typ	
Cs (Off)	22			pF typ	$V_{s} = 2.5 V_{s} f = 1 MHz$
$C_{\rm D}$ (Off)				F. 9F	$V_s = 2.5 V_s f = 1 MHz$
ADG1608	136			pF typ	
ADG1609	68			pF typ	
$C_{D}$ , $C_{S}$ (On)				1 91	$V_{s} = 2.5 V_{s} f = 1 MHz$
ADG1608	168			pF typ	
ADG1609	94			pF typ	
POWER REOUIREMENTS				17° 77°	V <sub>DD</sub> = 5.5 V
DD	0.001			uA typ	Digital inputs = $0 V \text{ or } V_{DD}$
			1.0	µA max	
V <sub>DD</sub>			3.3/16	V min/max	
			-		1

<sup>1</sup> Guaranteed by design, but not subject to production test.

### **3.3 V SINGLE SUPPLY**

 $V_{\text{DD}}$  = 3.3 V,  $V_{\text{SS}}$  = 0 V, GND = 0 V, unless otherwise noted.

### Table 4.

		–40°C to	–40°C to		
Parameter	25°C	+85°C	+125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$0 V to V_{DD}$	V	
On Resistance (R <sub>on</sub> )	13.5	15	16.5	Ωtyp	$V_{S}$ = 0 V to $V_{DD},$ $I_{S}$ = $-10$ mA; see Figure 25, $V_{DD}$ = 3.3 V, $V_{SS}$ = 0 V
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.25	0.28	0.3	Ωtyp	$V_s = 0 V$ to $V_{DD}$ , $I_s = -10 \text{ mA}$
On-Resistance Flatness (R <sub>FLAT(ON)</sub> )	5	5.5	6.5	Ωtyp	$V_s = 0$ V to $V_{DD}$ , $I_s = -10$ mA
LEAKAGE CURRENTS					$V_{DD} = 3.6 V, V_{SS} = 0 V$
Source Off Leakage, I <sub>s</sub> (Off)	±0.01			nA typ	$V_{s} = 0.6 \text{ V/3 V}, V_{D} = 3 \text{ V/0.6 V};$ see Figure 26
	±0.1	±0.5	±3	nA max	
Drain Off Leakage, $I_D$ (Off)	±0.01			nA typ	$V_{s} = 0.6 \text{ V/3 V}, V_{D} = 3 \text{ V/0.6 V};$ see Figure 26
ADG1608	±0.15	±2	±14	nA max	
ADG1609	±0.15	±1	±7	nA max	
Channel On Leakage, I <sub>D</sub> , I <sub>s</sub> (On)	±0.01			nA typ	$V_s = V_D = 0.6 V$ or 3 V; see Figure 27
	±0.15	±2	±14	nA max	
DIGITAL INPUTS					
Input High Voltage, V <sub>INH</sub>			2.0	V min	
Input Low Voltage, VINL			0.8	V max	
Input Current, I <sub>INL</sub> or I <sub>INH</sub>	±1			nA typ	$V_{IN} = V_{GND} \text{ or } V_{DD}$
			±0.1	μA max	
Digital Input Capacitance, C <sub>IN</sub>	4			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
Transition Time, transition	312			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	437	498	542	ns max	V <sub>s</sub> = 1.5 V; see Figure 28
t <sub>on</sub> (EN)	216			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	309	331	344	ns max	V <sub>s</sub> = 1.5 V; see Figure 30
t <sub>OFF</sub> (EN)	236			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
	316	367	411	ns max	V <sub>s</sub> = 1.5 V; see Figure 30
Break-Before-Make Time Delay, t <sub>D</sub>	104			ns typ	$R_L = 300 \Omega, C_L = 35 pF$
			48	ns min	$V_{S1} = V_{S2} = 1.5 V$ ; see Figure 29
Charge Injection	6			pC typ	$V_s$ = 1.5 V, $R_s$ = 0 $\Omega$ , $C_L$ = 1 nF; see Figure 31
Off Isolation	-64			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 100 kHz$ ; see Figure 32
Channel-to-Channel Crosstalk	-64			dB typ	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $f = 100 kHz$ ; see Figure 34
Total Harmonic Distortion + Noise (THD + N)	0.5			% typ	$R_L = 110 \Omega$ , f = 20 Hz to 20 kHz, V <sub>S</sub> = 2 V p-p; see Figure 35
–3 dB Bandwidth					$R_L = 50 \Omega$ , $C_L = 5 pF$ ; see Figure 33
ADG1608	34			MHz typ	
ADG1609	72			MHz typ	
Cs (Off)	23			pF typ	$V_{s} = 1.5 V, f = 1 MHz$
C <sub>D</sub> (Off)					$V_s = 1.5 V, f = 1 MHz$
ADG1608	145			pF typ	
ADG1609	72			pF typ	
C <sub>D</sub> , C <sub>s</sub> (On)					$V_{s} = 1.5 V, f = 1 MHz$
ADG1608	173			pF typ	
ADG1609	95			pF typ	
POWER REQUIREMENTS					$V_{DD} = 3.6 V$
lod	0.001			μA typ	Digital inputs = $0 \text{ V or } V_{DD}$
			1.0	μA max	
V <sub>DD</sub>			3.3/16	V min/max	

<sup>1</sup> Guaranteed by design, but not subject to production test.

## **CONTINUOUS CURRENT PER CHANNEL, S OR D**

### Table 5. ADG1608

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
$V_{DD} = +5 V, V_{SS} = -5 V$				
TSSOP ( $\theta_{JA} = 112.6^{\circ}C/W$ )	290	180	100	mA max
LFCSP ( $\theta_{JA} = 48.7^{\circ}C/W$ )	470	255	120	mA max
$V_{DD} = 12 V, V_{SS} = 0 V$				
TSSOP ( $\theta_{JA} = 112.6^{\circ}C/W$ )	213	129	73	mA max
LFCSP ( $\theta_{JA} = 48.7^{\circ}C/W$ )	346	185	84	mA max
$V_{DD} = 5 \text{ V}, \text{ V}_{SS} = 0 \text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^{\circ}C/W$ )	157	101	63	mA max
LFCSP ( $\theta_{JA} = 48.7^{\circ}C/W$ )	252	150	77	mA max
$V_{DD} = 3.3 \text{ V}, V_{SS} = 0 \text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^{\circ}C/W$ )	126	87	56	mA max
LFCSP ( $\theta_{JA} = 48.7^{\circ}$ C/W)	206	129	73.5	mA max

### Table 6. ADG1609

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
$V_{DD} = +5 V, V_{SS} = -5 V$				
TSSOP ( $\theta_{JA} = 112.6^{\circ}C/W$ )	147	98	63	mA max
LFCSP ( $\theta_{JA} = 48.7^{\circ}C/W$ )	245	147	77	mA max
$V_{DD} = 12 V, V_{SS} = 0 V$				
TSSOP ( $\theta_{JA} = 112.6^{\circ}C/W$ )	157	101	63	mA max
LFCSP ( $\theta_{JA} = 48.7^{\circ}$ C/W)	255	150	77	mA max
$V_{DD} = 5 \text{ V}, \text{ V}_{SS} = 0 \text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^{\circ}C/W$ )	115	80	52	mA max
LFCSP ( $\theta_{JA} = 48.7^{\circ}$ C/W)	189	119	70	mA max
$V_{DD} = 3.3 V, V_{SS} = 0 V$				
TSSOP ( $\theta_{JA} = 112.6^{\circ}C/W$ )	94	66	45	mA max
LFCSP ( $\theta_{JA} = 48.7^{\circ}C/W$ )	154	101	63	mA max

## **ABSOLUTE MAXIMUM RATINGS**

 $T_A = 25^{\circ}C$ , unless otherwise noted.

#### Table 7.

Parameter	Rating
V <sub>DD</sub> to V <sub>SS</sub>	18 V
V <sub>DD</sub> to GND	–0.3 V to +18 V
Vss to GND	+0.3 V to -18 V
Analog Inputs <sup>1</sup>	V <sub>ss</sub> – 0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND – 0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	710 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D <sup>2</sup>	Data + 15%
Operating Temperature Range	
Industrial	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θJA Thermal Impedance, 0 Airflow (4-Layer Board)	112.6°C/W
16-Lead LFCSP, θJA Thermal Impedance, 0 Airflow (4-Layer Board)	48.7°C/W
Reflow Soldering Peak Temperature, Pb-free	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### **ESD CAUTION**



**ESD** (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

<sup>2</sup> See Table 5 and Table 6.

## **PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS**



#### Table 8. ADG1608 Pin Function Descriptions

Pin	No.		
TSSOP	LFCSP	Mnemonic	Description
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, Ax logic inputs determine on switches.
3	1	Vss	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	2	S1	Source Terminal 1. Can be an input or an output.
5	3	S2	Source Terminal 2. Can be an input or an output.
6	4	S3	Source Terminal 3. Can be an input or an output.
7	5	S4	Source Terminal 4. Can be an input or an output.
8	6	D	Drain Terminal. Can be an input or an output.
9	7	S8	Source Terminal 8. Can be an input or an output.
10	8	S7	Source Terminal 7. Can be an input or an output.
11	9	S6	Source Terminal 6. Can be an input or an output.
12	10	S5	Source Terminal 5. Can be an input or an output.
13	11	V <sub>DD</sub>	Most Positive Power Supply Potential.
14	12	GND	Ground (0 V) Reference.
15	13	A2	Logic Control Input.
16	14	A1	Logic Control Input.
N/A	EP	EP	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, Vss.

#### Table 9. ADG1608 Truth Table

A2	A1	AO	EN	On Switch
X <sup>1</sup>	X <sup>1</sup>	X <sup>1</sup>	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

<sup>1</sup> X = don't care.



Pin No.					
TSSOP	LFCSP	Mnemonic	Description		
1	15	A0	Logic Control Input.		
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, Ax logic inputs determine on switches.		
3	1	Vss	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.		
4	2	S1A	Source Terminal 1A. Can be an input or an output.		
5	3	S2A	Source Terminal 2A. Can be an input or an output.		
6	4	S3A	Source Terminal 3A. Can be an input or an output.		
7	5	S4A	Source Terminal 4A. Can be an input or an output.		
8	6	DA	Drain Terminal A. Can be an input or an output.		
9	7	DB	Drain Terminal B. Can be an input or an output.		
10	8	S4B	Source Terminal 4B. Can be an input or an output.		
11	9	S3B	Source Terminal 3B. Can be an input or an output.		
12	10	S2B	Source Terminal 2B. Can be an input or an output.		
13	11	S1B	Source Terminal 1B. Can be an input or an output.		
14	12	V <sub>DD</sub>	Most Positive Power Supply Potential.		
15	13	GND	Ground (0 V) Reference.		
16	14	A1	Logic Control Input.		
N/A	EP	EP	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, Vss.		

#### Table 11. ADG1609 Truth Table

A1	A0	EN	On Switch Pair
X <sup>1</sup>	X <sup>1</sup>	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

<sup>1</sup> X = don't care.

## **TYPICAL PERFORMANCE CHARACTERISTICS**



Figure 7. On Resistance vs. V<sub>D</sub> (V<sub>s</sub>) for Dual Supply



Figure 8. On Resistance vs. V<sub>D</sub> (V<sub>s</sub>) for Single Supply



Figure 9. On Resistance vs.  $V_{\rm D}$  (Vs) for Different Temperatures,  $\pm 5$  V Dual Supply



Figure 10. On Resistance vs. V\_D (Vs) for Different Temperatures, 12 V Single Supply



Figure 11. On Resistance vs.  $V_D$  (Vs) for Different Temperatures, 5 V Single Supply



Figure 12. On Resistance vs.  $V_D$  ( $V_s$ ) for Different Temperatures, 3.3 V Single Supply

08318-018

08318-019

08318-026



#### 450 T<sub>A</sub> = 25°C 400 350 TRANSITION TIME (ns) $V_{DD} = +3.3V, V_{SS} = 0V$ 300 250 200 /<sub>DD</sub> = +5V, V<sub>SS</sub> = 0V 150 100 $V_{DD} = +5V, V_{SS} = -5V$ 50 12V, $V_{SS}$ ov DD/ 0 └─ -40 -20 0 20 40 60 80 100 120 08318-024 TEMPERATURE (°C) Figure 19. Transition Time vs. Temperature













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## **TEST CIRCUITS**



\*SIMILAR CONNECTION FOR ADG1609.

Figure 29. Break-Before-Make Delay, tBBM

## **Data Sheet**

# ADG1608/ADG1609



Figure 31. Charge Injection



Figure 32. Off Isolation



Figure 33. Bandwidth



Figure 34. Channel-to-Channel Crosstalk



Figure 35. THD + Noise

## TERMINOLOGY

Idd

The positive supply current.

Iss

The negative supply current.

 $V_D$  (Vs) The analog voltage on Terminal D and Terminal S.

 $\mathbf{R}_{ON}$ The ohmic resistance between Terminal D and Terminal S.

 $\mathbf{R}_{\text{FLAT(ON)}}$ Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

Is (Off) The source leakage current with the switch off.

 $\mathbf{I}_{\mathrm{D}}$  (Off) The drain leakage current with the switch off.

 $\mathbf{I}_{D}, \mathbf{I}_{S}\left(\mathbf{On}\right)$  The channel leakage current with the switch on.

 $\mathbf{V}_{\text{INL}}$  The maximum input voltage for Logic 0.

 $\mathbf{V}_{\text{INH}}$ The minimum input voltage for Logic 1.

I<sub>INL</sub> (I<sub>INH</sub>) The input current of the digital input.

Cs (Off) The off switch source capacitance, which is measured with reference to ground.

 $C_D$  (Off) The off switch drain capacitance, which is measured with reference to ground.

 $C_D$ ,  $C_S$  (On) The on switch capacitance, which is measured with reference to ground.

# ADG1608/ADG1609

### Cin

The digital input capacitance.

**t**<sub>TRANSITION</sub>

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

 $t_{ON}$  (EN) The delay between applying the digital control input and the output switching on.

 $t_{\text{OFF}} \left( EN \right)$  The delay between applying the digital control input and the output switching off.

**Charge Injection** A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**Off Isolation** A measure of unwanted signal coupling through an off switch.

### Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

**Bandwidth** The frequency at which the output is attenuated by 3 dB.

**On Response** The frequency response of the on switch.

**Insertion Loss** The loss due to the on resistance of the switch.

**Total Harmonic Distortion + Noise (THD + N)** The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

**Data Sheet** 

## **OUTLINE DIMENSIONS**



### **ORDERING GUIDE**

			Package	
Model <sup>1</sup>	Temperature Range	Package Description	Option	Branding
ADG1608BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1608BRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1608BCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	S38
ADG1609BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1609BRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1609BCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	S39

 $^{1}$  Z = RoHS Compliant Part.

# NOTES

## NOTES

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