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3/2017—Rev. C to Rev. D

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5/2007—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, V_{REF} = 2.5 V, G = 1, R_L = 10 kΩ, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER					
Offset Voltage	V_{OS} RTI = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}			4	15	µV
Average Temperature Drift	T_A = −40°C to +125°C		0.01	0.05	µV/°C
Output Offset, V_{OSO}			15	30	µV
Average Temperature Drift	T_A = −40°C to +125°C		0.05	0.5	µV/°C
Input Currents					
Input Bias Current			250	500	pA
	T_A = −40°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −40°C to +125°C			0.5	nA
Gains	1, 2, 4, 8, 16, 32, 64, or 128				
Gain Error					
G = 1				0.05	%
G = 2 to 128				0.8	%
Gain Drift	T_A = −40°C to +125°C				
G = 1 to 32			3	10	ppm/°C
G = 64			4	20	ppm/°C
G = 128			10	30	ppm/°C
Linearity	0.2 V to 4.8 V, 10 kΩ load		3		ppm
	0.2 V to 4.8 V, 2 kΩ load		5		ppm
CMRR					
G = 1		80			dB
G = 2		86			dB
G = 4		92			dB
G = 8		98			dB
G = 16		104			dB
G = 32		110			dB
G = 64		110			dB
G = 128		110			dB
Noise	$e_n = \sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$, V_{IN+}, V_{IN-} = 2.5 V				
Input Voltage Noise, e_{ni}	f = 1 kHz		32		nV/√Hz
	f = 1 kHz, T_A = −40°C		27		nV/√Hz
	f = 1 kHz, T_A = 125°C		39		nV/√Hz
	f = 0.1 Hz to 10 Hz		0.7		µV p-p
Output Voltage Noise, e_{no}	f = 1 kHz		58		nV/√Hz
	f = 1 kHz, T_A = −40°C		50		nV/√Hz
	f = 1 kHz, T_A = 125°C		70		nV/√Hz
	f = 0.1 Hz to 10 Hz		1.1		µV p-p
Current Noise	f = 10 Hz		20		fA/√Hz
Other Input Characteristics					
Common-Mode Input Impedance			10‖5		GΩ‖pF
Power Supply Rejection Ratio		100	115		dB
Input Operating Voltage Range		0.05		4.95	V
Reference Input					
Input Impedance			28		kΩ
Voltage Range		−0.2		+5.2	V

Parameter	Conditions	Min	Typ	Max	Unit
Dynamic Performance					
Bandwidth					
G = 1			2.7		MHz
G = 2			2.5		MHz
Gain Bandwidth Product					
G = 4 to 128			7		MHz
Slew Rate			1.1		V/µs
Output Characteristics					
Output Voltage High	R_L = 100 kΩ to ground	4.9	4.94		V
	R_L = 10 kΩ to ground	4.8	4.88		V
Output Voltage Low	R_L = 100 kΩ to 5 V		60	100	mV
	R_L = 10 kΩ to 5 V		80	200	mV
Short-Circuit Current			70		mA
Digital Interface					
Input Voltage Low	T_A = −40°C to +125°C			1.0	V
Input Voltage High	T_A = −40°C to +125°C	4.0			V
Setup Time to $\overline{CS}$ High	T_A = −40°C to +125°C	50			ns
Hold Time after $\overline{CS}$ High	T_A = −40°C to +125°C	20			ns
OPERATIONAL AMPLIFIER					
Input Characteristics					
Offset Voltage, V_{OS}			5	15	µV
Temperature Drift	T_A = −40°C to +125°C		0.01	0.06	µV/°C
Input Bias Current			250	500	pA
	T_A = −40°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −40°C to +125°C			0.5	nA
Input Voltage Range		0.05		4.95	V
Open-Loop Gain		100	120		V/mV
Common-Mode Rejection Ratio		100	120		dB
Power Supply Rejection Ratio		100	110		dB
Voltage Noise Density			20		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		0.4		µV p-p
Dynamic Performance					
Gain Bandwidth Product			1		MHz
Slew Rate			0.5		V/µs
Output Characteristics					
Output Voltage High	R_L = 100 kΩ to ground	4.9	4.96		V
	R_L = 10 kΩ to ground	4.8	4.92		V
Output Voltage Low	R_L = 100 kΩ to 5 V		60	100	mV
	R_L = 10 kΩ to 5 V		80	200	mV
Short-Circuit Current			70		mA
BOTH AMPLIFIERS					
Power Supply					
Quiescent Current			4	5	mA
Quiescent Current (Shutdown)			0.01	1	µA

V_S = 3.0 V, V_{REF} = 1.5 V, T_A = 25°C, G = 1, R_L = 10 kΩ, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER					
Offset Voltage	V_{OS} RTI = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}			4	15	µV
Average Temperature Drift			0.01	0.05	µV/°C
Output Offset, V_{OSO}			15	30	µV
Average Temperature Drift			0.05	0.5	µV/°C
Input Currents					
Input Bias Current			250	500	pA
	T_A = −40°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −40°C to +125°C			0.5	nA
Gains	1, 2, 4, 8, 16, 32, 64, or 128				
Gain Error					
G = 1				0.05	%
G = 2 to 128				0.8	%
Gain Drift	T_A = −40°C to +125°C				
G = 1 to 32			3	10	ppm/°C
G = 64			4	20	ppm/°C
G = 128			10	30	ppm/°C
CMRR					
G = 1		80			dB
G = 2		86			dB
G = 4		92			dB
G = 8		98			dB
G = 16		104			dB
G = 32		110			dB
G = 64		110			dB
G = 128		110			dB
Noise	$e_n = \sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$ V_{IN+}, V_{IN-} = 2.5 V, T_A = 25°C				
Input Voltage Noise, e_{ni}	f = 1 kHz		40		nV/√Hz
	f = 1 kHz, T_A = −40°C		35		nV/√Hz
	f = 1 kHz, T_A = 125°C		48		nV/√Hz
	f = 0.1 Hz to 10 Hz		0.8		µV p-p
Output Voltage Noise, e_{no}	f = 1 kHz		72		nV/√Hz
	f = 1 kHz, T_A = −40°C		62		nV/√Hz
	f = 1 kHz, T_A = 125°C		83		nV/√Hz
	f = 0.1 Hz to 10 Hz		1.4		µV p-p
Current Noise	f = 10 Hz		20		fA/√Hz
Other Input Characteristics					
Common-Mode Input Impedance			10‖5		GΩ‖pF
Power Supply Rejection Ratio		100	115		dB
Input Operating Voltage Range		0.05		2.95	V
Reference Input					
Input Impedance			28		kΩ‖pF
Voltage Range		−0.2		+3.2	V

Parameter	Conditions	Min	Typ	Max	Unit
Dynamic Performance					
Bandwidth					
G = 1			2.7		MHz
G = 2			2.5		MHz
Gain Bandwidth Product					
G = 4 to 128			7		MHz
Slew Rate			1.1		V/µs
Output Characteristics					
Output Voltage High	R_L = 100 kΩ to ground	2.9	2.94		V
	R_L = 10 kΩ to ground	2.8	2.88		V
Output Voltage Low	R_L = 100 kΩ to 3 V		60	100	mV
	R_L = 10 kΩ to 3 V		80	200	mV
Short-Circuit Current			40		mA
Digital Interface					
Input Voltage Low	T_A = −40°C to +125°C			0.7	V
Input Voltage High	T_A = −40°C to +125°C	2.3			V
Setup Time to $\overline{CS}$ High	T_A = −40°C to +125°C	60			ns
Hold Time after $\overline{CS}$ High	T_A = −40°C to +125°C	20			ns
OPERATIONAL AMPLIFIERS					
Input Characteristics					
Offset Voltage, V_{OS}			5	15	µV
Temperature Drift	T_A = −40°C to +125°C		0.01	0.06	µV/°C
Input Bias Current			250	500	pA
	T_A = −40°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −40°C to +125°C			0.5	nA
Input Voltage Range		0.05		2.95	V
Open-Loop Gain		100	120		V/mV
Common-Mode Rejection Ratio		100	120		dB
Power Supply Rejection Ratio		100	110		dB
Voltage Noise Density			27		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		0.6		µV p-p
Dynamic Performance					
Gain Bandwidth Product			1		MHz
Slew Rate			0.5		V/µs
Output Characteristics					
Output Voltage High	R_L = 100 kΩ to ground	2.9	2.96		V
	R_L = 10 kΩ to ground	2.8	2.82		V
Output Voltage Low	R_L = 100 kΩ to 3 V		60	100	mV
	R_L = 10 kΩ to 3 V		80	200	mV
Short-Circuit Current			40		mA
BOTH AMPLIFIERS					
Power Supply					
Quiescent Current			3.5	4.5	mA
Quiescent Current (Shutdown)			0.01	1	µA

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Output Short-Circuit Current	Indefinite[1]
Input Voltage (Common-Mode)	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Differential Input Voltage	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Storage Temperature Range	−65°C to +150°C
Operational Temperature Range	−40°C to +125°C
Package Glass Transition Temperature	130°C
ESD (Human Body Model)	1.5 kV
ESD (Charged Device Model)	1.5 kV
ESD (Machine Model)	0.2 kV

[1] For junction temperatures between 105°C and 130°C, short-circuit operation beyond 1000 hours can impact part reliability.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5.

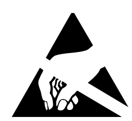
Thermal Pad	θ_{JA}	Unit
Soldered to Board	54	°C/W
Not Soldered to Board	96	°C/W

The θ_{JA} values in Table 5 assume a 4-layer JEDEC standard board. If the thermal pad is soldered to the board, it is also assumed it is connected to a plane. θ_{JC} at the exposed pad is 6.3°C/W.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8231 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 130°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 130°C for an extended period can result in a loss of functionality.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

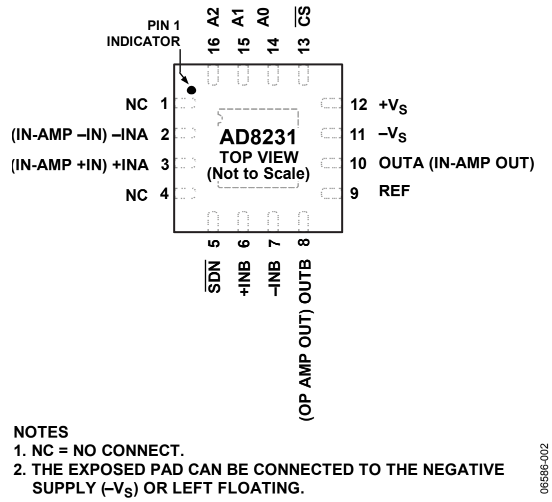


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	NC	No Connect.
2	−INA (IN-AMP −IN)	Instrumentation Amplifier Negative Input.
3	+INA (IN-AMP +IN)	Instrumentation Amplifier Positive Input.
4	NC	No Connect.
5	$\overline{\text{SDN}}$	Shutdown.
6	+INB	Operational Amplifier Positive Input.
7	−INB	Operational Amplifier Negative Input.
8	OUTB (OP AMP OUT)	Operational Amplifier Output.
9	REF	Instrumentation Amplifier Reference Pin. It should be driven with a low impedance. Output is referred to this pin.
10	OUTA (IN-AMP OUT)	Instrumentation Amplifier Output.
11	$-V_S$	Negative Power Supply. Connect to ground in single-supply applications.
12	$+V_S$	Positive Power Supply.
13	$\overline{\text{CS}}$	Chip Select. Enables digital logic interface.
14	A0	Gain Setting Bit (LSB).
15	A1	Gain Setting Bit.
16	A2	Gain Setting Bit (MSB).
	EPAD	Exposed Pad. Can be connected to the negative supply ($-V_S$) or left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

INSTRUMENTATION AMPLIFIER PERFORMANCE CURVES

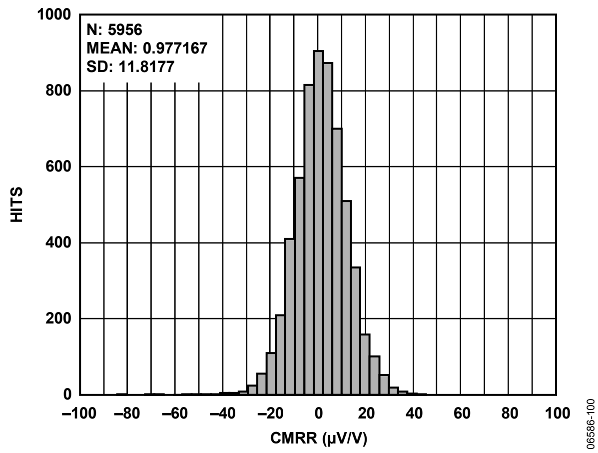


Figure 3. Instrumentation Amplifier CMR Distribution, G = 1

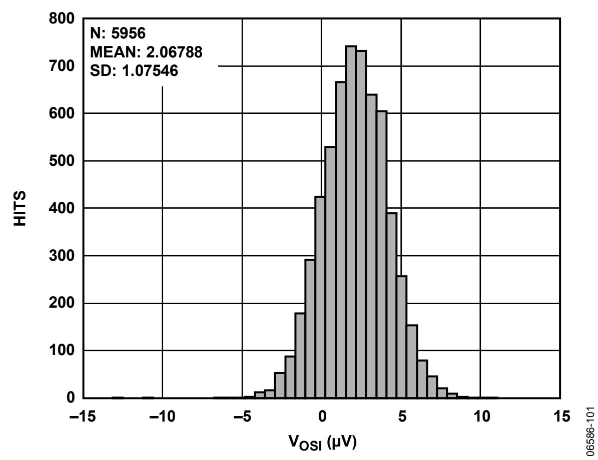


Figure 4. Instrumentation Amplifier Input Offset Voltage Distribution

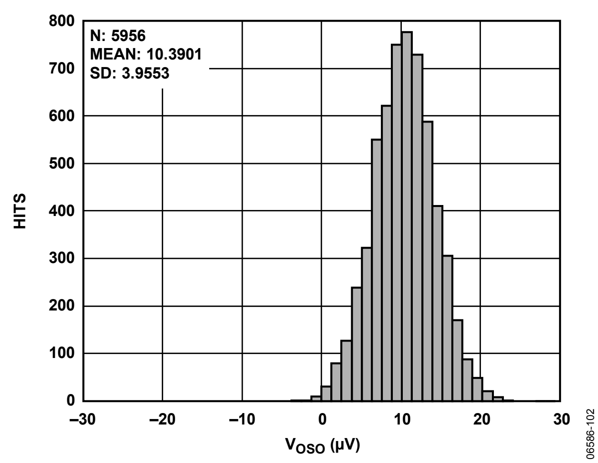


Figure 5. Instrumentation Amplifier Output Offset Voltage Distribution

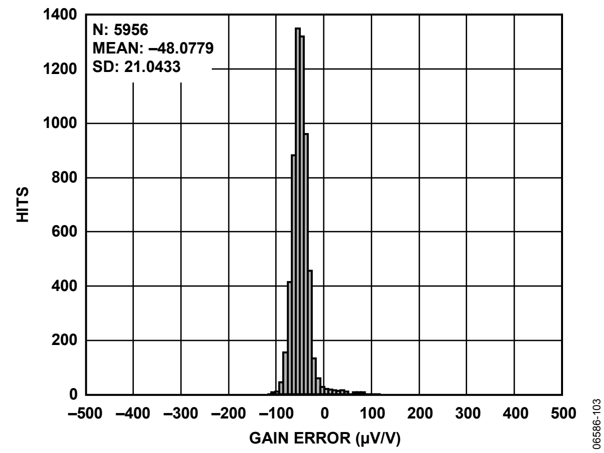


Figure 6. Instrumentation Amplifier Gain Distribution, G = 1

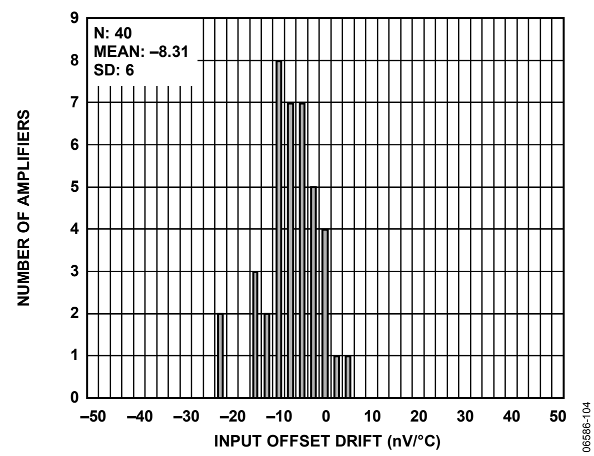


Figure 7. Instrumentation Amplifier Input Offset Voltage Drift, −40°C to +125°C

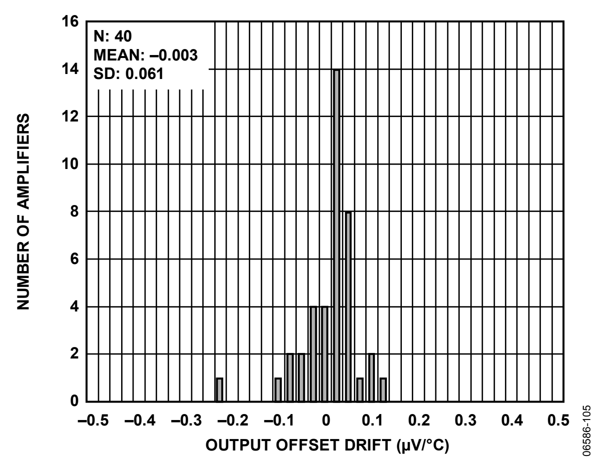


Figure 8. Instrumentation Amplifier Output Offset Drift, −40°C to +125°C

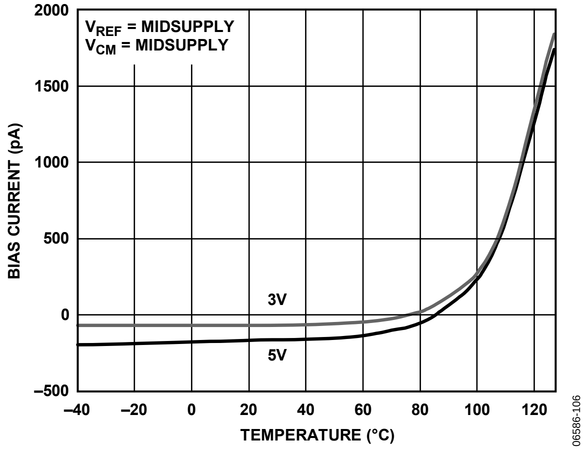


Figure 9. Instrumentation Amplifier Bias Current vs. Temperature

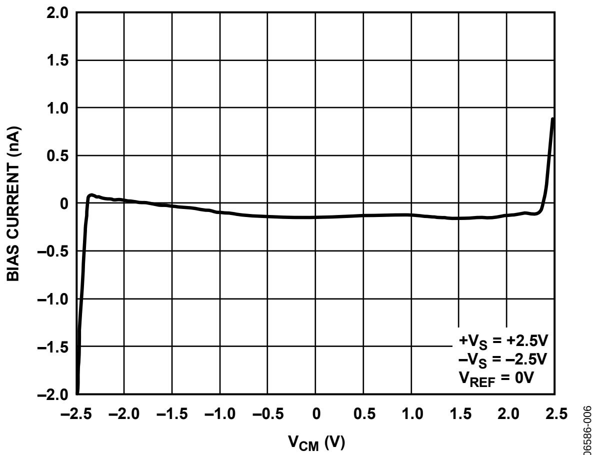


Figure 10. Instrumentation Amplifier Bias Current vs. Common-Mode Voltage, 5 V

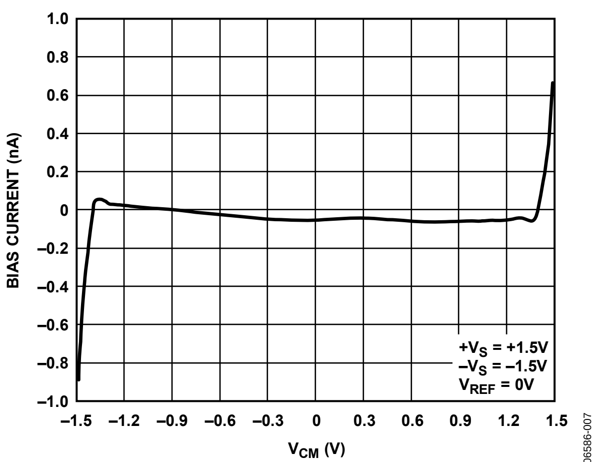


Figure 11. Instrumentation Amplifier Bias Current vs. Common-Mode Voltage, 3 V

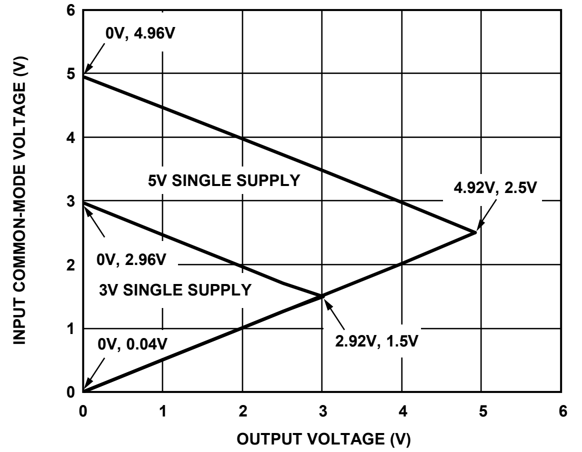


Figure 12. Instrumentation Amplifier Input Common-Mode Range vs. Output Voltage, All Gains, $V_{REF} = 0$ V

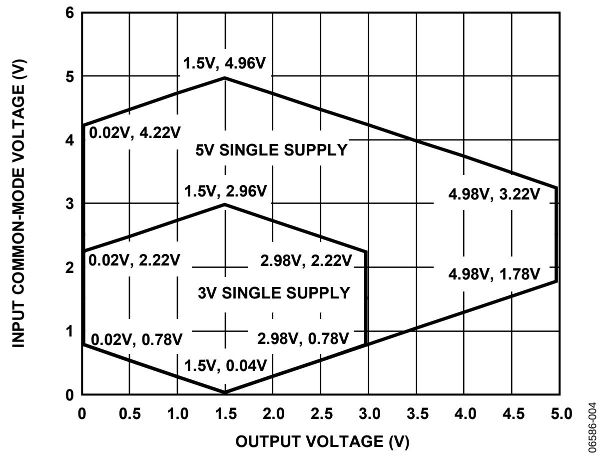


Figure 13. Instrumentation Amplifier Input Common-Mode Range vs. Output Voltage, All Gains, $V_{REF} = 1.5$ V

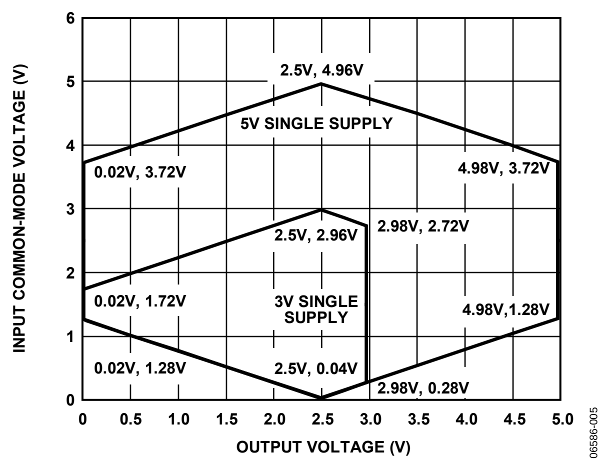


Figure 14. Instrumentation Amplifier Input Common-Mode Range vs. Output Voltage, All Gains, $V_{REF} = 2.5$ V

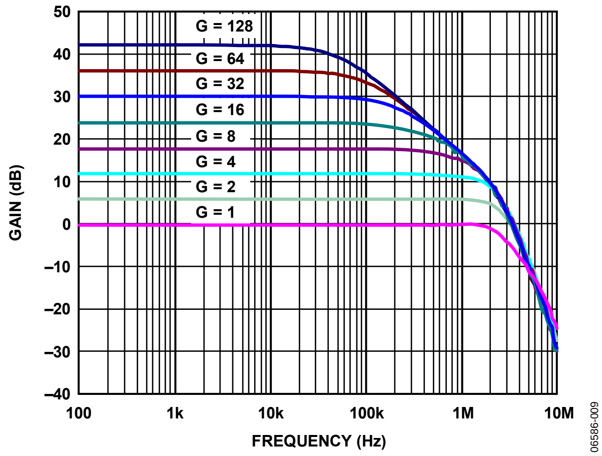


Figure 15. Instrumentation Amplifier Gain vs. Frequency

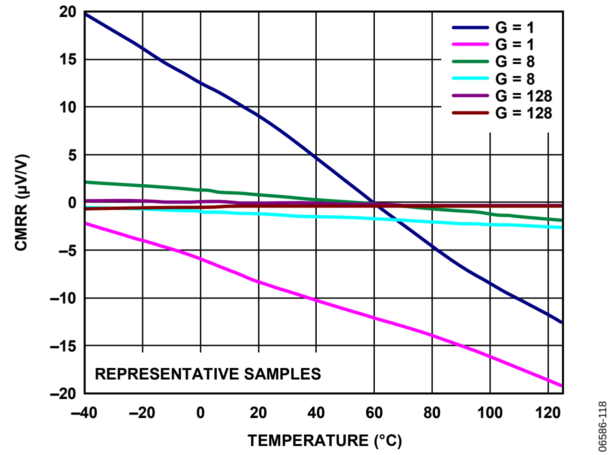


Figure 18. Instrumentation Amplifier CMRR vs. Temperature

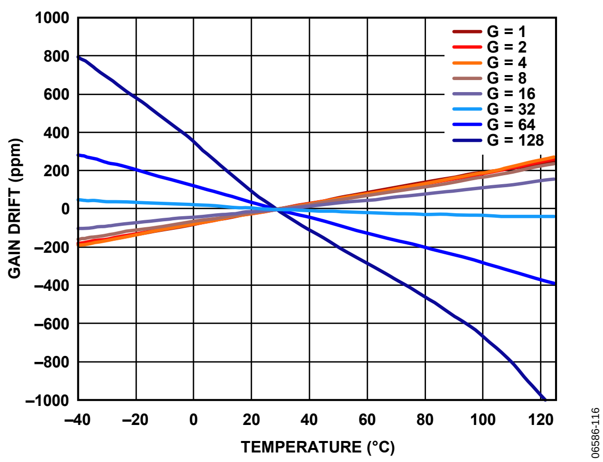


Figure 16. Instrumentation Amplifier Gain Drift vs. Temperature

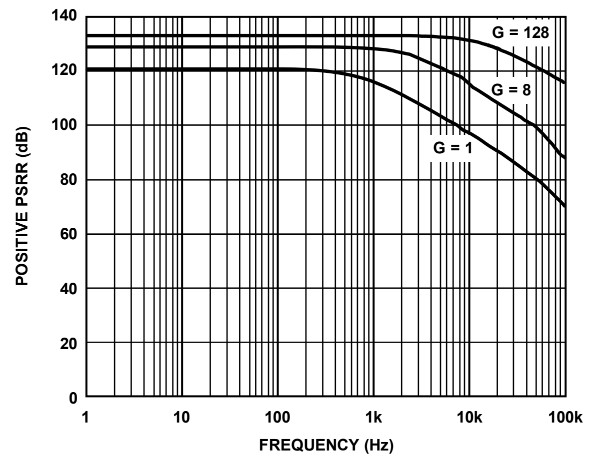


Figure 19. Instrumentation Amplifier Positive PSRR vs. Frequency

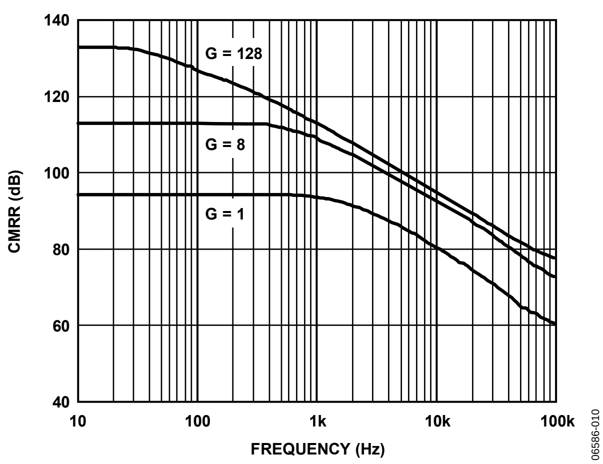


Figure 17. Instrumentation Amplifier CMRR vs. Frequency

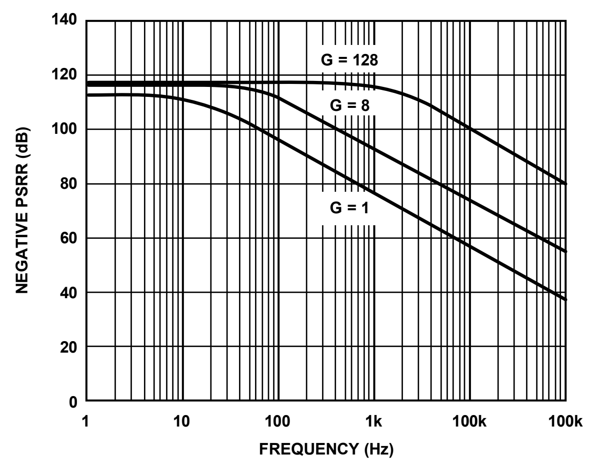


Figure 20. Instrumentation Amplifier Negative PSRR vs. Frequency

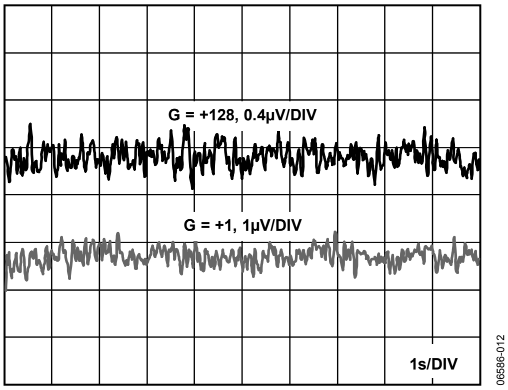


Figure 21. Instrumentation Amplifier 0.1 Hz to 10 Hz Noise

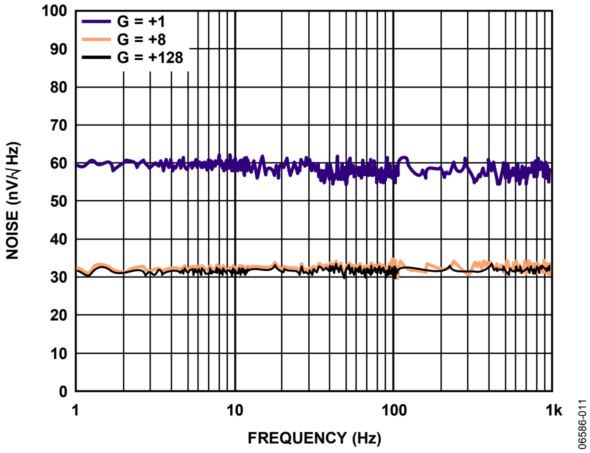


Figure 22. Instrumentation Amplifier Voltage Noise Spectral Density vs. Frequency, 5 V, 1 Hz to 1000 Hz

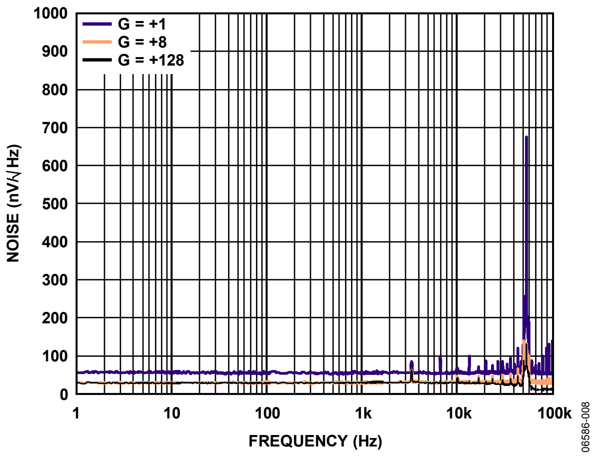


Figure 23. Instrumentation Amplifier Voltage Noise Spectral Density vs. Frequency, 5 V, 1 Hz to 1 MHz

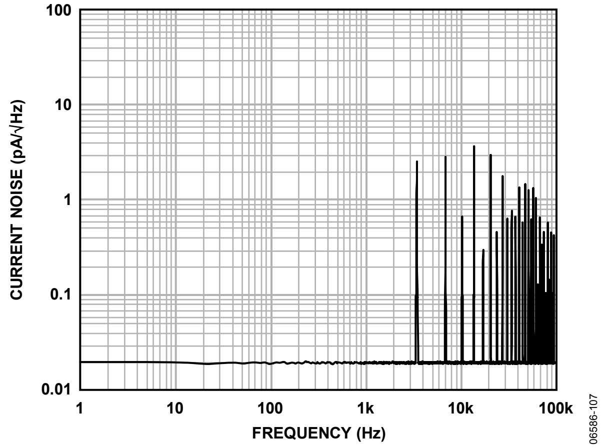


Figure 24. Instrumentation Amplifier Current Noise Spectral Density

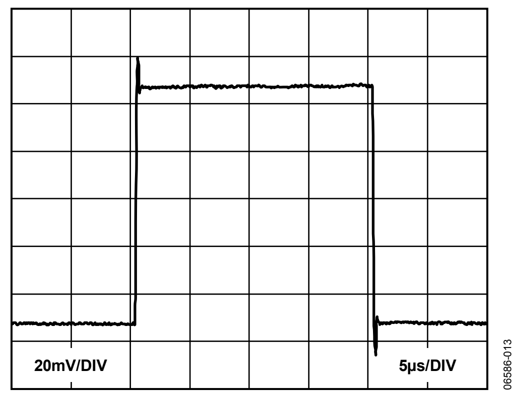


Figure 25. Instrumentation Amplifier Small Signal Pulse Response, G = 1, R_L = 2 kΩ, C_L = 500 pF

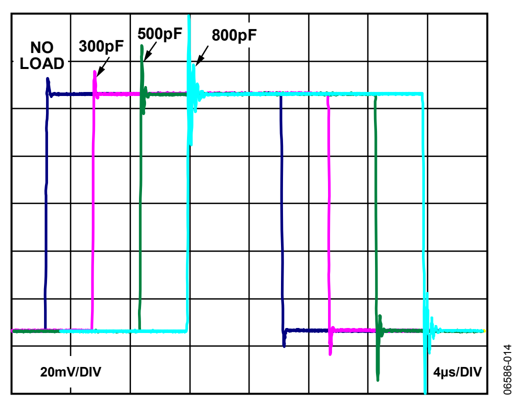


Figure 26. Instrumentation Amplifier Small Signal Pulse Response for Various Capacitive Loads, G = 1

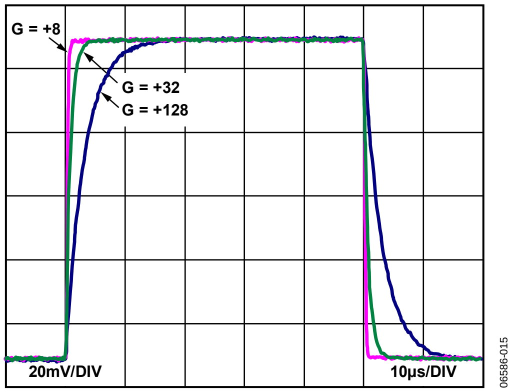


Figure 27. Instrumentation Amplifier Small Signal Pulse Response, G = 4, 16, and 128, R_L = 2 kΩ, C_L = 500 pF

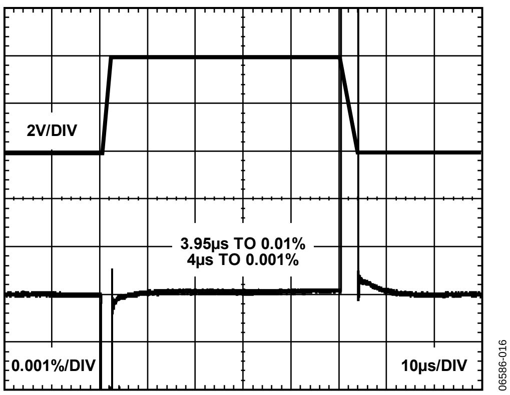


Figure 28. Instrumentation Amplifier Large Signal Pulse Response, G = 1, V_S = 5 V

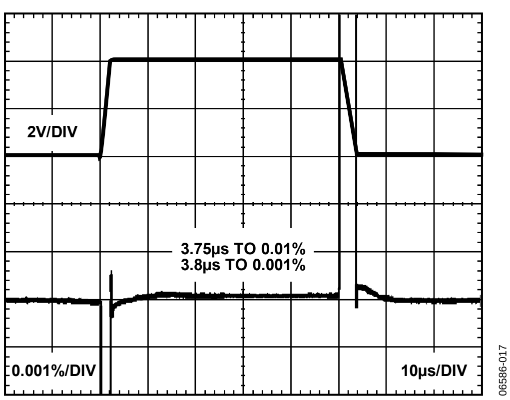


Figure 29. Instrumentation Amplifier Large Signal Pulse Response, G = 8, V_S = 5 V

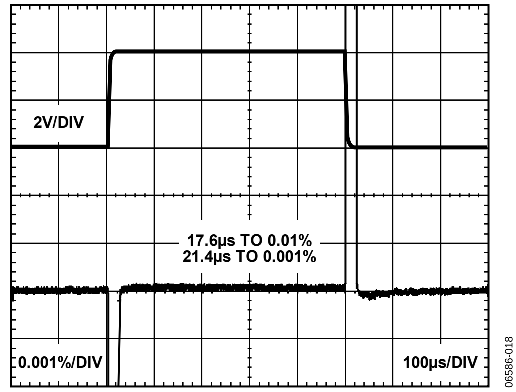


Figure 30. Instrumentation Amplifier Large Signal Pulse Response, G = 128, V_S = 5 V

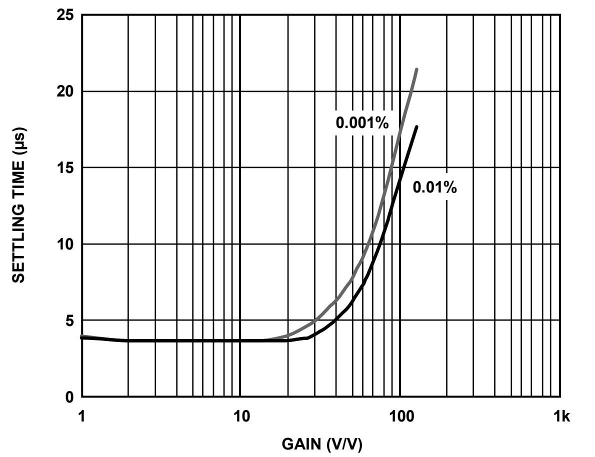


Figure 31. Instrumentation Amplifier Settling Time vs. Gain for a 4 V p-p Step, V_S = 5 V

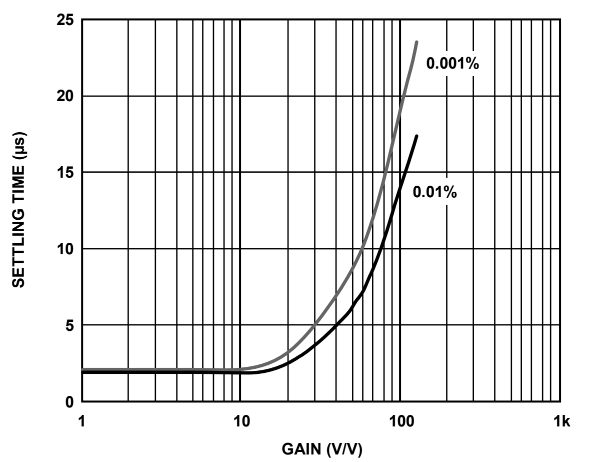


Figure 32. Instrumentation Amplifier Settling Time vs. Gain for a 2 V p-p Step, V_S = 3 V

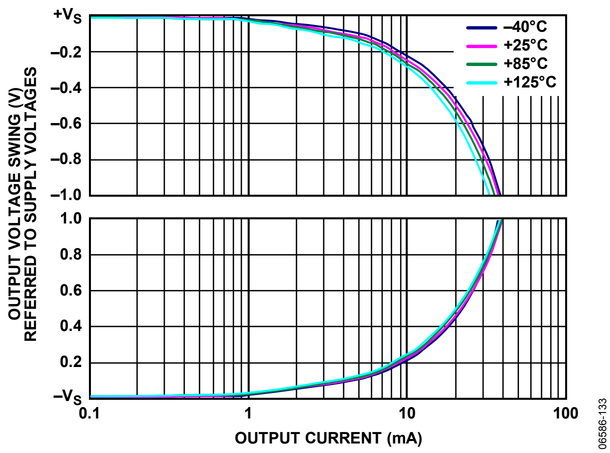


Figure 33. Instrumentation Amplifier Output Voltage Swing vs. Output Current, V_S = 3 V

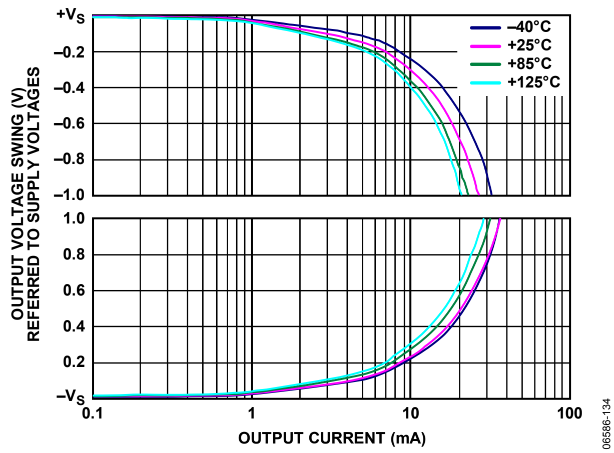


Figure 34. Instrumentation Amplifier Output Voltage Swing vs. Output Current, V_S = 5 V

OPERATIONAL AMPLIFIER PERFORMANCE CURVES

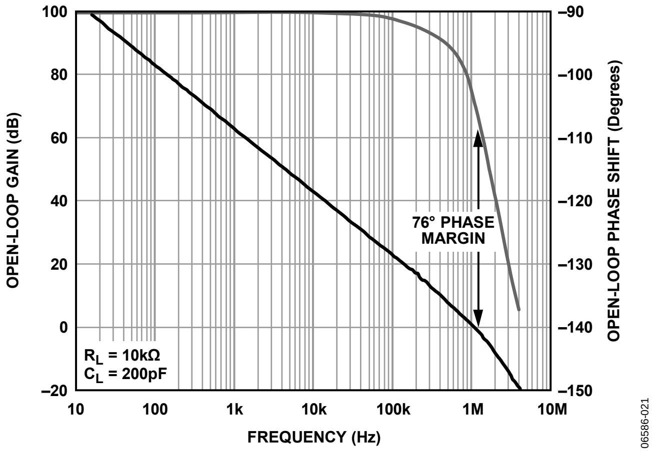


Figure 35. Operational Amplifier Open-Loop Gain and Phase vs. Frequency, V_S = 5 V

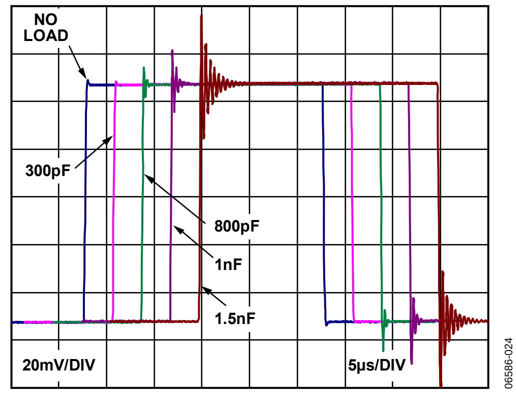


Figure 38. Operational Amplifier Small Signal Response for Various Capacitive Loads, V_S = 3 V

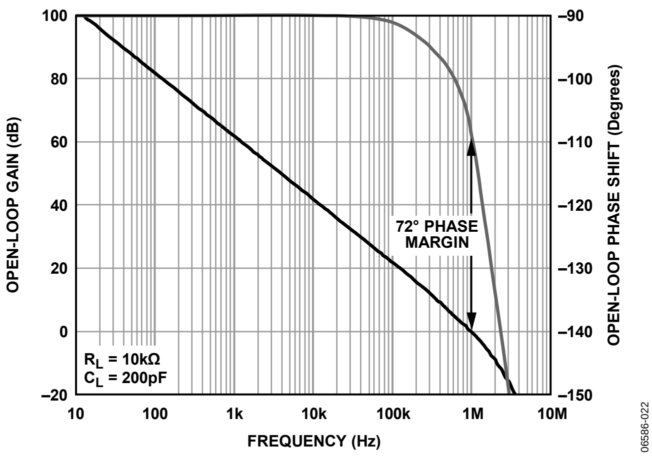


Figure 36. Operational Amplifier Open-Loop Gain and Phase vs. Frequency, V_S = 3 V

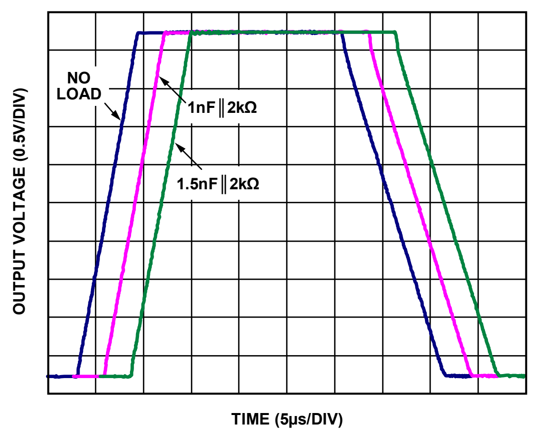


Figure 39. Operational Amplifier Large Signal Transient Response, V_S = 5 V

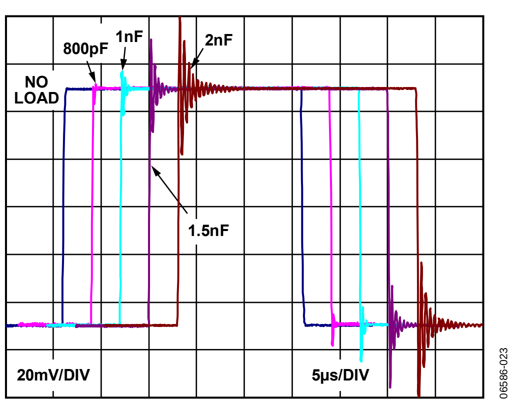


Figure 37. Operational Amplifier Small Signal Response for Various Capacitive Loads, V_S = 5 V

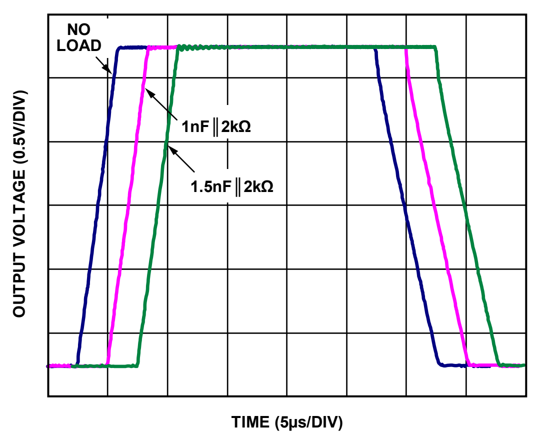


Figure 40. Operational Amplifier Large Signal Transient Response, V_S = 3 V

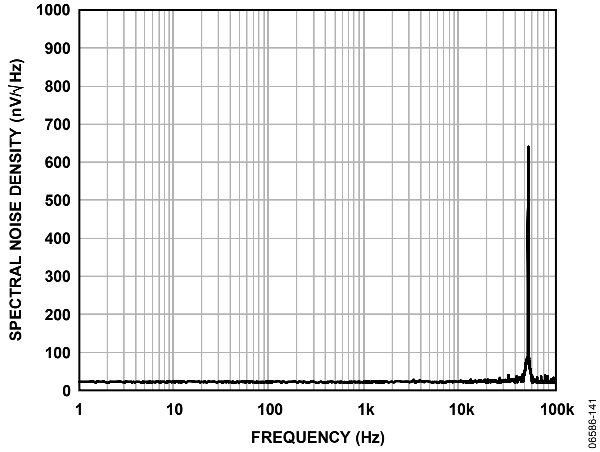


Figure 41. Operational Amplifier Voltage Spectral Noise Density vs. Frequency

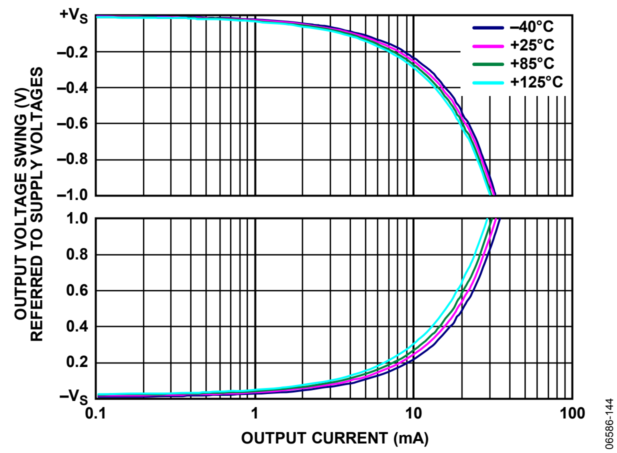


Figure 44. Operational Amplifier Output Voltage Swing vs. Output Current, $V_S = 3$ V

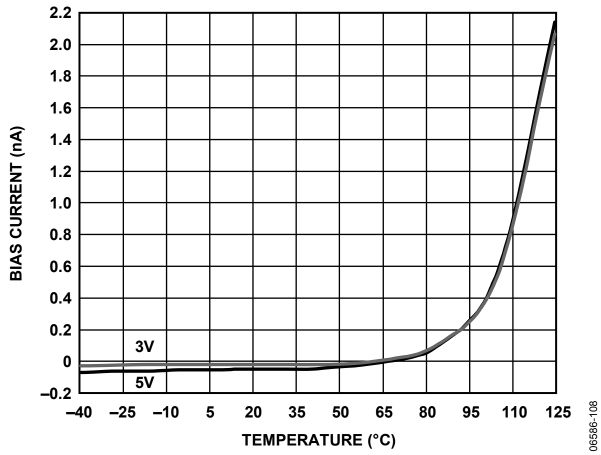


Figure 42. Operational Amplifier Bias Current vs. Temperature

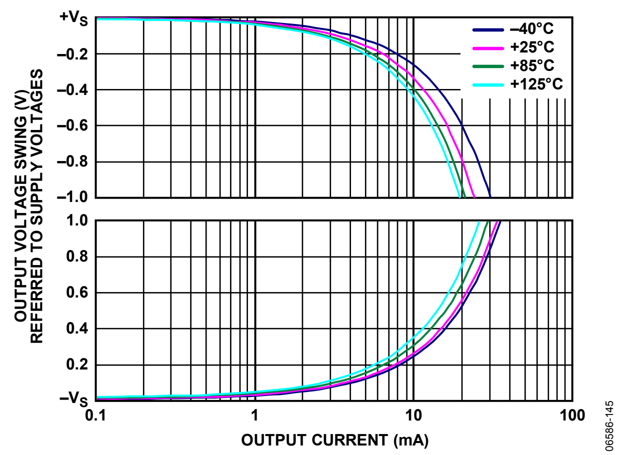


Figure 45. Operational Amplifier Output Voltage Swing vs. Output Current, $V_S = 5$ V

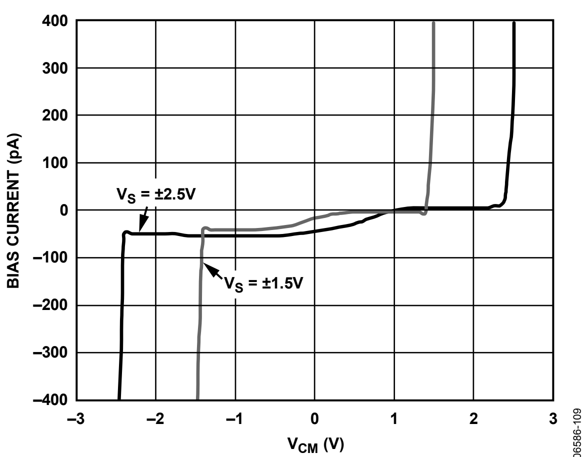


Figure 43. Operational Amplifier Bias Current vs. Common Mode

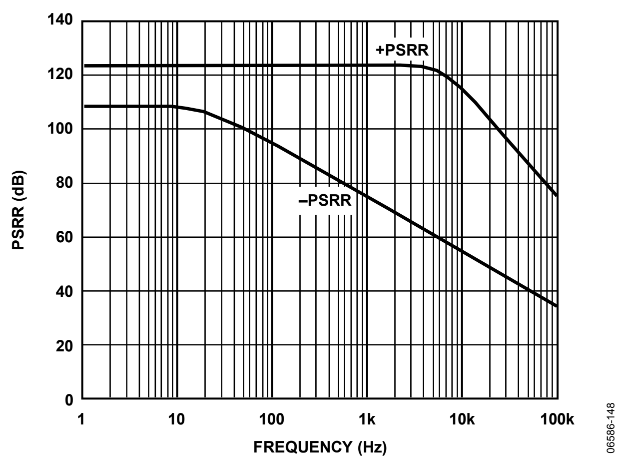


Figure 46. Operational Amplifier Power Supply Rejection Ratio

PERFORMANCE CURVES VALID FOR BOTH AMPLIFIERS

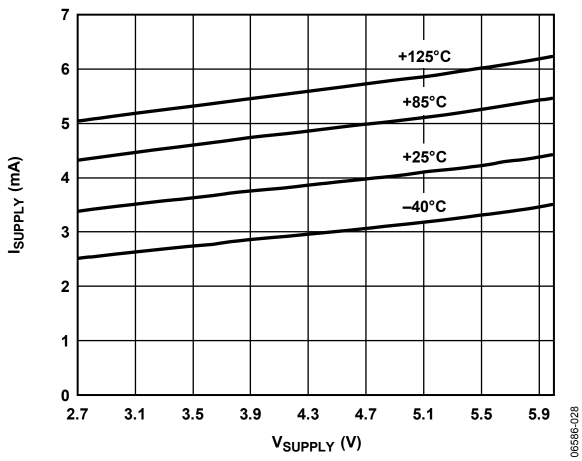


Figure 47. Supply Current vs. Supply Voltage

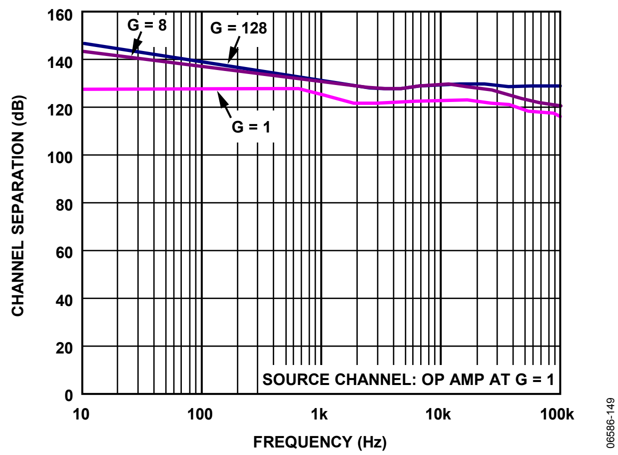


Figure 48. Channel Separation vs. Frequency

THEORY OF OPERATION

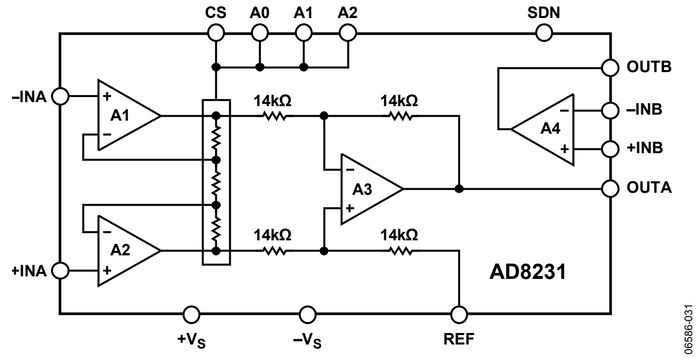


Figure 49. Simplified Schematic

AMPLIFIER ARCHITECTURE

The AD8231 is based on the classic 3-op amp topology. This topology has two stages: a preamplifier to provide amplification, followed by a difference amplifier to remove the common-mode voltage. Figure 49 shows a simplified schematic of the AD8231. The preamp stage is composed of Amplifier A1, Amplifier A2, and a digitally controlled resistor network. The second stage is a gain of 1 difference amplifier composed of Amplifier A3 and four 14 kΩ resistors. A1, A2, and A3 are all zero drift, rail-to-rail input, rail-to rail-output amplifiers.

The AD8231 design makes it extremely robust over temperature. The AD8231 uses an internal thin film resistor to set the gain. Because all of the resistors are on the same die, gain temperature drift performance and CMRR drift performance are better than can be achieved with topologies using external resistors. The AD8231 also uses an auto-zero topology to null the offsets of all its internal amplifiers. Because this topology continually corrects for any offset errors, offset temperature drift is nearly nonexistent.

The AD8231 also includes a free operational amplifier. Like the other amplifiers in the AD8231, it is a zero drift, rail-to-rail input, rail-to-rail output architecture.

GAIN SELECTION

The gain of the AD8231 is set by voltages applied to the A0, A1, and A2 pins. To change the gain, the $\overline{\text{CS}}$ pin must be driven low. When the $\overline{\text{CS}}$ pin is driven high, the gain is latched, and voltages at the A0 to A2 pins have no effect. Because the $\overline{\text{CS}}$ pin is level sensitive rather than edge sensitive, it can also be tied permanently low. Table 7 shows the different gain settings.

The time required for a gain change is dominated by the settling time of the amplifier. The AD8231 takes about 200 ns to switch gains, after which the amplifier begins to settle. Refer to Figure 28 through Figure 32 to determine the settling time for different gains.

Table 7. Truth Table for AD8231 Gain Settings

$\overline{\text{CS}}$	A2	A1	A0	Gain
Low	Low	Low	Low	1
Low	Low	Low	High	2
Low	Low	High	Low	4
Low	Low	High	High	8
Low	High	Low	Low	16
Low	High	Low	High	32
Low	High	High	Low	64
Low	High	High	High	128
High	X	X	X	No change

REFERENCE TERMINAL

The output voltage of the AD8231 is developed with respect to the potential on the reference terminal, which is useful when the output signal needs to be offset to a midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8231 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, source impedance to the REF terminal should be kept below 1 Ω. As shown in Figure 49, the reference terminal, REF, is at one end of a 14 kΩ resistor. Additional impedance at the REF terminal adds to this 14 kΩ resistor and results in amplification of the signal connected to the positive input, causing a CMRR error.

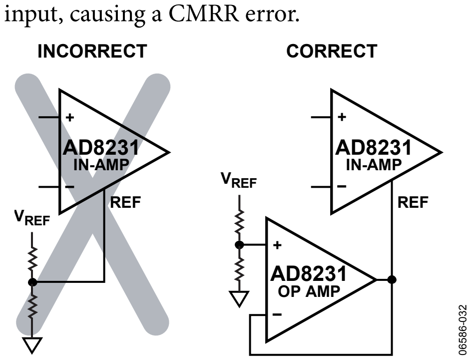


Figure 50. Driving the Reference (REF)

LAYOUT

The AD8231 is a high precision device. To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. The AD8231 pinout is arranged in a logical manner to aid in this task.

Power Supplies

The AD8231 should be decoupled with a 0.1 µF bypass capacitor between the two supplies. This capacitor should be placed as close as possible to Pin 11 and Pin 12, either directly next to the pins or beneath the pins on the backside of the board. The auto-zero architecture of the AD8231 requires a low ac impedance between the supplies. Long trace lengths to the bypass capacitor increase this impedance, which results in a larger input offset voltage.

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance.

Package Considerations

The AD8231 comes in a 4 mm × 4 mm LFCSP. Beware of blindly copying the footprint from another 4 mm × 4 mm LFCSP part; it cannot have the same thermal pad size and leads. Refer to the Outline Dimensions section to verify that the PCB symbol has the correct dimensions. Space between the leads and thermal pad should be kept as wide as possible for the best bias current performance.

Thermal Pad

The AD8231 4 mm × 4 mm LFCSP comes with a thermal pad. This pad is connected internally to $-V_S$. The pad can either be left unconnected or connected to the negative supply rail. For high vibration applications, a landing is recommended.

Because the AD8231 dissipates little power, heat dissipation is rarely an issue. If improved heat dissipation is desired (for example, when ambient temperatures are near 125°C or when driving heavy loads), connect the thermal pad to the negative supply rail. For the best heat dissipation performance, the negative supply rail should be a plane in the board. See the Thermal Resistance section for thermal coefficients with and without the pad soldered.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8231 must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 51.

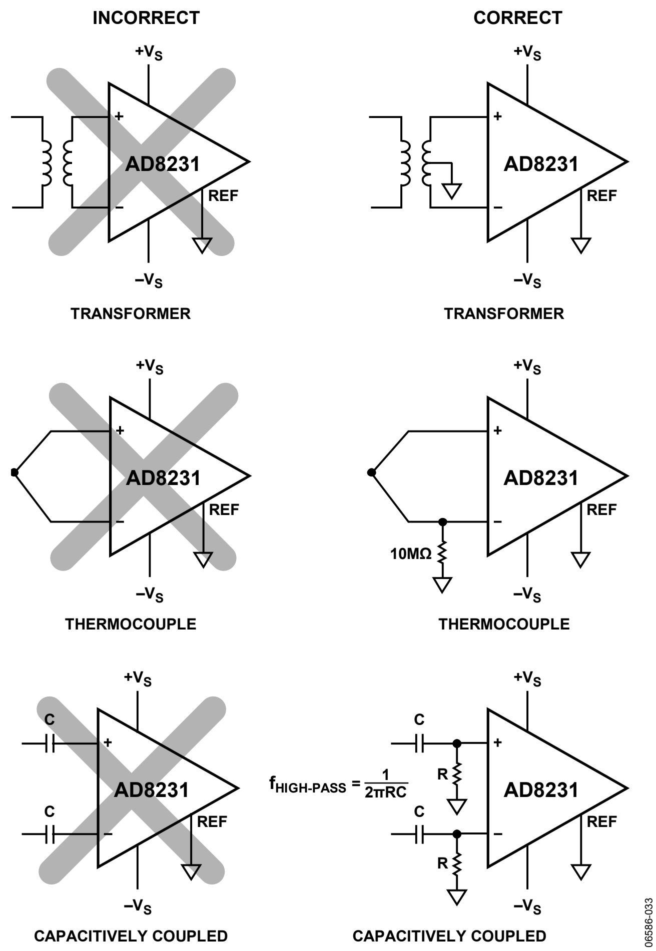


Figure 51. Creating an I_{BIAS} Path

INPUT PROTECTION

All terminals of the AD8231 are protected against ESD. In addition, the input structure allows for dc overload conditions a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond these limits cause the ESD diodes to conduct and current to flow. If overvoltage events are anticipated, an external resistor should be used in series with each of the inputs to limit the current to below 10 mA. Currents up to 100 mA can be sustained for a few seconds.

Note that if either input is brought below the negative supply to the point where the ESD diode turns on, the AD8231 output can phase-reverse.

RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass, RC network placed at the input of the instrumentation amplifier, as shown in Figure 52. The filter limits the input signal bandwidth according to the following relationship

$$FilterFreq_{Diff} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

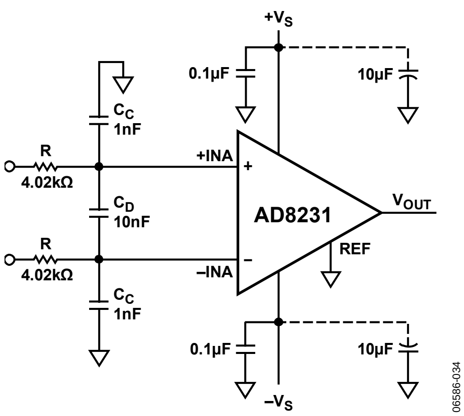


Figure 52. RFI Suppression

Figure 52 shows an example where the differential filter frequency is approximately 2 kHz, and the common-mode filter frequency is approximately 40 kHz.

Values of R and C_C should be chosen to minimize RFI. Mismatch between the R × C_C at the positive input and the R × C_C at the negative input degrades the CMRR of the AD8231. By using a value of C_D that is ten times larger than the value of C_C, the effect of the mismatch is reduced and performance is improved.

COMMON-MODE INPUT VOLTAGE RANGE

The 3-op amp architecture of the AD8231 applies gain and then removes the common-mode voltage. Therefore, internal nodes in the AD8231 experience a combination of both the gained signal and the common-mode signal. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. To determine whether the signal could be limited, refer to Figure 12 through Figure 14 or use the following formula

$$-V_S + 0.04\ \text{V} < V_{CM} \pm \frac{|V_{DIFF}| \times Gain}{2} < +V_S - 0.04\ \text{V}$$

If more common-mode range is required, the simplest solution is to apply less gain in the instrumentation amplifier. The extra op amp can be used to provide another gain stage after the in-amp. Because the AD8231 has good offset and noise performance at low gains, applying less gain in the instrumentation amplifier generally has a limited impact on the overall system performance.

REDUCING NOISE

Because the AD8231 has no 1/f noise, reducing the bandwidth corresponds directly to less noise. Table 8 shows the AD8231 performance at a gain of 1 at different bandwidths, assuming a 2-pole Butterworth filter roll off.

Table 8. AD8231 noise at various bandwidths

Bandwidth (Hz)	Noise (µV rms)	SNR Single-Ended[1]		SNR Differential Output[2]	
		dB	Bits	dB	Bits
1	0.07	148.3	24.3	154.3	25.3
3.2	0.12	143.2	23.5	149.2	24.5
10	0.21	138.3	22.7	144.3	23.7
32	0.37	133.2	21.8	139.2	22.8
100	0.66	128.3	21.0	137.63	22.0
320	1.17	123.2	20.2	129.2	21.2
1 k	2.07	118.3	19.3	124.3	20.3
3.2 k	3.71	113.2	18.5	119.2	19.5
10 k	6.55	108.3	17.7	117.3	18.7
32 k	11.73	103.2	16.9	109.2	17.9

[1] SNR for single-ended output configuration calculated with output signal of 4.8 V p-p, which corresponds to 1.697 V rms.

[2] SNR for differential output configuration calculated with output signal of 9.6 V p-p, which corresponds to 3.397 V rms.

The AD8231 has two clocks: an auto-zero clock at 3.4 kHz and a commutating clock at 54 kHz. While the auto-zero clock has negligible energy and can generally be ignored, the commutating clock has enough energy to significantly affect the noise of the part. Therefore, in applications where low noise is critical, limiting the bandwidth of the system below 54 kHz is recommended.

APPLICATIONS INFORMATION

DIFFERENTIAL OUTPUT

Figure 53 shows how to create a differential output in-amp using the AD8231 uncommitted op amp. Because this configuration makes use of the reference terminal of the in-amp, errors from the op amp and resistor mismatch result in common-mode errors, rather than differential errors. Because common-mode errors are typically rejected by the next device in the signal chain, this circuit configuration adds almost no extra error.

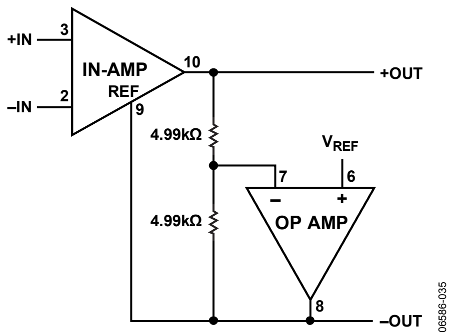


Figure 53. Differential Output Using Operational Amplifier

MULTIPLEXING

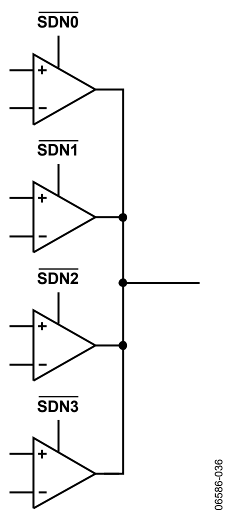


Figure 54. Four AD8231s in Multiplexing Configuration

The outputs of both the AD8231 in-amp and op amp are high impedance in the shutdown state. This feature allows several AD8231s to be multiplexed together without any external switches. Figure 54 shows an example of such a configuration. All the outputs are connected together and only one amplifier is turned on at a time. This feature is analogous to the high-Z mode of the digital tristate logic.

The resistors in the AD8231 instrumentation amplifier create a resistive path from the output to the reference pin of about 100 kΩ. If a higher output impedance in shutdown mode is desired, the reference pin can be driven with the op amp of the AD8231. In this configuration, the output impedance in shutdown is several GΩ, and many thousand AD8231s can theoretically be multiplexed in such a way.

The AD8231 can enter and leave shutdown mode very quickly. However, when the amplifier wakes up and reconnects its input circuitry, the voltage at its internal input nodes changes dramatically. It takes time for the output of the amplifier to settle. Refer to Figure 28 through Figure 32 to determine the settling time for different gains. This settling time limits how quickly the AD8231 can be multiplexed with the $\overline{SDN}$ pin.

USING THE AD8231 WITH BIPOLAR SUPPLIES

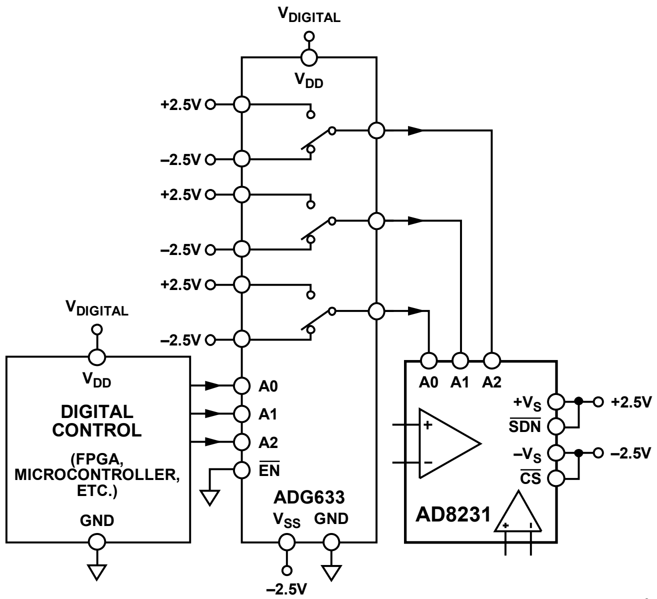
The AD8231 can be used with bipolar supplies as long as the maximum voltage drop between the supply rails is kept below 6 V and all input voltages are kept within the supply rails.

With bipolar supplies, the acceptable levels for the digital inputs A0, A1, A2, $\overline{CS}$, and $\overline{SDN}$ shift. Table 9 shows acceptable values for low and high signals for both single and dual supplies.

Table 9. Digital Pin Thresholds

	Low		High	
Supply Voltage (V)	**Min (V)**	**Max (V)**	**Min (V)**	**Max (V)**
0 to 5	0	+1	4	5
0 to 3	0	+0.8	2.2	3
−2.5 to +2.5	−2.5	−1.5	1.5	2.5
−1.5 to +1.5	−1.5	−0.7	0.7	1.5

When operating the AD8231 on dual supplies, a level-shift is typically needed from standard single-supply control logic. One easy way to accomplish the level-shift is through a single-pole, double-throw switch, such as the ADG633. Figure 55 shows an application schematic for ±2.5 V operation.



V_DIGITAL IS THE DIGITAL SUPPLY VOLTAGE. IT CAN BE ANY VOLTAGE BETWEEN 2.5V AND 9.5V.

Figure 55. Converting Single-Supply Control Signals to Dual Supply.

SALLEN KEY FILTER

The extra op amp in the AD8231 can be used to create a 2-pole Sallen Key filter. Such a filter can remove excess noise or perform antialiasing before an analog-to-digital converter.

Figure 56 shows how to create a 2-pole low-pass Butterworth filter. Components R1, R2, C1, and C2 set the frequency of the filter. The ratio of R3 and R4 sets the peaking of the filter. If R4 equals 10 kΩ, R3 should equal 5.9 kΩ for an optimum 2-pole response.

Depending on the circuitry before and after the AD8231, a 3-pole filter can be possible. If the previous stage has a small output impedance, an additional pole can be added before the in amp (R6, R7, and C4). If the following stage has a high input impedance, an additional pole can be added after the op amp (R5 and C3). Peaking from the Sallen Key stage should be higher to compensate for the extra attenuation of the third pole; both R3 and R4 should be 10 kΩ for optimum response.

Note that in addition to setting the peaking of the filter, the ratio R3/R4 also sets the dc gain: G = 1 + R3/R4. If lower dc gain is required, replace R1 with a voltage divider, where the output resistance of the divider is equal to the required value of R1.

Figure 56 shows a bias point connected to R4 and the in-amp reference. The filter stage amplifies the signal around this bias point. The bias point is typically midsupply and should be low impedance.

Table 10. Recommended Component Values for Butterworth Low-Pass Filter in Figure 56

	Sallen Key		Optional Poles			
			Before In-Amp		After Op Amp	
3 dB Freq	R1, R2 (kΩ)	C1, C2 (nF)	R6, R7 (kΩ)	C4 (nF)	R5 (kΩ)	C3 (nF)
32 Hz	499	10	499	4.7	49.9	100
100 Hz	158	10	158	4.7	16	100
320 Hz	49.9	10	49.9	4.7	4.99	100
1 kHz	158	1	158	0.47	1.6	100
3.2 kHz	49.9	1	49.9	0.47	0.499	100
10 kHz	15.8	1	15.8	0.47	0.16	100
32 kHz	4.99	1	4.99	0.47	0.049	100

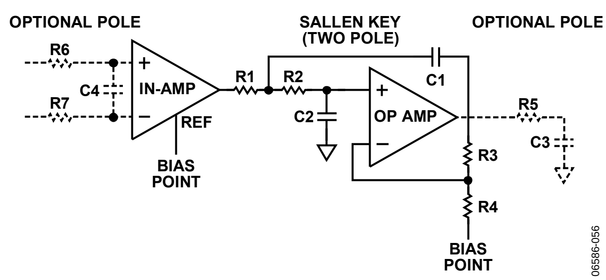


Figure 56. Butterworth Low-Pass Filter (Dotted Sections Indicate Optional Poles)

OUTLINE DIMENSIONS

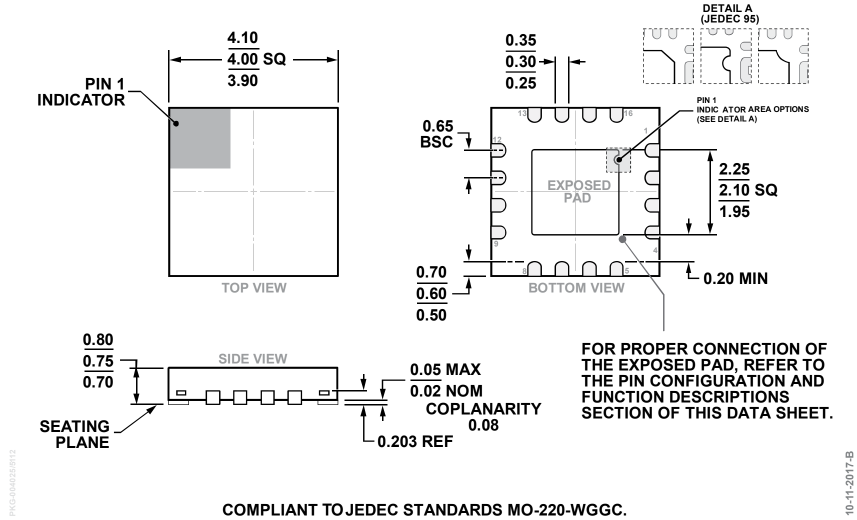


Figure 57. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75mm Package Height
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1,2]	Temperature Range	Package Description	Package Option
AD8231ACPZ-R7	−40°C to +125°C	16-Lead LFCSP, 7" Tape and Reel	CP-16-23
AD8231ACPZ-RL	−40°C to +125°C	16-Lead LFCSP, 13" Tape and Reel	CP-16-23
AD8231ACPZ-WP	−40°C to +125°C	16-Lead LFCSP, Waffle Pack	CP-16-23
AD8231WACPZ-RL	−40°C to +125°C	16-Lead LFCSP, 13" Tape and Reel	CP-16-23
AD8231-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD8231W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices, Inc. account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

D06586-0-10/17(E)

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