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REVISION HISTORY

11/2017—Rev. 0 to Rev. A

Changes to Table 1 ... 4
Changes to Input Offset, V_{OSI}, Average TC Parameter, Table 2 ... 5

4/2017—Revision 0: Initial Version

SPECIFICATIONS

$+V_S$ = 15 V, $-V_S$ = −15 V, V_{REF} = 0 V, T_A = 25°C, T_{OPR} = −55°C to +125°C, G = 1, R_L = 2 kΩ,[1] unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	T_{OPR}				
CMRR from DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = ±10 V				
G = 1		77			dB
G = 10		92			dB
G = 100		92			dB
G = 1000		92			dB
CMRR at 5 kHz	V_{CM} = ±10 V				
G = 1		72			dB
G = 10		80			dB
G = 100		80			dB
G = 1000		80			dB
NOISE	Referred to input (RTI) noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$, T_A				
Voltage Noise, 1 kHz					
Input Voltage Noise, e_{ni}	$V_{IN}+$, $V_{IN}-$ = 0 V		14		nV/√Hz
Output Voltage Noise, e_{no}	$V_{IN}+$, $V_{IN}-$ = 0 V		90		nV/√Hz
RTI, 0.1 Hz to 10 Hz					
G = 1			5		μV p-p
G = 1000			0.8		μV p-p
Current Noise	f = 1 kHz		1		fA/√Hz
VOLTAGE OFFSET	$V_{OS} = V_{OSI} + V_{OSO}/G$				
Input Offset, V_{OSI}	T_A	−250		+250	μV
Average Temperature Coefficient (TC)	T_{OPR}	−10		+10	μV/°C
Output Offset, V_{OSO}	T_A	−750		+750	μV
Average TC	T_{OPR}	−10		+10	μV/°C
Offset RTI vs. Supply (PSR)	V_S = ±5 V to ±15 V, T_{OPR}				
G = 1		80			dB
G = 10		92			dB
G = 100		92			dB
G = 1000		92			dB
INPUT CURRENT					
Input Bias Current	T_A			25	pA
Over Temperature	T_{OPR}			100	nA
Input Offset Current	T_A			2	pA
Over Temperature	T_{OPR}			10	nA
DYNAMIC RESPONSE					
Small Signal Bandwidth, −3 dB	T_A				
G = 1			1500		kHz
G = 10			800		kHz
G = 100			120		kHz
G = 1000			14		kHz
Settling Time 0.01%	10 V step, T_A				
G = 1			5		μs
G = 10			4.3		μs
G = 100			8.1		μs
G = 1000			58		μs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Settling Time 0.001%	10 V step, T_A				
G = 1			6		µs
G = 10			4.6		µs
G = 100			9.6		µs
G = 1000			74		µs
Slew Rate					
G = 1 to 100	T_A	2			V/µs
GAIN	G = 1 + (49.4 kΩ/R_G), T_{OPR}				
Gain Range		1		1000	V/V
Gain Error	V_{OUT} = ±10 V				
G = 1		−0.1		+0.1	%
G = 10		−0.8		+0.8	%
G = 100		−0.8		+0.8	%
G = 1000		−0.8		+0.8	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V, T_A				
G = 1	R_L = 10 kΩ		10	15	ppm
G = 10	R_L = 10 kΩ		5	10	ppm
G = 100	R_L = 10 kΩ		30	60	ppm
G = 1000	R_L = 10 kΩ		400	500	ppm
G = 1	R_L = 2 kΩ		10	15	ppm
G = 10	R_L = 2 kΩ		10	15	ppm
G = 100	R_L = 2 kΩ		50	75	ppm
Gain vs. Temperature					
G = 1			3	10	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Impedance (Pin to Ground)[2]	T_A		10^4||5		GΩ||pF
Input Operating Voltage Range[3]	V_S = ±2.25 V to ±18 V for dual supplies, T_A	$-V_S - 0.1$		$+V_S - 2$	V
Over Temperature	T_{OPR}	$-V_S - 0.1$		$+V_S - 2.2$	V
OUTPUT					
Output Swing	R_L = 10 kΩ, T_A	−14.7		+14.7	V
Over Temperature	T_{OPR}	−14.3		+14.3	V
Short-Circuit Current	T_A		15		mA
REFERENCE INPUT	T_A				
R_{IN}			40		kΩ
I_{IN}	$V_{IN}+$, $V_{IN}-$ = 0 V			70	µA
Voltage Range				$+V_S$	V
Gain to Output	T_A			1 ± 0.0001	V/V
POWER SUPPLY					
Operating Range[4]		±2.25		±18	V
Quiescent Current	T_A			750	µA
Over Temperature	T_{OPR}			1000	µA
TEMPERATURE RANGE					
For Specified Performance	T_{OPR}	−55		+125	°C

[1] When the output sinks more than 4 mA, use a 47 pF capacitor in parallel with the load to prevent ringing. Otherwise, use a larger load, such as 10 kΩ.
[2] Differential and common-mode input impedance (Z_{DIFF} and Z_{CM}) can be calculated from the pin impedance (Z_{PIN}): $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[3] The AD8220-EP can operate up to a diode drop below the negative supply but the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current is within the specification.
[4] At the minimum supply voltage of ±2.25 V, ensure that the input common-mode voltage is within the input voltage range specification.

$+V_S = 5$ V, $-V_S = 0$ V, $V_{REF} = 2.5$ V, $T_A = 25°C$, $T_{OPR} = -55°C$ to $+125°C$, G = 1, $R_L = 2$ kΩ[1], unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	T_{OPR}				
CMRR from DC to 60 Hz with 1 kΩ Source Imbalance	$V_{CM} = 0$ V to 2.5 V				
G = 1		77			dB
G = 10		92			dB
G = 100		92			dB
G = 1000		92			dB
CMRR at 5 kHz	$V_{CM} = 0$ V to 2.5 V				
G = 1		72			dB
G = 10		80			dB
G = 100		80			dB
G = 1000		80			dB
NOISE	RTI noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$, T_A				
Voltage Noise, 1 kHz	$V_S = \pm 2.5$ V				
Input Voltage Noise, e_{ni}	$V_{IN}+$, $V_{IN}- = 0$ V, $V_{REF} = 0$ V		14		nV/√Hz
Output Voltage Noise, e_{no}	$V_{IN}+$, $V_{IN}- = 0$ V, $V_{REF} = 0$ V		90		nV/√Hz
RTI, 0.1 Hz to 10 Hz					
G = 1			5		µV p-p
G = 1000			0.8		µV p-p
Current Noise	f = 1 kHz		1		fA/√Hz
VOLTAGE OFFSET	$V_{OS} = V_{OSI} + V_{OSO}/G$				
Input Offset, V_{OSI}	T_A	−300		+300	µV
Average TC	T_{OPR}	−10		+10	µV/°C
Output Offset, V_{OSO}	T_A	−800		+800	µV
Average TC	T_{OPR}	−10		+10	µV/°C
Offset RTI vs. Supply (PSR)	T_{OPR}				
G = 1		80			dB
G = 10		92			dB
G = 100		92			dB
G = 1000		92			dB
INPUT CURRENT					
Input Bias Current	T_A			25	pA
Over Temperature	T_{OPR}			100	nA
Input Offset Current	T_A			2	pA
Over Temperature	T_{OPR}			10	nA
DYNAMIC RESPONSE	T_A				
Small Signal Bandwidth, −3 dB					
G = 1			1500		kHz
G = 10			800		kHz
G = 100			120		kHz
G = 1000			14		kHz
Settling Time 0.01%	T_A				
G = 1	3 V step		2.5		µs
G = 10	4 V step		2.5		µs
G = 100	4 V step		7.5		µs
G = 1000	4 V step		30		µs
Settling Time 0.001%	T_A				
G = 1	3 V step		3.5		µs
G = 10	4 V step		3.5		µs
G = 100	4 V step		8.5		µs
G = 1000	4 V step		37		µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Slew Rate					
G = 1 to 100	T_A	2			V/µs
GAIN	G = 1 + (49.4 kΩ/R_G), T_{OPR}				
Gain Range		1		1000	V/V
Gain Error	V_{OUT} = 0.3 V to 2.9 V for G = 1, V_{OUT} = 0.3 V to 3.8 V for G > 1				
G = 1		−0.1		+0.1	%
G = 10		−0.8		+0.8	%
G = 100		−0.8		+0.8	%
G = 1000		−0.8		+0.8	%
Nonlinearity	V_{OUT} = 0.3 V to 2.9 V for G = 1, V_{OUT} = 0.3 V to 3.8 V for G > 1, T_A				
G = 1	R_L = 10 kΩ			50	ppm
G = 10	R_L = 10 kΩ			50	ppm
G = 100	R_L = 10 kΩ			75	ppm
G = 1000	R_L = 10 kΩ			750	ppm
G = 1	R_L = 2 kΩ			50	ppm
G = 10	R_L = 2 kΩ			50	ppm
G = 100	R_L = 2 kΩ			75	ppm
Gain vs. Temperature					
G = 1			3	10	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Impedance (Pin to Ground)[2]	T_A		10^4‖6		GΩ‖pF
Input Voltage Range[3]	T_A				V
Over Temperature	T_{OPR}	−0.1		$+V_S$ − 2.2	V
OUTPUT					
Output Swing	R_L = 10 kΩ	0.15		4.85	V
Over Temperature	T_{OPR}	0.3		4.70	V
Short-Circuit Current			15		mA
REFERENCE INPUT	T_A				
R_{IN}			40		kΩ
I_{IN}	$V_{IN}+$, $V_{IN}-$ = 0 V			70	µA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output	T_A		1 ± 0.0001		V/V
POWER SUPPLY					
Operating Range		4.5		36	V
Quiescent Current	T_A			750	µA
Over Temperature	T_{OPR}			1000	µA
TEMPERATURE RANGE					
T_{OPR}, For Specified Performance	T_{OPR}	−55		+125	°C

[1] When the output sinks more than 4 mA, use a 47 pF capacitor in parallel with the load to prevent ringing. Otherwise, use a larger load, such as 10 kΩ.
[2] Differential and common-mode impedance can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[3] The AD8220-EP can operate up to a diode drop below the negative supply but the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current is within the specification.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Power Dissipation	See Figure 3
Output Short-Circuit Current	Indefinite[1]
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−55°C to +125°C
Reflow Temperature	260°C
Junction Temperature	140°C
θ_{JA} (4-Layer JEDEC Standard Board)[2]	189°C/W
ESD	
Human Body Model	7 kV
Charge Device Model	1.25 kV
Machine Model	0.4 kV

[1] Assumes the load is referenced to midsupply.
[2] θ_{JA} value is an approximation.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the MSOP on a 4-layer JEDEC standard board.

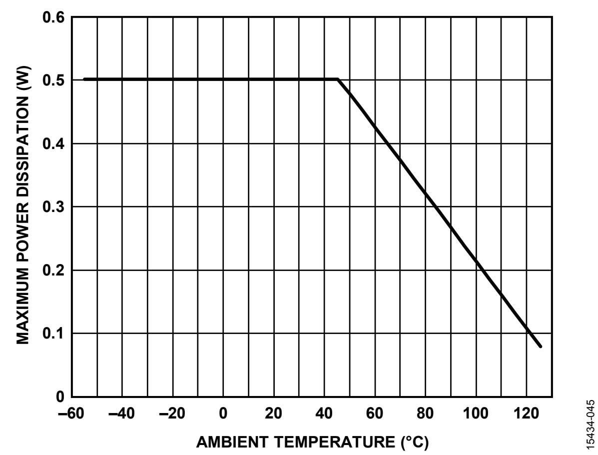

Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

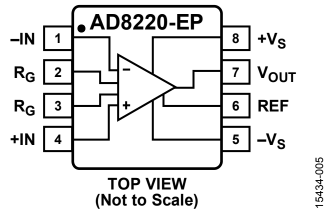

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input Terminal (True Differential Input).
2, 3	R_G	Gain Setting Terminals. Place a resistor across the R_G pins.
4	+IN	Positive Input Terminal (True Differential Input).
5	$-V_S$	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level shift the output.
7	V_{OUT}	Output Terminal.
8	$+V_S$	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

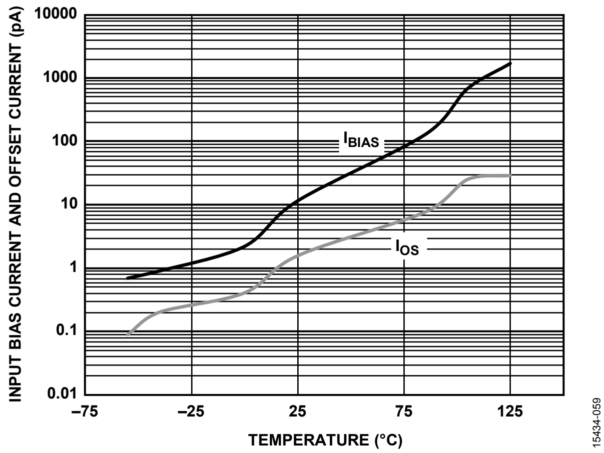

Figure 5. Input Bias Current and Offset Current vs. Temperature, $V_S = \pm 15$ V, $V_{REF} = 0$ V

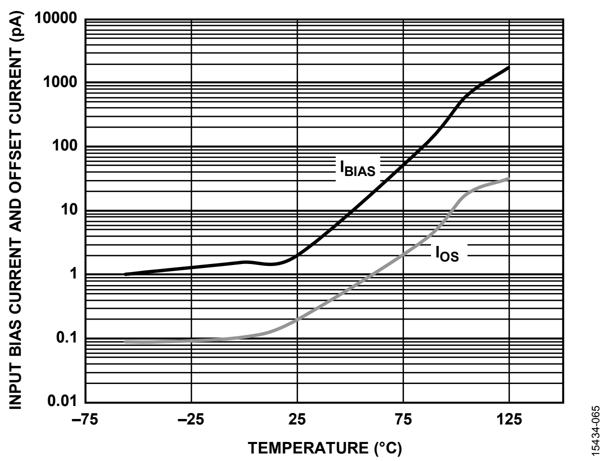

Figure 6. Input Bias Current and Offset Current vs. Temperature, $V_S = 5$ V, $V_{REF} = 2.5$ V

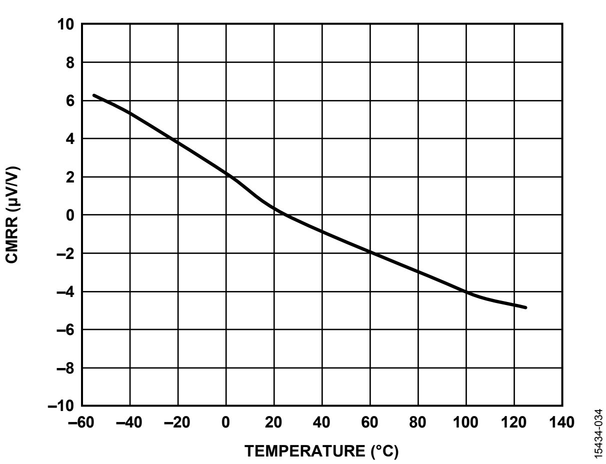

Figure 7. CMRR vs. Temperature, G = 1

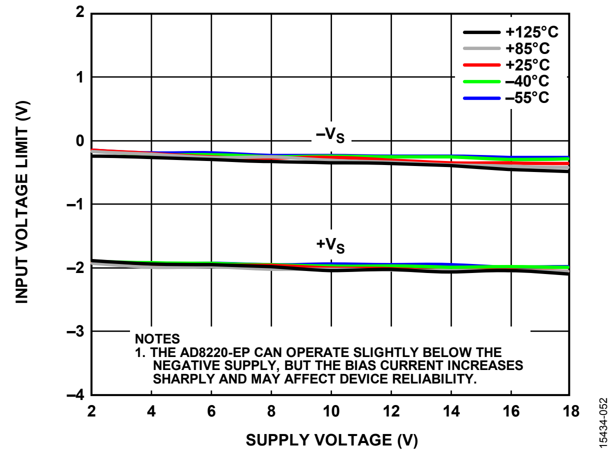

Figure 8. Input Voltage Limit vs. Supply Voltage, G = 1, $V_{REF} = 0$ V

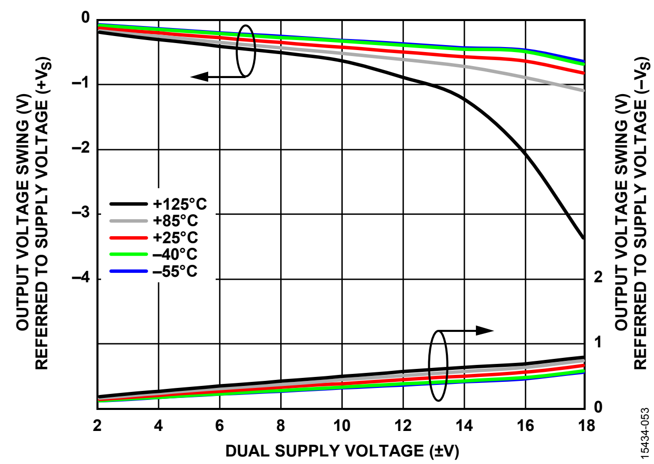

Figure 9. Output Voltage Swing Referred to Supply Voltage vs. Dual Supply Voltage, $R_{LOAD} = 2$ kΩ, G = 10, $V_{REF} = 0$ V

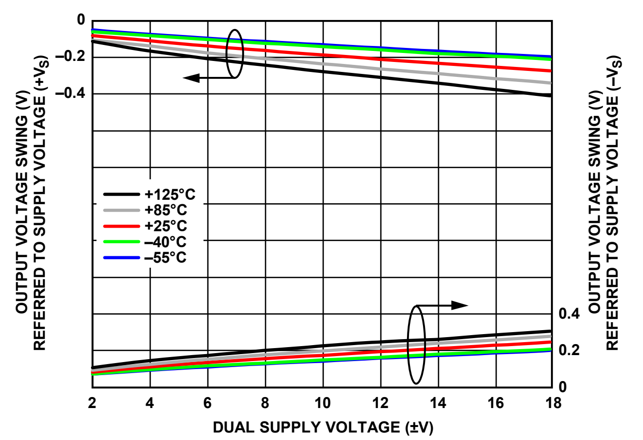

Figure 10. Output Voltage Swing Referred to Supply Voltage vs. Dual Supply Voltage, $R_{LOAD} = 10$ kΩ, G = 10, $V_{REF} = 0$ V

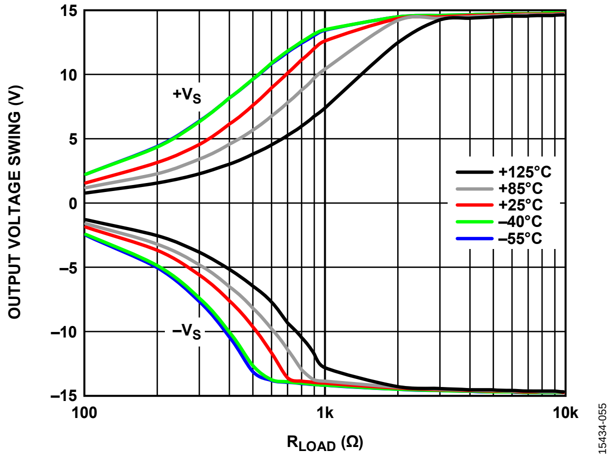

Figure 11. Output Voltage Swing vs. Load Resistance (R_{LOAD}), V_S = ±15 V, V_{REF} = 0 V

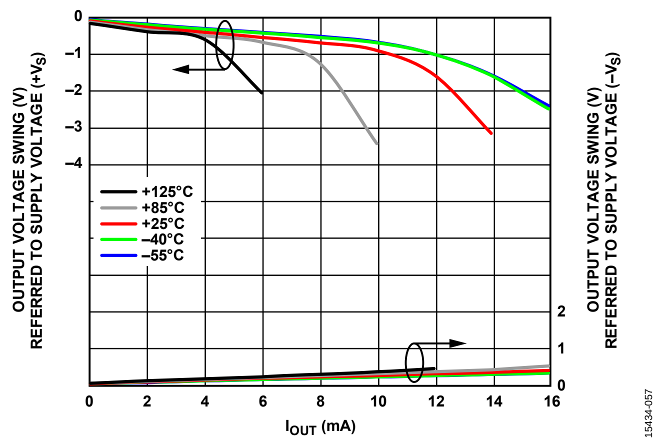

Figure 13. Output Voltage Swing Referred to Supply Voltage vs. Output Current (I_{OUT}), V_S = ±15 V, V_{REF} = 0 V

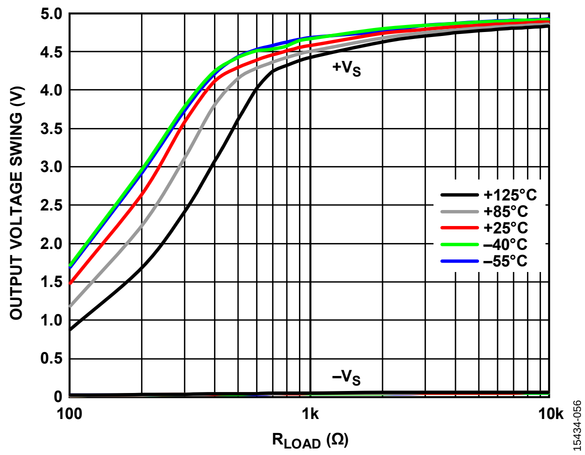

Figure 12. Output Voltage Swing vs. Load Resistance (R_{LOAD}), V_S = 5 V, V_{REF} = 2.5 V

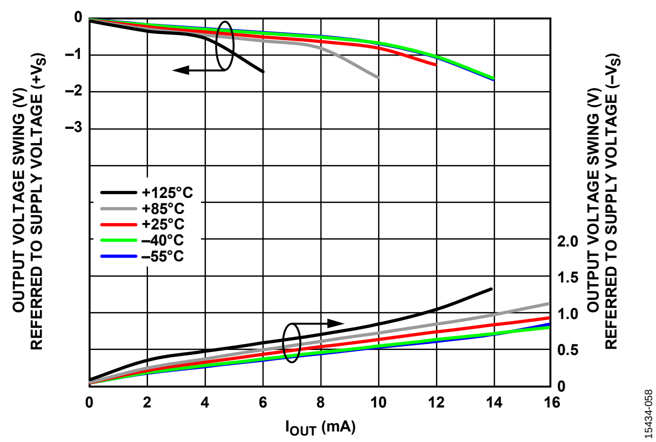

Figure 14. Output Voltage Swing Referred to Supply Voltage vs. Output Current (I_{OUT}), V_S = 5 V, V_{REF} = 2.5 V

OUTLINE DIMENSIONS

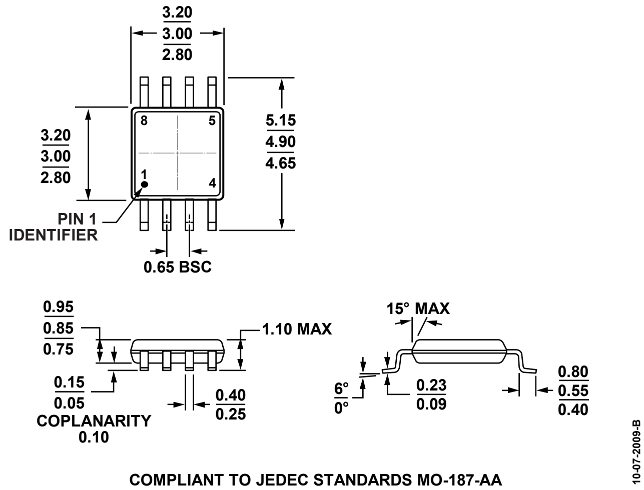

Figure 15. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8220TRMZ-EP	−55°C to +125°C	8-Lead MSOP	RM-8	Y6T
AD8220TRMZ-EP-R7	−55°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y6T

[1] Z = RoHS Compliant Part.