AD7549* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-137: A Digitally Programmable Gain and Attenuation Amplifier Design
- AN-206: CMOS Multiplying DAC Based Panning Circuit Provides Almost Constant Output Power
- AN-209: 8th Order Programmable Low-Pass Analog Filter Using Dual 12-Bit CMOS Multiplying DACs
- AN-225: 12-Bit Voltage-Output DACs for Single-Supply 5V and 12V Systems
- AN-320A: CMOS Multiplying DACs and Op Amps Combine to Build Programmable Gain Amplifier, Part 1
- AN-325: 12-Bit Analog I/O Port Uses AD7549 Dual 12-Bit DAC and 8051 Microcomputer
- AN-326: Interfacing the AD7549 to the MCS-48 and MCS-51 Microcomputer Families
- AN-912: Driving a Center-Tapped Transformer with a Balanced Current-Output DAC

Data Sheet

- AD7549: LC^{2}MOS Dual 12-Bit µP-Compatible DAC Scanned Data Sheet
- AD7549: Military Data Sheet

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD7549 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7549 EngineerZone Discussions.

SAMPLE AND BUY

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TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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AD7549—SPECIFICATIONS[1] (V_{DD} = +15V ±5%[2], V_{REFA} = V_{REFB} = 10V; I_{OUTA} = I_{OUTB} = AGND = 0V. All specifications T_{min} to T_{max} unless otherwise specified.)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC.
Gain Temperature Coefficient[3];						
ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current						
I_{OUTA} (Pin 17)						
+25°C	20	20	20	20	nA max	DAC A Register loaded with all 0's
T_{min} to T_{max}	150	150	250	250	nA max	
I_{OUTB} (Pin 15)						
+25°C	20	20	20	20	nA max	DAC B Register loaded with all 0's
T_{min} to T_{max}	150	150	250	250	nA max	
REFERENCE INPUT						
Input Resistance (Pin 19, Pin 13)	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	18	18	18	18	kΩ max	
V_{REFA}/V_{REFB}						
Input Resistance Match	±3	±2	±3	±2	% max	Typically ±1%
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
I_{DD}	5	5	5	5	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V, Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full scale range. I_{OUT} load = 100Ω; C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. Typical value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	10	–	nV-sec typ	Measured with V_{REFA} = V_{REFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20V p-p 10kHz sine wave.
V_{REFB} to I_{OUTB}	−70	−65	dB max	DAC registers loaded with all 0s.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUTA}	80	80	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	80	80	pF max	
C_{OUTA}	160	160	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	160	160	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−62	–	dB typ	V_{REFA} = 20V p-p 100kHz sine wave, V_{REFB} = 0V
V_{REFB} to I_{OUTA}	−62	–	dB typ	V_{REFB} = 20V p-p 100kHz sine wave, V_{REFA} = 0V
Digital Crosstalk	10	–	nV-sec typ	Measured for a Code Transition of all 0's to all 1's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}
Harmonic Distortion	−90	–	dB typ	V_{IN} = 6V rms 1kHz

NOTES

[1]Temperature range as follows: J, K, Versions: −40°C to +85°C
A, B, Versions: −40°C to +85°C
S, T, Versions: −55°C to +125°C

[2]At V_{DD} = 5V, the device is fully functional with degraded performance.

[3]Guaranteed by Product Assurance testing.

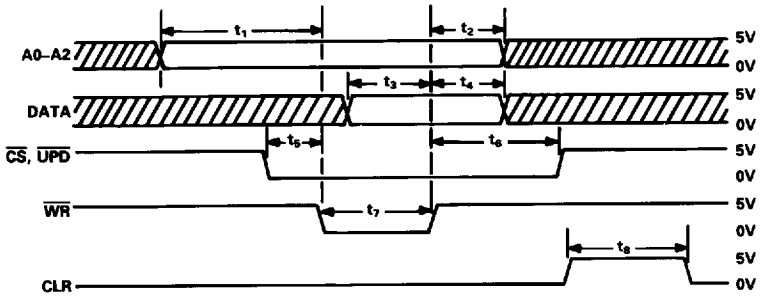
[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +15V, V_{REFA} = V_{RFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V, unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	50	80	110	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	180	200	240	ns min	Data Setup Time
t_4	0	0	0	ns min	Data Hold Time
t_5	20	20	20	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	170	200	250	ns min	Write Pulse Width
t_8	170	200	250	ns min	Clear Pulse Width

Specifications subject to change without notice.



NOTES
1. All input signal rise and fall times measured from 10% to 90% of +5V. $t_r = t_f = 20$ns.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (Pin 20) to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} (Pins 19, 13) to AGND . . . . . ±25V
V_{RFBA}, V_{RFBB} (Pins 18, 14) to AGND . . . . . ±25V
Digital Input Voltage (Pins 1–11)
to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{PIN15}, V_{PIN17}, to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C

Operating Temperature Range
Commercial (J, K Versions) . . . . . −40°C to +85°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Full Scale Error	Package Option[2]
AD7549JN	−40°C to +85°C	±1LSB	±6LSB	N-20
AD7549KN	−40°C to +85°C	±1/2LSB	±3LSB	N-20
AD7549JP	−40°C to +85°C	±1LSB	±6LSB	P-20A
AD7549KP	−40°C to +85°C	±1/2LSB	±3LSB	P-20A
AD7549AQ	−40°C to +85°C	±1LSB	±6LSB	Q-20
AD7549BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-20
AD7549SQ	−55°C to +125°C	±1LSB	±6LSB	Q-20
AD7549TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-20
AD7549SE	−55°C to +125°C	±1LSB	±6LSB	E-20A
AD7549TE	−55°C to +125°C	±1/2LSB	±3LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip.

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of 1LSB max over the operating temperature range ensures montonicity.

FULL-SCALE ERROR
Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero.

OUTPUT CAPACITANCE
This is the capacitance from I_{OUTA} or I_{OUTB} to AGND.

DIGITAL-TO-ANALOG GLITCH IMPULSE
The amount of charge injected into the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{REFA} and V_{REFB} equal to AGND.

OUTPUT LEAKAGE CURRENT
Output Leakage Current is current which appears at I_{OUTA} or I_{OUTB} with the DAC registers loaded to all zeros.

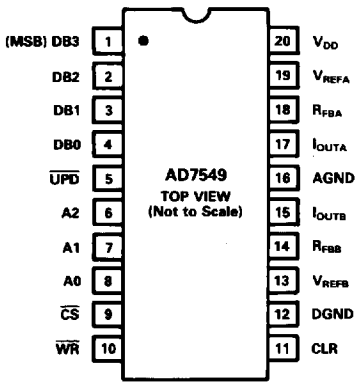
MULTIPLYING FEEDTHROUGH ERROR
This is the error due to capacitive feedthrough from V_{REFA} to I_{OUTA} or V_{REFB} to I_{OUTB} with the DAC registers loaded to all zeros.

CHANNEL-TO-CHANNEL ISOLATION
Channel-to-Channel Isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

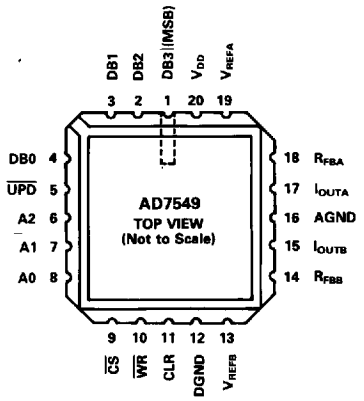
DIGITAL CROSSTALK
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as Digital Crosstalk and is specified in nV-secs.

PIN CONFIGURATIONS

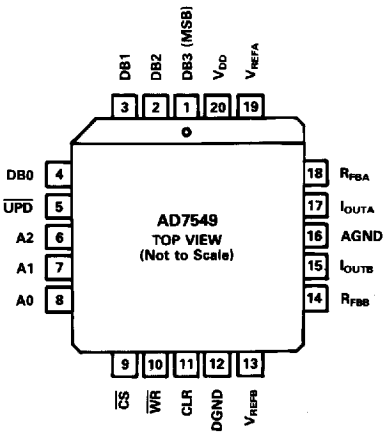
DIP



LCCC



PLCC



PIN	FUNCTION	DESCRIPTION
1	DB3	Data Bit 3, Data Bit 7 or Data Bit 11 (MSB)
2	DB2	Data Bit 2, Data Bit 6 or Data Bit 10.
3	DB1	Data Bit 1, Data Bit 5 or Data Bit 9.
4	DB0	Data Bit 0, Data Bit 4 or Data Bit 8.
5	$\overline{UPD}$	Updates DAC Registers from 4-bit input registers. DAC A and DAC B both updated simultaneously.
6	A2	Address line 2.
7	A1	Address line 1.
8	A0	Address line 0.
9	$\overline{CS}$	Chip Select Input. Active low.
10	$\overline{WR}$	Write Input. Active low.
11	CLR	Clear Input. Active High. Clears all registers.
12	DGND	Digital Ground.
13	V_{REFB}	Voltage reference input to DAC B.
14	R_{FBB}	Feedback resistor of DAC B.
15	I_{OUTB}	Current output terminal of DAC B.
16	AGND	Analog ground.
17	I_{OUTA}	Current output terminal of DAC A.
18	R_{FBA}	Feedback resistor of DAC A.
19	V_{REFA}	Voltage reference input to DAC A.
20	V_{DD}	+15V supply input.

CLR	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A2	A1	A0	FUNCTION
0	X	X	1	X	X	X	No data transfer.
0	1	1	X	X	X	X	No data transfer.
1	X	X	X	X	X	X	All registers cleared.
0	1	0	⊓	0	0	0	DAC A LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	0	1	DAC A MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	1	0	DAC A HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	1	1	DAC A Register loaded from Input Registers.
0	1	0	⊓	1	0	0	DAC B LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	0	1	DAC B MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	1	0	DAC B HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	1	1	DAC B Register loaded from Input Registers.
0	0	1	⊓	X	X	X	DAC A, DAC B Registers updated simultaneously from Input Registers.

NOTE: X = Don't Care

Table I. AD7549 Truth Table

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (i.e. AD644) or separate packages (AD544). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high speed op-amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all O's and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is at a minimum (i.e. $\leq 120\mu V$). Full scale trimming is accomplished by loading the DAC register with all 1's and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, 10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

Resistors R5, R6, R7 (R8, R9, R10) must be ratio matched to 0.01%. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 3 is given in Table III.

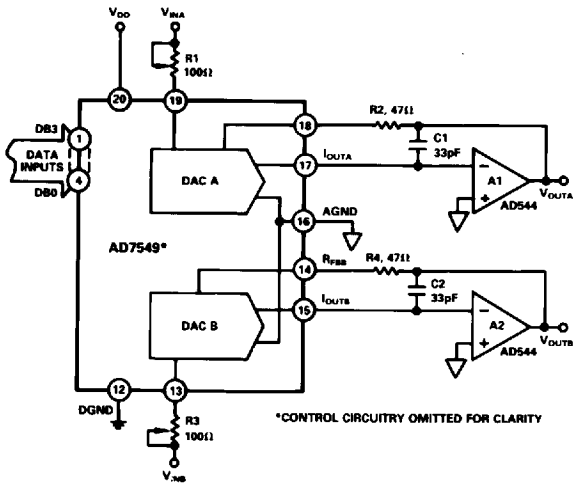


Figure 2. AD7549 Unipolar Binary Operation

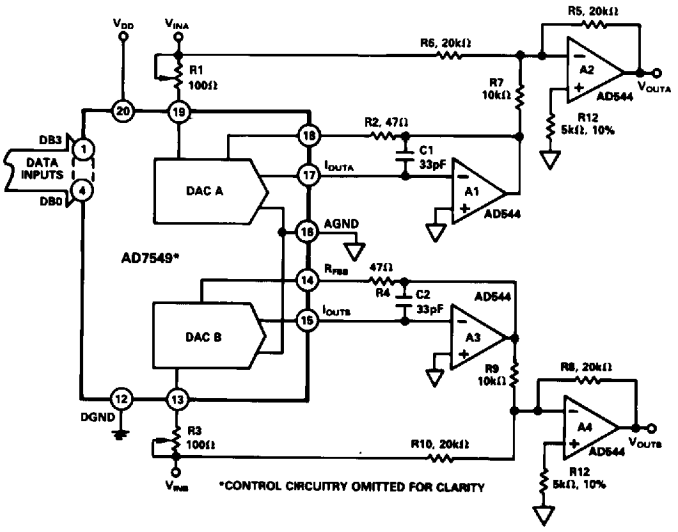


Figure 3. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 2

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 3

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 2 and 3 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD644L, AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

Temperature Coefficients: The gain temperature coefficient of the AD7549 has a maximum value of 5ppm/°C and typical value of 1ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.4LSBs respectively over a 100°C temperature range. When trim resistors R1(R3) and R2(R4) are used to adjust full scale range, the temperature coefficient of R1(R3) and R2(R4) should also be taken into account.

High Frequency Considerations: AD7549 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

Feedthrough: The dynamic performance of the AD7549 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 2 is shown in Figure 4 which minimizes feedthrough from V_{REFA}, V_{REFB} to the output in multiplying applications.

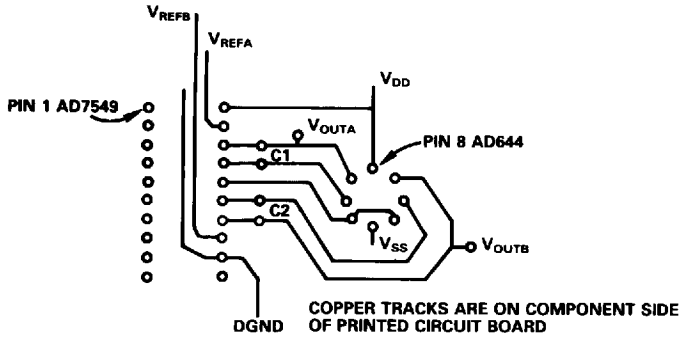


Figure 4. Suggested Layout for AD7549 with AD644 (Dual Op Amp)

AD7549 – 8085A INTERFACE

A typical interface circuit for the AD7549 and the 8085A microprocessor is given in Figure 5. Only the bottom 4 bits of the microprocessor data bus are used. The address decoder provides both the $\overline{CS}$ and $\overline{UPD}$ signals for the DAC. Address lines A0, A1, A2 select one of six DAC Input Registers for accepting data. In applications where simultaneous loading of the DACs is required then the $\overline{UPD}$ pin must be used to strobe both DAC registers. Otherwise, $\overline{UPD}$ may be tied high and address lines A0-A2, in conjunction with $\overline{CS}$ and $\overline{WR}$ signals, will select each DAC register separately (see Pin Function Description).

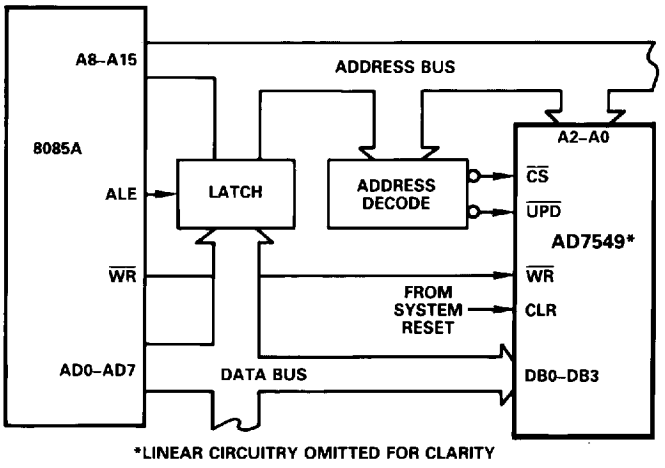


Figure 5. AD7549–8085A Interface

AD7549 – Z80 INTERFACE

Figure 6 shows the AD7549 connected to the Z80 microprocessor. The interface structure is similar to that for the 8085A.

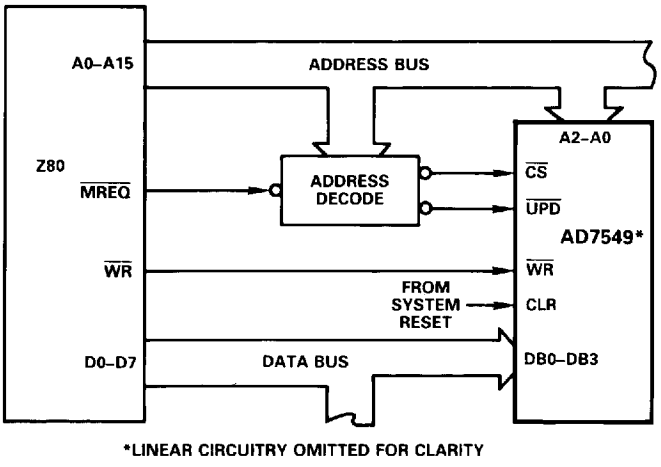


Figure 6. AD7549–Z80 Interface

AD7549 – 8048 INTERFACE

The AD7549 can be interfaced to the 8048 single component microcomputer using the circuit of Figure 7. A minimum number of I/O lines are needed. The system is easily expanded by using extra port lines to provide Chip Selects for more AD7549's. The advantage of this interface lies in its simplicity. In either single or multiple DAC applications both the software and chip select decoding are simplified over what would be required if the devices were memory mapped in a conventional manner.

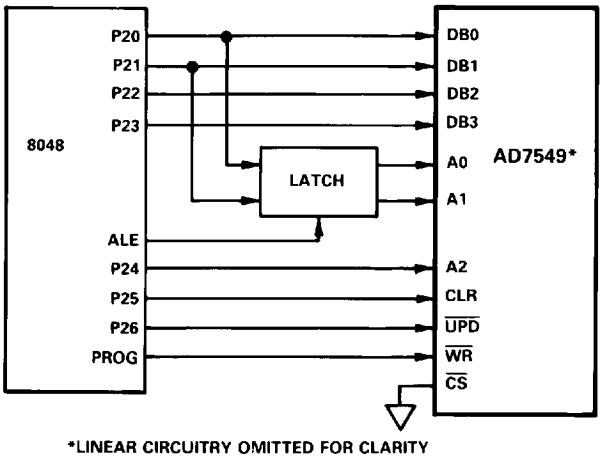


Figure 7. AD7549–8048 Interface

The combination of 8048 system and AD7549 is particularly suitable for dedicated control applications. By adding reference and output circuitry a complete control system can be configured with a minimum number of components.

AD7549 – MC6809 INTERFACE

Figure 8 is the interface circuit for the popular MC6809 8-bit microprocessor. $\overline{CS}$ and $\overline{UPD}$ signals are decoded from the address for the simultaneous update facility while the $\overline{WR}$ pulse is provided by inverting the microprocessor clock, E.

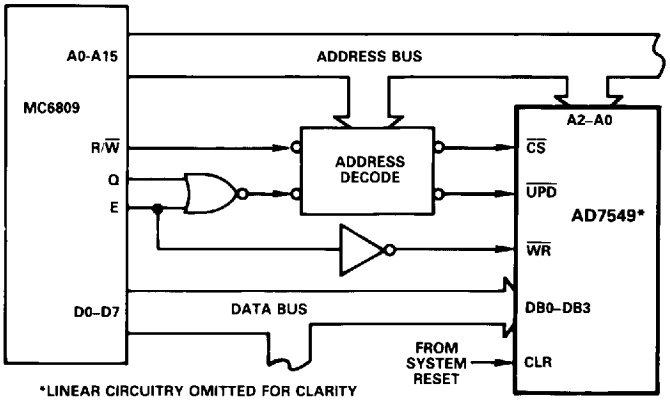
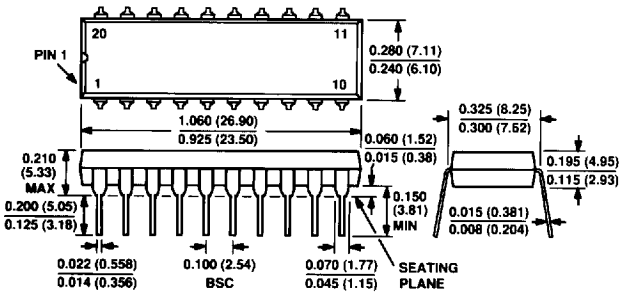


Figure 8. AD7549–MC6809 Interface

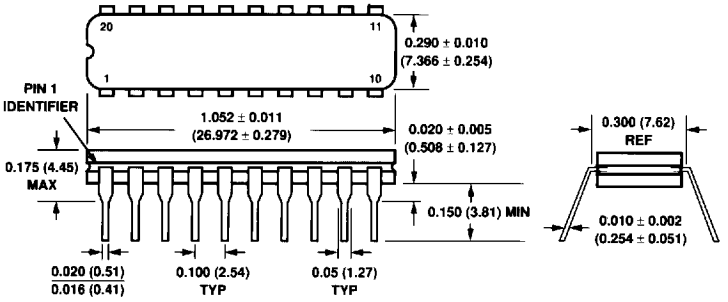
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

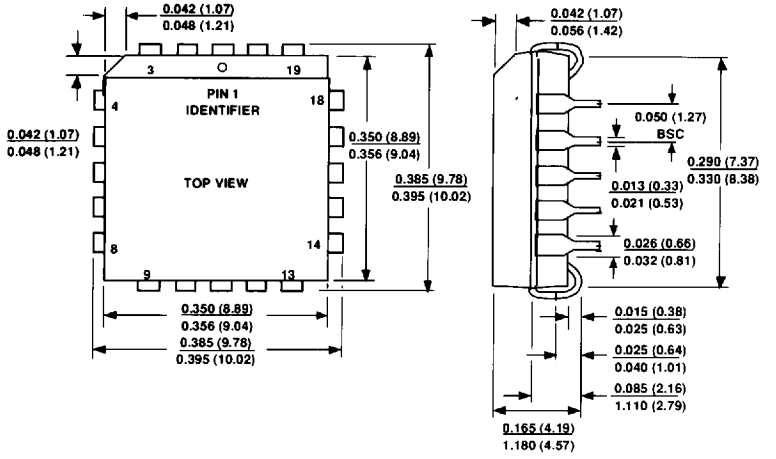
20-Pin Plastic DIP (N-20)



20-Pin Cerdip (Q-20)



20-Terminal Plastic Leaded Chip Carrier (P-20A)



E-20 LCCC E Package