# TABLE OF CONTENTS



## REVISION HISTORY

**9/2020—Rev. D to Rev. E**

Changed CP-32-2 to CP-32-7 ... Throughout
Changes to Figure 4 ... 8
Updates Outline Dimensions ... 26
Changes to Ordering Guide ... 26

**1/2018—Rev. C to Rev. D**

Changed CP-32-7 to CP-32-2 ... Throughout
Changes to Figure 1 ... 1
Changed FAULT, IFAULT, TEMP, VFAULT Parameter to FAULT, IFAULT, TEMP Parameter; Table 2 ... 4
Changes to Figure 4 and Table 5 ... 8
Updates Outline Dimensions ... 26
Changes to Ordering Guide ... 26

**3/2017—Rev. B to Rev. C**

Changed CP-32-2 to CP-32-7 ... Throughout
Changes to Figure 4 ... 8
Changes to Theory of Operation Section ... 16
Updated Outline Dimensions ... 26
Changes to Ordering Guide ... 26

**10/2013—Rev. A to Rev. B**

Changes to Table 4 ... 7
Changes to Thermal Considerations Section and Table 12 ... 24
Updated Outline Dimensions ... 26

**7/2012—Rev. 0 to Rev. A**

Changes to Figure 3 ... 6
Changes to Status Bit Read Operation Section ... 21
Updated Outline Dimensions ... 26

**7/2010—Revision 0: Initial Version**

# SPECIFICATIONS

$AV_{DD}$ = 12 V (± 10%) to 55 V (maximum), $DV_{CC}$ = 2.7 V to 5.5 V, GND = 0 V. $R_{LOAD}$ = 300 Ω. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter[1] | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| INPUT VOLTAGE RANGE | | 0 to 4.096 | | V | Output unloaded |
| Input Leakage Current | −1 | | +1 | µA | |
| REFERENCE INPUT | | | | | |
| Reference Input Voltage | | 4.096 | | V | External reference must be exactly as stated; otherwise, accuracy errors show up as error in output |
| Input Leakage Current | −1 | | +1 | µA | |
| CURRENT OUTPUT | | | | | |
| Output Current Ranges | 0 | | 24 | mA | |
| | 4 | | 20 | mA | |
| Output Current Overranges[2] | 0 | | 24.5 | mA | See Detailed Description of Features section |
| | 3.92 | | 20.4 | mA | See Detailed Description of Features section |
| ACCURACY (INTERNAL $R_{SET}$) | | | | | |
| Total Unadjusted Error (TUE) | | | | | |
| A Version[2] | −0.5 | | +0.5 | % FSR | |
| | −0.3 | ±0.15 | +0.3 | % FSR | $T_A$ = 25°C |
| Relative Accuracy (INL) | −0.02 | ±0.01 | +0.02 | % FSR | |
| Offset Error | −16 | | +16 | µA | |
| | −10 | +5 | +10 | µA | $T_A$ = 25°C |
| Offset Error TC[2] | | ±3 | | ppm FSR/°C | |
| Dead Band on Output, RTI | | 8 | 14 | mV | Referred to 4.096 V input range |
| Gain Error | −0.2 | | +0.2 | % FSR | |
| | −0.125 | ±0.02 | +0.125 | % FSR | $T_A$ = 25°C |
| Gain TC[2] | | ±10 | | ppm FSR/°C | |
| Full-Scale Error | −0.2 | | +0.2 | % FSR | |
| | −0.125 | ±0.02 | +0.125 | % FSR | $T_A$ = 25°C |
| Full-Scale TC[2] | | ±4 | | ppm FSR/°C | |
| ACCURACY (EXTERNAL $R_{SET}$) | | | | | |
| Total Unadjusted Error (TUE) | | | | | |
| A Version[2] | −0.3 | | +0.3 | % FSR | |
| | −0.1 | ±0.02 | +0.1 | % FSR | $T_A$ = 25°C |
| Relative Accuracy (INL) | −0.02 | ±0.01 | +0.02 | % FSR | |
| Offset Error | −14 | | +14 | µA | |
| | −11 | +5 | +11 | | $T_A$ = 25°C |
| Offset Error TC[2] | | ±2 | | ppm FSR/°C | |
| Dead Band on Output, RTI | | 8 | +14 | mV | Referred to 4.096 V input range |
| Gain Error | −0.08 | | +0.08 | % FSR | |
| | −0.07 | ±0.02 | +0.07 | % FSR | $T_A$ = 25°C |
| Gain TC[2] | | ±1 | | ppm FSR/°C | |
| Full-Scale Error | −0.1 | | +0.1 | % FSR | |
| | −0.07 | ±0.02 | +0.07 | % FSR | $T_A$ = 25°C |
| Full-Scale TC[2] | | ±2 | | ppm FSR/°C | |

| Parameter[1] | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| OUTPUT CHARACTERISTICS[2] | | | | | |
| Current Loop Compliance Voltage | 0 | | $AV_{DD}$ − 2.75 | V | |
| Resistive Load | | | | | Chosen such that compliance is not exceeded |
| Inductive Load | | See the Test Conditions/ Comments column | | H | Needs appropriate capacitor at higher inductance values; see the Driving Inductive Loads section |
| Settling Time | | | | | |
| 4 mA to 20 mA, Full-Scale Step | | 8.5 | | µs | 250 Ω load |
| 120 µA Step, 4 mA to 20 mA Range | | 1.2 | | µs | 250 Ω load |
| DC PSRR | | | 1 | µA/V | |
| Output Impedance | | 130 | | MΩ | |
| DIGITAL INPUTS[2] | | | | | JEDEC compliant |
| Input High Voltage, $V_{IH}$ | 2 | | | V | |
| Input Low Voltage, $V_{IL}$ | | | 0.8 | V | |
| Input Current | −1 | | +1 | µA | Per pin |
| Pin Capacitance | | 5 | | pF | Per pin |
| DIGITAL OUTPUTS[2] | | | | | |
| FAULT, IFAULT, TEMP | | | | | |
| $V_{OL}$, Output Low Voltage | | | 0.4 | V | 10 kΩ pull-up resistor to DVCC |
| | | 0.6 | | V | At 2.5 mA |
| $V_{OH}$, Output High Voltage | 3.6 | | | V | 10 kΩ pull-up resistor to DVCC |
| SDO | | | | | |
| $V_{OL}$, Output Low Voltage | 0.5 | 0.5 | | V | Sinking 200 µA |
| $V_{OH}$, Output High Voltage | $DV_{CC}$ − 0.5 | $DV_{CC}$ − 0.5 | | V | Sourcing 200 µA |
| High Impedance Output Capacitance | | 3 | | pF | |
| High Impedance Leakage Current | −1 | | +1 | µA | |
| POWER REQUIREMENTS | | | | | |
| $AV_{DD}$ | 10.8 | | 55 | V | |
| $DV_{CC}$ | | | | | |
| Input Voltage | 2.7 | | 5.5 | V | |
| $AI_{DD}$ | | 4.4 | 5.6 | mA | Output unloaded, output disabled; R3, R2, R1, R0 = 0000, RSET = 0 |
| | | 5.2 | 6.2 | mA | Output enabled |
| $DI_{CC}$ | | 0.3 | 1 | mA | $V_{IH} = DV_{CC}$, $V_{IL}$ = GND |
| Power Dissipation | | 108 | | mW | $AV_{DD}$ = 24 V, output unloaded |

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Guaranteed by design and characterization, not production tested.

## TIMING CHARACTERISTICS

$AV_{DD}$ = 12 V (± 10%) to 55 V (maximum), $DV_{CC}$ = 2.7 V to 5.5 V, GND = 0 V. $R_{LOAD}$ = 300 Ω. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter[1, 2] | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description |
|---|---|---|---|
| $t_1$ | 20 | ns min | SCLK cycle time |
| $t_2$ | 8 | ns min | SCLK high time |
| $t_3$ | 8 | ns min | SCLK low time |
| $t_4$ | 5 | ns min | $\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time |
| $t_5$ | 10 | ns min | 16th SCLK falling edge to $\overline{\text{SYNC}}$ rising edge (on 24th SCLK falling edge if using PEC) |
| $t_6$ | 5 | ns min | Minimum $\overline{\text{SYNC}}$ high time (write mode) |
| $t_7$ | 5 | ns min | Data setup time |
| $t_8$ | 5 | ns min | Data hold time |
| $t_9$, $t_{10}$ | 1.5 | µs max | CLEAR pulse low/high activation time |
| $t_{11}$ | 5 | ns min | Minimum $\overline{\text{SYNC}}$ high time (read mode) |
| $t_{12}$ | 40 | ns max | SCLK rising edge to SDO valid (SDO $C_L$ = 15 pF) |
| $t_{13}$ | 10 | ns min | $\overline{\text{RESET}}$ pulse low time |

[1] Guaranteed by characterization, but not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of $DV_{CC}$) and timed from a voltage level of 1.2 V.

### *Timing Diagrams*

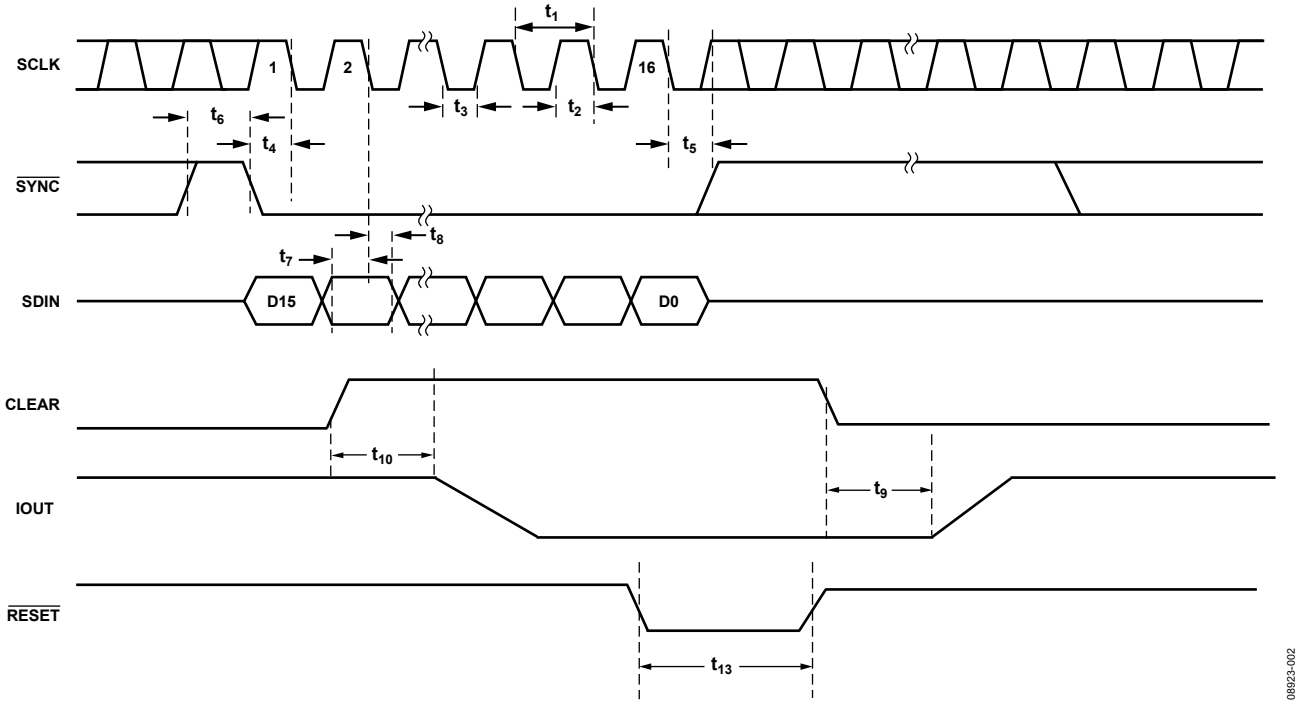



*Figure 2. Write Mode Timing Diagram*

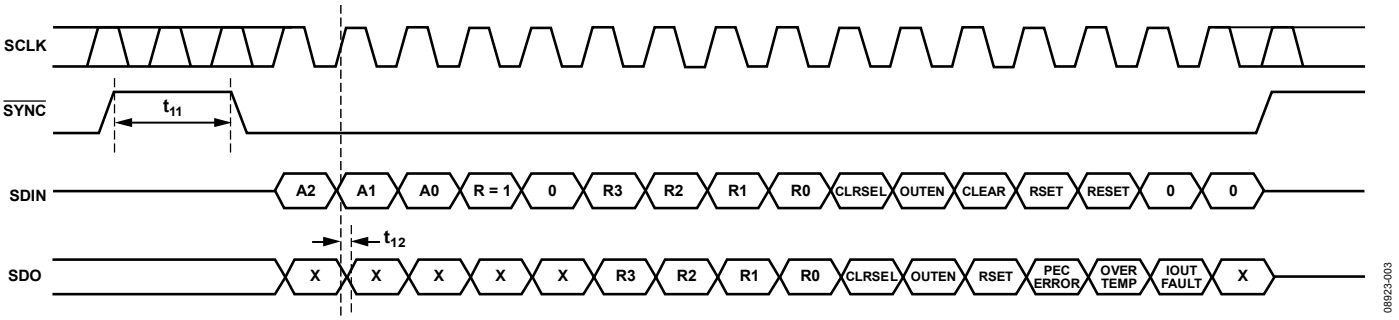



*Figure 3. Readback Mode Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

**Table 4.**

| Parameter | Rating |
|---|---|
| AVDD to GND | −0.3 V to +58 V |
| DVCC to GND | −0.3 V to +7 V |
| Digital Inputs to GND | −0.3 V to $DV_{CC}$ + 0.3 V, or 7 V (whichever is less) |
| Digital Outputs to GND | −0.3 V to $DV_{CC}$ + 0.3 V, or 7 V (whichever is less) |
| VREF to GND | −0.3 V to +7 V |
| VIN to GND | −0.3 V to +7 V |
| IOUT to GND | −0.3 V to $AV_{DD}$ |
| Operating Temperature Range | |
| Industrial | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature ($T_J$ max) | 125°C |
| 32-Lead LFCSP Package | |
| $\theta_{JA}$ Thermal Impedance[1] | 42°C/W |
| Lead Temperature | JEDEC industry standard |
| Soldering | J-STD-020 |

[1] Simulated data based on a JEDEC 2S2P test board with thermal vias.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

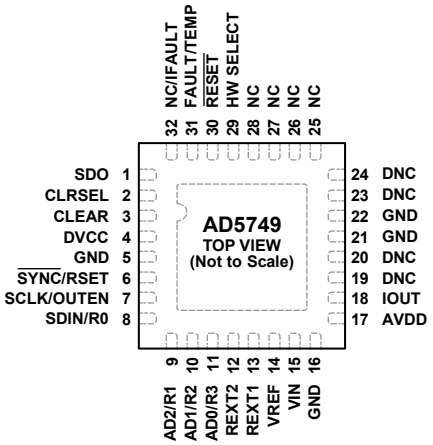



*Figure 4. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | SDO | Serial Data Output (SDO). In software mode, this pin is used to clock data from the input shift register in readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK. This pin is a CMOS output. |
| 2 | CLRSEL | In hardware or software mode, this pin selects the clear value, either zero scale or midscale. In software mode, this pin is implemented as a logic OR with the internal CLRSEL bit. |
| 3 | CLEAR | Active High Input. Asserting this pin sets the output current to zero-scale code or midscale of range selected (user selectable). CLEAR is a logic OR with the internal CLEAR bit. See the Asynchronous Clear (CLEAR) section for more details. |
| 4 | DVCC | Digital Power Supply. |
| 5 | GND | Ground Connection. |
| 6 | $\overline{\text{SYNC}}$/RSET | Positive Edge-Sensitive Latch ($\overline{\text{SYNC}}$). In software mode, a rising edge parallel loads the input shift register data into the AD5749 and also updates the output.<br>Resistor Select (RSET). In hardware mode, this pin selects whether the internal or the external current sense resistor is used.<br>If RSET = 0, the external sense resistor is chosen.<br>If RSET = 1, the internal sense resistor is chosen. |
| 7 | SCLK/OUTEN | Serial Clock Input (SCLK). In software mode, data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz.<br>Output Enable (OUTEN). In hardware mode, this pin acts as an output enable pin. |
| 8 | SDIN/R0 | Serial Data Input (SDIN). In software mode, data must be valid on the falling edge of SCLK.<br>Range Decode Bit (R0). In hardware mode, this pin, in conjunction with R1, R2, and R3, selects the output current range setting on the part. |
| 9 | AD2/R1 | Device Addressing Bit (AD2). In software mode, this pin, in conjunction with AD0 and AD1, allows up to eight devices to be addressed on one bus.<br>Range Decode Bit (R1). In hardware mode, this pin, in conjunction with R0, R2, and R3, selects the output current range setting on the part. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 10 | AD1/R2 | Device Addressing Bit (AD1). In software mode, this pin, in conjunction with AD0 and AD2, allows up to eight devices to be addressed on one bus.<br>Range Decode Bit (R2). In hardware mode, this pin, in conjunction with R0, R1, and R3, selects the output current range setting on the part. |
| 11 | AD0/R3 | Device Addressing Bit (AD0). In software mode, this pin, in conjunction with AD1 and AD2, allows up to eight devices to be addressed on one bus.<br>Range Decode Bit (R3). In hardware mode, this pin, in conjunction with R0, R1, and R2, selects the output current range setting on the part. |
| 12, 13 | REXT2, REXT1 | A 15 kΩ external current setting resistor can be connected between the REXT1 and REXT2 pins to improve the IOUT temperature drift performance. |
| 14 | VREF | Buffered Reference Input. |
| 15 | VIN | Buffered Analog Input (0 V to 4.096 V). |
| 16 | GND | Ground Connection. |
| 17 | AVDD | Positive Analog Supply. |
| 18 | IOUT | Current Output. |
| 19, 20, 23, 24 | DNC | Do not connect to these pins. |
| 21, 22 | GND | Ground Connection. |
| 25, 26, 27, 28 | NC | No Connect. Can be tied to GND. |
| 29 | HW SELECT | This part is used to configure the part to hardware or software mode.<br>HW SELECT = 0 selects software control.<br>HW SELECT = 1 selects hardware control. |
| 30 | $\overline{\text{RESET}}$ | In software mode, this pin resets the part to its power-on state. Active low.<br>In hardware mode, there is no reset. If using the part in hardware mode, the $\overline{\text{RESET}}$ pin should be tied high. |
| 31 | FAULT/TEMP | Fault Alert (FAULT). In software mode, this pin acts as a general fault alert pin. It is asserted low when an open-circuit, overtemperature error, or PEC interface error is detected. This pin is an open-drain output and must be connected to a pull-up resistor.<br>Overtemperature Fault (TEMP). In hardware mode, this pin acts as an overtemperature fault pin. It is asserted low when an overtemperature error is detected. This pin is an open-drain output and must be connected to a pull-up resistor. |
| 32 | NC/IFAULT | No Connect (NC). In software mode, this pin is a no connect. Instead, tie this pin to GND.<br>Open-Circuit Fault Alert (IFAULT). In hardware mode, this pin acts as an open-circuit fault alert pin. It is asserted low when an open-circuit error is detected. This pin is an open-drain output and must be connected to a pull-up resistor. |
| 33 (EPAD) | EPAD | The exposed paddle is tied to GND. |

# TYPICAL PERFORMANCE CHARACTERISTICS

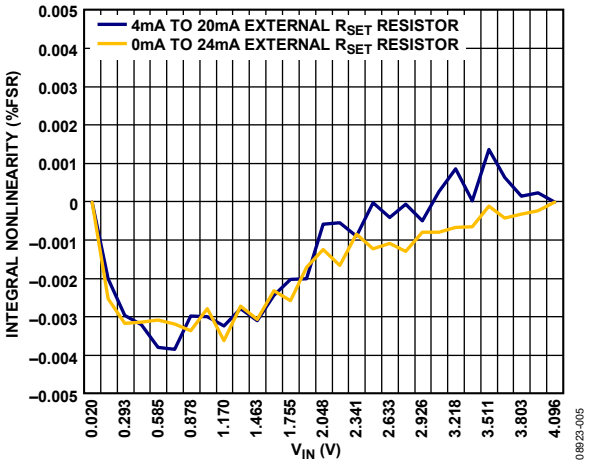



Figure 5. Integral Nonlinearity Error vs. $V_{IN}$, External $R_{SET}$ Resistor

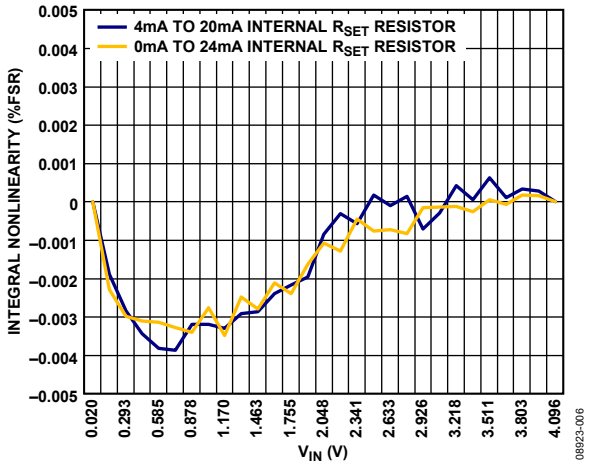



Figure 6. Integral Nonlinearity Error vs. $V_{IN}$, Internal $R_{SET}$ Resistor

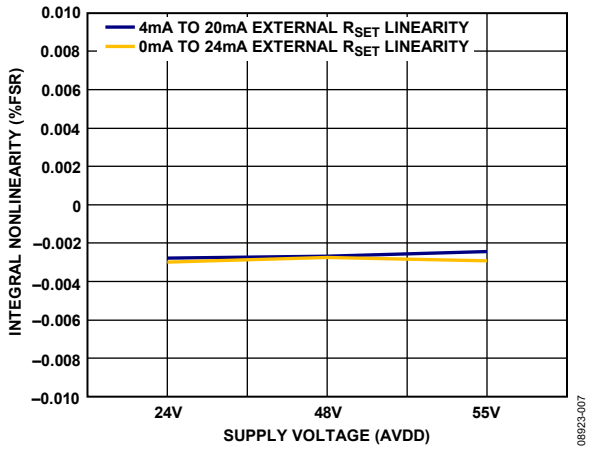



Figure 7. Integral Nonlinearity Current Mode, External $R_{SET}$ Sense Resistor

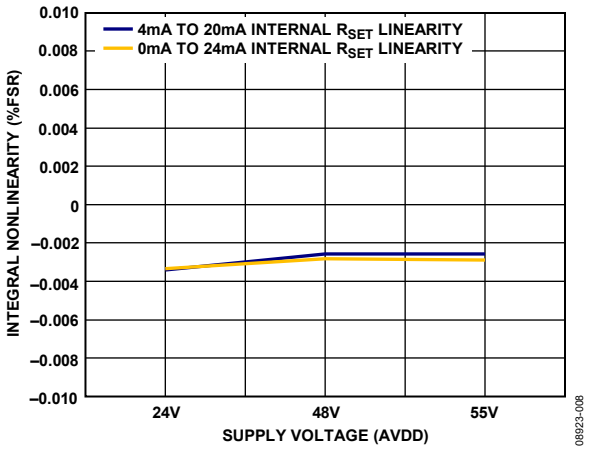



Figure 8. Integral Nonlinearity Current Mode, Internal $R_{SET}$ Sense Resistor

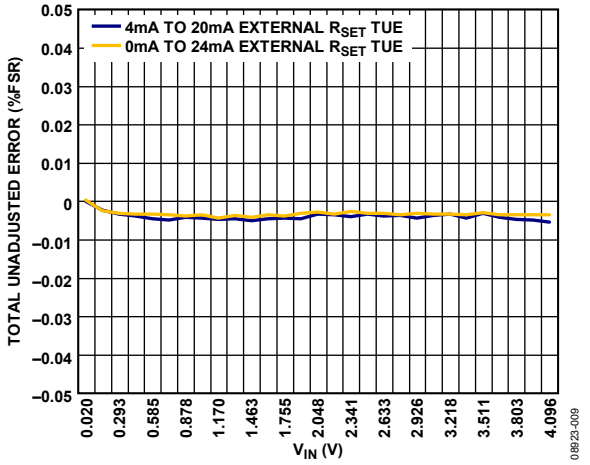



Figure 9. Total Unadjusted Error vs. $V_{IN}$, External $R_{SET}$ Resistor

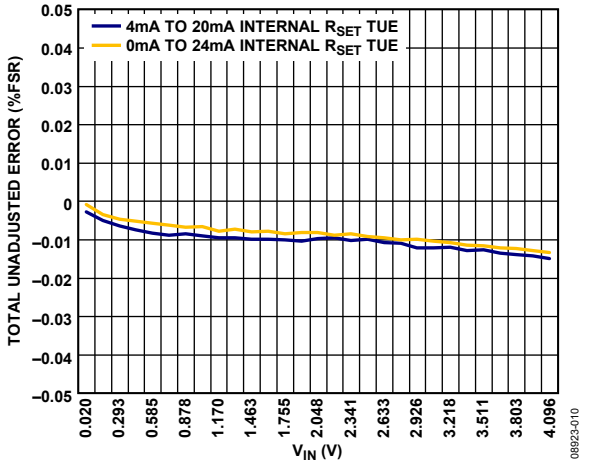



Figure 10. Total Unadjusted Error vs. $V_{IN}$, Internal $R_{SET}$ Resistor

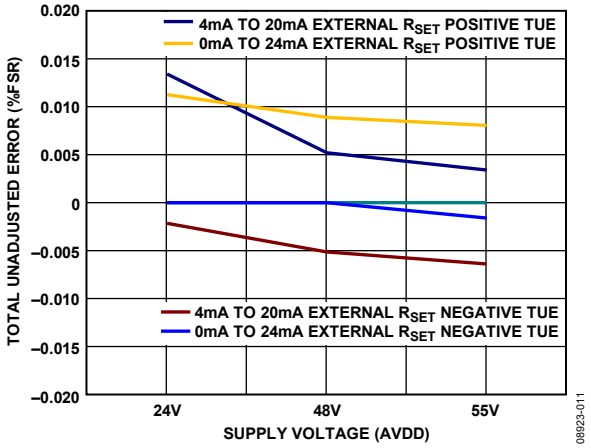



*Figure 11. Total Unadjusted Error Current Mode, External $R_{SET}$ Sense Resistor*

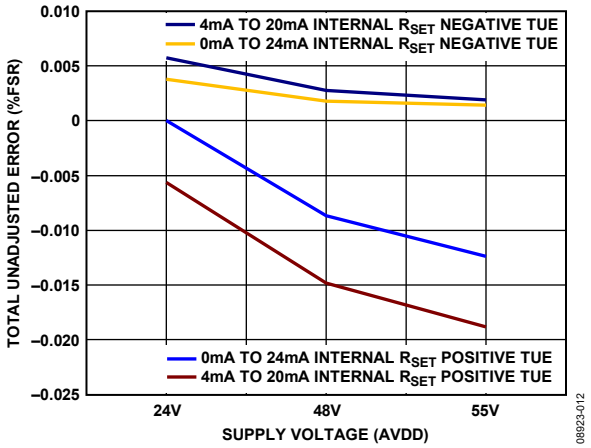



*Figure 12. Total Unadjusted Error Current Mode, Internal $R_{SET}$ Sense Resistor*

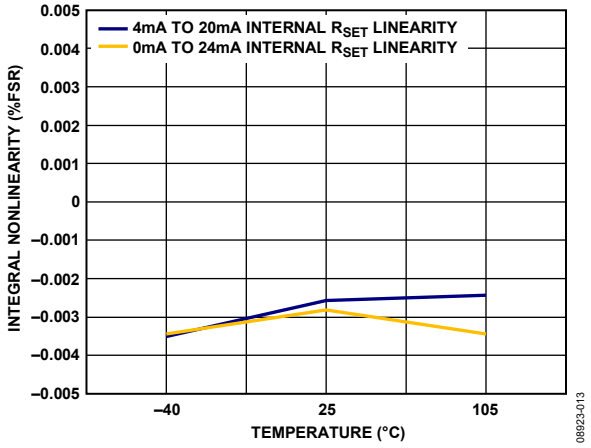



*Figure 13. Integral Nonlinearity Error vs. Temperature, Internal $R_{SET}$ Sense Resistor*

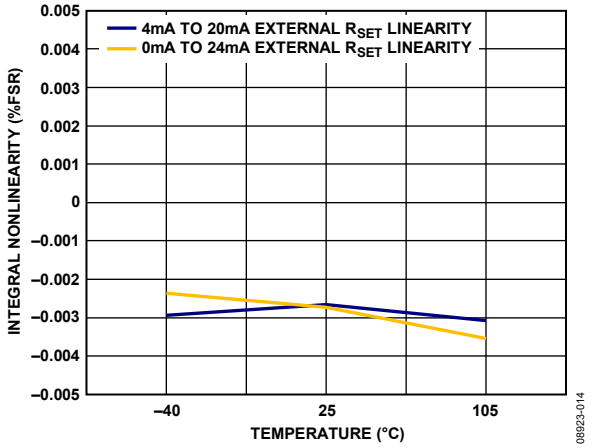



*Figure 14. Integral Nonlinearity Error vs. Temperature, External $R_{SET}$ Sense Resistor*

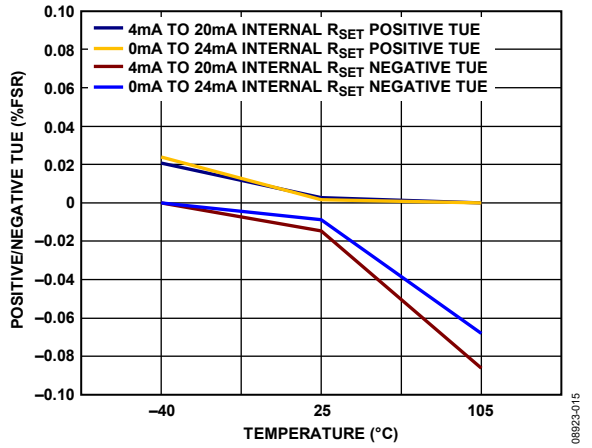



*Figure 15. Total Unadjusted Error vs. Temperature, Internal $R_{SET}$ Sense Resistor*

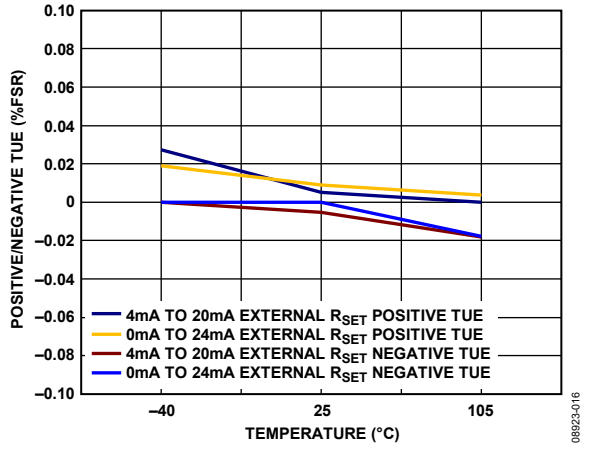



*Figure 16. Total Unadjusted Error vs. Temperature, External $R_{SET}$ Sense Resistor*

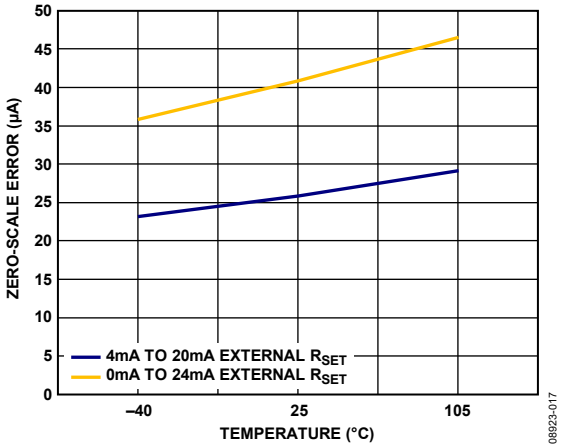



Figure 17. Zero-Scale Error vs. Temperature, External $R_{SET}$ Sense Resistor

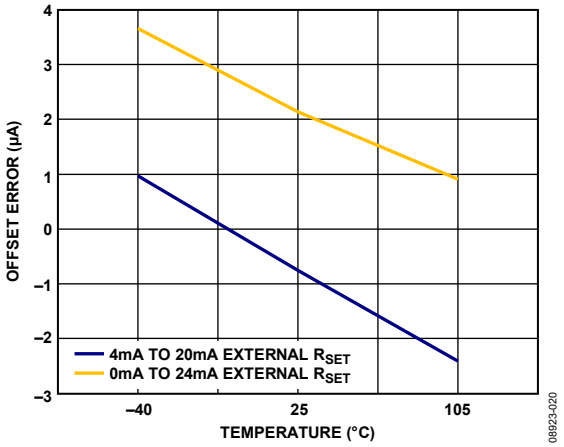



Figure 20. Offset Error vs. Temperature, External $R_{SET}$ Sense Resistor

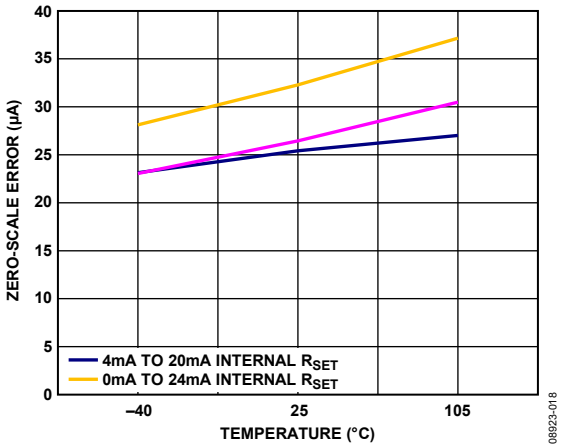



Figure 18. Zero-Scale Error vs. Temperature, Internal $R_{SET}$ Sense Resistor

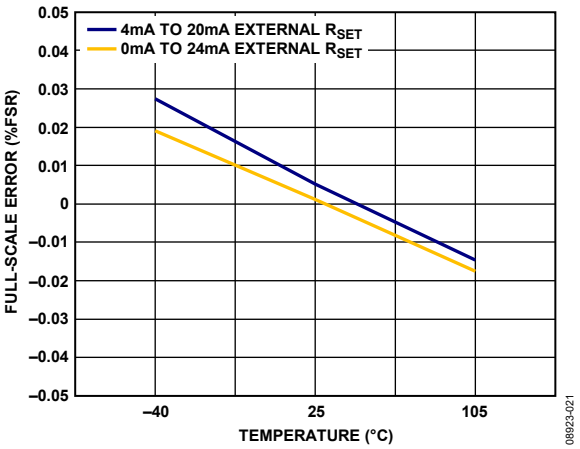



Figure 21. Full-Scale Error vs. Temperature, External $R_{SET}$ Sense Resistor

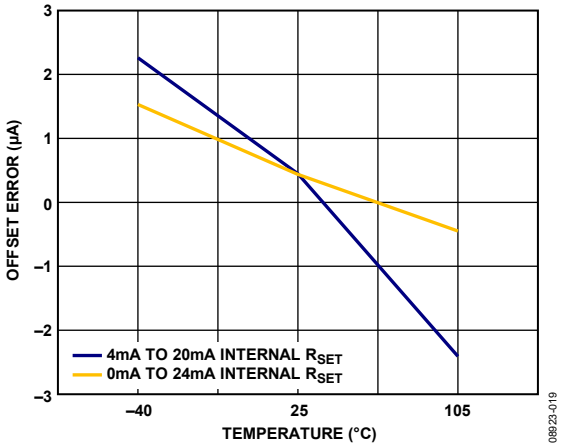



Figure 19. Offset Error vs. Temperature, Internal $R_{SET}$ Sense Resistor

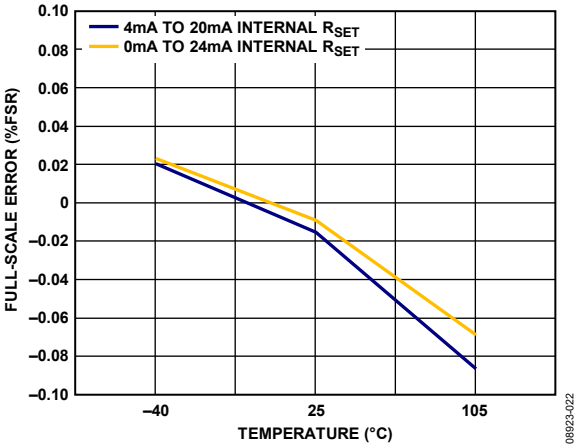



Figure 22. Full-Scale Error vs. Temperature, Internal $R_{SET}$ Sense Resistor

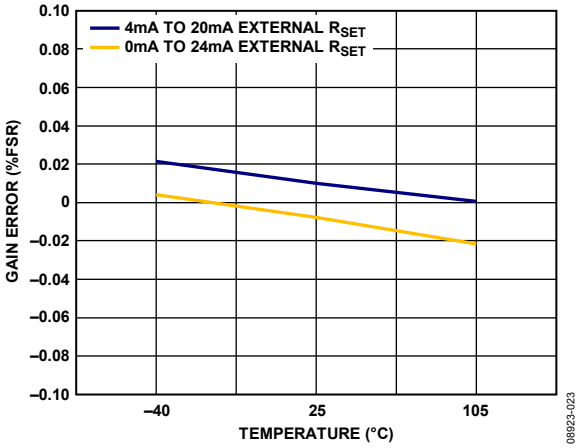



Figure 23. Gain Error vs. Temperature, External $R_{SET}$ Sense Resistor

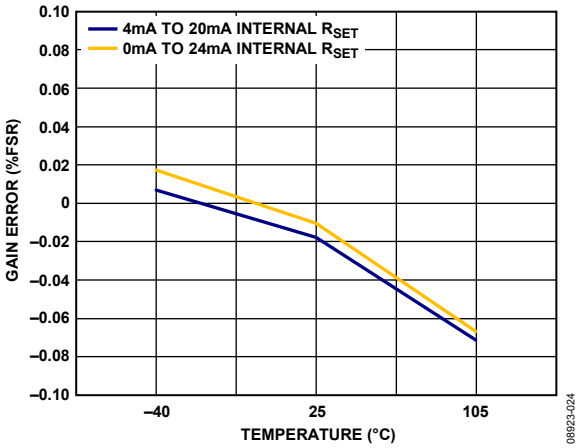



Figure 24. Gain Error vs. Temperature, Internal $R_{SET}$ Sense Resistor

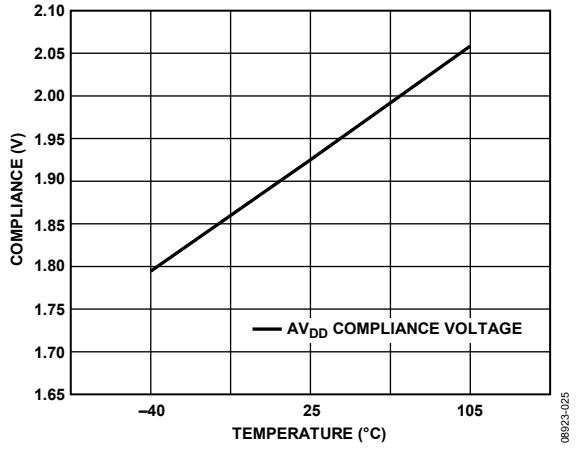



Figure 25. Output Compliance vs. Temperature
Tested When $I_{OUT}$ = 10.8 mA, 0 mA to 24 mA Range Selected

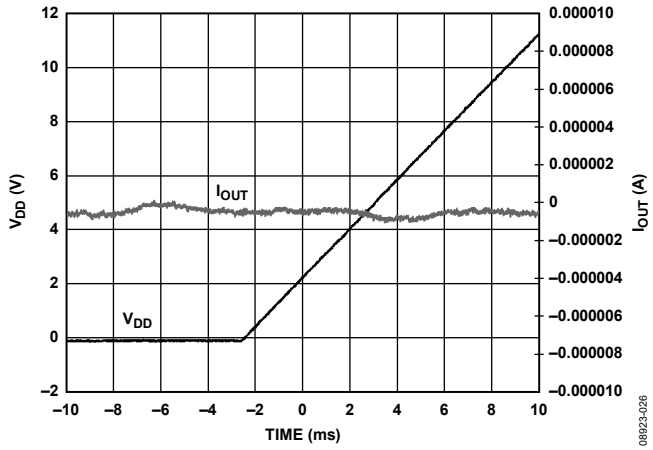



Figure 26. Output Current vs. Time on $V_{DD}$ Power-Up

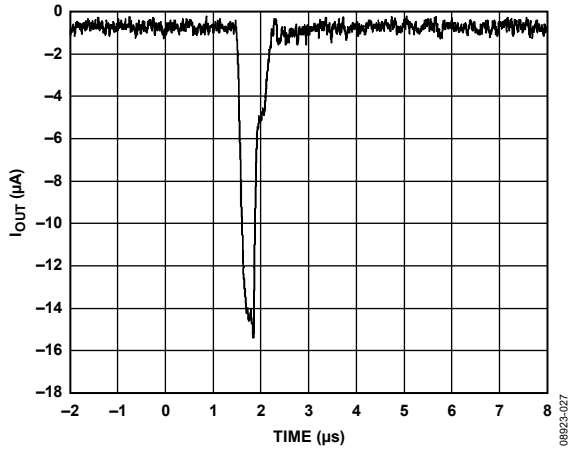



Figure 27. Output Current vs. Time on Output Enable, 0 mA to 24 mA Range

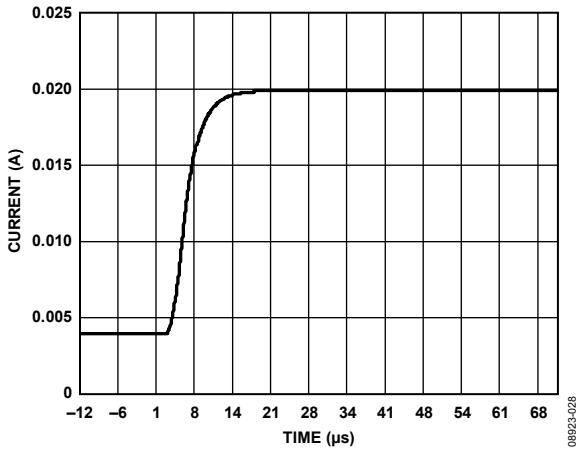



Figure 28. 4 mA to 20 mA Output Current Step

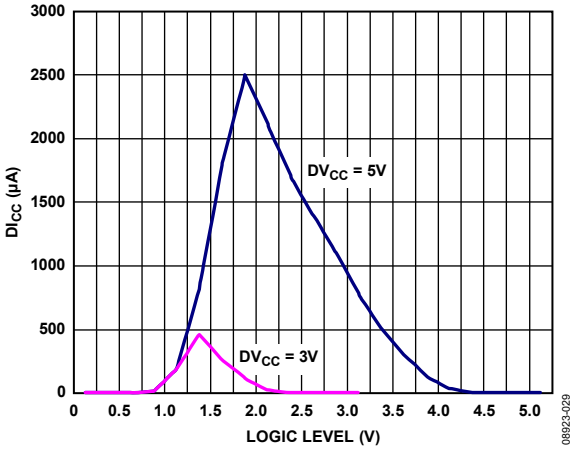



Figure 29. $DI_{CC}$ vs. Logic Input Voltage

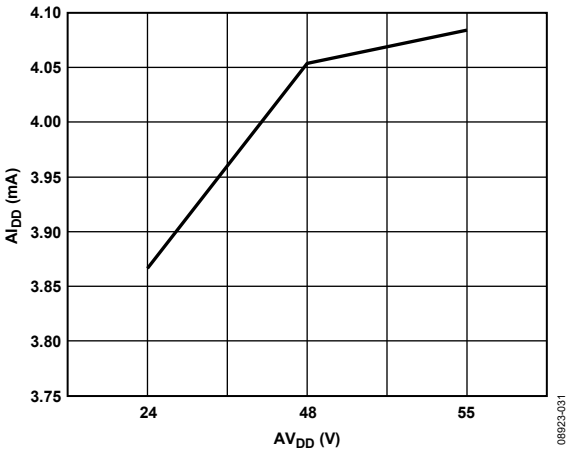



Figure 30. $AI_{DD}$ vs. $AV_{DD}$, $I_{OUT}$ = 0 mA

# TERMINOLOGY

**Total Unadjusted Error (TUE)**
TUE is a measure of the output error taking all the various errors into account: INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed as a percentage of full-scale range (% FSR).

**Relative Accuracy or Integral Nonlinearity (INL)**
INL is a measure of the maximum deviation, in % FSR, from a straight line passing through the endpoints of the output driver transfer function. A typical INL vs. input voltage plot is shown in Figure 5.

**Full-Scale Error**
Full-scale error is the deviation of the actual full-scale analog output from the ideal full-scale output. Full-scale error is expressed as a percentage of full-scale range (% FSR).

**Full-Scale TC**
Full-scale TC is a measure of the change in the full-scale error with a change in temperature. It is expressed in ppm FSR/°C.

**Gain Error**
Gain error is a measure of the span error of the output. It is the deviation in slope of the output transfer characteristic from the ideal expressed in % FSR. A plot of gain error vs. temperature is shown in Figure 23.

**Gain Error TC**
Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/°C.

**Zero-Scale Error**
Zero-scale error is the deviation of the actual zero-scale analog output from the ideal zero-scale output. Zero-scale error is expressed in millivolts (mV).

**Zero-Scale TC**
Zero-scale TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

**Offset Error**
Offset error is a measurement of the difference between the actual VOUT and the ideal VOUT expressed in millivolts (mV) in the linear region of the transfer function. It can be negative or positive.

**Output Voltage Settling Time**
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a half-scale input change.

**Slew Rate**
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is expressed in V/µs.

**Current Loop Voltage Compliance**
Current loop voltage compliance is the maximum voltage at the IOUT pin for which the output current is equal to the programmed value.

**Power-On Glitch Energy**
Power-on glitch energy is the impulse injected into the analog output when the AD5749 is powered on. It is specified as the area of the glitch in nV-sec.

**Power Supply Rejection Ratio (PSRR)**
PSRR indicates how the output is affected by changes in the power supply voltage.

# THEORY OF OPERATION

The AD5749 is a single-channel, low cost, precision, current output driver with hardware or software programmable output ranges. The software ranges are configured via an SPI-/MICROWIRE-compatible serial interface. The hardware ranges are programmed using the range pins (R0 to R3). The analog input to the AD5749 is provided from a low voltage, single-supply DAC (0 V to 4.096 V), which is internally conditioned to provide the desired output current range.

The output current range is programmable across two ranges: 0 mA to 24 mA, or 4 mA to 20 mA. An overrange of 2% is available on the 0 mA to 24 mA and 4 mA to 20 mA current ranges. The output range is selected by programming the R3 to R0 bits in the control register (see Table 7 and Table 8).

Figure 31 and Figure 32 show a typical configuration of AD5749 in software mode and in hardware mode, respectively, in an output module system. The HW SELECT pin chooses whether the part is configured in software or hardware mode. The analog input to the AD5749 is provided from a low voltage, single-supply DAC such as the AD5060 and AD5066 or AD5660 and AD5668, which can provide an output range of 0 V to 4.096 V. The supply and reference for the DAC, as well as the reference for the AD5749, can be supplied from a reference such as the ADR392. The AD5749 can operate with a single supply up to 55 V.

## SOFTWARE MODE

The software-selectable output ranges are 0 mA to 24 mA, or 4 mA to 20 mA.

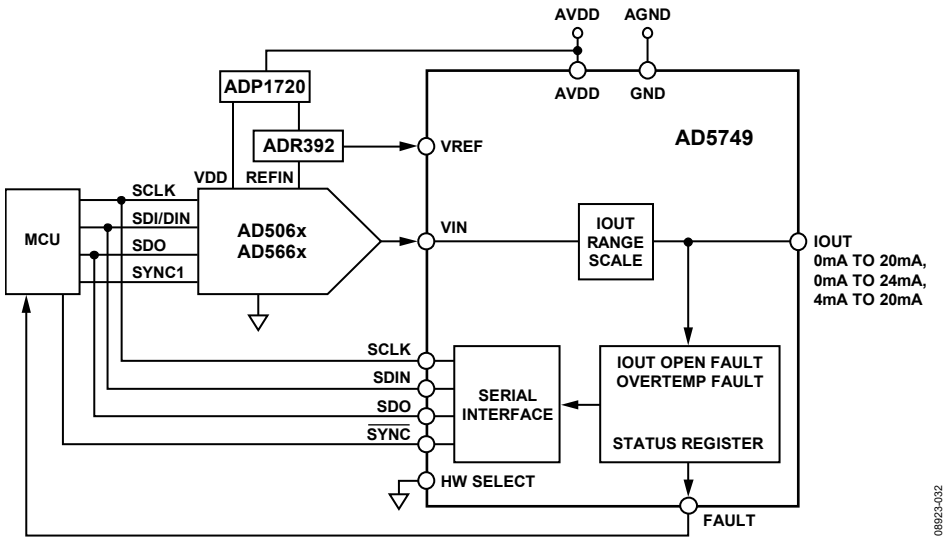



*Figure 31. Typical System Configuration in Software Mode (Pull-Up Resistors Not Shown for Open-Drain Outputs)*

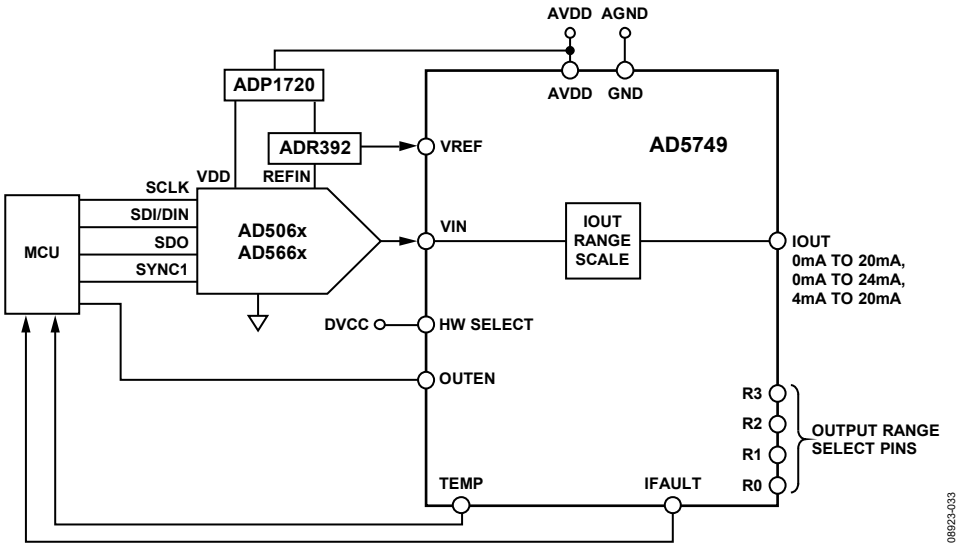



*Figure 32. Typical System Configuration in Hardware Mode Using Internal DAC Reference (Pull-Up Resistors Not Shown for Open-Drain Outputs)*

**Table 6. Suggested Parts for Use with the AD5749**

| DAC | Reference | Power | Resolution/Accuracy | Description |
|---|---|---|---|---|
| AD5660 | Internal | ADP1720[1] | 16-bit/12-bit | Mid-end system, single channel, internal reference |
| AD5664R | Internal | N/A | 16-bit/12-bit | Mid-end system, quad channel, internal reference |
| AD5668 | Internal | N/A | 16-bit/12-bit | Mid-end system, octal channel, internal reference |
| AD5060 | ADR434 | ADP1720 | 16-bit/16-bit | High-end system, single channel, external reference |
| AD5064/AD5066 | ADR434 | N/A | 16-bit/16-bit | High-end system, quad channel, external reference |
| AD5662 | ADR392[2] | ADR392[2] | 16-bit/12-bit | Mid-end system, single channel, external reference |
| AD5664 | ADR392[2] | N/A | 16-bit/12-bit | Mid-end system, quad channel, external reference |

[1] ADP1720 input range up to 28 V.
[2] ADR392 input range up to 15 V.

## CURRENT OUTPUT ARCHITECTURE

The voltage input from the analog input VIN core (0 V to 4.096 V) is converted to a current (see Figure 33), which is then mirrored to the supply rail so that the application simply sees a current source output with respect to an internal reference voltage. The reference is used to provide internal offsets for range and gain scaling. The selectable output range is programmable through the digital interface (software mode) or via the range pins (R0 to R3) (hardware mode).

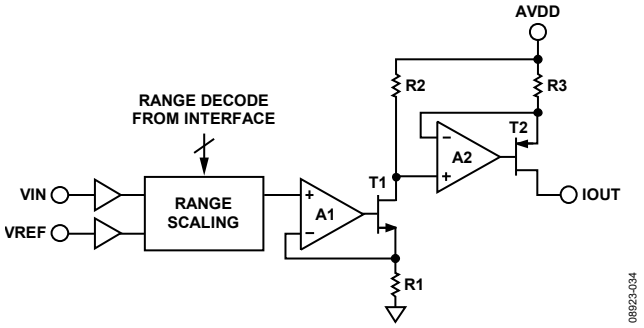



*Figure 33. Current Output Configuration*

## DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads, connect a 0.01 µF capacitor between IOUT and GND. This ensures stability with loads beyond 50 mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling.

## POWER-ON STATE OF THE AD5749

On power-up, the AD5749 senses whether hardware or software mode is loaded and sets the power-up conditions accordingly.

In software SPI mode, the output powers up in the tristate condition (0 mA).

To put the part into normal operation, the user must set the OUTEN bit in the control register to enable the output and, in the same write, set the output range configuration using the R3 to R0 range bits. If the CLEAR pin is still high (active) during this write, the part automatically clears to its normal clear state as defined by the programmed range and by the CLRSEL pin or the CLRSEL bit (see the Asynchronous Clear (CLEAR) section for more details). The CLEAR pin must be taken low to operate the part in normal mode.

The CLEAR pin is typically driven directly from a microcontroller. In cases where the power supply for the AD5749 supply is independent of the microcontroller power supply, the user can connect a weak pull-up resistor to DVCC or a pull-down resistor to ground to ensure that the correct power-up condition is achieved independent of the microcontroller. A 10 kΩ pull-up/pull-down resistor on the CLEAR pin should be sufficient for most applications.

If hardware mode is selected, the part powers up to the conditions defined by the R3 to R0 range bits and the status of the OUTEN or CLEAR pin. It is recommended to keep the output disabled when powering up the part in hardware mode.

## DEFAULT REGISTERS AT POWER-ON

The AD5749 power-on-reset circuit ensures that all registers are loaded with zero code.

In software SPI mode, the part powers up with the output disabled (OUTEN bit = 0). The user must set the OUTEN bit in the control register to enable the output and, in the same write, set the output range configuration using the R3 to R0 bits.

If hardware mode is selected, the part powers up to the conditions defined by the R3 to R0 bits and the status of the OUTEN pin. It is recommended to keep the output disabled when powering up the part in hardware mode.

## RESET FUNCTION

In software mode, the part can be reset using the $\overline{\text{RESET}}$ pin (active low) or the reset bit (reset = 1). A reset disables the output to its power-on condition. The user must write to the OUTEN bit to enable the output and, in the same write, set the output range configuration. The $\overline{\text{RESET}}$ pin is a level sensitive input; the part stays in reset mode as long as the $\overline{\text{RESET}}$ pin is low. The reset bit clears to 0 following a reset command to the control register.

In hardware mode, there is no reset. If using the part in hardware mode, the $\overline{\text{RESET}}$ pin should be tied high.

## OUTEN

In software mode, the output can be enabled or disabled using the OUTEN bit in the control register. When the output is disabled, it is placed into tristate. The user must set the OUTEN bit to enable the output and simultaneously set the output range configuration.

In hardware mode, the output can be enabled or disabled using the OUTEN pin. When the output is disabled, it is placed into tristate. The user must write to the OUTEN pin to enable the output. It is recommended that the output be disabled when changing the ranges.

## SOFTWARE CONTROL

Software control is enabled by connecting the HW SELECT pin to ground. In software mode, the AD5749 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 50 MHz. It is compatible with SPI, QSPI™, MICROWIRE, and DSP standards.

### *Input Shift Register*

The input shift register is 16 bits wide. Data is loaded into the device MSB first as a 16-bit word under the control of a serial clock input, SCLK. Data is clocked in on the falling edge of SCLK. The input shift register consists of 16 control bits, as shown in Table 7. The timing diagram for this write operation is shown in Figure 2. The first three bits of the input shift register are used to set the hardware address of the AD5749 device on the printed circuit board (PCB). Up to eight devices can be addressed per board.

Bit D11, Bit D1, and Bit D0 must always be set to 0 during any write sequence.

**Table 7. Input Shift Register Contents for a Write Operation—Control Register**

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| A2 | A1 | A0 | R/$\overline{W}$ | 0 | R3 | R2 | R1 | R0 | CLRSEL | OUTEN | CLEAR | RSET | RESET | 0 | 0 |

**Table 8. Input Shift Register Descriptions for Control Register**

| **Bit** | **Description** | | | | | |
|---|---|---|---|---|---|---|
| A2, A1, A0 | Used in association with the AD2, AD1, and AD0 external pins to determine which part is being addressed by the system controller. | | | | | |
| | **A2** | **A1** | **A0** | **Function** | | |
| | 0 | 0 | 0 | Addresses part with Pin AD2 = 0, Pin AD1 = 0, Pin AD0 = 0. | | |
| | 0 | 0 | 1 | Addresses part with Pin AD2 = 0, Pin AD1 = 0, Pin AD0 = 1. | | |
| | 0 | 1 | 0 | Addresses part with Pin AD2 = 0, Pin AD1 = 1, Pin AD0 = 0. | | |
| | 0 | 1 | 1 | Addresses part with Pin AD2 = 0, Pin AD1 = 1, Pin AD0 = 1. | | |
| | 1 | 0 | 0 | Addresses part with Pin AD2 = 1, Pin AD1 = 0, Pin AD0 = 0. | | |
| | 1 | 0 | 1 | Addresses part with Pin AD2 = 1, Pin AD1 = 0, Pin AD0 = 1. | | |
| | 1 | 1 | 0 | Addresses part with Pin AD2 = 1, Pin AD1 = 1, Pin AD0 = 0. | | |
| | 1 | 1 | 1 | Addresses part with Pin AD2 = 1, Pin AD1 = 1, Pin AD0 = 1. | | |
| R/$\overline{W}$ | Indicates a read from or a write to the addressed register. | | | | | |
| R3, R2, R1, R0 | Selects the output configuration in conjunction with RSET. | | | | | |
| | **RSET** | **R3** | **R2** | **R1** | **R0** | **Output Configuration** |
| | 0 | 0 | 0 | 0 | 0 | 4 mA to 20 mA (external 15 kΩ current sense resistor). |
| | 0 | 0 | 0 | 0 | 1 | Unused command. Do not program. |
| | 0 | 0 | 0 | 1 | 0 | 0 mA to 24 mA (external 15 kΩ current sense resistor). |
| | 0 | 0 | 0 | 1 | 1 | Unused command. Do not program. |
| | 0 | 0 | 1 | 0 | 0 | Unused command. Do not program. |
| | 0 | 0 | 1 | 0 | 1 | Unused command. Do not program. |
| | 0 | 0 | 1 | 1 | 0 | Unused command. Do not program. |
| | 0 | 0 | 1 | 1 | 1 | Unused command. Do not program. |
| | 0 | 1 | 0 | 0 | 0 | Unused command. Do not program. |
| | 0 | 1 | 0 | 0 | 1 | Unused command. Do not program. |
| | 0 | 1 | 0 | 1 | 0 | Unused command. Do not program. |
| | 0 | 1 | 0 | 1 | 1 | Unused command. Do not program. |
| | 0 | 1 | 1 | 0 | 0 | Unused command. Do not program. |
| | 0 | 1 | 1 | 0 | 1 | Unused command. Do not program. |
| | 0 | 1 | 1 | 1 | 0 | Unused command. Do not program. |
| | 0 | 1 | 1 | 1 | 1 | Unused command. Do not program. |
| | 1 | 0 | 0 | 0 | 0 | 4 mA to 20 mA (internal current sense resistor). |
| | 1 | 0 | 0 | 0 | 1 | Unused command. Do not program. |
| | 1 | 0 | 0 | 1 | 0 | 0 mA to 24 mA (internal current sense resistor). |
| | 1 | 0 | 0 | 1 | 1 | Unused command. Do not program. |
| | 1 | 0 | 1 | 0 | 0 | Unused command. Do not program. |
| | 1 | 0 | 1 | 0 | 1 | Unused command. Do not program. |
| | 1 | 0 | 1 | 1 | 0 | Unused command. Do not program. |
| | 1 | 0 | 1 | 1 | 1 | Unused command. Do not program. |
| | 1 | 1 | 0 | 0 | 0 | Unused command. Do not program. |
| | 1 | 1 | 0 | 0 | 1 | Unused command. Do not program. |
| | 1 | 1 | 0 | 1 | 0 | Unused command. Do not program. |
| | 1 | 1 | 0 | 1 | 1 | Unused command. Do not program. |
| | 1 | 1 | 1 | 0 | 0 | Unused command. Do not program. |
| | 1 | 1 | 1 | 0 | 1 | 3.92 mA to 20.4 mA (internal current sense resistor). |
| | 1 | 1 | 1 | 1 | 0 | Unused command. Do not program. |
| | 1 | 1 | 1 | 1 | 1 | 0 mA to 24.5 mA (internal current sense resistor). |

| Bit | Description | |
|---|---|---|
| CLRSEL | Sets clear mode to zero scale or midscale. See the Asynchronous Clear (CLEAR) section. | |
| | **CLRSEL** | **Function** |
| | 0 | Clear to zero-scale. |
| | 1 | Clear to midscale. |
| OUTEN | Output enable bit. This bit must be set to 1 to enable the output. | |
| CLEAR | Software clear bit; active high. | |
| RSET | Select internal/external current sense resistor. | |
| | **RSET** | **Function** |
| | 1 | Select internal current sense resistor; used with R3 to R0 bits to select range. |
| | 0 | Select external current sense resistor; used with R3 to R0 bits to select range. |
| RESET | Resets the part to its power-on state. | |

### *Status Bit Read Operation*

A read of the status bits can be initiated as part of a normal write operation. The read is activated by selecting the correct device address (A2, A1, A0) and then setting the R/$\overline{W}$ bit to 1. By default, the SDO pin is disabled. After having addressed the AD5749 and setting R/$\overline{W}$ to 1 the SDO pin is enabled and data is clocked out on the 5th rising edge of SCLK. After all the data has been clocked out on SDO, a rising edge on $\overline{SYNC}$ disables (tristates) the SDO pin again. Status register data (see Table 9) and control register data are both available during the same read cycle. Data contained in Bit D10 to Bit D0 of the write operation are still valid and can be used to change the operating mode of the AD5749 if required.

The status bits comprise three read-only bits. They are used to notify the user of specific fault conditions that occur, such as an open circuit on the output, over-temperature error or an interface error. If any of these fault conditions occur, a hardware FAULT is also asserted low, which can be used as a hardware interrupt to the controller.

See the Detailed Description of Features section for a full explanation of fault conditions.

## HARDWARE CONTROL

Hardware control is enabled by connecting the HW SELECT pin to DVCC. In this mode, the R3, R2, R1, and R0 pins, in conjunction with the RSET pin, are used to configure the output range, as per Table 8.

In hardware mode, there is no status register. The fault conditions (open circuit, and overtemperature) are available on Pin IFAULT and Pin TEMP. If any one of these fault conditions is set, a low is asserted on the specific fault pin. IFAULT and TEMP are open-drain outputs and, therefore, can be connected together to allow the user to generate one interrupt to the system controller to communicate a fault. If hardwired in this way, it is not possible to isolate which fault occurred in the system.

## TRANSFER FUNCTION

The AD5749 consists of an internal signal conditioning block that maps the analog input voltage to a programmed output range. The available analog input range is 0 V to 4.096 V.

For all ranges, the AD5749 implements a straight linear mapping function, where 0 V maps to the lower end of the selected range and 4.096 V maps to the upper end of the selected range.

**Table 9. Input Shift Register Contents for a Read Operation—Status Register**

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| A2 | A1 | A0 | 1 | 0 | R3 | R2 | R1 | R0 | CLRSEL | OUTEN | RSET | PEC Error | OVER TEMP | IOUT Fault | Unused |

**Table 10. Status Bit Options**

| Bit | Description |
|---|---|
| PEC Error | This bit is set if there is an interface error detected by CRC-8 error checking. See the Detailed Description of Features section. |
| OVER TEMP | This bit is set if the AD5749 core temperature exceeds approximately 150°C. |
| IOUT Fault | This bit is set if there is an open circuit on the IOUT pin. |

# DETAILED DESCRIPTION OF FEATURES

## OUTPUT FAULT ALERT—SOFTWARE MODE

In software mode, the AD5749 is equipped with one FAULT pin; this is an open-drain output allowing several AD5749 devices to be connected together to one pull-up resistor for global fault detection. In software mode, the FAULT pin is forced active low by any one of the following fault scenarios:

- The voltage at IOUT attempts to rise above the compliance range due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with window limits because this requires an actual output error before the fault output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability. Thus, the fault output activates slightly before the compliance limit is reached. Because the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain, and an output error does not occur before the fault output becomes active.
- An interface error is detected due to the packet error checking failure (PEC). See the Packet Error Checking section.
- The core temperature of the AD5749 exceeds approximately 150°C.

## OUTPUT FAULT ALERT—HARDWARE MODE

In hardware mode, the AD5749 is equipped with two fault pins: IFAULT and TEMP. These are open-drain outputs allowing several AD5749 devices to be connected together to one pull-up resistor for global fault detection. In hardware control mode, these fault pins are forced active by any one of the following fault scenarios:

- An open-circuit is detected. The voltage at IOUT attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with window limits because this requires an actual output error before the fault output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability. Thus, the fault output activates slightly before the compliance limit is reached. Because the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain, and an output error does not occur before the fault output becomes active. If this fault is detected, the IFAULT pin is forced low.
- The core temperature of the AD5749 exceeds approximately 150°C. If this fault is detected, the TEMP pin is forced low.

## ASYNCHRONOUS CLEAR (CLEAR)

CLEAR is an active high clear that allows the output to be cleared to either zero-scale or midscale, and is user-selectable via the CLRSEL pin or the CLRSEL bit of the input shift register, as described in Table 8. (The clear select feature is a logical OR function of the CLRSEL pin and the CLRSEL bit). When the CLEAR signal is returned low, the output returns to its programmed value or to a new programmed value. A clear operation can also be performed via the clear command in the control register.

**Table 11. CLRSEL Options**

| CLRSEL | Output Clear Value |
|---|---|
| 0 | Zero scale; for example:<br>4 mA on the 4 mA to 20 mA range<br>0 mA on the 0 mA to 24 mA range |
| 1 | Midscale; for example:<br>12 mA on the 4 mA to 20 mA range<br>12 mA on the 0 mA to 24 mA range |

## EXTERNAL CURRENT SETTING RESISTOR

Referring to Figure 1, $R_{SET}$ is an internal sense resistor and is part of the voltage-to-current conversion circuitry. The nominal value of the internal current sense resistor is 15 kΩ. To allow for overrange capability in current mode, the user can also select the internal current sense resistor to be 14.7 kΩ, giving a nominal 2% overrange capability. This feature is available in the 0 mA to 24 mA, and 4 mA to 20 mA current ranges.

The stability of the output current value over temperature is dependent on the stability of the value of $R_{SET}$. As a method of improving the stability of the output current over temperature, an external low drift resistor can be connected to the REXT1 and REXT2 pins of the AD5749, which can be used instead of the internal resistor. The external resistor is selected via the input shift register. If the external resistor option is not used, the REXT1 and REXT2 pins should be left floating.

## PROGRAMMABLE OVERRANGE MODES

The AD5749 contains an overrange mode The overranges are selected by configuring the R3, R2, R1, and R0 bits (or pins) accordingly.

The overranges are typically 2%. For these ranges, the analog input remains the same (0 V to 4.096 V).

## PACKET ERROR CHECKING

To verify that data has been received correctly in noisy environments, the AD5749 offers the option of error checking based on an 8-bit (CRC-8) cyclic redundancy check. The device controlling the AD5749 should generate an 8-bit frame check sequence using the following polynomial:

$$C(x) = x_8 + x_2 + x_1 + 1$$

This is added to the end of the data-word, and 24 data bits are sent to the AD5749 before taking $\overline{\text{SYNC}}$ high. If the AD5749 receives a 24-bit data frame, it performs the error check when $\overline{\text{SYNC}}$ goes high. If the check is valid, then the data is written to the selected register. If the error check fails, the FAULT pin goes low and Bit D3 of the status register is set. After reading this register, this error flag is cleared automatically and the FAULT pin goes high again.

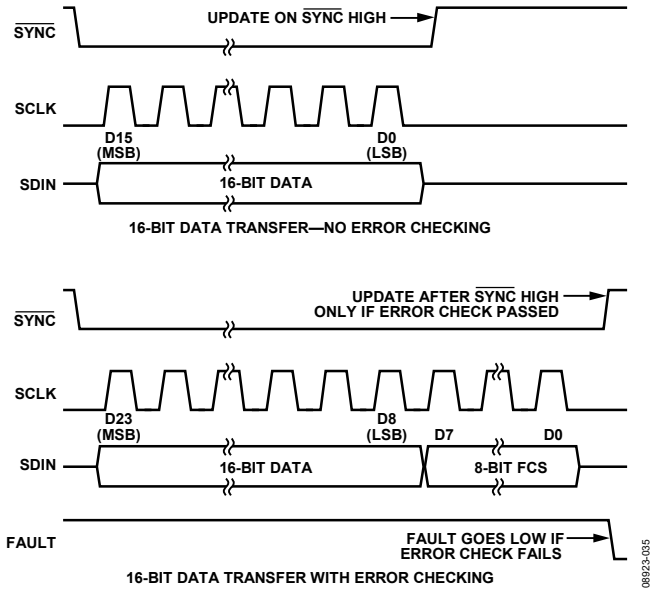



*Figure 34. PEC Error Checking Timing*

# APPLICATIONS INFORMATION

## TRANSIENT VOLTAGE PROTECTION

The AD5749 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5749 from excessively high voltage transients, external power diodes and a surge current limiting resistor may be required, as shown in Figure 35. The constraint on the resistor value is that during normal operation the output level at IOUT must remain within its voltage compliance limit of $AV_{DD}$ − 2.75 V and the two protection diodes and resistor must have appropriate power ratings. Further protection can be added with transient voltage suppressors if needed.

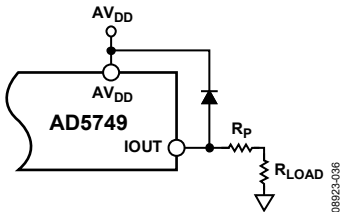



*Figure 35. Output Transient Voltage Protection*

## THERMAL CONSIDERATIONS

It is important to understand the effects of power dissipation on the package and how it affects junction temperature. The internal junction temperature should not exceed 125°C. The AD5749 is packaged in a 32-lead, 5 mm × 5 mm LFCSP package. The thermal impedance, $\theta_{JA}$, is 42°C/W. It is important that the devices not be operated under conditions that cause the junction temperature to exceed its limit. Worst-case conditions occur when the AD5749 is operated from the maximum $AV_{DD}$ (55 V) and driving the maximum current (24 mA) directly to ground. The quiescent current of the AD5749 should also be taken into account, nominally ~4 mA.

The calculations in Table 12 estimate maximum power dissipation under these worst-case conditions, and determine maximum ambient temperature based on this. These figures assume that proper layout and grounding techniques are followed to minimize power dissipation, as outlined in the Layout Guidelines section.

**Table 12. Thermal and Supply Considerations**

| Considerations | 32-Lead LFCSP Package |
|---|---|
| Maximum allowed power dissipation when operating at an ambient temperature of 85°C | $\frac{T_{JMAX} - T_A}{\theta_{JA}} = \frac{125 - 85}{42} = 0.95\ \text{W}$ |
| Maximum allowed ambient temperature when operating from a supply of 55 V and driving 24 mA directly to ground (include 4 mA for internal AD5749 current) | $T_{JMAX} - (P_D \times \theta_{JA}) = 125 - ((55 \times 0.028) \times 42) = 60.3°\text{C}$ |
| Maximum allowed supply voltage when operating at an ambient temperature of 85°C and driving 24 mA directly to ground | $\frac{T_{JMAX} - T_A}{AI_{DD} \times \theta_{JA}} = \frac{125 - 85}{(0.028 \times 42)} = 34\ \text{V}$ |

## LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5749 is mounted should be designed so that the AD5749 lies on the analog plane.

The AD5749 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

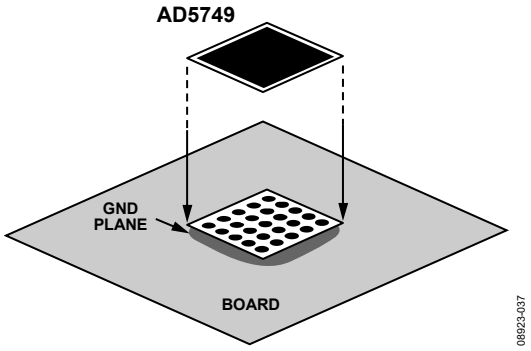



*Figure 36. Paddle Connection to Board*

The AD5749 has an exposed paddle beneath the device. Connect this paddle to the GND of the AD5749. For optimum performance, special considerations should be used to design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, the exposed paddle on the bottom of the package should be soldered to the corresponding thermal land paddle on the PCB (GND). Thermal vias should be designed into the PCB land paddle area to further improve heat dissipation.

## GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The *i*Coupler® family of products from Analog Devices, Inc., provides voltage isolation in excess of 5.0 kV. The serial loading structure of the AD5749 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 37 shows a 4-channel isolated interface to the AD5749 using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

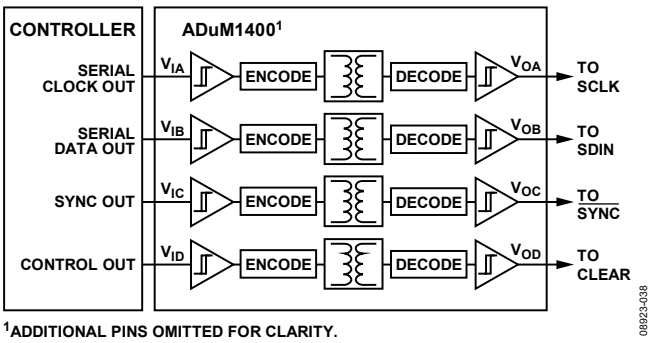
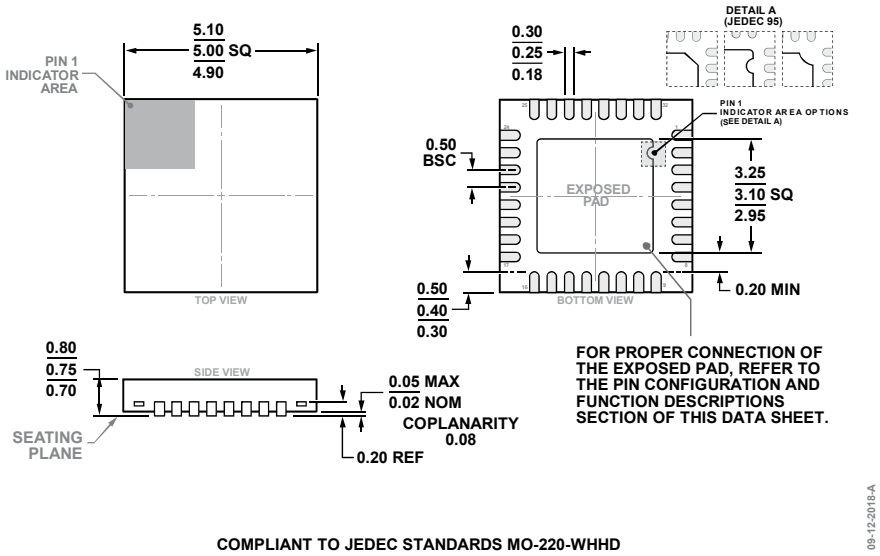



*Figure 37. Isolated Interface*

## MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5749 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communication channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a $\overline{\text{SYNC}}$ signal. The AD5749 requires a 16-bit data-word with data valid on the falling edge of SCLK.

# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MO-220-WHHD**

*Figure 38. 32-Lead Lead Frame Chip Scale Package [LFCSP]*
*5 mm × 5 mm Body and 0.75 mm Package Height*
*(CP-32-7)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD5749ACPZ | −40°C to +105°C | 32-Lead LFCSP | CP-32-7 |
| AD5749ACPZ-RL7 | −40°C to +105°C | 32-Lead LFCSP | CP-32-7 |

[1] Z = RoHS Compliant Part.

## NOTES

# NOTES