Pin Definitions

Pin Name	Pin No. (SOIC)	Pin No. (TSSOP)(-01)	Pin Type	Pin Description
CLKOUT	5	8	O	**Output Modulated Frequency**: Frequency modulated copy of the unmodulated input clock (SSON# asserted).
CLKIN or X1	1	2	I	**Crystal Connection or External Reference Frequency Input**: This pin has dual functions. It may either be connected to an external crystal, or to an external reference clock.
NC or X2	2	3	I	**Crystal Connection**: If using an external reference, this pin must be left unconnected.
SSON#	8(02/03/52/53)	--	I	**Spread Spectrum Control (Active LOW)**: Asserting this signal (active LOW) turns the internal modulation waveform on. This pin has an internal pull-down resistor.
FS1:2	7, 8 (01/51)	12, 1	I	**Frequency Selection Bit(s) 1 and 2**: These pins select the frequency range of operation. Refer to *Table 2*. These pins have internal pull-up resistors.
SS%	4	6	I	**Modulation Width Selection**: When Spread Spectrum feature is turned on, this pin is used to select the amount of variation and peak EMI reduction that is desired on the output signal. This pin has an internal pull-up resistor.
VDD	6	10	P	**Power Connection**: Connected to 3.3V or 5V power supply.
GND	3	4	G	**Ground Connection**: Connect all ground pins to the common system ground plane.
NC		5, 7, 9, 11, 13, 14	NC	No Connection

Key Specifications

Supply Voltages: ....V_{DD} = 3.3V ± 5%
....or V_{DD} = 5V ± 10%
Frequency Range: .... 28 MHz $\leq F_{in} \leq$ 75 MHz
Crystal Reference Range.................. 28 MHz $\leq F_{in} \leq$ 40 MHz
Cycle to Cycle Jitter: .... 300 ps (max.)
Selectable Spread Percentage: .... 1.25% or 3.75%
Output Duty Cycle: .... 40/60% (worst case)
Output Rise and Fall Time: .... 5 ns (max.)

Table 1. Modulation Width Selection

SS%	W181-01, 02, 03 Output	W181-51, 52, 53 Output
0	−1.25% (Down Spread)	±0.625 (Center Spread)
1	−3.75% (Down Spread)	±1.875% (Center Spread)

Table 2. Frequency Range Selection

		W181 Option#		
FS2	FS1	-01, 51 (MHz)	-02, 52 (MHz)	-03, 53 (MHz)
0	0	$28 \leq F_{IN} \leq 38$	$28 \leq F_{IN} \leq 38$	N/A
0	1	$38 \leq F_{IN} \leq 48$	$38 \leq F_{IN} \leq 48$	N/A
1	0	$46 \leq F_{IN} \leq 60$	N/A	$46 \leq F_{IN} \leq 60$
1	1	$58 \leq F_{IN} \leq 75$	N/A	$58 \leq F_{IN} \leq 75$

Overview

The W181 products are one series of devices in the Cypress PREMIS family. The PREMIS family incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low-frequency carrier, peak EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or redesign.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. The Simplified Block Diagram on page 1 shows a simple implementation.

Functional Description

The W181 uses a phase-locked loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in *Figure 1*. The input reference signal is divided by Q and fed to the phase detector. A signal from the VCO is divided by P and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency. (Note: For the W181 the output frequency is equal to the input frequency.) The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

Frequency Selection With SSFTG

In Spread Spectrum Frequency Timing Generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed for a given frequency, the modulation percentage may be varied.

Using frequency select bits (FS1:2 pins), the frequency range can be set. Spreading percentage is set to be 1.25% or 3.75% (see *Table 1*).

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentages between 0.5% and 2.5% are most common.
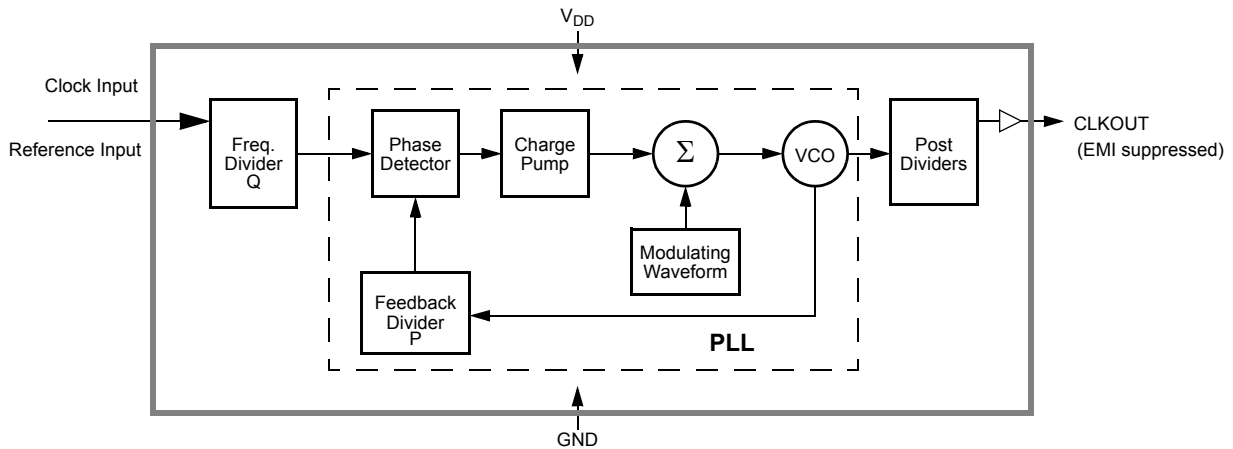

Figure 1. Functional Block Diagram

Spread Spectrum Frequency Timing Generation

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 2*.

As shown in *Figure 2*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$dB = 6.5 + 9*log_{10}(P) + 9*log_{10}(F)$

where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 3*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. *Figure 3* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.
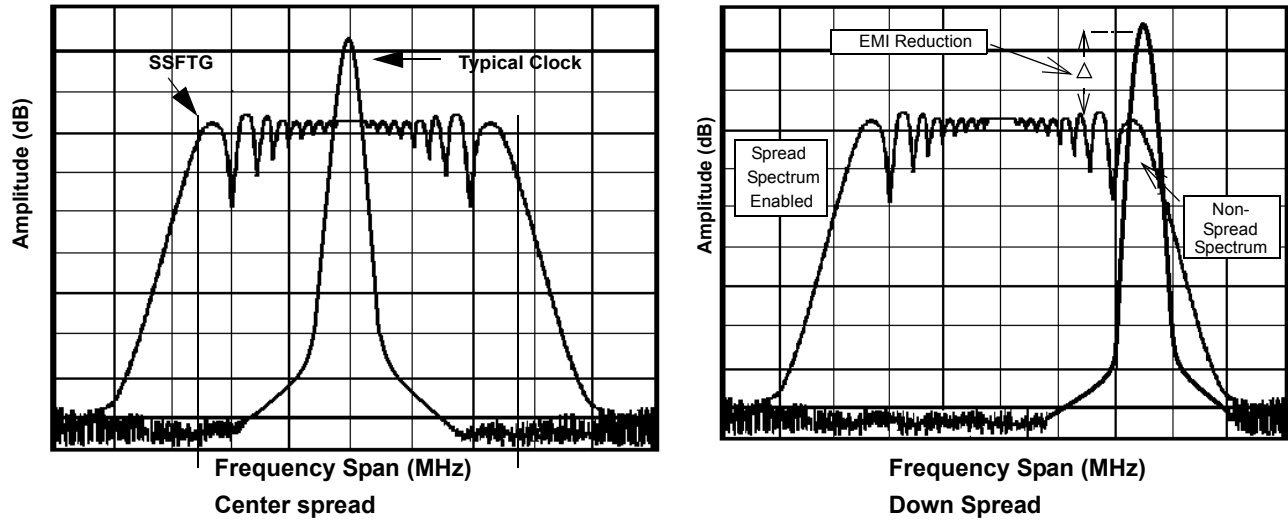
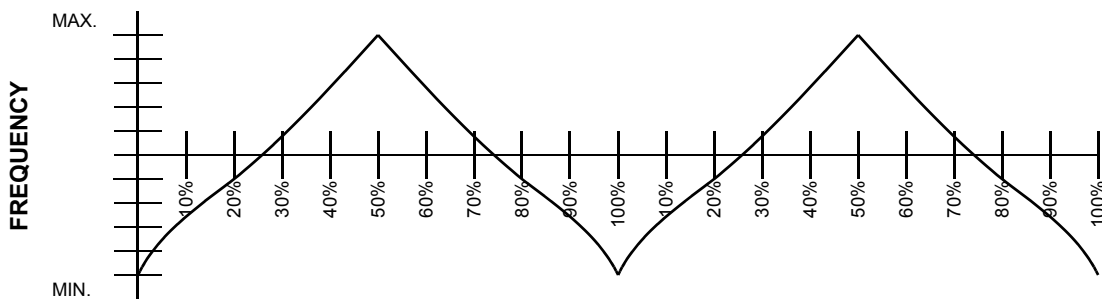**Figure 2. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation**

Figure 3. Typical Modulation Profile

Absolute Maximum Conditions[2]

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	−0.5 to +7.0	V
T_{STG}	Storage Temperature	−65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	−55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: 0°C < T_A < 70°C, V_{DD} = 3.3V ±5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current		–	18	32	mA
t_{ON}	Power-Up Time	First locked clock cycle after Power Good	–	–	5	ms
V_{IL}	Input Low Voltage		–	–	0.8	V
V_{IH}	Input High Voltage		2.4	–	–	V
V_{OL}	Output Low Voltage		–	–	0.4	V
V_{OH}	Output High Voltage		2.4	–	–	V
I_{IL}	Input Low Current	Note 3	–	–	−100	μA
I_{IH}	Input High Current	Note 3	–	–	10	μA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 3.3V	–	15	–	mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 3.3V	–	15	–	mA
C_I	Input Capacitance	All pins except CLKIN	–	v	7	pF
C_I	Input Capacitance	CLKIN pin only	–	6	10	pF
R_P	Input Pull-Up Resistor[3]		–	500	–	kΩ
Z_{OUT}	Clock Output Impedance		–	25	–	Ω

DC Electrical Characteristics: 0°C < T_A < 70°C, V_{DD} = 5V ±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current			30	50	mA
t_{ON}	Power-Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				$0.15V_{DD}$	V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 3			−100	μA
I_{IH}	Input High Current	Note 3			10	μA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 5V		24		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 5V		24		mA
C_I	Input Capacitance	All pins except CLKIN			7	pF
C_I	Input Capacitance	CLKIN pin only		6	10	pF
R_P	Input Pull-Up Resistor			500		kΩ

Notes:
1. Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability
2. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power-up.
3. Inputs FS1:2 have a pull-up resistor; Input SSON# has a pull-down resistor.

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V ±5% or 5V±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	Input Clock	28		75	MHz
f_{OUT}	Output Frequency	Spread Off	28		75	MHz
t_R	Output Rise Time	V_{DD}, 15-pF load 0.8V–2.4V		2	5	ns
t_F	Output Fall Time	V_{DD}, 15-pF load 2.4V–0.8V		2	5	ns
t_{OD}	Output Duty Cycle	15-pF load	40		60	%
t_{ID}	Input Duty Cycle		40		60	%
t_{JCYC}	Jitter, Cycle-to-Cycle			250	300	ps
	Harmonic Reduction	f_{out} = 40 MHz, third harmonic measured, reference board, 15-pF load	8			dB

CLKOUT Frequency Offset (Shift)[4,5]: T_A = 0°C to +70°C, V_{DD} = 3.3V ±5% or 5V±10% (For only W181-02, -02 and -03 products)

Parameter	Description	Frequency Range (MHz)	Min.	Typ.	Max.	Unit
FOFFSET-1	Frequency Offset (Shift)	FS2=0, FS1=0, 28≤F_{IN}≤38	–0.8	–1.0	–1.2	%
FOFFSET-2	Frequency Offset (Shift)	FS2=0, FS1=1, 38≤F_{IN}≤48	–1.1	–1.4	–1.7	%
FOFFSET-3	Frequency Offset (Shift)	FS2=1, FS1=0, 46≤F_{IN}≤60	–0.2	–0.5	–0.8	%
FOFFSET-4	Frequency Offset (Shift)	FS2=1, FS1=1, 58≤F_{IN}≤75	–0.8	–1.0	–1.2	%

Application Information

Recommended Circuit Configuration

For optimum performance in system applications the power supply decoupling scheme shown in *Figure 4* should be used.

V_{DD} decoupling is important to both reduce phase jitter and EMI radiation. The 0.1-μF decoupling capacitor should be placed as close to the V_{DD} pin as possible, otherwise the increased trace inductance will negate its decoupling capability. The 10-μF decoupling capacitor shown should be a tantalum type. For further EMI protection, the V_{DD} connection can be made via a ferrite bead, as shown.

Recommended Board Layout

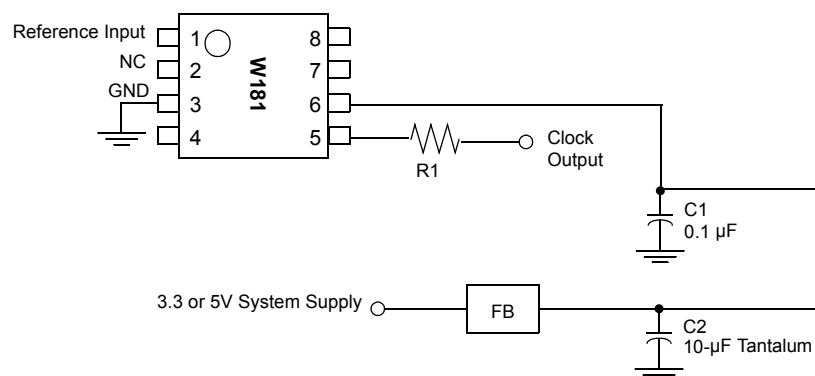*Figure 5* shows a recommended 2-layer board layout.

Figure 4. Recommended Circuit Configuration

Notes:
4. The frequency offset (shift) is given with respect to ideal peak value which is the same as input reference frequency in the case of down spread only for W180-01,-02 and -03 products.
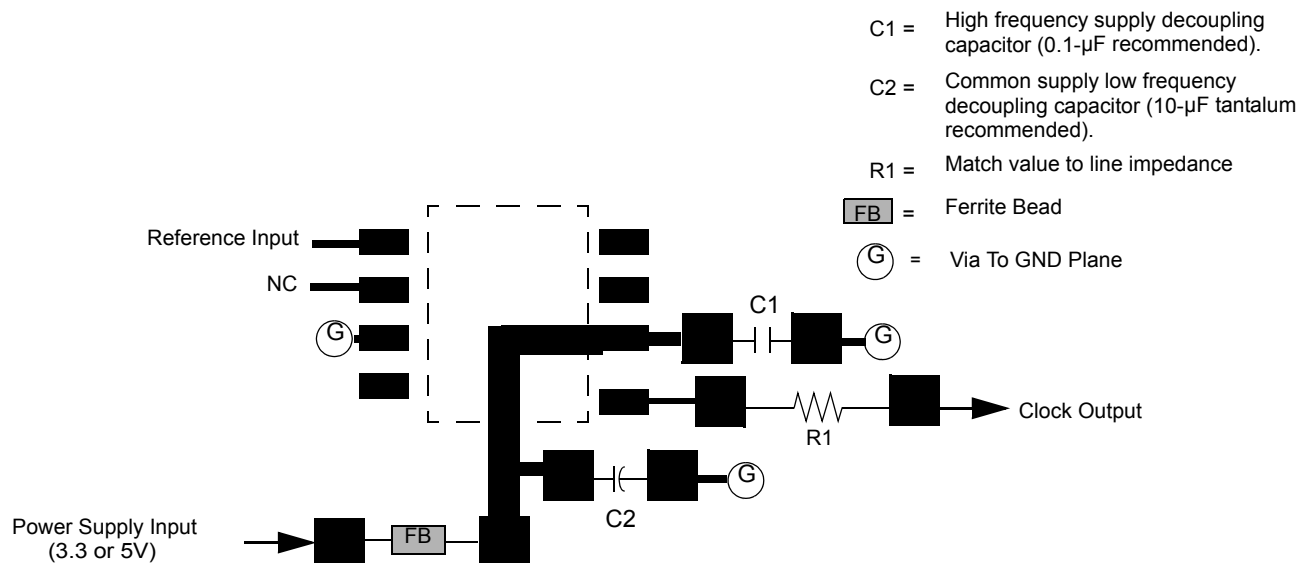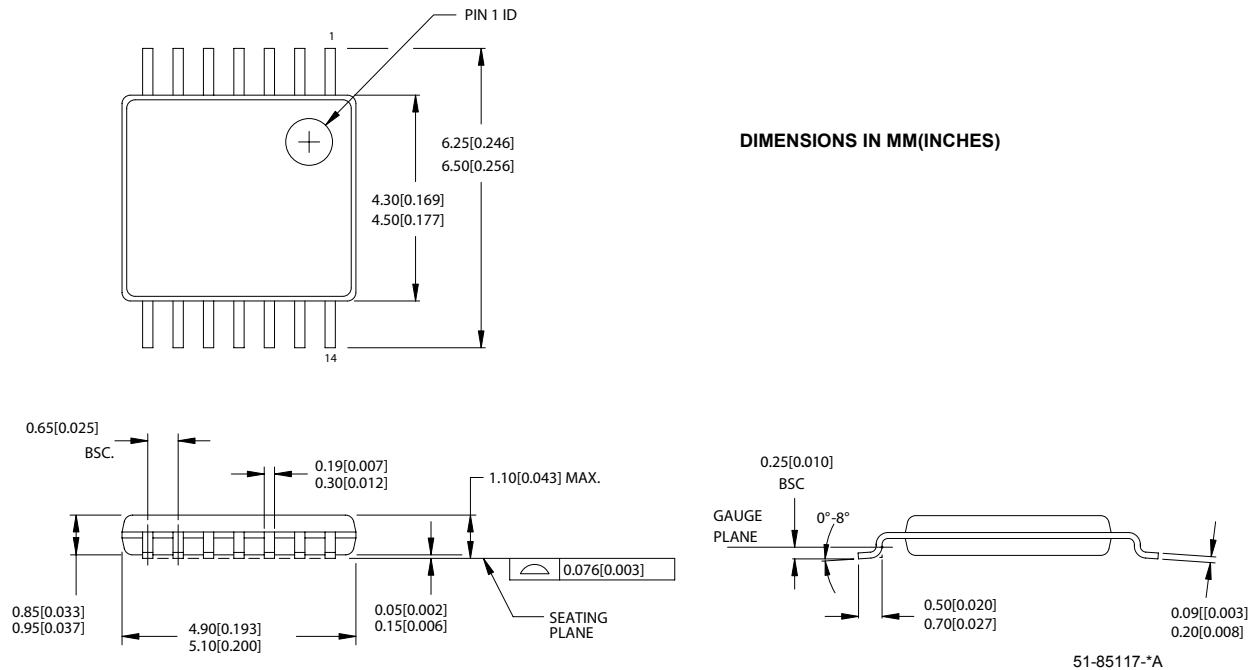5. There is no offset (shift) for center spread for W180-51,-52 and -53 products.

C1 = High frequency supply decoupling capacitor (0.1-µF recommended).

C2 = Common supply low frequency decoupling capacitor (10-µF tantalum recommended).

R1 = Match value to line impedance

FB = Ferrite Bead

G = Via To GND Plane

Figure 5. Recommended Board Layout (2-Layer Board)

Ordering Information

Ordering Code	Package Type	Product Flow
W181-01G	8-pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
W181-01GT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
W181-02G	8 pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
W181-02GT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
W181-03G	8 pin Plastic SOIC (150-mil	Commercial, 0° to 70°C
W181-03GT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
W181-51G	8-pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
W181-51GT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
W181-52G	8 pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
W181-52GT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
W181-53G	8 pin Plastic SOIC (150-mil	Commercial, 0° to 70°C
W181-53GT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
W181-01X	14-pin Plastic TSSOP	Commercial, 0° to 70°C
W181-01XT	14-pin Plastic TSSOP – Tape and Reel	Commercial, 0° to 70°C
Lead-free Devices		
CYW181-01SX	8 pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
CYW181-01SXT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
CYW181-02SX	8 pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
CYW181-02SXT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
CYW181-03SX	8 pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
CYW181-03SXT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
CYW181-51SX	8 pin Plastic SOIC (150-mil))	Commercial, 0° to 70°C
CYW181-51SXT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
CYW181-52SX	8 pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
CYW181-52SXT	8-pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C
CYW181-53SX	8 pin Plastic SOIC (150-mil)	Commercial, 0° to 70°C
CYW181-53SXT	8 pin Plastic SOIC (150-mil) – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimension

14-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z14

PIN 1 ID

1

DIMENSIONS IN MM(INCHES)

6.25[0.246]
6.50[0.256]

4.30[0.169]
4.50[0.177]

14

0.65[0.025]
BSC.

0.19[0.007]
0.30[0.012]

1.10[0.043] MAX.

0.25[0.010]
BSC

GAUGE
PLANE

0°-8°

0.85[0.033]
0.95[0.037]

4.90[0.193]
5.10[0.200]

0.05[0.002]
0.15[0.006]

0.076[0.003]

SEATING
PLANE

0.50[0.020]
0.70[0.027]

0.09[[0.003]
0.20[0.008]

51-85117-*A

8-lead (150-Mil) SOIC S8

PIN 1 ID

4   1

0.150[3.810]
0.157[3.987]

0.230[5.842]
0.244[6.197]

5   8

1. DIMENSIONS IN INCHES[MM] MIN.
                                              MAX.

2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME

3. REFERENCE JEDEC MS-012

4. PACKAGE WEIGHT 0.07gms

PART #
S08.15 STANDARD PKG.
SZ08.15 LEAD FREE PKG.

0.189[4.800]
0.196[4.978]

SEATING PLANE

0.010[0.254]
0.016[0.406]   X 45°

0.061[1.549]
0.068[1.727]

0.004[0.102]

0.050[1.270]
BSC

0.004[0.102]
0.0098[0.249]

0°~8°

0.016[0.406]
0.035[0.889]

0.0075[0.190]
0.0098[0.249]

0.0138[0.350]
0.0192[0.487]

51-85066-*C

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Document History Page

Document Title: W181 Peak Reducing EMI Solution				
Document Number: 38-07152				

REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	110262	12/15/01	SZV	Change from Spec number: 38-00790 to 38-07152
*A	122687	12/27/02	RBI	Added power up requirements to maximum ratings information.
*B	127906	07/07/03	IJA	Changed Modulation Width Selection values in *Table 1* Added CLKOUT Frequency Offset Table Created Cypress approved drawings to replace old ones Updated Ordering Information to clarify and match ordering codes to Dev Master
*C	131492	01/22/04	RGL	Added Lead-free for all the SOIC packages in the ordering information
*D	241879	See ECN	RGL	Corrected the Lead Free Coding in the Ordering Information table