Absolute Maximum Ratings

V_{DDH} to V_{SS} .....-0.3V to +23V
VX to V_{SS} (DC) .....-0.3V to +23V
VX to V_{SS} (AC) (Notes 1, 2) .....-10V to +23V
V_{DDH} to VX (DC).....-0.3V to +23V
V_{DDH} to VX (AC) (Notes 1, 2).....-10V to +23V
BST to V_{SS} (DC) .....-0.3V to +25.5V
BST to V_{SS} (AC) (Note 2) .....-7V to +25.5V
BST to VX Differential .....-0.3V to +2.5V

V_{DD}, V_{CC} to GND .....-0.3V to +2.5V
PWM, ISENSE, $\overline{TS\_FAULT}$ to GND.....-0.3V to V_{DD} + 0.3V
V_{SS} to GND.....-0.3V to +0.3V
Peak VX Current (Note 3).....±100A
Junction Temperature (T_J).....+150°C
Storage Temperature Range..... -65°C to +150°C
Peak Reflow Temperature Lead-Free .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ratings

V_{DD}, V_{CC} .....1.71V to 1.98V
12V Supply (V_{DDH}) .....8.5V to 14.0V

Junction Temperature (T_J)..... -40°C to +125°C
Frequency (f_{SW})..... 300kHz to 1.3MHz

Note 1: Input HF capacitors placed not more than 40 mils away from the V_{DDH} pin required to keep inductive-voltage spikes within Absolute Maximum limits.
Note 2: AC is limited to 25ns.
Note 3: Peak OCP clamp levels limit the application below the peak VX current rating.

Package Information

16 FCQFN

Package Code	P163A6F+2
Outline Number	**21-0986**
Land Pattern Number	**90-0490**
THERMAL RESISTANCE	
Junction to Case (θ_{JC}) VT1697SB	0.42°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{DD} = V_{CC} = 1.71V - 1.98V, V_{DDH} = 12V. Specifications are for T_J = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES, SUPPLY CURRENT						
Bias Supply Voltage	V_{DD}, V_{CC}		1.71		1.98	V
Power-Train Input Voltage	V_{DDH}		8.5	12.0	14.0	V
1.8V Bias Supply Current	I_{CC} + I_{DD}	Shutdown (Note 4)		0.5	2	µA
		Inactive, no switching (Note 5)		3.2	5.0	mA
		Load = 0A, V_{OUT} = 1.8V, f_{SW} = 1.5MHz		43	61	mA
		Load = 0A, V_{OUT} = 1.8V, f_{SW} = 300kHz		14	20	
		Load = 0A, V_{OUT} = 1.8V, f_{SW} = 600kHz		29	41	
12V Bias Supply Current	I_{DDH}	Shutdown (Note 4)		1.3	10	µA
		Inactive, no switching (Note 5)		6.5	20	
I_{RECON} SPECIFICATION						
Current Gain (I_L to ISENSE)	A_I	-70A < I_L < 70A	95000	100000	105000	A/A
TEMPERATURE-SENSOR SPECIFICATIONS						
Temperature-Sensor Dynamic Range	T_{RANGE}		0		150	°C
Temperature-Sensor Gain	A_{TEMP}			3.01		mV/°C
Temperature-Sensor Voltage	–	T_J = 0°C		832		mV
PROTECTION FEATURES						
V_{DD} UVLO Threshold (Rising)	V_{DD_UVLO}		1.47	1.57	1.64	V
V_{DD} UVLO Threshold (Falling)			1.41	1.5	1.58	
V_{DDH} OVLO Threshold (Rising)	V_{DDH_OVLO}		15.48	16	16.41	V
V_{DDH} OVLO Threshold (Falling)			14.95	15.50	15.81	
V_{DDH} UVLO Threshold (Rising)	V_{DDH_UVLO}		4.05	4.27	4.40	V
V_{DDH} UVLO Threshold (Falling)			3.90	4.09	4.25	
V_{BST} UVLO Threshold (Rising)	V_{BST_UVLO}	Note 6	1.39	1.52	1.66	V
V_{BST} UVLO Threshold (Falling)		Note 6	1.32	1.45	1.57	

Electrical Characteristics (continued)

(V_{DD} = V_{CC} = 1.71V - 1.98V, V_{DDH} = 12V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak Positive-OCP Clamp Level	OCP	VT1697SB	59	67	80	A
Peak Positive-OCP Clamp Delay					63	ns
Peak Negative-OCP Clamp Level		VT1697SB	-79.1	-71.9	-64.7	A
Peak Negative-OCP Delay					110	ns
Overtemperature Shutdown	OTP	Rising threshold	140	150	165	°C
PWM INPUT						
Input Voltage, High State	V_{IH}		V_{DD} - 0.20			V
Input Voltage, Low State	V_{IL}				0.20	V
Three-State Control Threshold (PWM Input Rising)	–			0.63		V
$\overline{\text{TS\_FAULT}}$ INPUT						
$\overline{\text{TS\_FAULT}}$ Digital Threshold V_{IH}	V_{IH}		0.41			V
$\overline{\text{TS\_FAULT}}$ Digital Threshold V_{IL}	V_{IL}				0.17	V

Note 4: T_{SENSE}, PWM and ISENSE pins of the slave are pulled low by the master. The slave is in this state before master OE is enabled.

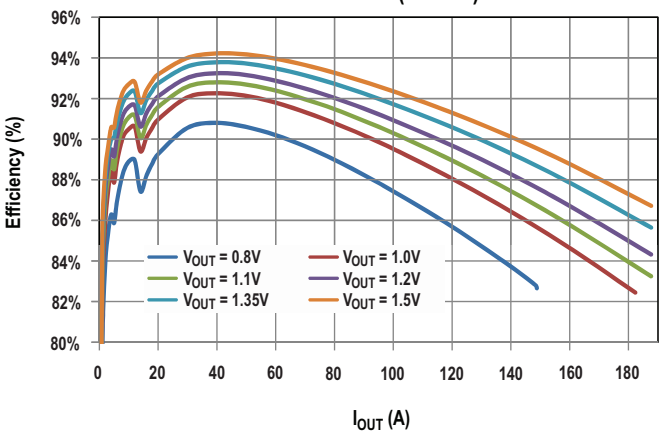
Note 5: Inactive, no switching: PWM signal is three stated by the master. The slave is in this mode when the master sheds a phase (temporarily disabling this slave) to save power at lighter loads.

Note 6: V_{BST_UVLO} is measured with respect to VX and not from ground.

VT1697SB Typical Operating Characteristics

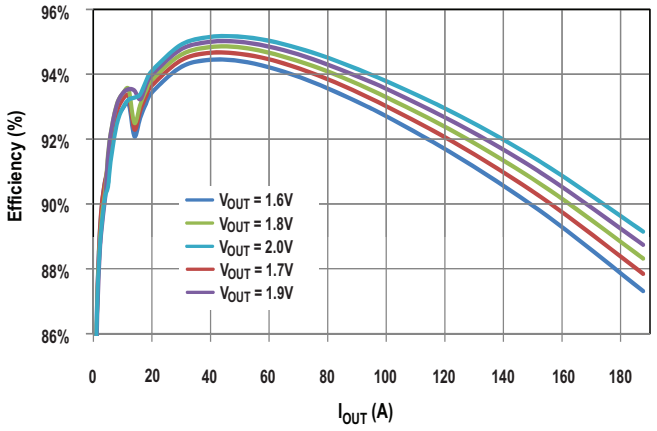
(Master: T_A = 25°C; f_{SW} = 600kHz.)

Efficiency vs. Load Current
4 VT1697SB (VR12.0)



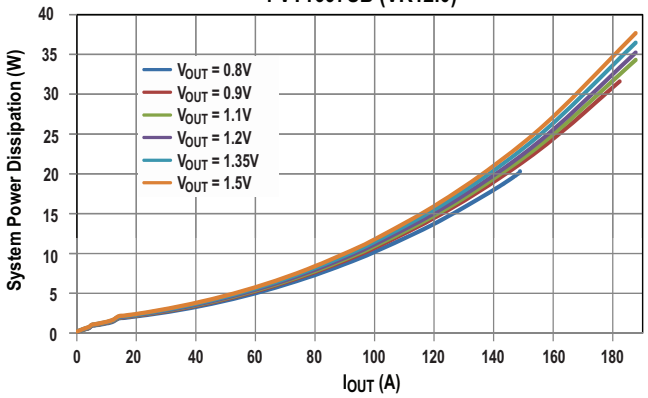
Conditions: V_{IN} = 12V
V_{BIAS} = 1.8V
Inductor: CLB1108-4-50TR-R

Efficiency vs. Load Current
4 VT1697SB (VR12.5)



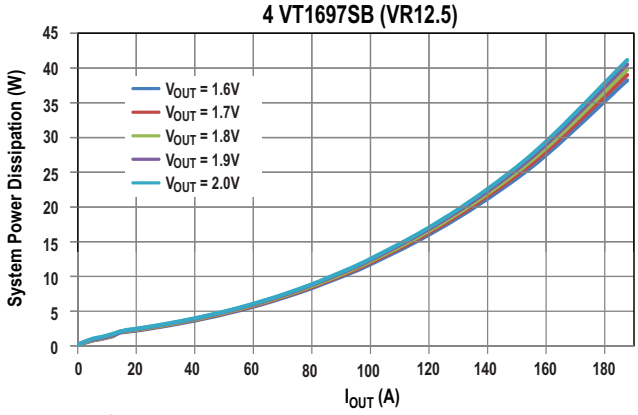
Conditions: V_{IN} = 12V
V_{BIAS} = 1.8V
Inductor: CLB1108-4-50TR-R

System Power Dissipation vs. Load Current
4 VT1697SB (VR12.0)



Conditions: V_{IN} = 12V
V_{BIAS} = 1.8V
Inductor: CLB1108-4-50TR-R

System Power Dissipation vs. Load Current
4 VT1697SB (VR12.5)

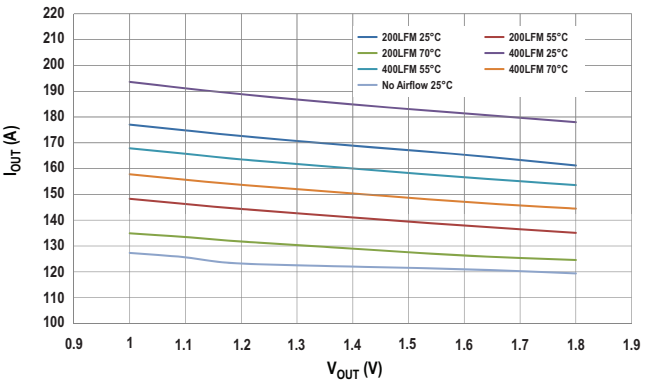


Conditions: V_{IN} = 12V
V_{BIAS} = 1.8V
Inductor: CLB1108-4-50TR-R

VT1697SB Typical Operating Characteristics (continued)

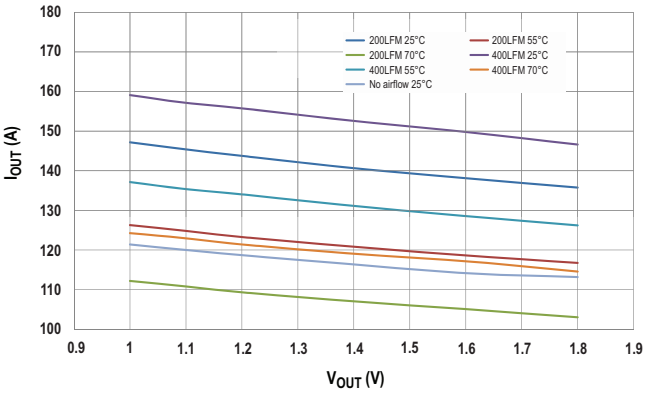
(Master: T_A = 25°C; f_{SW} = 600kHz.)

VT1697SB 4-Phase Safe Operating Area (Heatsink)



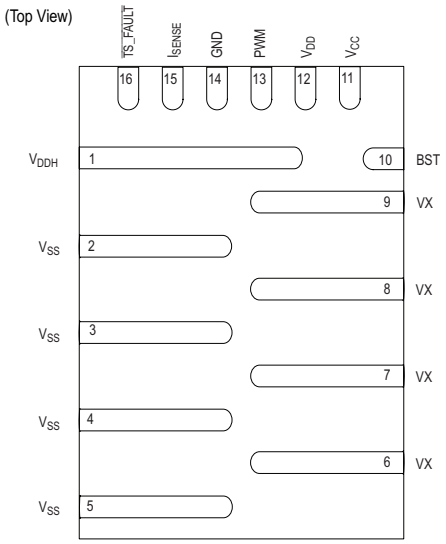
Conditions: V_{IN} = 12V
V_{BIAS} = 1.8V
Inductor: CL1108-4-50TR-R

VT1697SB 4-Phase Safe Operating Area (No Heatsink)



Conditions: V_{IN} = 12V
V_{BIAS} = 1.8V
Inductor: CL1108-4-50TR-R

Pin Configuration (continued)

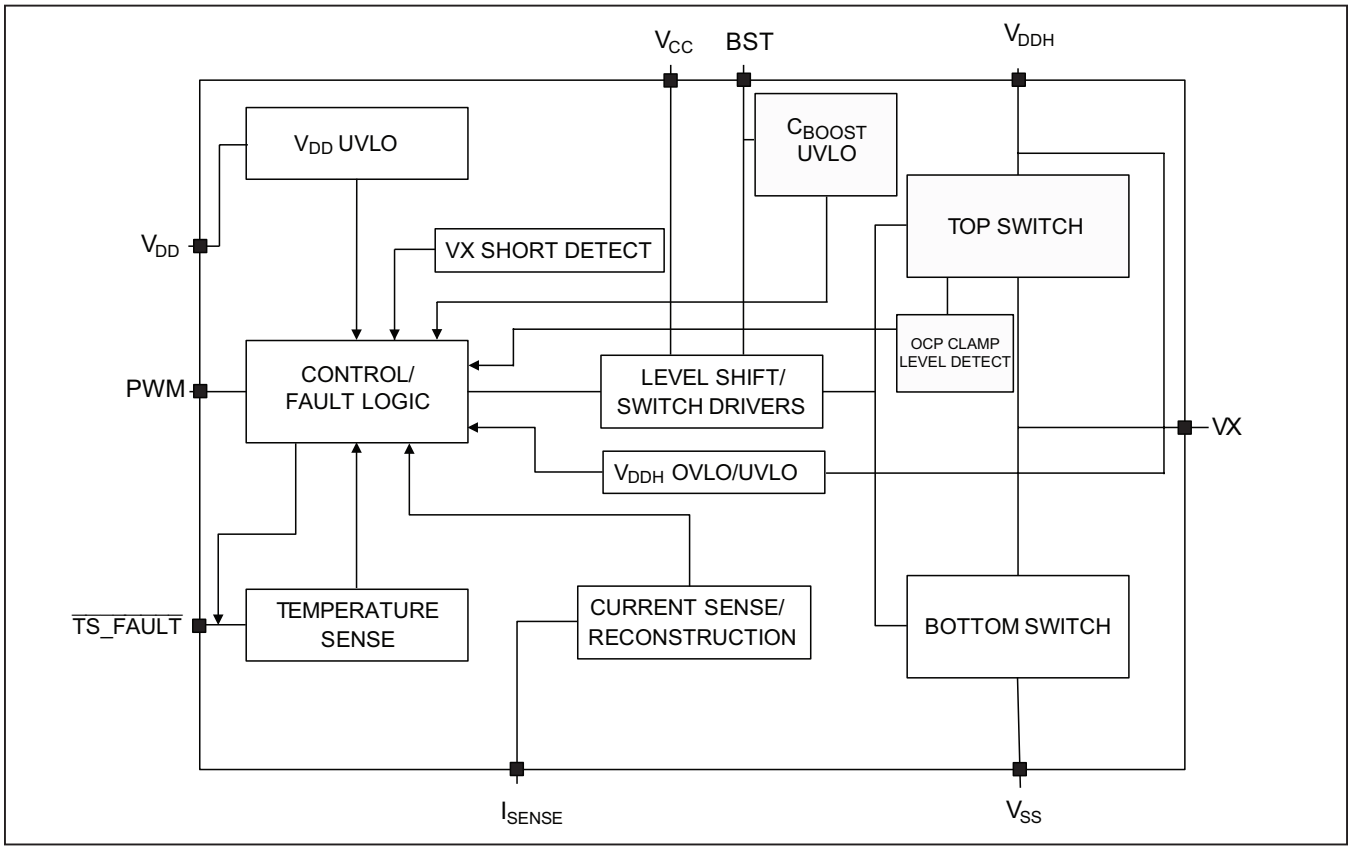


VT1697SB 16-Pin FCQFN

Pin Description (VT1697SB Smart Slave Device)

PIN	NAME	FUNCTION
1	V_{DDH}	Drain of High-Side Power FET. Connect to the 12V input supply. See Table 2 for decoupling requirements.
2–5	V_{SS}	Power Ground. Connect to the return path of the output load.
6–9	VX	Switching Node. Connect to the switching node of the output inductor.
10	BST	Boost Supply Input. Connect a 0.22µF ceramic capacitor placed 40 mils or closer to the IC between BST and VX.
11	V_{CC}	Gate-Drive Supply. Connect to the 1.8V bias supply. See Table 2 for decoupling requirements.
12	V_{DD}	Control Circuit Supply. Connect to the 1.8V bias supply. See Table 2 for decoupling requirements.
13	PWM	PWM Input. Connect to the appropriate PWM_ output of the controller. PWM Logic Levels: • High: HS FET on, LS FET off • Mid: Diode emulation mode; both FETs are off when the current reaches zero • Low: LS FET on, HS FET off
14	GND	Analog Ground. Connect to the ground plane using a single via placed 40 mils or closer to the IC.
15	I_{SENSE}	Current-Sense Output. Connect to the appropriate ISENSE input pin of the controller through a simple passive filter. The ISENSE current is an attenuated replica of the VX current.
16	$\overline{TS\_FAULT}$	Smart Power-Stage Temperature and Fault Output. This dual-function pin is used to report the junction temperature and to communicate a fault condition to the controller. Connect $\overline{TS\_FAULT}$ to the TSENSE input of the controller.

Block Diagram



Voltage Regulation

This Maxim smart slave IC provides control logic, drivers, monitoring circuits, and power semiconductors for a synchronous buck converter with fault protection, status monitoring and accurate lossless current sensing. Phases are controlled by the master IC independently by separate phase-control signals.

Power Switch Control and Drivers

The smart slave IC operates in conjunction with a Maxim master IC. The master controller configures the voltage regulator based on its configuration resistors and the number of phases populated. The smart slave device's switching is controlled by the proprietary command signals on the phase-control lines. The phase-control signal has three defined states: high, low, and "three state." Three state is used for phase shedding and DCM modes. An external boost capacitor is required to supply the voltage for the high-side switch driver. V_{DD} and V_{CC} are brought out separately to allow separate decoupling to improve noise immunity on the V_{DD} rail.

Current-Sense Output

The integrated lossless current sense (or "current reconstruction") produces a precise ratiometric current-sense signal for both positive and negative currents which is sent to the master as an analog current signal. This current-sense technology provides accurate current information over load and temperature that is not affected by tolerances of passive elements such as the output inductor, resistors and capacitors.

Phase Configuration

The ability for the master to dynamically disable and reenable a phase is an integral part of the Maxim master/slave architecture. The master sets the phase-control signal to three state to disable a phase. The same state is used to control DCM operation. When using a coupled inductor, a proprietary mode (coupled-inductor mode) can be set by the master and communicated to the smart slave through the phase-control signal to minimize losses due to coupled currents in inactive phases.

Protection Circuits

Overcurrent Protection

The smart slave IC incorporates instantaneous overcurrent fault protection using the lossless current-sense/reconstruction. This overcurrent protection is separate from the system overcurrent protection, and is intended to operate only in extreme fault conditions to protect the IC and other components. The system overcurrent protection set by the master should be set with sufficient margin below the slave IC's threshold to ensure correct system operation.

For current sourcing operation, if the instantaneous current in the top switch (based on the current-sense/reconstruction circuit) exceeds the overcurrent-protection value shown in the *Electrical Characteristics* table, the slave regulates the period of the top-side switch to keep its peak current at a safe level. The protection threshold has been set to ensure that the IC's maximum allowable peak current is not exceeded when using the recommended inductors. The sourcing current limiting is not considered a hard fault condition for slave, and therefore $\overline{TS\_FAULT}$ is not asserted. Since clamping is based on instantaneous reconstructed current, the ripple current must be considered when calculating the maximum average current per slave. The maximum average current before clamping can be calculated as shown in Equation 1. Note that the clamping is based on reconstructed current. Limits shown in the *Electrical Characteristics* table for Clamp Level reflect expected variations in application conditions and external component characteristics. Also note that the master (i.e., system) overcurrent protection should be set lower than the slave's maximum operating current as stated above.

Equation 1:

$$\text{Maximum Average DC Slave Current} = OCP - \frac{I_{RIPPLE}}{2}$$

where:

OCP = Peak OCP clamp level (A)

I_{RIPPLE} = Peak-to-peak inductor ripple current (A)

For current-sinking protection, if the negative overcurrent-protection threshold is reached, the slave limits the current and $\overline{TS\_FAULT}$ is not asserted.

The VT1697SB implements an additional OCP shutdown level (beyond the clamp levels). If the current in the top switch exceeds the OCP shutdown level (shown in the *Electrical Characteristics* table), the IC is turned off and fault is reported by asserting the $\overline{TS\_FAULT}$ pin. The slave is then latched off until the power is cycled.

V_{DD} and V_{BOOST} Undervoltage Lockout

The smart slave IC includes undervoltage-lockout circuits: V_{DD} and V_{BOOST}. For power-sequencing guidelines and operation with separate bias rails for master and slaves, refer to appropriate master data sheet. V_{BOOST} UVLO is active at all times after the initial system startup. It is not active during the initial system power-on state (before regulation is enabled) and is activated approximately 20µs after initial startup. If either of these UVLO circuits is tripped during operation, the smart slave stops switching and a fault signal ($\overline{TS\_FAULT}$ pulled low) is sent to the master.

V_{DDH} (V_{IN}) Undervoltage and Overvoltage Lockout

The slave includes protection circuits that shut down the slave and assert $\overline{TS\_FAULT}$ if V_{DDH} is above or below the correct operating range. If either of these circuits is tripped during operation, the slave stops switching and a fault signal ($\overline{TS\_FAULT}$ pulled low) is sent to the master.

Temperature Sensing and Overtemperature Protection

The smart slave IC incorporates an accurate die temperature sensor. The temperature-sense signal is sent to the master as an analog signal through the temperature-sense pin. The actual temperature of the smart slave device is then made available through the SMBus of the master. The smart slave IC also includes overtemperature protection. If the trip point is reached, the IC immediately shuts down and the fault is reported to the master through the $\overline{TS\_FAULT}$ pin.

VX Short Protection

The smart slave IC includes a VX short detection to detect a local short circuit from the VX node to either V_{DDH} or ground. If such a fault is detected, the slave shuts down and communicates a fault to the master through the $\overline{TS\_FAULT}$ pin.

$\overline{TS\_FAULT}$ Signal

If a fault is detected, the smart slave sends a signal to the master by pulling the $\overline{TS\_FAULT}$ pin to ground. Under normal conditions, this pin is used to send an accurate analog representation of the slave temperature. If a fault is detected, this pin is asserted low to indicate that a fault condition was detected by the slave IC. Table 1 shows the faults that result in this signal being asserted. For a latching fault, the fault must be cleared and the V_{DD} power cycled to reenable the IC (for on-latching faults, see the note below the Table 1).

Table 1. Fault Detection and Protection Circuits

FAULT	DESCRIPTION	TYPE	FAULT FLAG ($\overline{TS\_FAULT}$)
Boost UVLO	Undervoltage Lockout on Boost Supply	Shutdown*	Asserted
V_{DDH} UVLO	Undervoltage Lockout on V_{DDH}	Shutdown*	Asserted
V_{DDH} OVLO	Overvoltage Lockout Signal on V_{DDH}	Shutdown*	Asserted
V_{DD} UVLO	Undervoltage Lockout Signal on V_{DD}	Shutdown*	Asserted
V_X Short	VX Short-to-Ground or V_{DDH}	Shutdown	Asserted
POCP (Sourcing)	Positive/Sourcing Overcurrent Protection	Cycle-by-Cycle Current Limit	Not Asserted
NOCP (Sinking)	Negative/Sinking Overcurrent Protection	Cycle-by-Cycle Current Limit	Not Asserted
OTP	Overtemperature Protection	Shutdown	Asserted

**V_{DDH} UVLO, V_{DDH} OVLO, Boost UVLO and V_{DD} UVLO are nonlatching faults. If a nonlatching fault is detected by the slave, it asserts $\overline{TS\_FAULT}$ signal low and stops switching. The slave resumes switching and deasserts $\overline{TS\_FAULT}$ around 37µs from when the fault condition is removed. Refer to the master data sheet for master response to $\overline{TS\_FAULT}$ asserted low by the slave device.*

Design Considerations

Phase Current Sharing and Steering Control

Maxim master/slave chipsets offer options for thermal balancing in applications where one or more phases have different thermal characteristics. The current sense and chipset regulation system offer the potential for current steering, where a percentage of current can be steered away from any phase, allowing that phase to operate at a different current than the other phases. This allows a precise scaling of current in any slave(s) to achieve proper thermal balance between phases. Refer to the applicable Maxim master IC data sheet for more information on how to program this feature.

Thermal Path and PCB Design

The smart slave IC has an exposed pad on the top-side of the package that is designed as an additional thermal path. This pad is electrically connected to A_{GND}/V_{SS}, but is not intended for use as an electrical connection. Since there is normally sufficient airflow above the regulator, conducting heat from the top of the package results in a low junction-to-ambient thermal impedance, and hence lower junction temperature. This method provides an additional thermal path to the heat flow from the die to the PCB to ambient, and also reduces the temperature of the PCB. Thermal performance is presented for various thermal conditions and airflow rates in the SOA plots.

PCB Layout

PCB layout can significantly affect the performance of the regulator. Careful attention should be paid to the location of the input capacitors and the output inductor, which should be placed close to the IC. The VX traces include large voltage swings (greater than 12V) with dv/dt greater than 10V/ns. It is recommended that these traces are not only kept short, but also are shielded with a ground plane immediately beneath.

Gerber files with layout information and complete reference designs can be obtained by contacting a Maxim account representative. Also contact Maxim to obtain QFN layout guidelines for optimal design.

Table 2. Typical Boost, Filtering, and Decoupling Capacitor Requirements

DESCRIPTION	VALUE	TYPE	PACKAGE	QTY
V_{DD} Capacitor	0.1µF/6.3V	X7R/125°C	0603	1
V_{CC} Capacitor (Note 1)	1µF/6.3V	X7R/125°C	0603	1
Boost Capacitor	0.22µF/6.3V	X7R/125°C	0402	1
V_{DD} RFILTER	10Ω	1/16W 1%	0402	1
V_{DDH} HF Capacitor (Note 2)	1µF/16V	X7R/125°C	0603	2
V_{DDH} HF Capacitor (Note 2)	0.1µF/16V	X7R/125°C	0402	2
V_{DDH} Bulk Capacitor (Note 3)	10µF/16V	X5R	0805/1206	2

Note 1: V_{CC} should be directly connected to bias supply.
Note 2: All V_{DDH} high-frequency capacitors must be placed in close proximity to the slave IC and on the same side of the PCB as the slave IC. Refer to Maxim's layout guideline for component placement requirements and recommendations.
Note 3: For operation below 10.8V, two 22µF bulk capacitor are recommended instead of two 10µF capacitors.

Ordering Information

PART	DESCRIPTION	PACKAGE	SHIPPING METHOD	PACKAGE MARKING
VT1697SBFQX*	55A Smart-Slave Device	16 FCQFN	2.5ku Tape & Reel	VT1697SBF

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES
0	1/14	Initial Release	—
1	4/14	Updated Operating Current Rating	1
2	5/14	Updated *Electrical Characteristics* table and *Overcurrent Protection* section	3
3	10/16	Updated *Absolute Maximum Ratings* section	2
4	3/17	Updated *Package Information*, *Absolute Maximum Ratings* sections, and *Electrical Characteristics* and *Pin Description* tables	2–3, 7

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

