

PROTECTION PRODUCTS
Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	200	Watts
Maximum Peak Pulse Current ($t_p = 8/20\mu s$)	I_{pp}	8	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{pp}	+/- 20 +/- 15	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

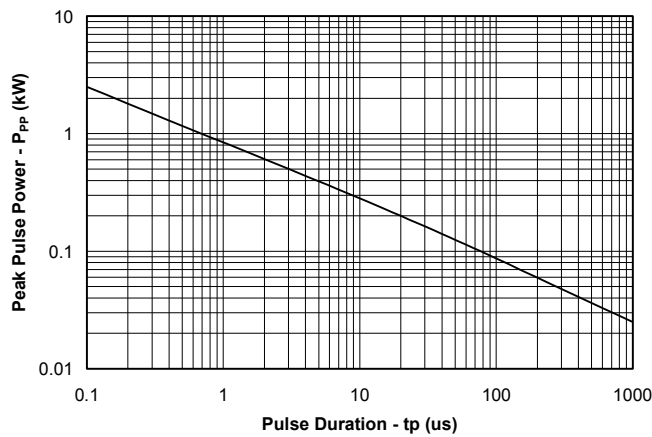
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	13.3			V
Reverse Leakage Current	I_R	$V_{RWM} = 12V, T=25^\circ C$			1	μA
Forward Voltage	V_F	$I_F = 10mA$		0.8		V
Clamping Voltage	V_C	$I_{pp} = 1A, t_p = 8/20\mu s$			19	V
Clamping Voltage	V_C	$I_{pp} = 8A, t_p = 8/20\mu s$			25	V
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$			60	pF

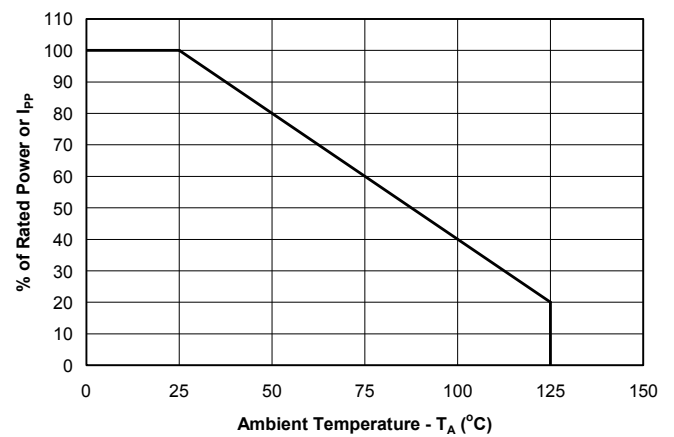
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Typical Characteristics

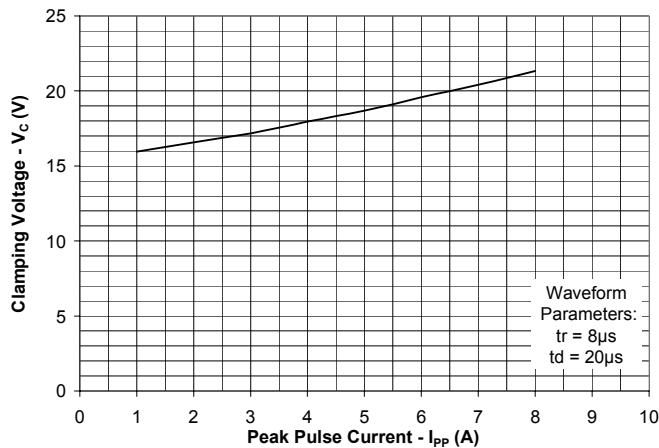
Non-Repetitive Peak Pulse Power vs. Pulse Time



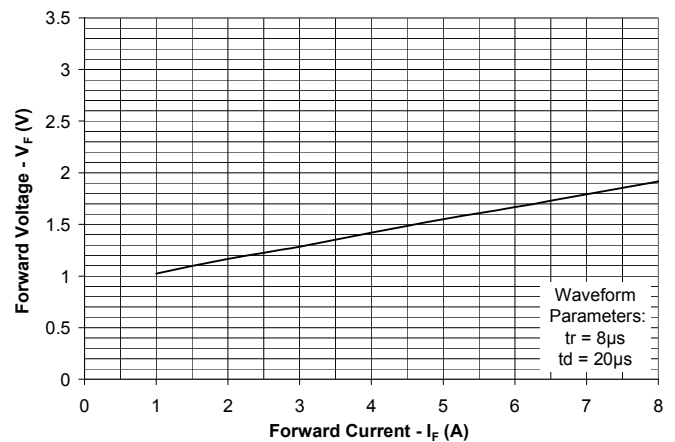
Power Derating Curve



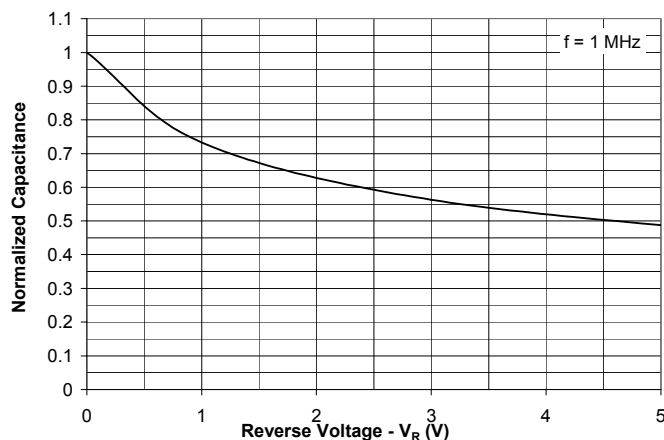
Clamping Voltage vs. Peak Pulse Current



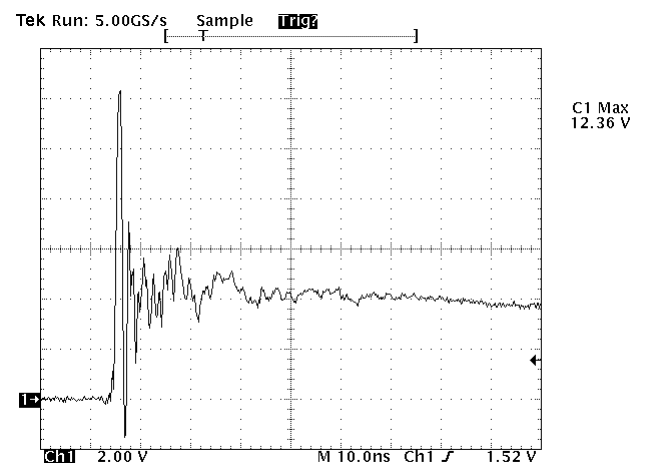
Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage



**ESD Clamping
(8kV Contact per IEC 61000-4-2)**



PROTECTION PRODUCTS**Applications Information****Device Connection Options**

These TVS diodes are designed to protect one data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode band should be placed towards the line that is to be protected.

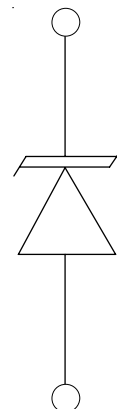
Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Circuit Diagram

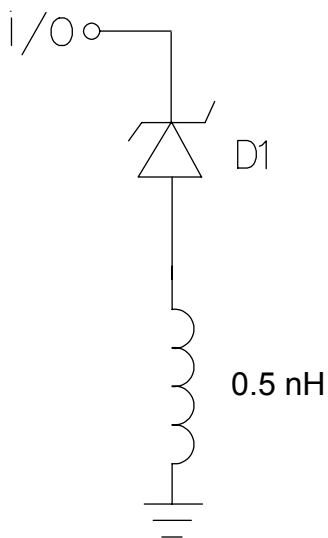
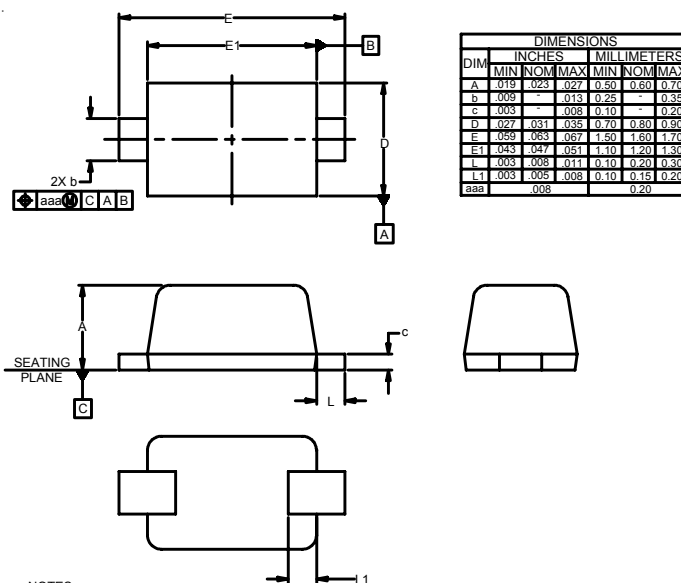
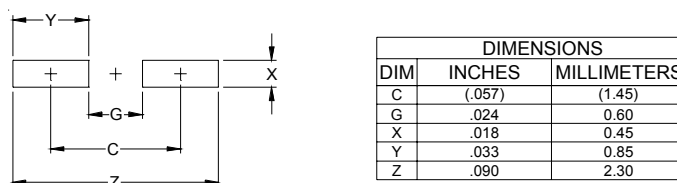
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Applications Information - Spice Model

Figure 1 - uClamp1201H Spice Model

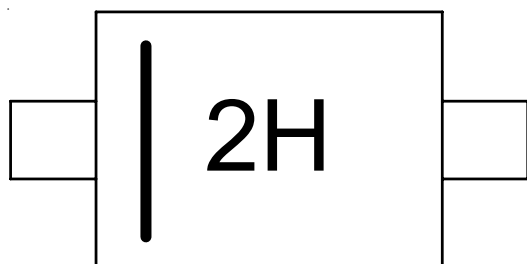
Table 1 - uClamp1201H Spice Parameters		
Parameter	Unit	D1 (TVS)
IS	Amp	1.48E-14
BV	Volt	15.33
VJ	Volt	0.723
RS	Ohm	0.772
IBV	Amp	1.0E-3
CJO	Farad	52E-12
TT	sec	2.541E-9
M	--	0.268
N	--	1.1
EG	eV	1.11

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Outline Drawing - SOD-523

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SOD-523

NOTES:

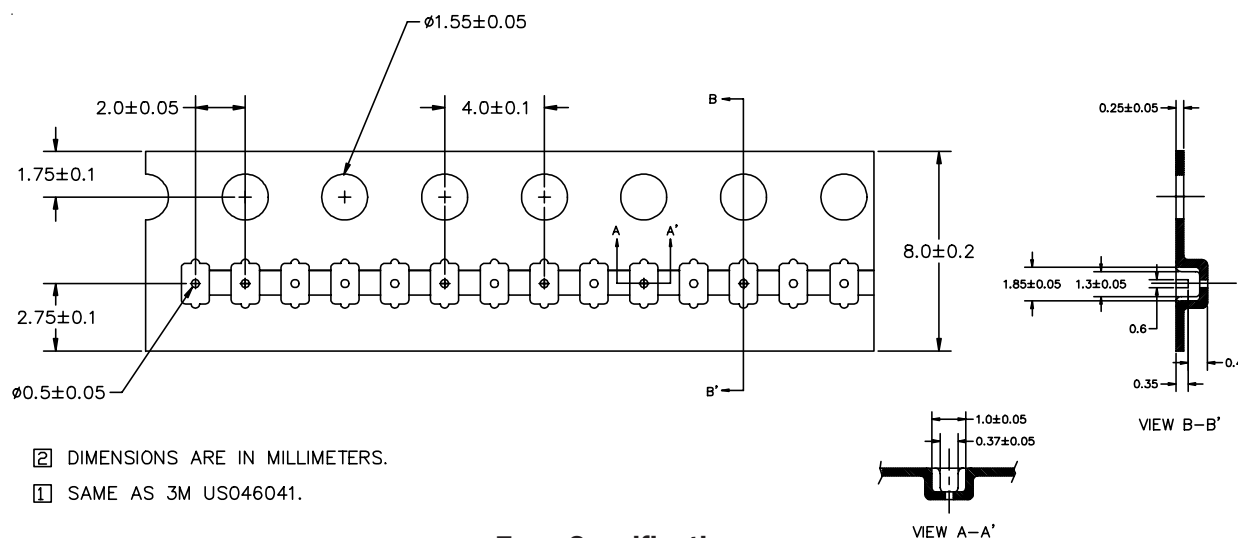
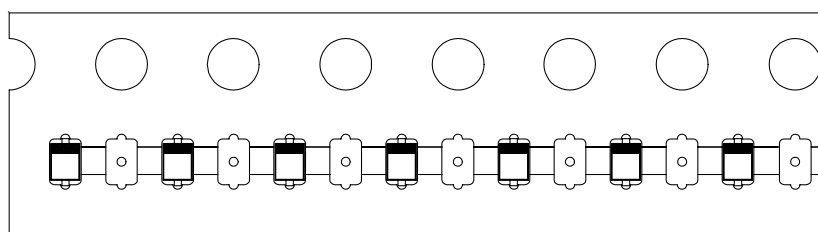
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
COMPANY'S MANUFACTURING GUIDELINES ARE MET.

PROTECTION PRODUCTS
Marking Code

Ordering Information

Part Number	Working Voltage	Device Marking	Qty per Reel	Reel Size
uClamp1201H.TCT	12V	2H	3,000	7 Inch

Note: Devices are lead-free

MicroClamp, uClamp and μ Clamp are marks of Semtech Corporation

Tape and Reel Specification

Tape Specifications

Device Orientation in Tape
Contact Information

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