ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
V_i	Input Voltage	-0.3V to V_{CC} +0.3V	V
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient SO8 MiniSO8 DFN8	 175 215 70	°C/W
Pd	Power Dissipation [2] SO8 MiniSO8 DFN8	 0.71 0.58 1.79	W
ESD	Human Body Model (pin to pin): TS419[3], TS421	1.5	kV
ESD	Machine Model - 220pF - 240pF (pin to pin)	100	V
Latch-up	Latch-up Immunity (All pins)	200	mA
	Lead Temperature (soldering, 10sec)	250	°C
	Output Short-Circuit to Vcc or GND	continous [4]	

1. All voltage values are measured with respect to the ground pin.
2. Pd has been calculated with Tamb = 25°C, Tjunction = 150°C.
3. TS419 stands 1.5KV on all pins except standby pin which stands 1KV.
4. Attention must be paid to continous power dissipation (V_{DD} x 300mA). Exposure of the IC to a short circuit for an extended time period is dramatically reducing product life expectancy.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 5.5	V
R_L	Load Resistor	≥ 16	Ω
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
C_L	Load Capacitor R_L = 16 to 100Ω R_L > 100Ω	 400 100	pF
V_{ICM}	Common Mode Input Voltage Range	GND to V_{CC}-1V	V
V_{STB}	Standby Voltage Input TS421 ACTIVE / TS419 in STANDBY TS421 in STANDBY / TS419 ACTIVE	 $1.5 \le V_{STB} \le V_{CC}$ $GND \le V_{STB} \le 0.4$ [1]	V
R_{THJA}	Thermal Resistance Junction to Ambient SO8 MiniSO8 DFN8 [2]	 150 190 41	°C/W
T_{wu}	Wake-up time from standby to active mode (Cb = 1µF) [3]	≥ 0.12	s

1. The minimum current consumption ($I_{STANDBY}$) is guaranteed at V_{CC} (TS419) or GND (TS421) for the whole temperature range.
2. When mounted on a 4-layer PCB
3. For more details on T_{WU}, please refer to application note section on Wake-up time page 28.

FIXED GAIN VERSION SPECIFIC ELECTRICAL CHARACTERISTICS

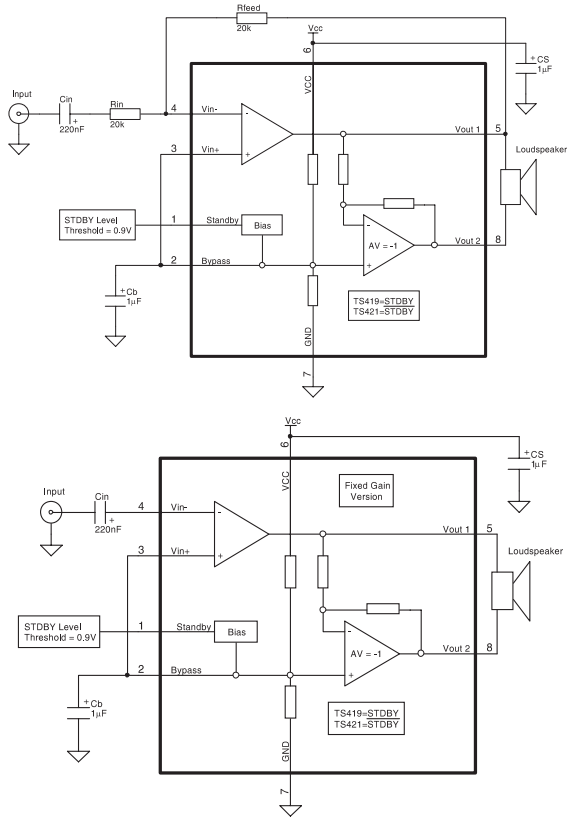
V_{CC} from **+5V to +2V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{IN}	Input Resistance		20		kΩ
G	Gain value for Gain TS419/TS421-2 Gain value for Gain TS419/TS421-4 Gain value for Gain TS419/TS421-8		6dB 12dB 18dB		dB

APPLICATION COMPONENTS INFORMATION

Components	Functional Description
R_{IN}	Inverting input resistor which sets the closed loop gain in conjunction with R_{FEED}. This resistor also forms a high pass filter with C_{IN} (fcl = 1 / (2 x Pi x R_{IN} x C_{IN})). **Not needed in fixed gain versions.**
C_{IN}	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminal
R_{FEED}	Feedback resistor which sets the closed loop gain in conjunction with R_{IN}. A_V= Closed Loop Gain= 2xR_{FEED}/R_{IN}. **Not needed in fixed gain versions.**
C_S	Supply Bypass capacitor which provides power supply filtering.
C_B	Bypass capacitor which provides half supply filtering.

TYPICAL APPLICATION SCHEMATICS:



ELECTRICAL CHARACTERISTICS

V_{CC} = **+5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.8	2.5	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{STANDBY}$=GND for TS421 No input signal, $V_{STANDBY}$=Vcc for TS419		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 16 or 32Ω, Rfeed=20kΩ		5	25	mV
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 10% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω THD+N = 10% Max, F = 1kHz, R_L = 16Ω	166 240	190 207 258 270 295 367		mW
THD + N	Total Harmonic Distortion + Noise (A_V=2) R_L = 32Ω, P_{out} = 150mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 220mW, 20Hz ≤ F ≤ 20kHz		0.15 0.2		%
PSRR	Power Supply Rejection Ratio (A_V=2) [1] F = 1kHz, Vripple = 200mVpp, input grounded, Cb=1µF	50	56		dB
SNR	Signal-to-Noise Ratio (Filter Type A, A_V=2) [1] (R_L = 32Ω, THD +N < 0.5%, 20Hz ≤ F ≤ 20kHz)	85	98		dB
Φ_M	Phase Margin at Unity Gain R_L = 16Ω, C_L = 400pF		58		Degrees
GM	Gain Margin R_L = 16Ω, C_L = 400pF		18		dB
GBP	Gain Bandwidth Product R_L = 16Ω		1.1		MHz
SR	Slew Rate R_L = 16Ω		0.4		V/µS

1. Guaranteed by design and evaluation.

ELECTRICAL CHARACTERISTICS

V_{CC} = **+3.3V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified) **1)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.8	2.5	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{STANDBY}$=GND for TS421 No input signal, $V_{STANDBY}$=Vcc for TS419		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 16 or 32Ω, Rfeed=20kΩ		5	25	mV
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 10% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω THD+N = 10% Max, F = 1kHz, R_L = 16Ω	 65 91 	 75 81 102 104 113 143		mW
THD + N	Total Harmonic Distortion + Noise (A_V=2) R_L = 32Ω, P_{out} = 50mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 70mW, 20Hz ≤ F ≤ 20kHz		 0.15 0.2		%
PSRR	Power Supply Rejection Ratio inputs grounded, F = 1kHz, Vripple = 200mVpp, Cb=1µF	50	56		dB
SNR	Signal-to-Noise Ratio (Weighted A, A_V=2) (R_L = 32Ω, THD +N < 0.5%, 20Hz ≤ F ≤ 20kHz)	82	94		dB
Φ_M	Phase Margin at Unity Gain R_L = 16Ω, C_L = 400pF		58		Degrees
GM	Gain Margin R_L = 16Ω, C_L = 400pF		18		dB
GBP	Gain Bandwidth Product R_L = 16Ω		1.1		MHz
SR	Slew Rate R_L = 16Ω		0.4		V/µS

1. All electrical values are guaranted with correlation measurements at 2V and 5V

ELECTRICAL CHARACTERISTICS

V_{CC} = **+2.5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)[1)]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.7	2.5	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{STANDBY}$=GND for TS421 No input signal, $V_{STANDBY}$=Vcc for TS419		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 16 or 32Ω, Rfeed=20kΩ		5	25	mV
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 10% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω THD+N = 10% Max, F = 1kHz, R_L = 16Ω	32 44	37 41 52 50 55 70		mW
THD + N	Total Harmonic Distortion + Noise (A_V=2) R_L = 32Ω, P_{out} = 30mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 40mW, 20Hz ≤ F ≤ 20kHz		0.15 0.2		%
PSRR	Power Supply Rejection Ratio (A_V=2) inputs grounded, F = 1kHz, Vripple = 200mVpp, Cb=1µF	50	56		dB
SNR	Signal-to-Noise Ratio (Weighted A, A_V=2) (R_L = 32Ω, THD +N < 0.5%, 20Hz ≤ F ≤ 20kHz)	80	91		dB
Φ_M	Phase Margin at Unity Gain R_L = 16Ω, C_L = 400pF		58		Degrees
GM	Gain Margin R_L = 16Ω, C_L = 400pF		18		dB
GBP	Gain Bandwidth Product R_L = 16Ω		1.1		MHz
SR	Slew Rate R_L = 16Ω		0.4		V/µS

1. All electrical values are guaranted with correlation measurements at 2V and 5V

ELECTRICAL CHARACTERISTICS

V_{CC} = **+2V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.7	2.5	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{STANDBY}$=GND for TS421 No input signal, $V_{STANDBY}$=Vcc for TS419		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 16 or 32Ω, Rfeed=20kΩ		5	25	mV
P_O	Output Power THD+N = 0.1% Max, F = 1kHz, R_L = 32Ω THD+N = 1% Max, F = 1kHz, R_L = 32Ω THD+N = 10% Max, F = 1kHz, R_L = 32Ω THD+N = 0.1% Max, F = 1kHz, R_L = 16Ω THD+N = 1% Max, F = 1kHz, R_L = 16Ω THD+N = 10% Max, F = 1kHz, R_L = 16Ω	19 24	20 23 30 26 30 40		mW
THD + N	Total Harmonic Distortion + Noise (A_V=2) R_L = 32Ω, P_{out} = 13mW, 20Hz ≤ F ≤ 20kHz R_L = 16Ω, P_{out} = 20mW, 20Hz ≤ F ≤ 20kHz		0.1 0.15		%
PSRR	Power Supply Rejection Ratio (A_V=2) [1] inputs grounded, F = 1kHz, Vripple = 200mVpp, Cb=1µF	49	54		dB
SNR	Signal-to-Noise Ratio (Weighted A, A_V=2) [1] (R_L = 32Ω, THD +N < 0.5%, 20Hz ≤ F ≤ 20kHz)	80	89		dB
Φ_M	Phase Margin at Unity Gain R_L = 16Ω, C_L = 400pF		58		Degrees
GM	Gain Margin R_L = 16Ω, C_L = 400pF		20		dB
GBP	Gain Bandwidth Product R_L = 16Ω		1.1		MHz
SR	Slew Rate R_L = 16Ω		0.4		V/µS

1. Guaranteed by design and evaluation.

Index of Graphs

Note : All measurements made with Rin=20kΩ, Cb=1µF, and Cin=10µF unless otherwise specified.

Fig. 1: Open Loop Gain and Phase vs Frequency

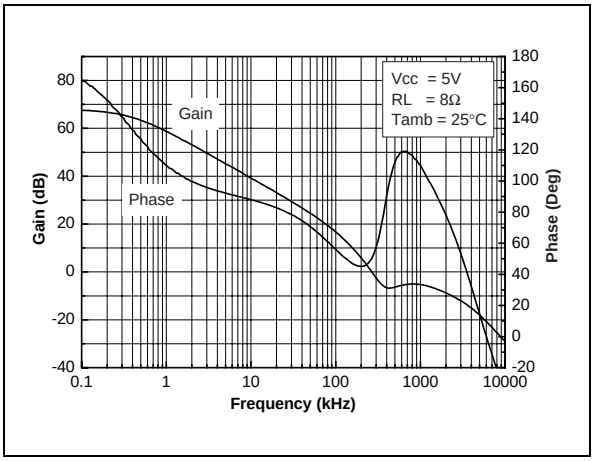


Fig. 2: Open Loop Gain and Phase vs Frequency

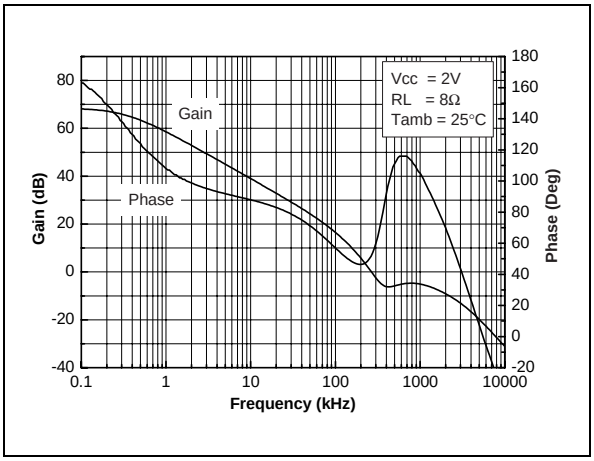


Fig. 3: Open Loop Gain and Phase vs Frequency

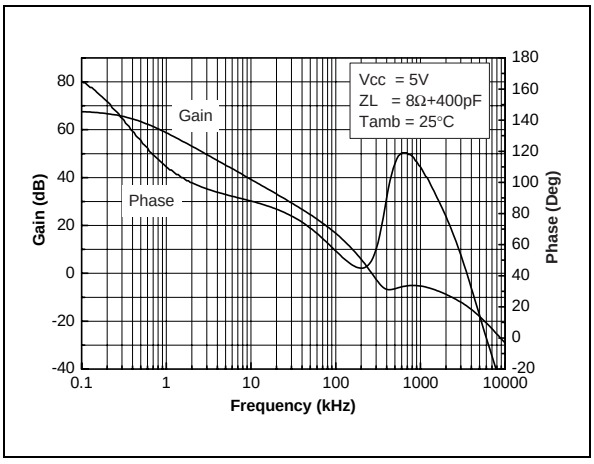


Fig. 4: Open Loop Gain and Phase vs Frequency

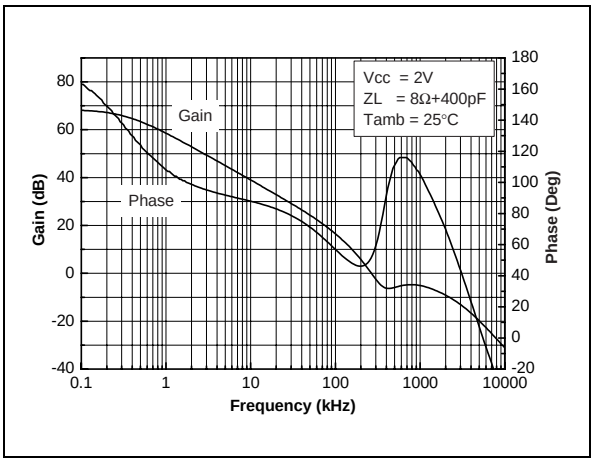


Fig. 5: Open Loop Gain and Phase vs Frequency

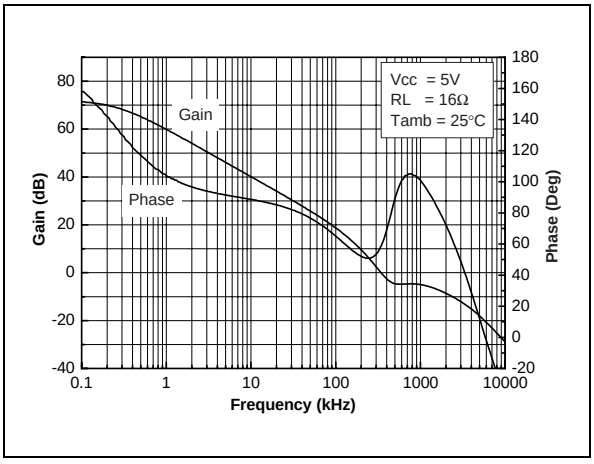


Fig. 6: Open Loop Gain and Phase vs Frequency

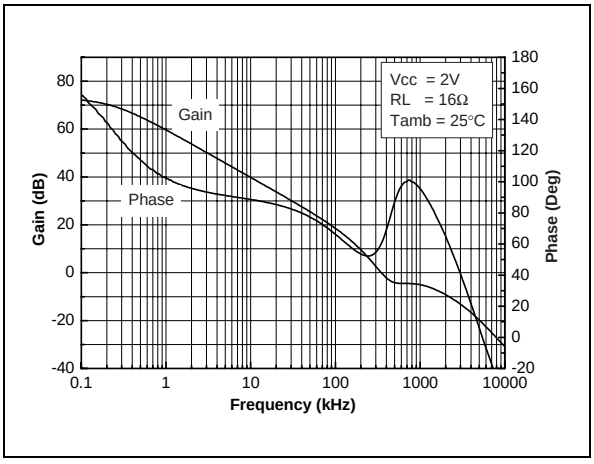


Fig. 7: Open Loop Gain and Phase vs Frequency

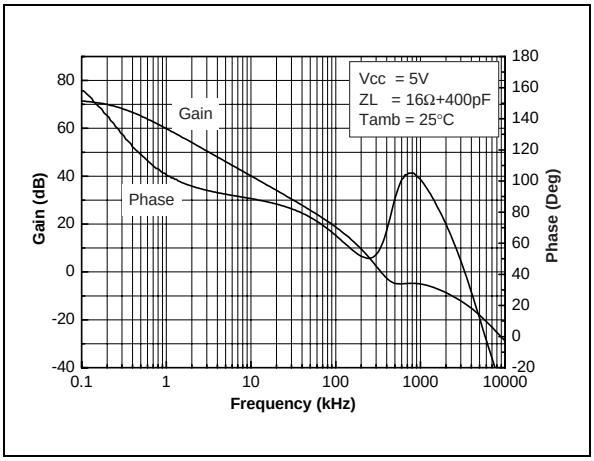


Fig. 8: Open Loop Gain and Phase vs Frequency

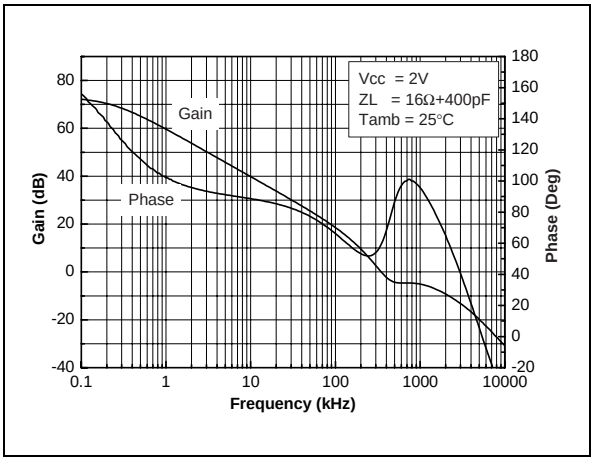


Fig. 9: Open Loop Gain and Phase vs Frequency

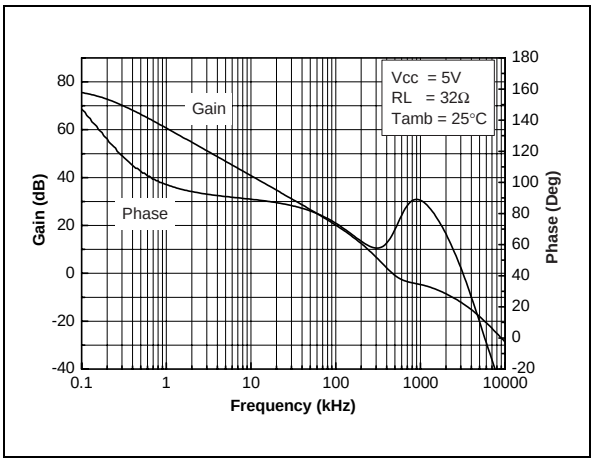


Fig. 10: Open Loop Gain and Phase vs Frequency

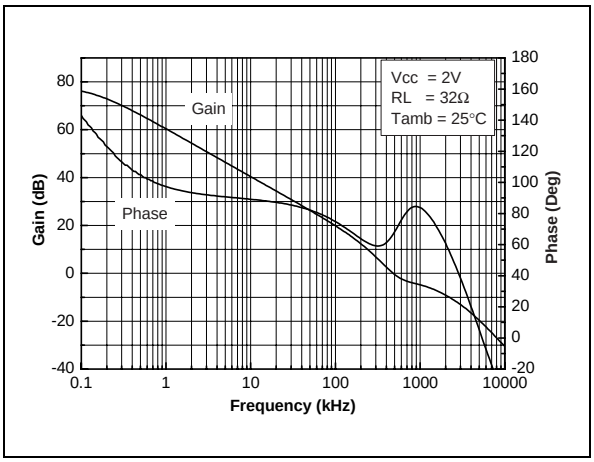


Fig. 11: Open Loop Gain and Phase vs Frequency

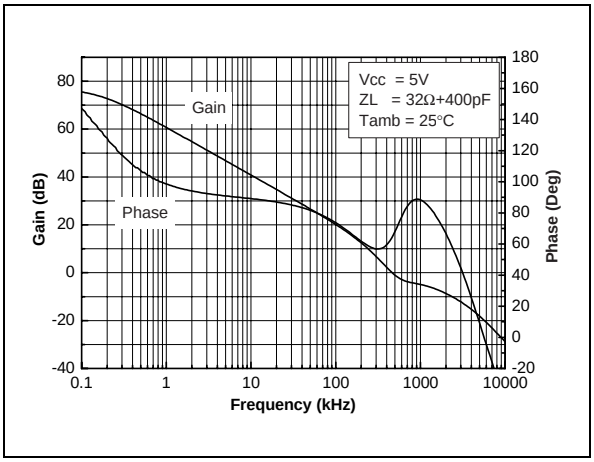


Fig. 12: Open Loop Gain and Phase vs Frequency

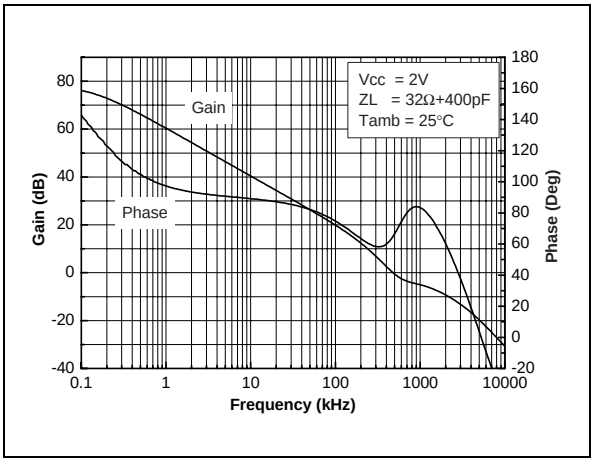


Fig. 13: Current Consumption vs Power Supply Voltage

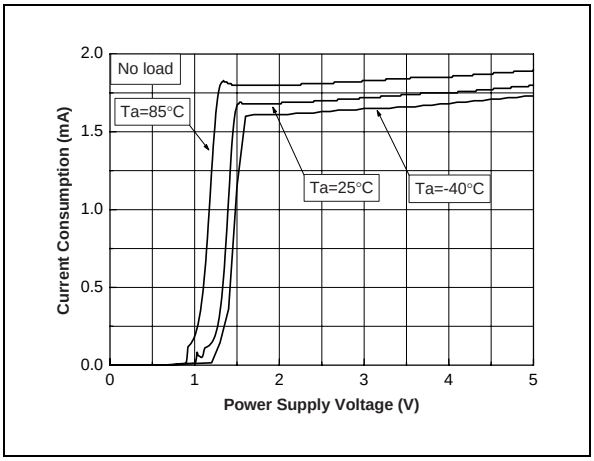


Fig. 14: Current Consumption vs Standby Voltage

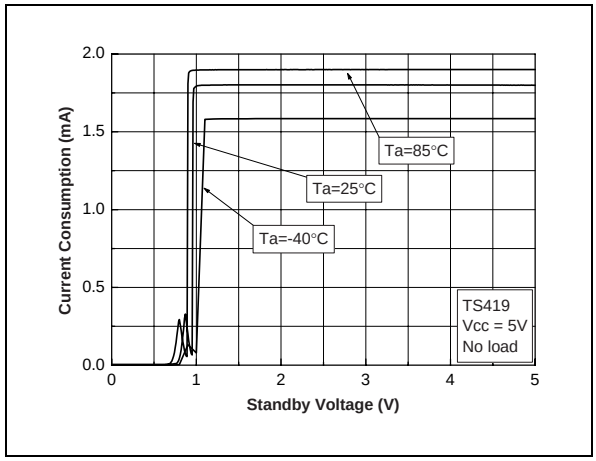


Fig. 15: Current Consumption vs Standby Voltage

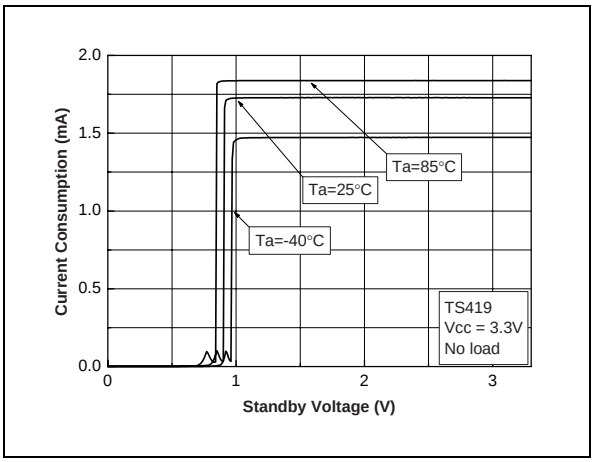


Fig. 16: Current Consumption vs Standby Voltage

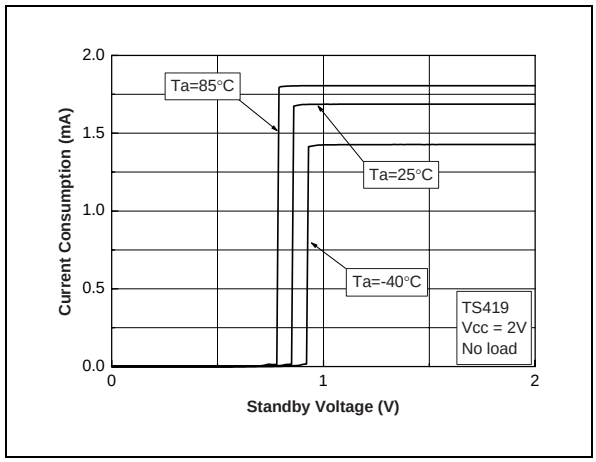


Fig. 17: Current Consumption vs Standby Voltage

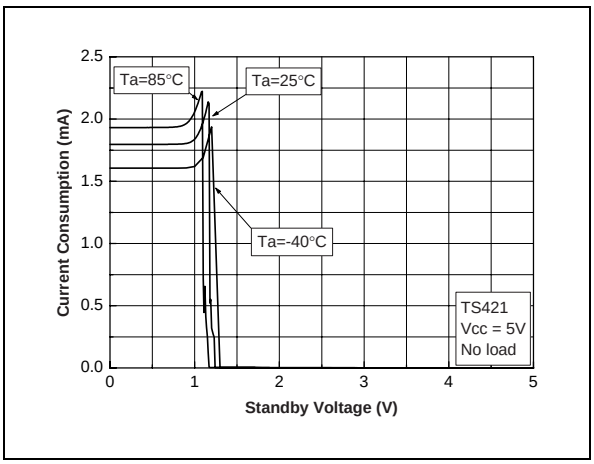


Fig. 18: Current Consumption vs Standby Voltage

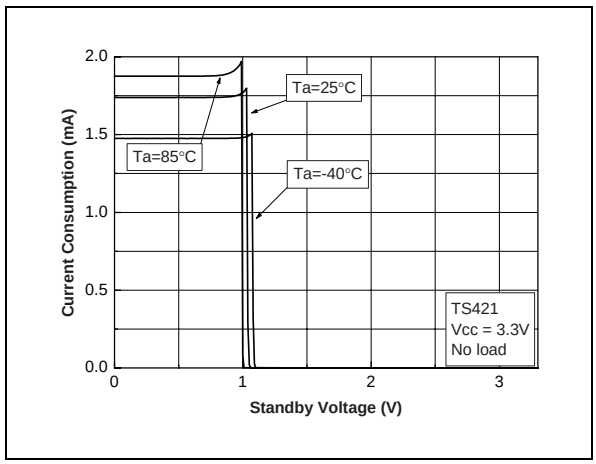


Fig. 19: Current Consumption vs Standby Voltage

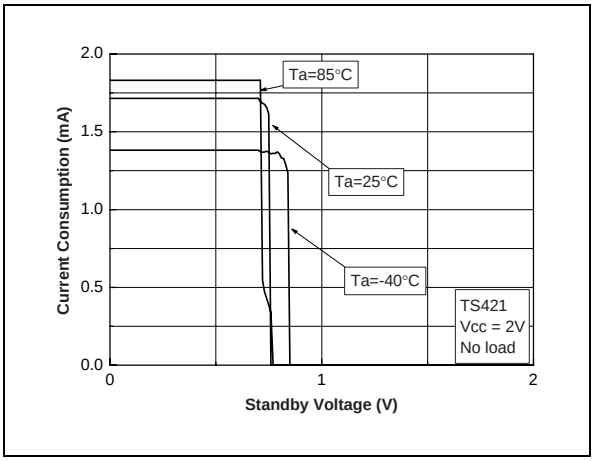


Fig. 20: Output Power vs Power Supply Voltage

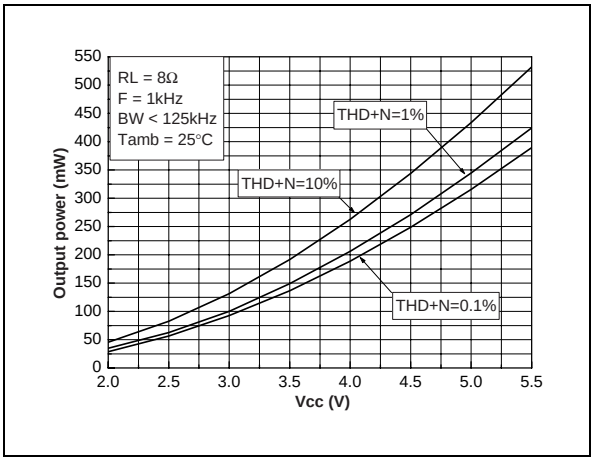


Fig. 21: Output Power vs Power Supply Voltage

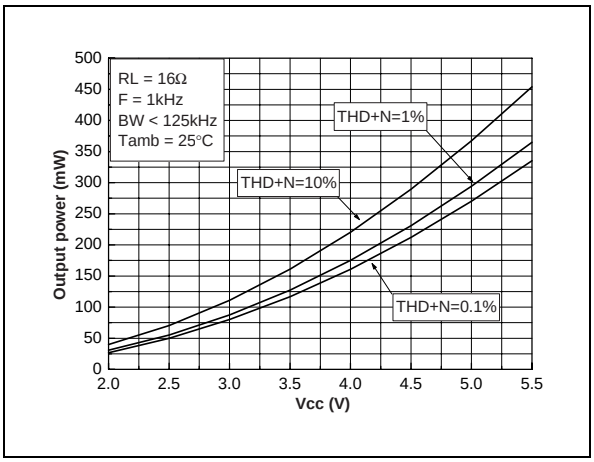


Fig. 22: Output Power vs Power Supply Voltage

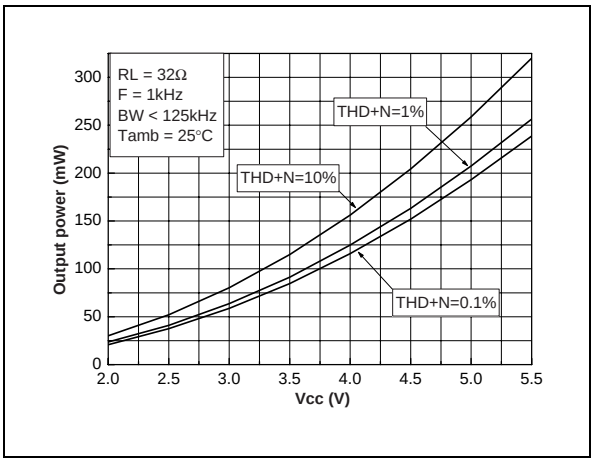


Fig. 23: Output Power vs Power Supply Voltage

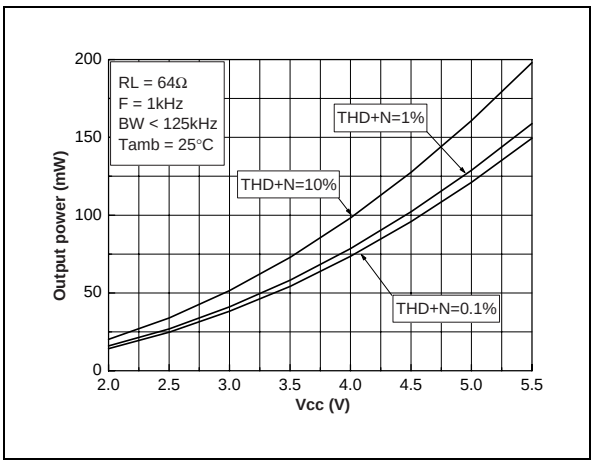


Fig. 24: Output Power vs Load Resistor

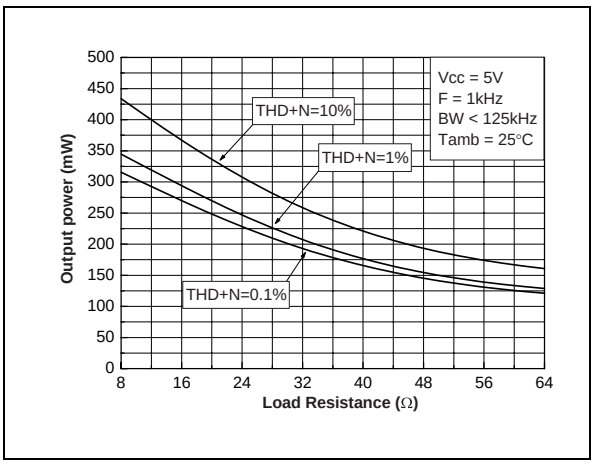


Fig. 25: Output Power vs Load Resistor

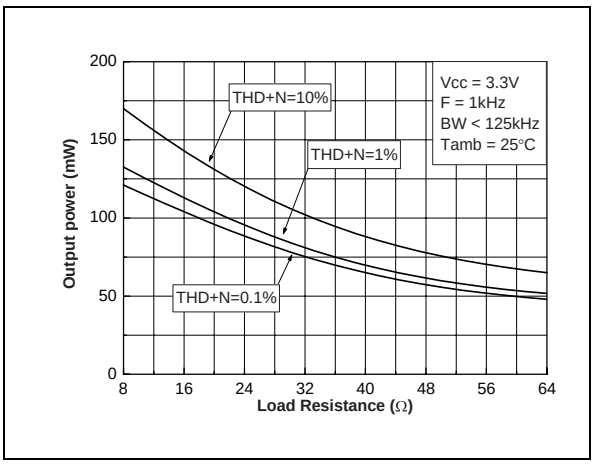


Fig. 26: Output Power vs Load Resistor

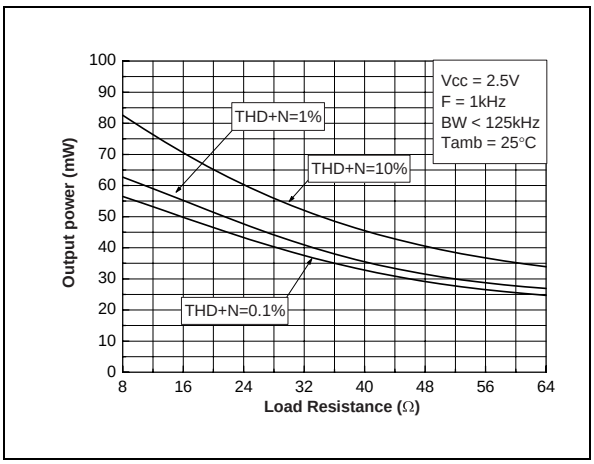


Fig. 27: Output Power vs Load Resistor

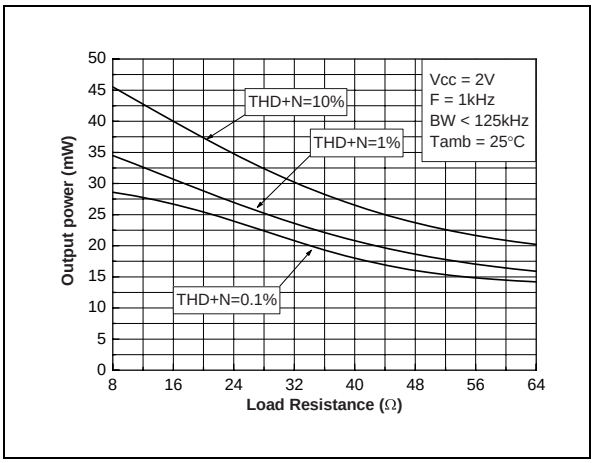


Fig. 28: Power Dissipation vs Output Power

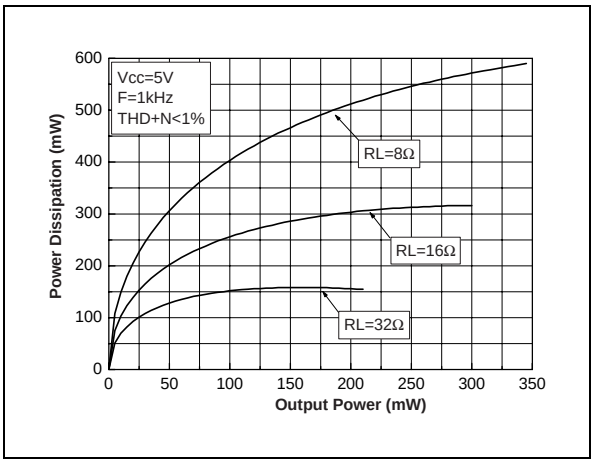


Fig. 29: Power Dissipation vs Output Power

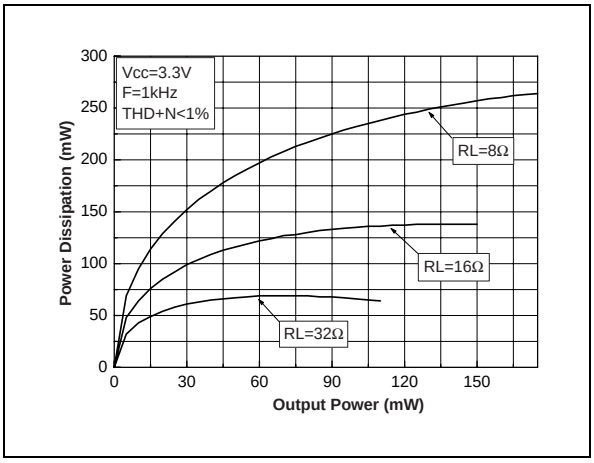


Fig. 30: Power Dissipation vs Output Power

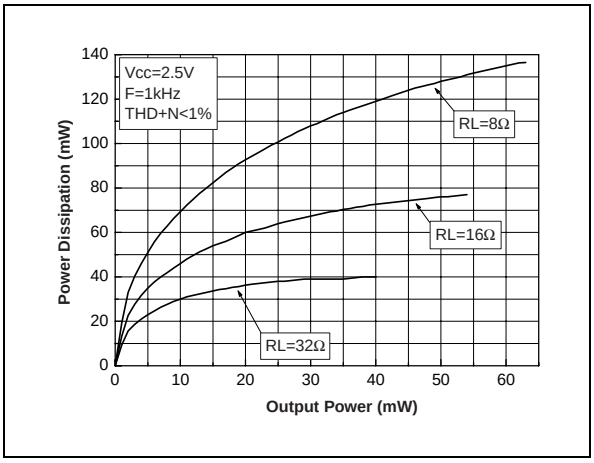


Fig. 31: Power Dissipation vs Output Power

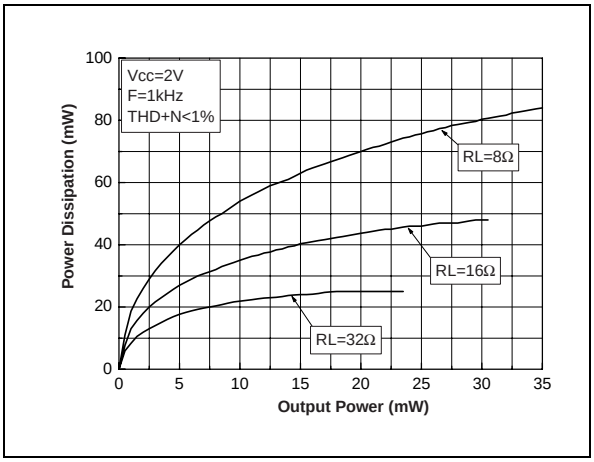


Fig. 32: Power Derating Curves

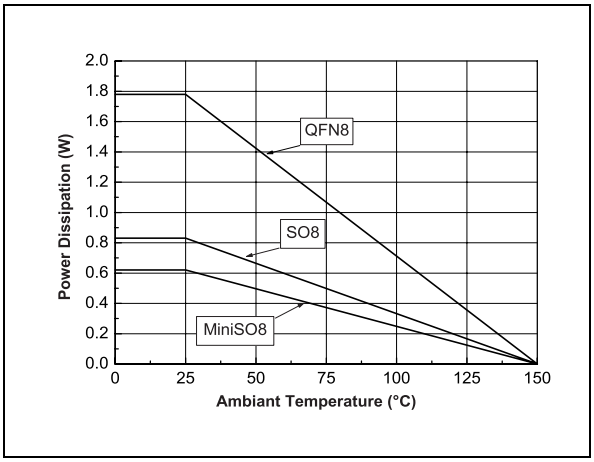


Fig. 33: Output Voltage Swing For One Amp. vs Power Supply Voltage

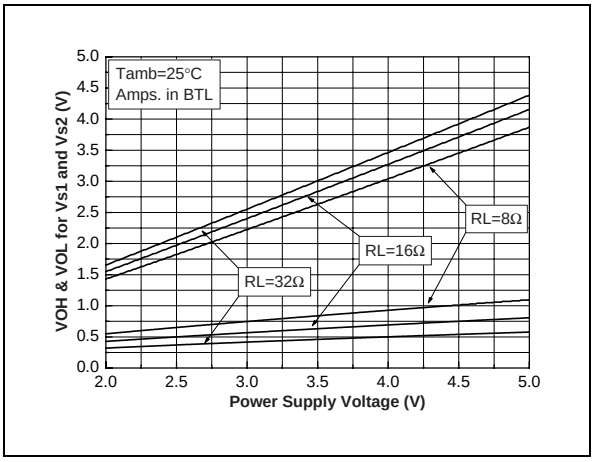


Fig. 34: Low Frequency Cut Off vs Input Capacitor for fixed gain versions

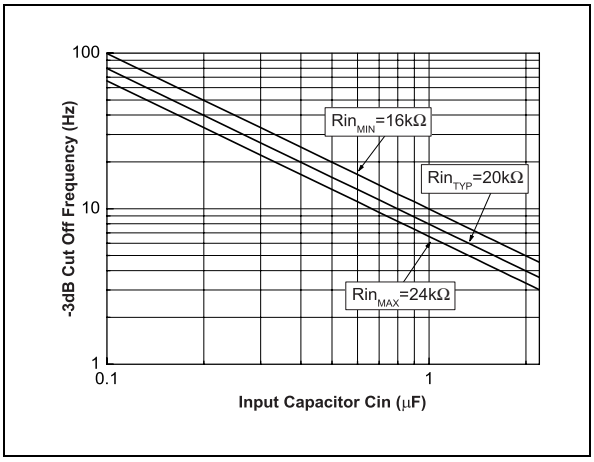


Fig. 35: THD + N vs Output Power

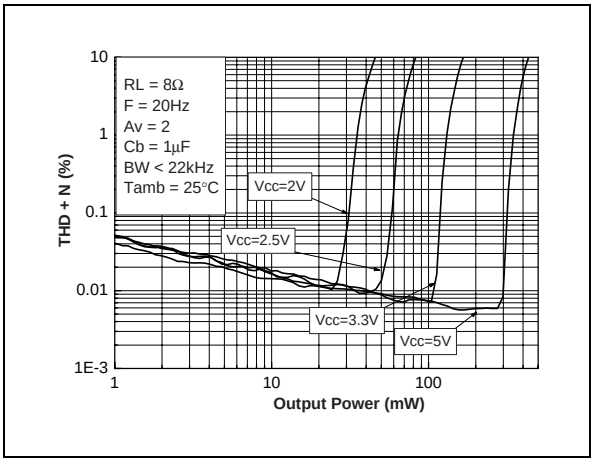


Fig. 36: THD + N vs Output Power

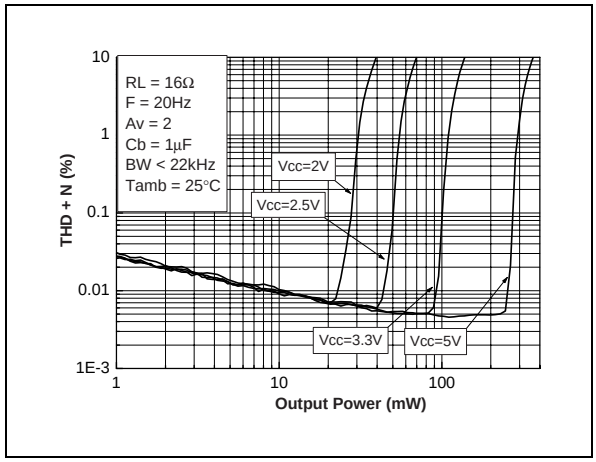


Fig. 37: THD + N vs Output Power

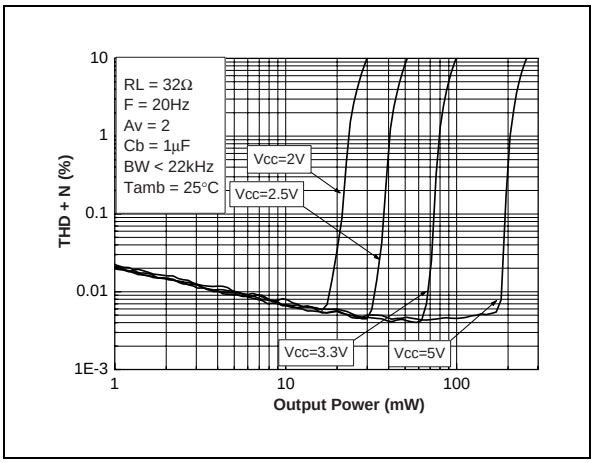


Fig. 38: THD + N vs Output Power

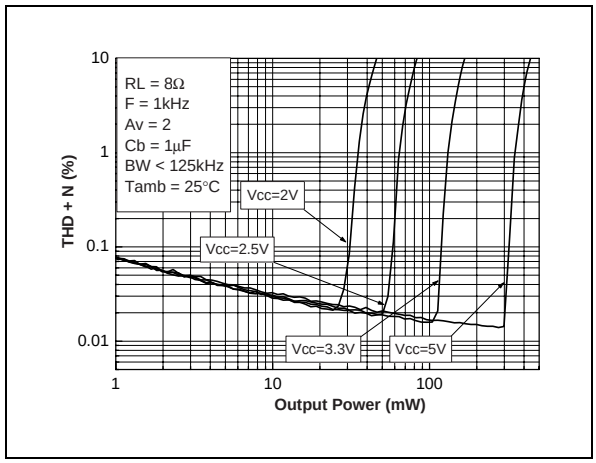


Fig. 39: THD + N vs Output Power

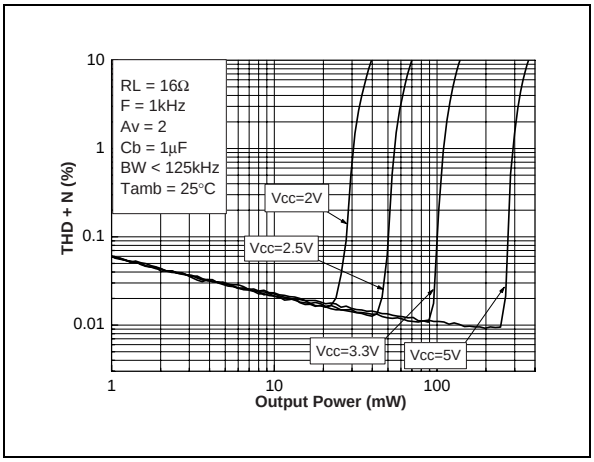


Fig. 40: THD + N vs Output Power

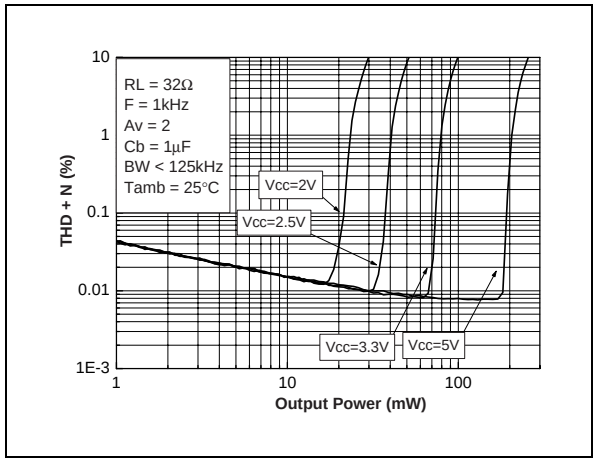


Fig. 41: THD + N vs Output Power

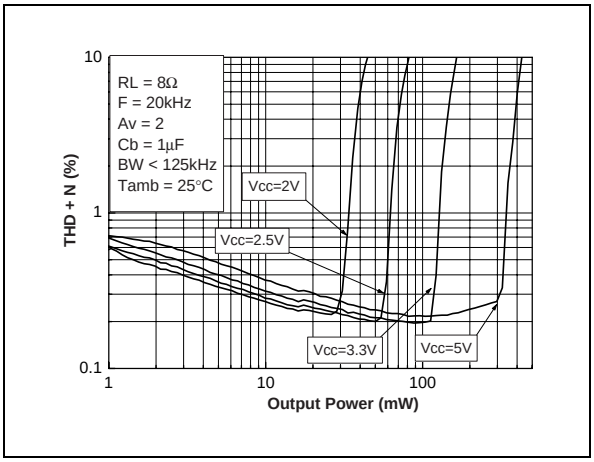


Fig. 42: THD + N vs Output Power

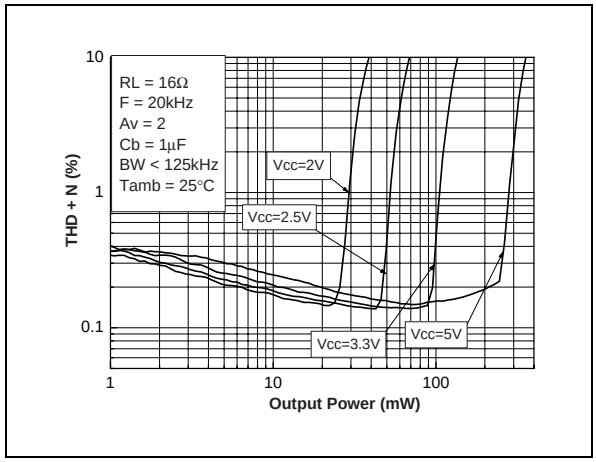


Fig. 43: THD + N vs Output Power

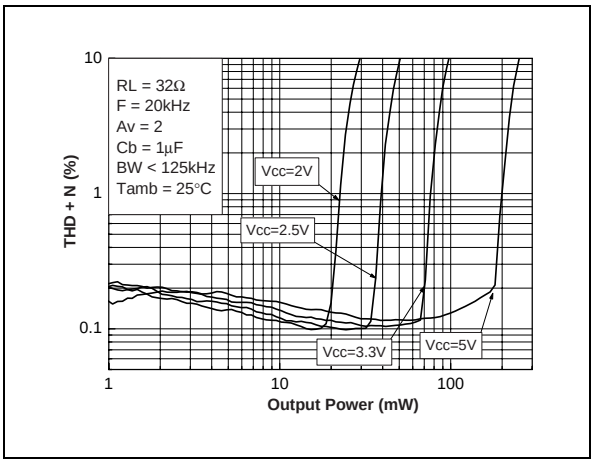


Fig. 44: THD + N vs Frequency

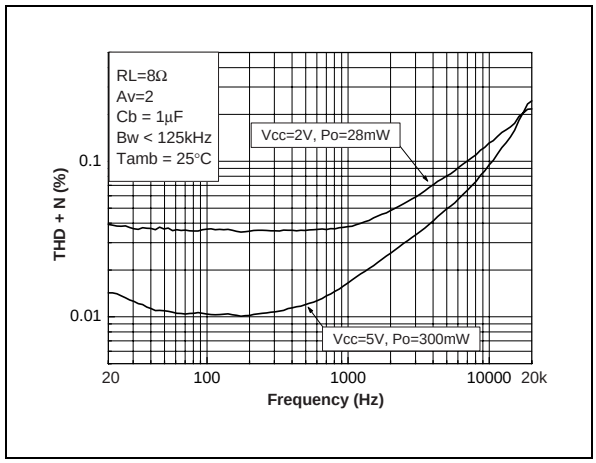


Fig. 45: THD + N vs Frequency

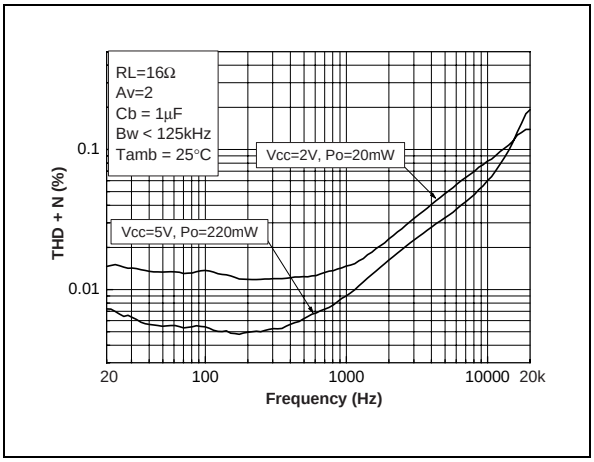


Fig. 46: THD + N vs Frequency

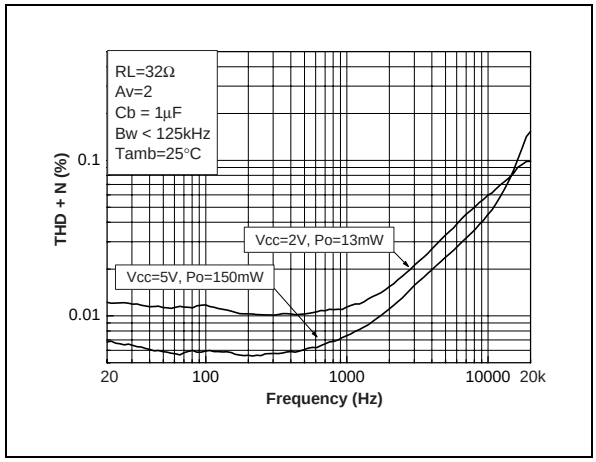


Fig. 47: Signal to Noise Ratio vs Power Supply Voltage with Unweighted Filter (20Hz to 20kHz)

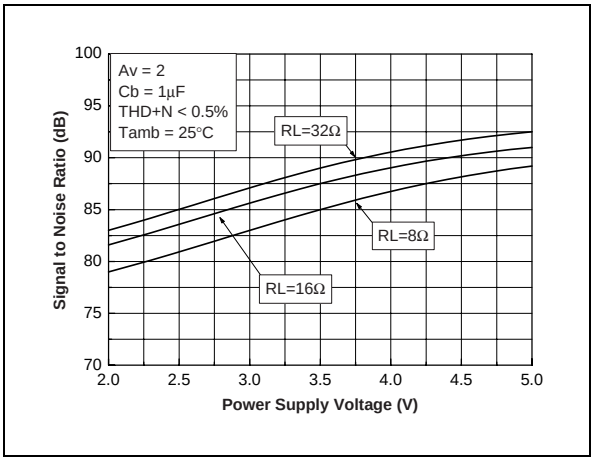


Fig. 48: Signal to Noise Ratio vs Power Supply Voltage with Weighted Filter Type A

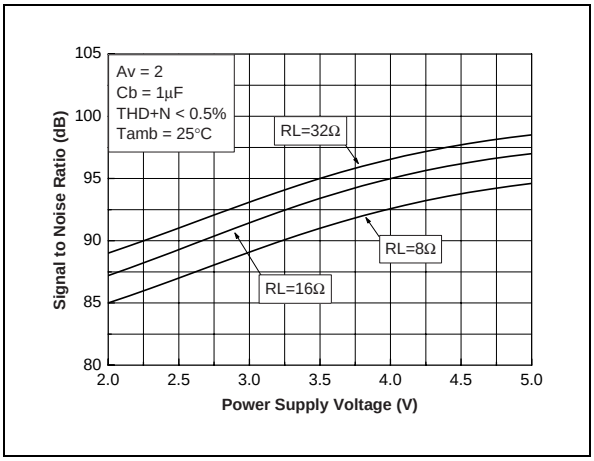


Fig. 49: Noise Floor

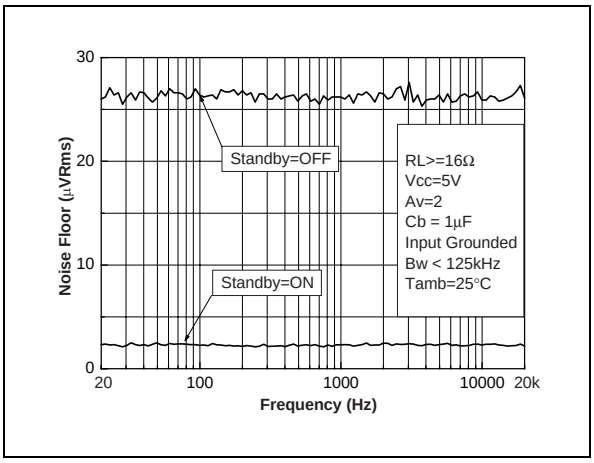


Fig. 50: Noise Floor

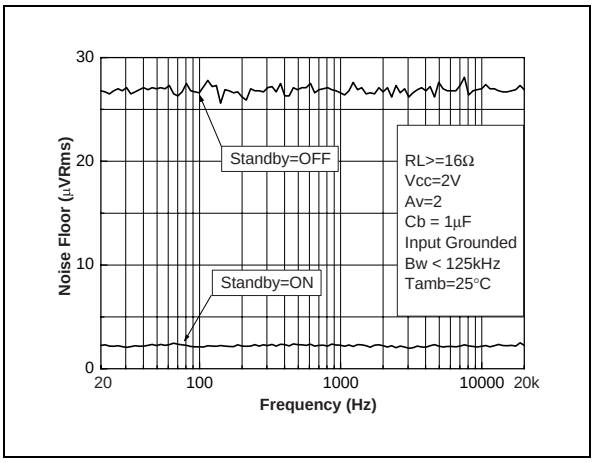


Fig. 51: PSRR vs Input Capacitor

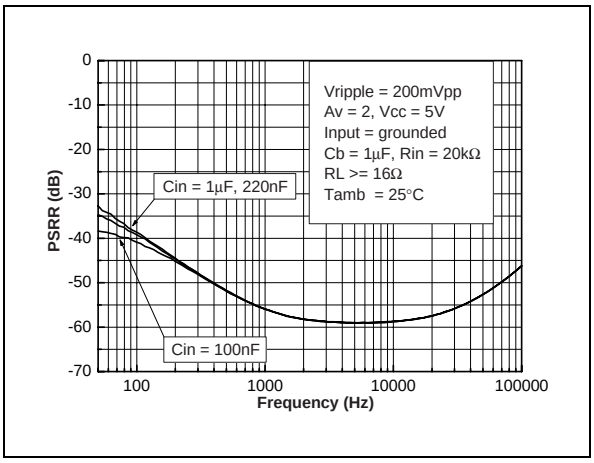


Fig. 52: PSRR vs Power Supply Voltage

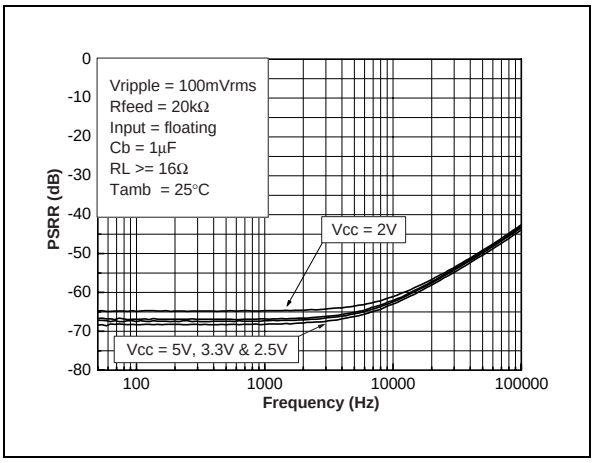


Fig. 53: PSRR vs Bypass Capacitor

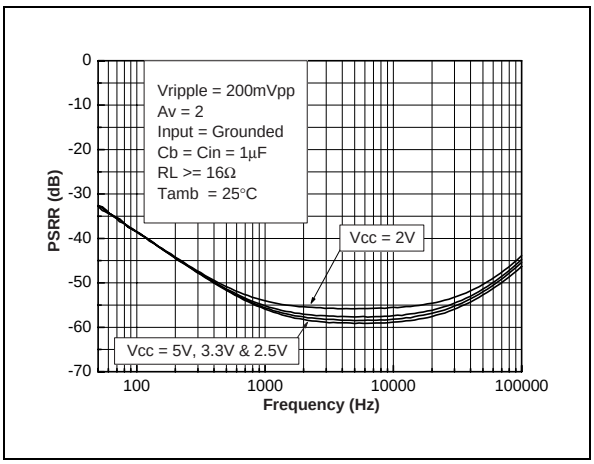


Fig. 54: PSRR vs Bypass Capacitor

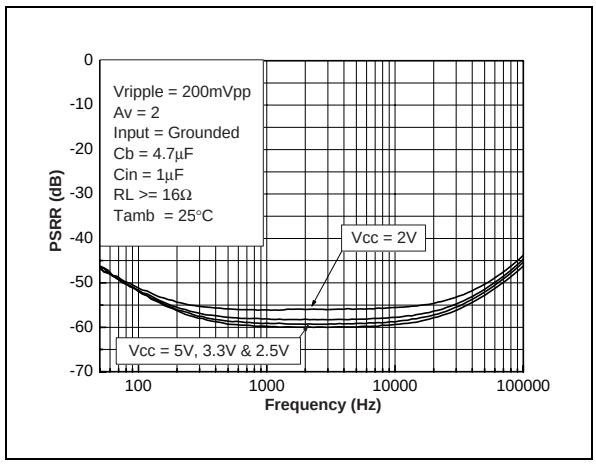


Fig. 55: PSRR vs Bypass Capacitor

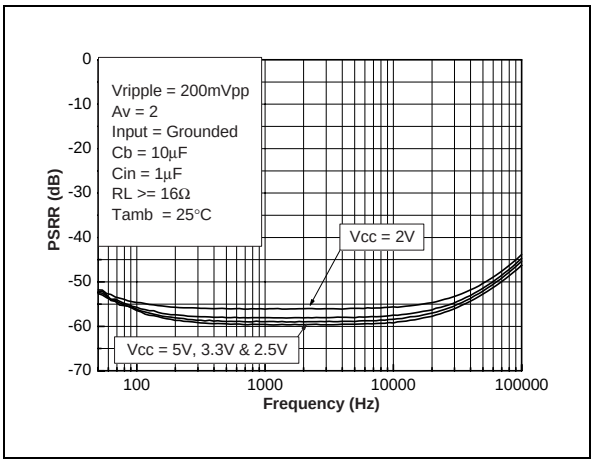


Fig. 56: THD + N vs Output Power

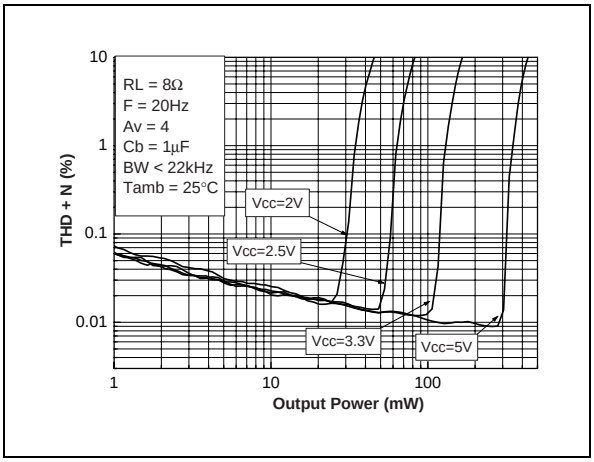


Fig. 57: THD + N vs Output Power

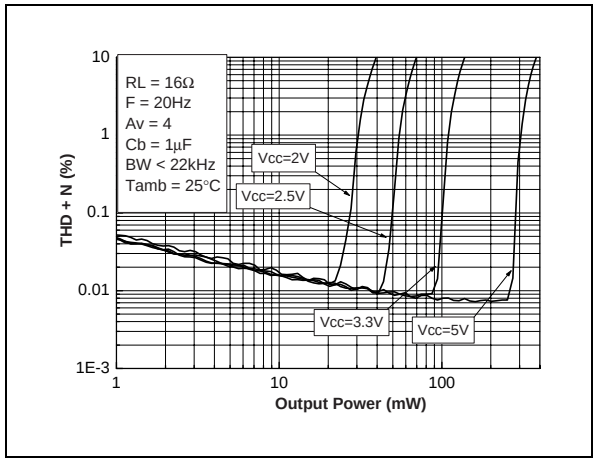


Fig. 58: THD + N vs Output Power

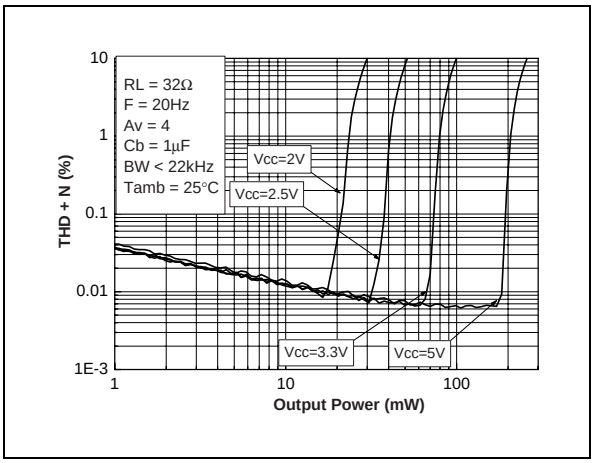


Fig. 59: THD + N vs Output Power

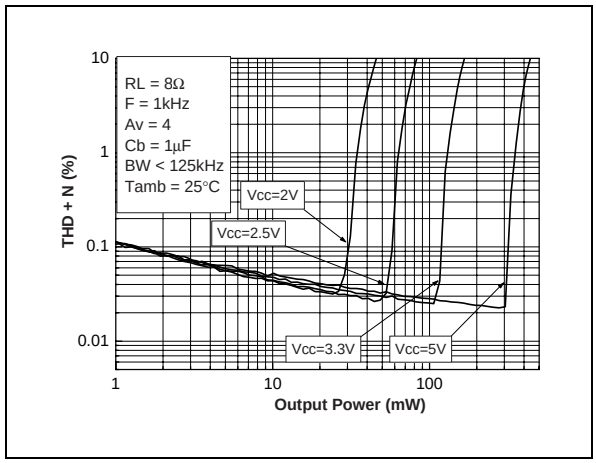


Fig. 60: THD + N vs Output Power

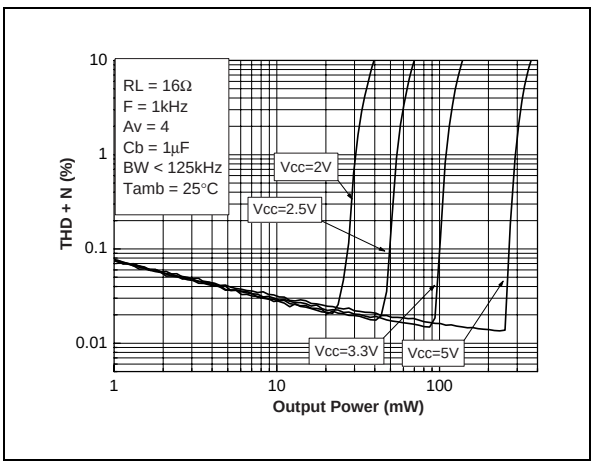


Fig. 61: THD + N vs Output Power

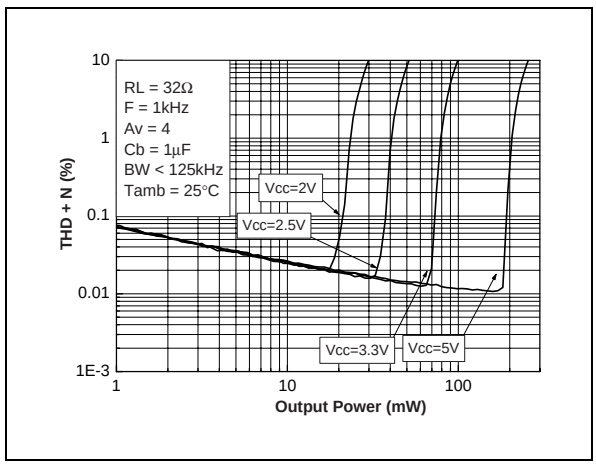


Fig. 62: THD + N vs Output Power

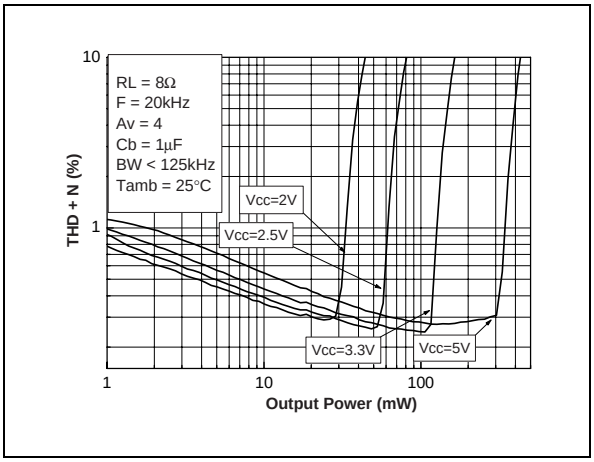


Fig. 63: THD + N vs Output Power

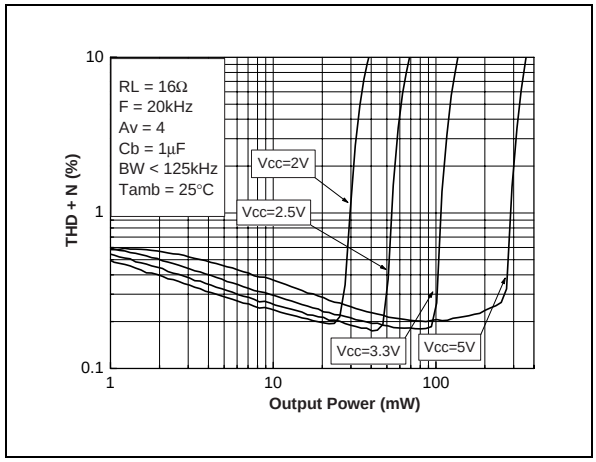


Fig. 64: THD + N vs Output Power

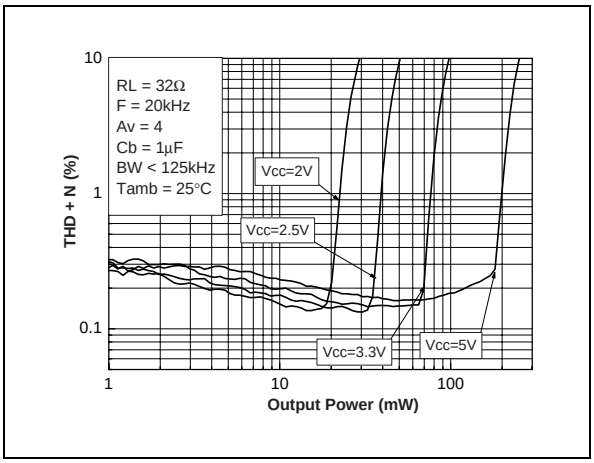


Fig. 65: THD + N vs Frequency

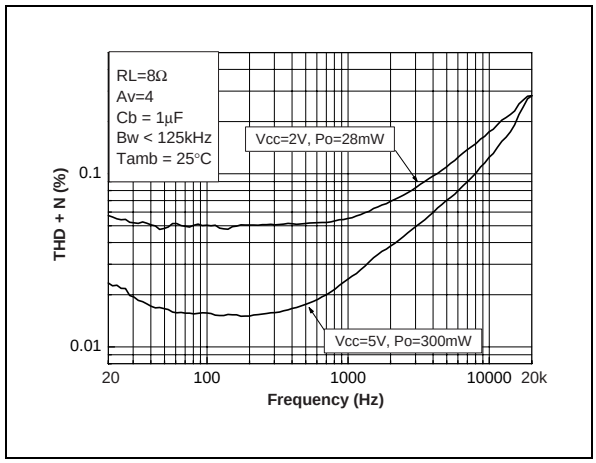


Fig. 66: THD + N vs Frequency

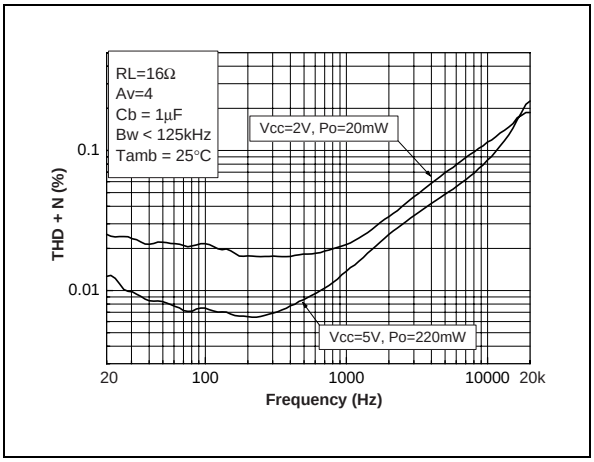


Fig. 67: THD + N vs Frequency

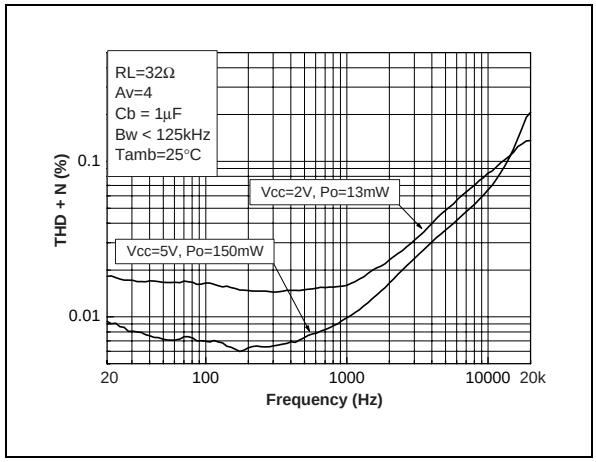


Fig. 68: Signal to Noise Ratio vs Power Supply Voltage with Unweighted Filter (20Hz to 20kHz)

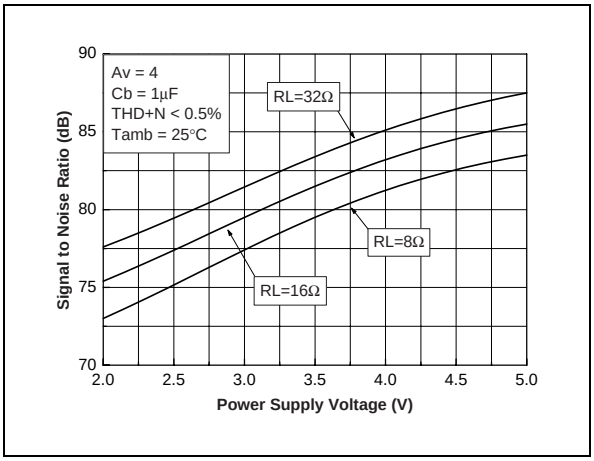


Fig. 69: Signal to Noise Ratio vs Power Supply Voltage with Weighted Filter Type A

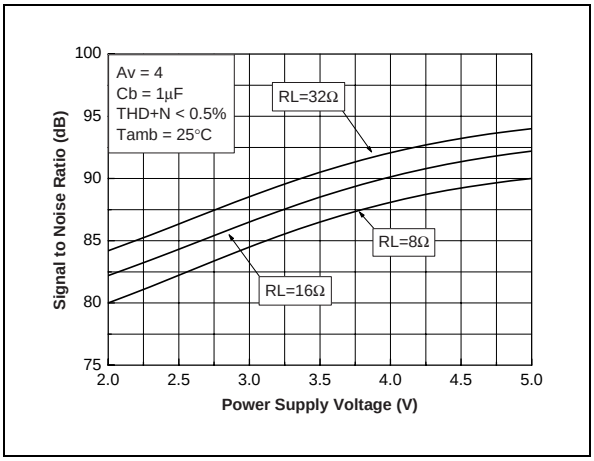


Fig. 70: Noise Floor

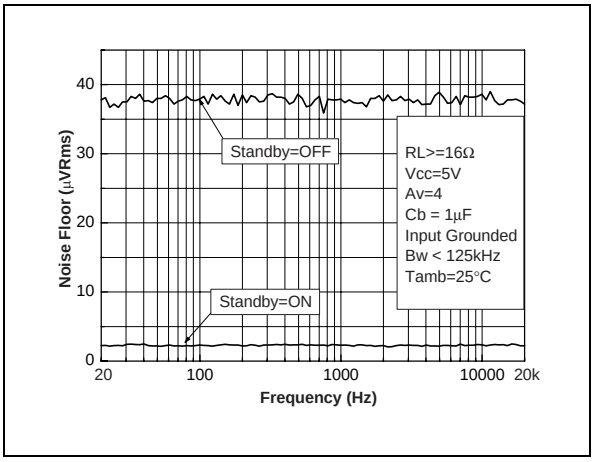


Fig. 71: Noise Floor

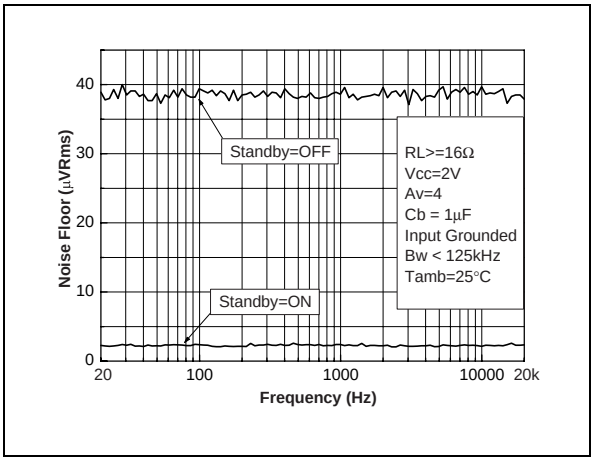


Fig. 72: PSRR vs Power Supply Voltage

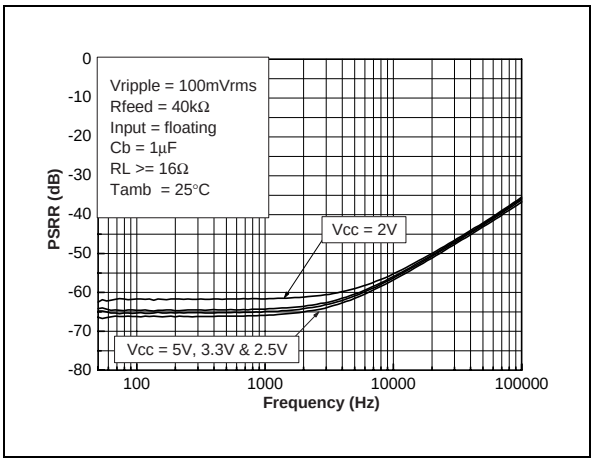


Fig. 73: PSRR vs Input Capacitor

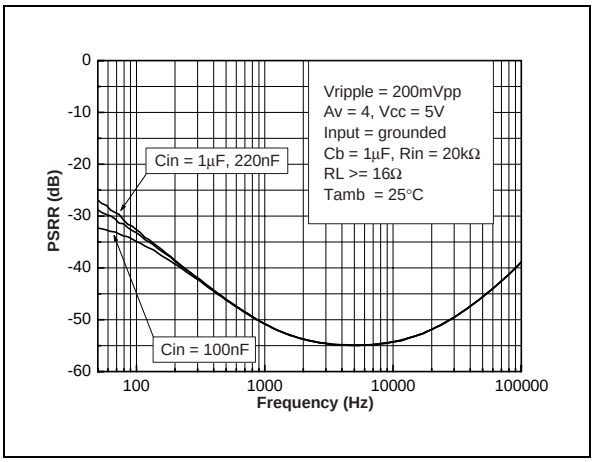


Fig. 74: PSRR vs Bypass Capacitor

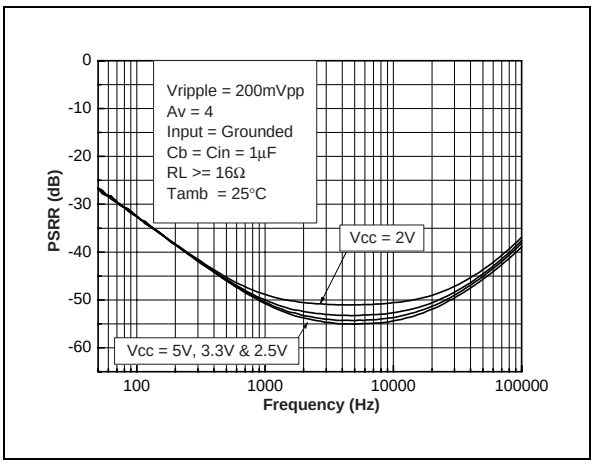


Fig. 75: PSRR vs Bypass Capacitor

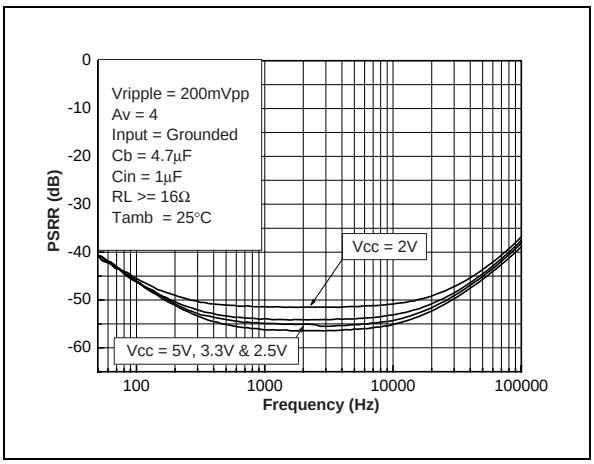


Fig. 76: PSRR vs Bypass Capacitor

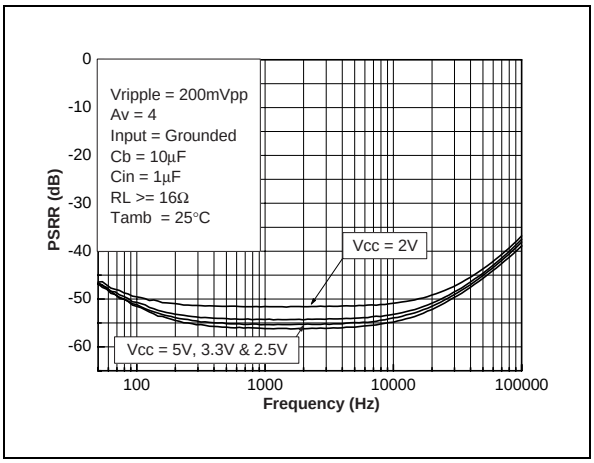


Fig. 77: THD + N vs Output Power

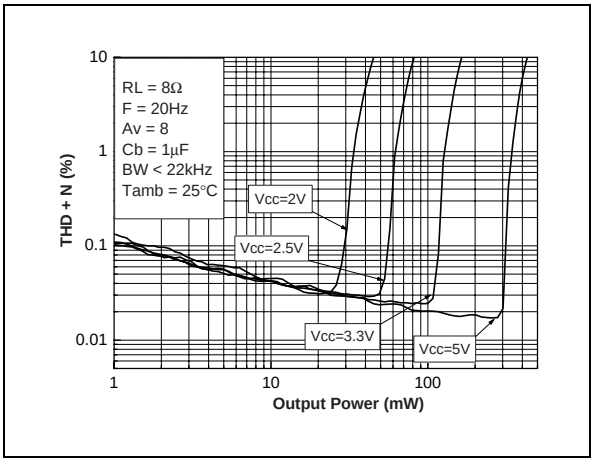


Fig. 78: THD + N vs Output Power

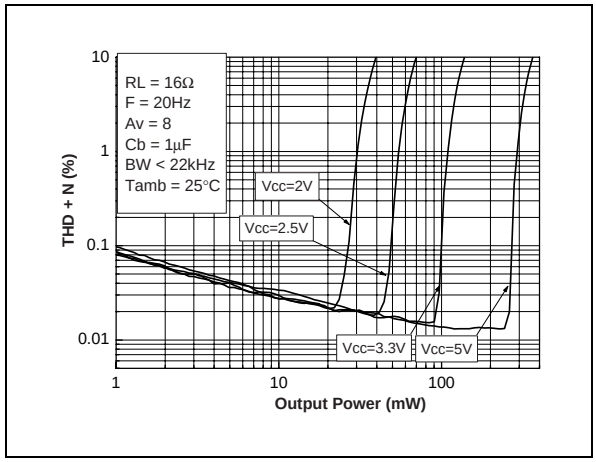


Fig. 79: THD + N vs Output Power

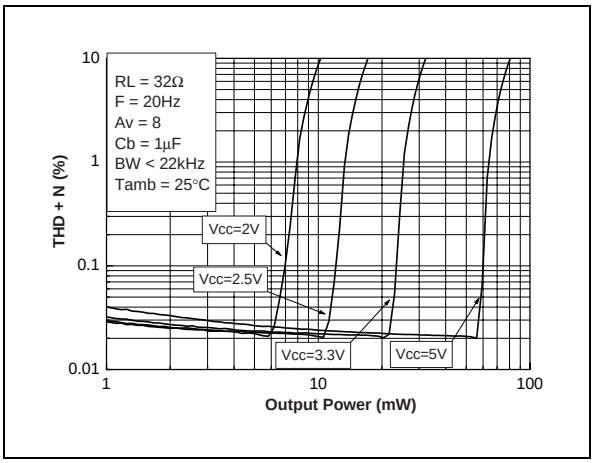


Fig. 80: THD + N vs Output Power

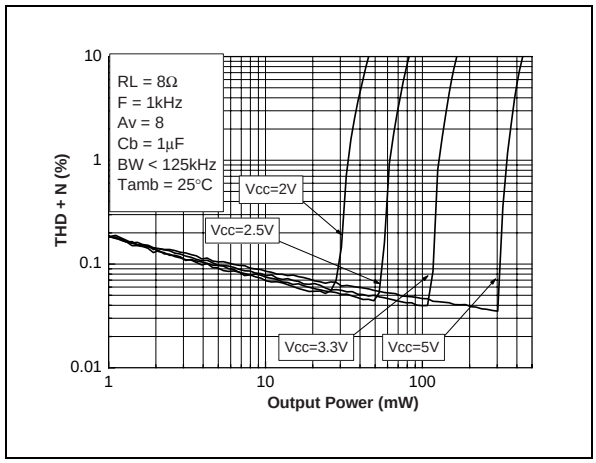


Fig. 81: THD + N vs Output Power

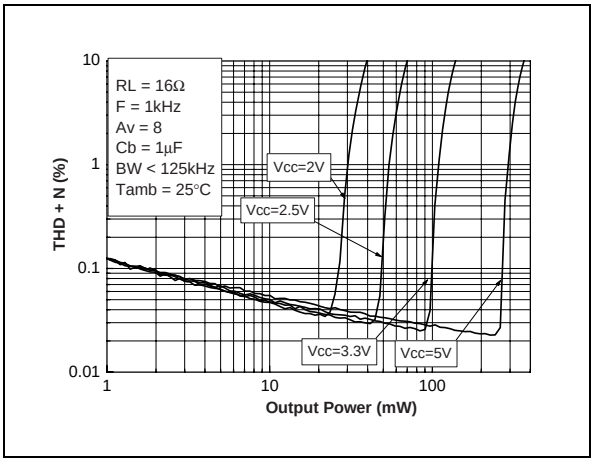


Fig. 82: THD + N vs Output Power

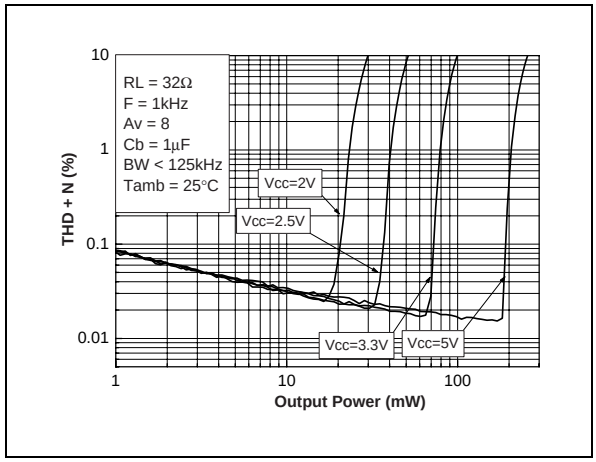


Fig. 83: THD + N vs Output Power

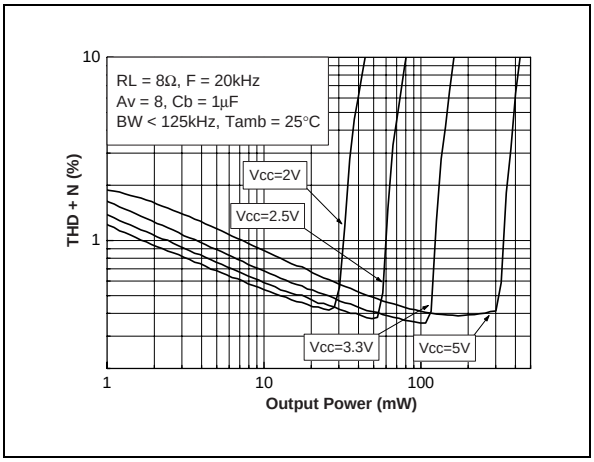


Fig. 84: THD + N vs Output Power

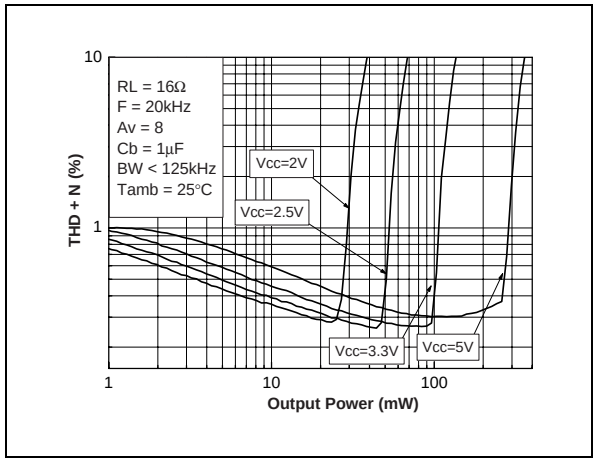


Fig. 85: THD + N vs Output Power

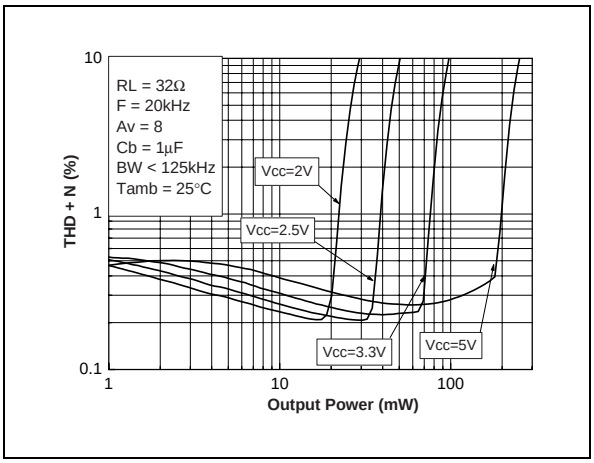


Fig. 86: THD + N vs Frequency

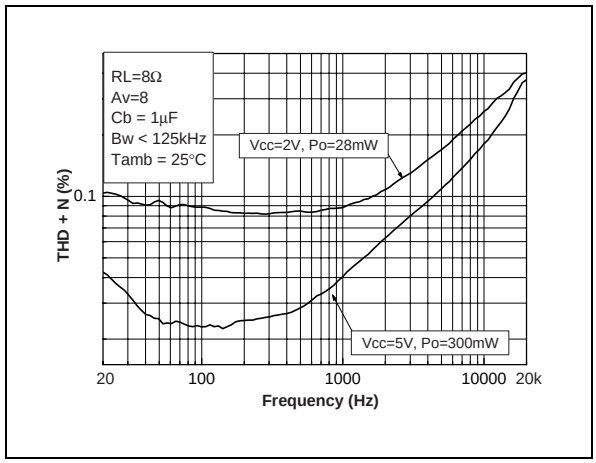


Fig. 87: THD + N vs Frequency

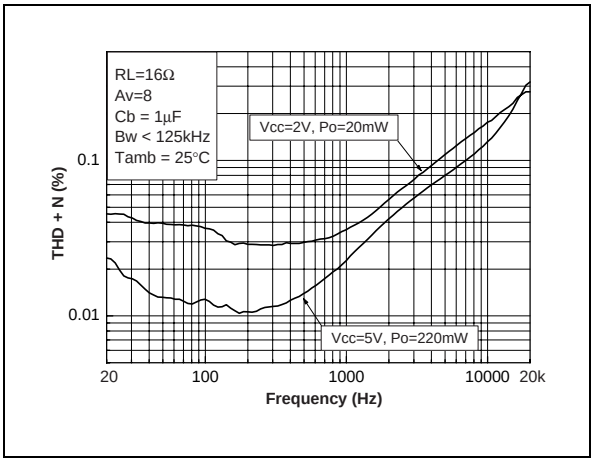


Fig. 88: THD + N vs Frequency

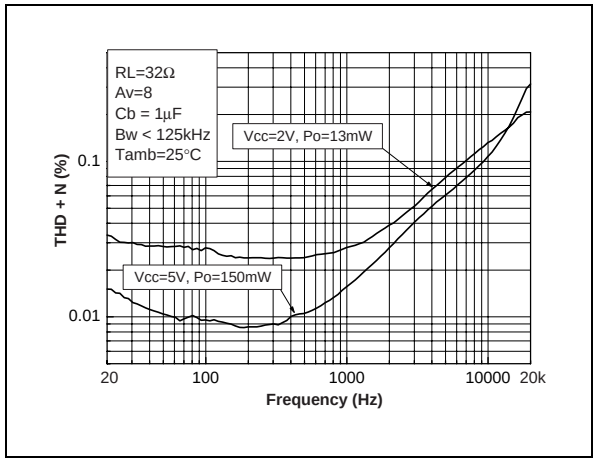


Fig. 89: Signal to Noise Ratio vs Power Supply Voltage with Unweighted Filter (20Hz to 20kHz)

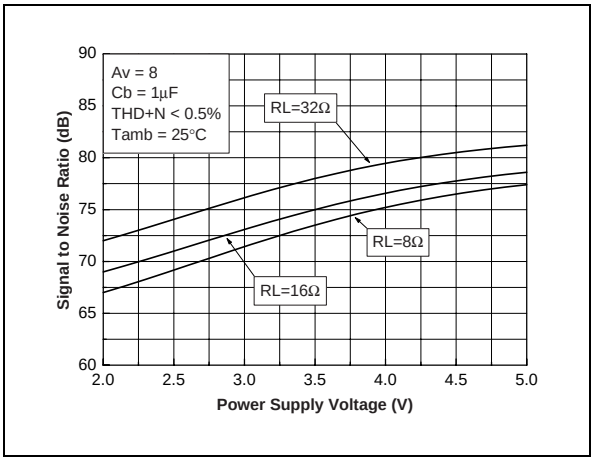


Fig. 90: Signal to Noise Ratio vs Power Supply Voltage with Weighted Filter Type A

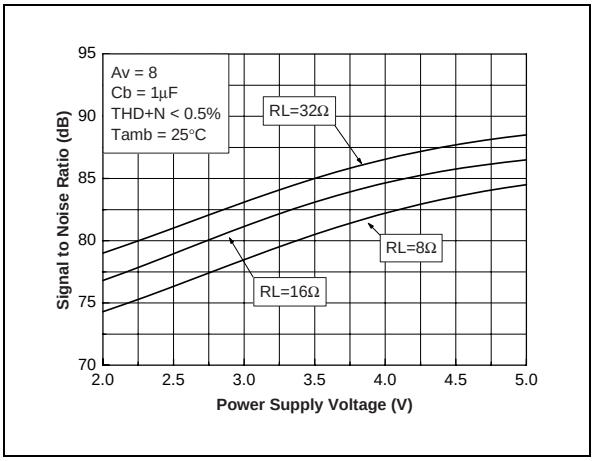


Fig. 91: Noise Floor

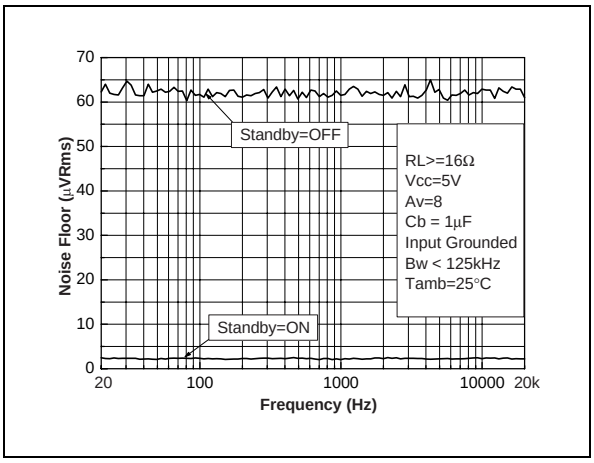


Fig. 92: Noise Floor

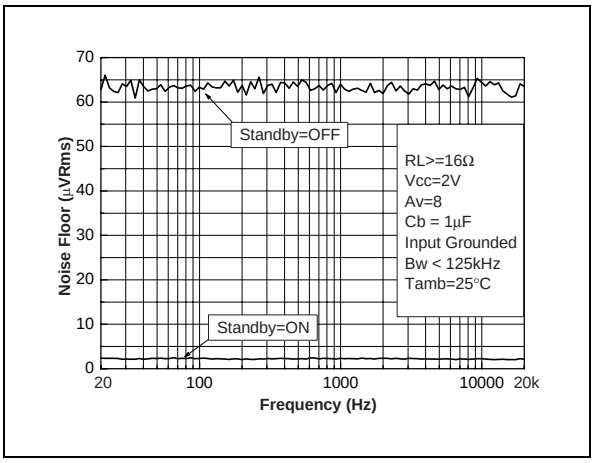


Fig. 93: PSRR vs Power Supply Voltage

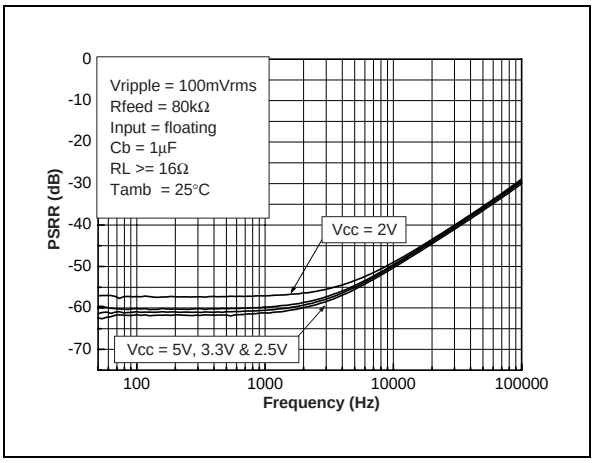


Fig. 94: PSRR vs Input Capacitor

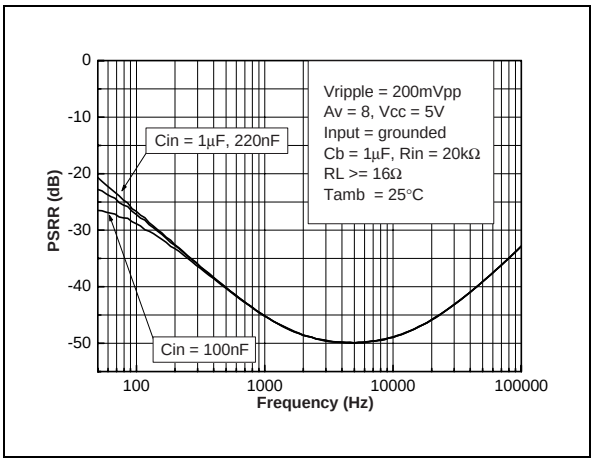


Fig. 95: PSRR vs Bypass Capacitor

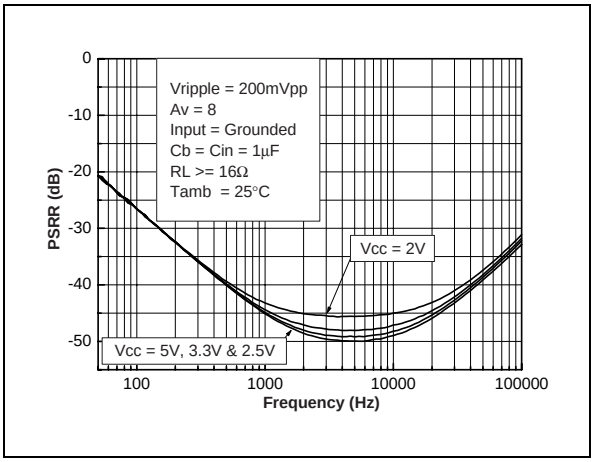


Fig. 96: PSRR vs Bypass Capacitor

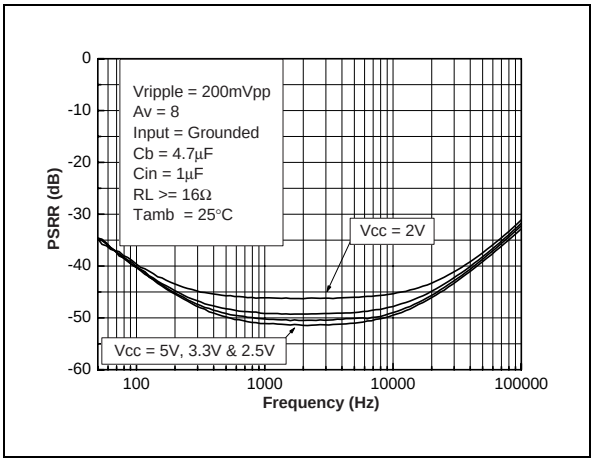
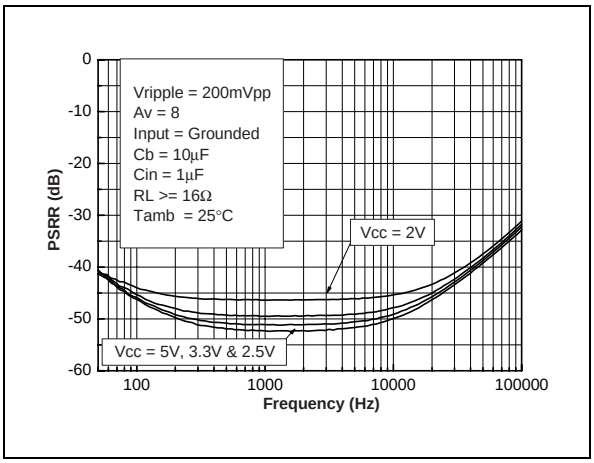


Fig. 97: PSRR vs Bypass Capacitor



APPLICATION INFORMATION

■ BTL Configuration Principle

The TS419 & TS420 are monolithic power amplifiers with a BTL output type. BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single ended output 1 = Vout1 = Vout (V)
Single ended output 2 = Vout2 = -Vout (V)

And Vout1 - Vout2 = 2Vout (V)

The output power is :

$$Pout = \frac{(2\,Vout_{RMS})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

■ Gain In Typical Application Schematic (cf. page 3 of TS419-TS421 datasheet)

In the flat region (no C_{IN} effect), the output voltage of the first stage is:

$$Vout1 = -Vin\frac{Rfeed}{Rin} (V)$$

For the second stage : Vout2 = -Vout1 (V)

The differential output voltage is

$$Vout2 - Vout1 = 2Vin\frac{Rfeed}{Rin} (V)$$

The differential gain named gain (Gv) for more convenient usage is :

$$Gv = \frac{Vout2 - Vout1}{Vin} = 2\frac{Rfeed}{Rin}$$

Remark : Vout2 is in phase with Vin and Vout1 is phased 180° with Vin. This means that the positive terminal of the loudspeaker should be connected to Vout2 and the negative to Vout1.

■ Low and high frequency response

In the low frequency region, C_{IN} starts to have an effect. C_{IN} forms with R_{IN} a high-pass filter with a -3dB cut off frequency .

$$F_{CL} = \frac{1}{2\pi RinCin} (Hz)$$

In the high frequency region, you can limit the bandwidth by adding a capacitor (Cfeed) in parallel with Rfeed. It forms a low-pass filter with a -3dB cut off frequency .

$$F_{CH} = \frac{1}{2\pi\,Rfeed\,Cfeed} (Hz)$$

■ Power dissipation and efficiency

Hypothesis:

• Load voltage and current are sinusoidal (Vout and Iout)
• Supply voltage is a pure DC source (Vcc)

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin\omega t (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A)$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} (W)$$

Then, the average current delivered by the supply voltage is:

$$Icc_{AVG} = 2\frac{V_{PEAK}}{\pi R_L} (A)$$

The power delivered by the supply voltage is:
$Psupply = Vcc\ Icc_{AVG}$ (W)

Then, the **power dissipated by the amplifier** is:
Pdiss = Psupply - Pout (W)

$$Pdiss = \frac{2\sqrt{2}\,Vcc}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT} (W)$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{OUT}} = 0$$

and its value is:

$$Pdissmax = \frac{2Vcc^2}{\pi^2 R_L} (W)$$

Remark : This maximum value is only dependent upon power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P\,supply} = \frac{\pi V_{PEAK}}{4\,Vcc}$$

The maximum theoretical value is reached when Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\%$$

■ Decoupling of the circuit

Two capacitors are needed to bypass properly the TS419/TS421. A power supply bypass capacitor C_S and a bias voltage bypass capacitor C_B.

C_S has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With 1µF, you can expect similar THD+N performances to those shown in the datasheet.

In the high frequency region, if C_S is lower than 1µF, it increases THD+N and disturbances on the power supply rail are less filtered.
On the other hand, if C_S is higher than 1µF, those disturbances on the power supply rail are more filtered.

C_B has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_B is lower than 1µF, THD+N increases at lower frequencies and PSRR worsens.
If C_B is higher than 1µF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that C_{IN} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{IN}, the higher the PSRR.

■ Wake-up Time: T_{WU}

When standby is released to put the device ON, the bypass capacitor C_B will not be charged immediatly. As C_B is directly linked to the bias of the amplifier, the bias will not work properly until the C_B voltage is correct. The time to reach this voltage is called wake-up time or T_{WU} and typically equal to:
T_{WU}=0.15xC_B (s) with C_B in µF.

Due to process tolerances, the range of the wake-up time is :
0.12xCb < T_{WU} < 0.18xC_B (s) with C_B in µF

Note : When the standby command is set, the time to put the device in shutdown mode is a few microseconds.

■ Pop performance

Pop performance is intimately linked with the size of the input capacitor Cin and the bias voltage bypass capacitor C_B.

The size of C_{IN} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_B is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_B determines the speed with which the amplifier turns ON. The slower the speed is, the softer the turn ON noise is.

The charge time of C_B is directly proportional to the internal generator resistance 150kΩ..
Then, the charge time constant for C_B is
$\tau_B = 150k\Omega x C_B$ (s)
As C_B is directly connected to the non-inverting input (pin 2 & 3) and if we want to minimize, in amplitude and duration, the output spike on Vout1 (pin 5), C_{IN} must be charged faster than C_B. The equivalent charge time constant of C_{IN} is:
$\tau_{IN} = (Rin+Rfeed) x C_{IN}$ (s)

Thus we have the relation:
$\tau_{IN} < \tau_B$ (s)

Proper respect of this relation allows to minimize the pop noise.

Remark : Minimizing C_{IN} and C_B benefits both the pop phenomena, and the cost and size of the application.

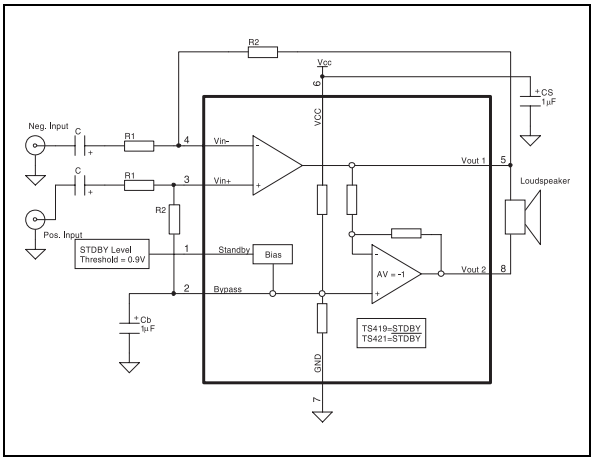
■ Application : Differential inputs BTL power amplifier.

The schematic on figure 98, shows how to design the TS419/21 to work in a differential input mode.

The gain of the amplifier is: $G_{VDIFF} = 2\frac{R_2}{R_1}$

In order to reach optimal performances of the differential function, R_1 and R_2 should be matched at 1% max.

Fig. 98 : Differential Input Amplifier Configuration



Input capacitance C can be calculated by the following formula using the -3dB lower frequency required. (F_L is the lower frequency required)

$$C \approx \frac{1}{2\pi R_1 F_L} (F)$$

Note : This formula is true only if:

$$F_{CB} = \frac{1}{942000 \times C_B} (Hz)$$

is ten times lower than F_L.

The following bill of material is an example of a differential amplifier with a gain of 2 and a -3dB lower cuttoff frequency of about 80Hz.

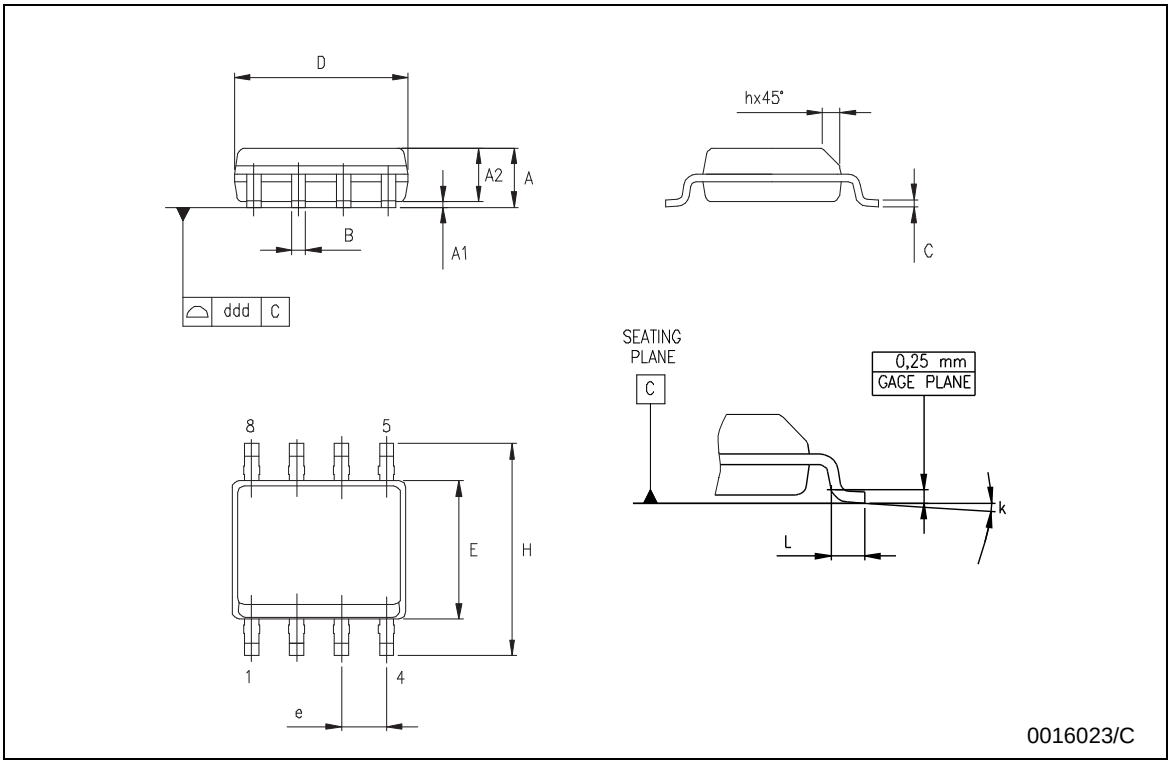
Components :

Designator	Part Type
R1	20k / 1%
R2	20k / 1%
C	100nF
C_B=C_S	1µF
U1	TS419/21

PACKAGE MECHANICAL DATA

SO-8 MECHANICAL DATA

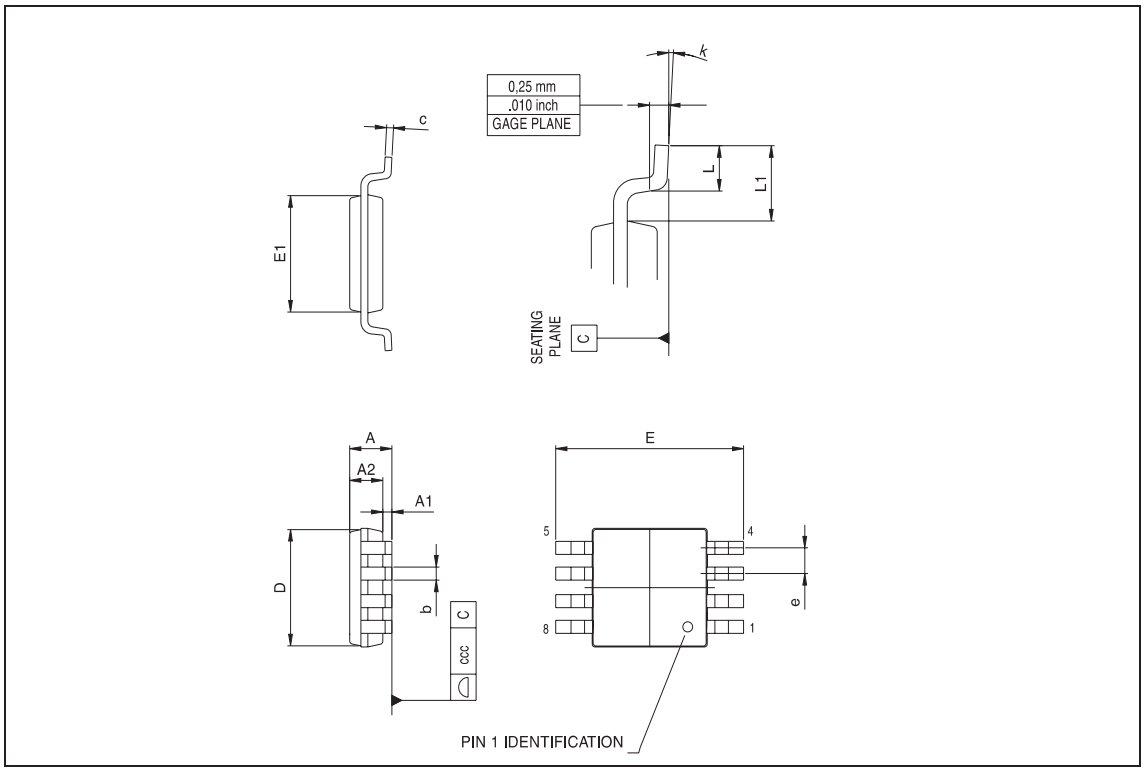
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



PACKAGE MECHANICAL DATA

miniSO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



PACKAGE MECHANICAL DATA

DFN8 (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.23	2.38	2.48	87.8	93.7	97.7
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.30	0.40	0.50	11.8	15.7	19.7