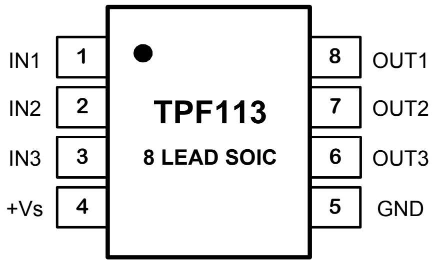
Order Information

Order Number	Operating Temperature Range	Package	Package Options	Transport Media, Quantity
TPF113-SR	-40 to 85°C	SOIC-8	MSL-3	Tape and Reel, 4000

Configuration (Top View)



Pin Number	Pin Name	Function
1	IN1	First Input
2	IN2	Second input
3	IN3	Third input
4	+Vs	Positive power supply
5	GND	Ground
6	OUT3	Third output
7	OUT2	Second output
8	OUT1	First output

Absolute Maximum Ratings*

Parameters		Value	Unit
Power Supply, V_{DD} to GND		6.0	V
PD	Power dissipation , T_A = 25°C, 8-Lead SOIC	800(1)	mW
V_{IN}	Input Voltage	V_{DD} + 0.3V to GND - 0.3V	
I_O	Output Current	65	mA
T_J	Maximum Junction Temperature	150	°C
T_A	Operating Temperature Range	–45 to 85	°C
T_{STG}	Storage Temperature Range	–65 to 150	°C
TL	Lead Temperature (Soldering, 10 sec)	300	°C
θ_{JA}	8-Lead SOIC	130(2)	°C/W

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Electrical Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Electrical Specifications						
V_{DD}	Supply Voltage Range		3.0		5.5	V
I_{DD}	Quiescent current (I_Q) (1)	V_{DD} = 3.3V, V_{IN} = 500mV, no load		11.6	14.3	mA
		V_{DD} = 5.0V, V_{IN} = 500mV, no load		14.7	18.4	mA
$I_{CLAMP-DOWN}$	Clamp Charge Current	V_{IN}=300mV, measure current	1.5	2.0	5.1	µA
$I_{CLAMP-UP}$	Clamp Discharge Current	V_Y = -0.2V	-1.5	-1.7		mA
V_{CLAMP}	Input Voltage Clamp	I_Y = -100µA	-40	0	+40	mV
R_{IN}	Input Impedance	0.5V < V_Y < 1V	0.5	3		MΩ
AV	Voltage Gain (1)	V_{IN}=0.5V,1V or 2V R_L=150Ω to GND	5.9	6.01	6.025	dB
ΔAV	Channel Mismatch		-2		+2	%
V_{OLS}	Output Level Shift Voltage	V_{IN} = 0V, no load, input referred	53	80	124	mV
V_{OL}	Output Voltage Low Swing	V_{IN} = -0.3V, R_L =75Ω		0.05		V
V_{OH}	Output Voltage High Swing	V_{IN} = 3V, R_L =75Ω to GND (dual load)		3.18		V
PSRR	Power Supply Rejection Ratio	$ΔV_{DD}$ = 3.3V to 3.6V		61		dB
		$ΔV_{DD}$ = 5.0V to 5.5V, 50Hz		67		dB
I_{SC}	Short-circuit current	V_{IN} = 2V, 10Ω, output to GND	65			mA
		V_{IN} =0.1V, output short to V_{DD}	65			mA
AC Electrical Specifications						
f_{-1dB}	-1dB Bandwidth	R_L=150Ω	7.6	8.2	9.1	MHz
f_{-3dB}	-3dB Bandwidth	R_L=150Ω	7.8	9	10.5	MHz
Att_{27MHz}	Stop Band Attenuation	f = 27MHz	38.2	57.2		dB
SR	Slew Rate	2V output step, 80% to 20%		38		V/µs
dG	Differential Gain	Video input range 1V	-0.1	0.4	0.8	%
dP	Differential Phase	Video input range 1V	-1.1	0.7	1.1	°
THD	Output Distortion(All Channel)	f=1MHz, V_{OUT}=1.4V_{PP}	0.03	0.1	0.2	%
D/DT	Group Delay Variation	f = 100kHz, 5MHz		5.4		Ns
t_{PD}	Propagation Delay	Maximum delay from input to output: 100kHz to 4.43MHz		80	127	Ns
X_{TALK}	Channel Crosstalk	f = 1MHz, V_{OUT}=1.4V_{PP}	-68	-74		dB
SNR	Signal-to-Noise Ration	f= 100kHz to 4.43MHz	65	69		dB
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
R_{OUT_AC}	Output Impedance	f = 4.2MHz		1.5		Ω
CLG	Chroma-Luma-Gain	400kHz to 3.58MHz and 4.43MHz		0.18	0.4	dB
CLD	Chroma-Luma-Delay	400kHz to 3.58MHz and 4.43MHz		5		ns

Note: (1). 100% tested at T_A=25°C.

Typical Performance Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

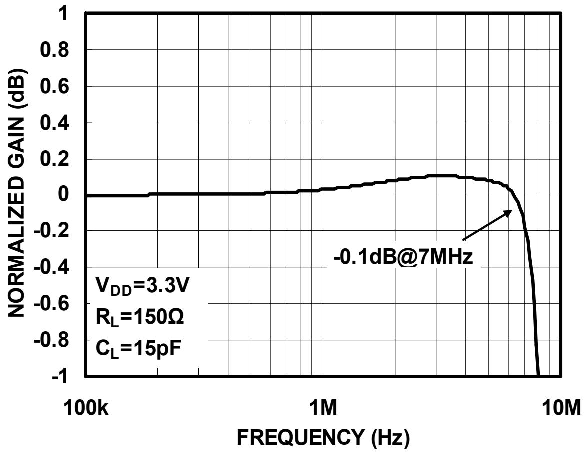


Figure1. Small-Scale Frequency Response

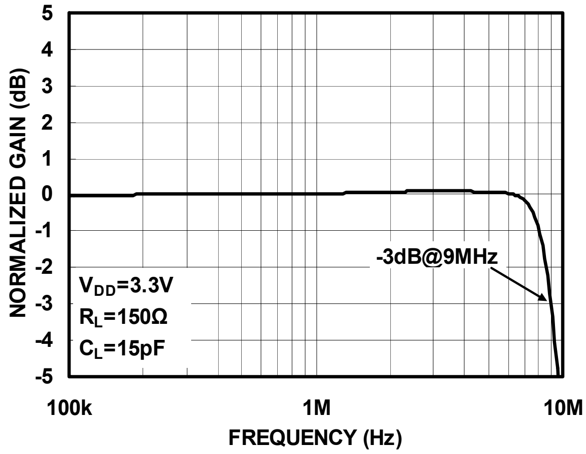


Figure2. Large-Scale Frequency Response

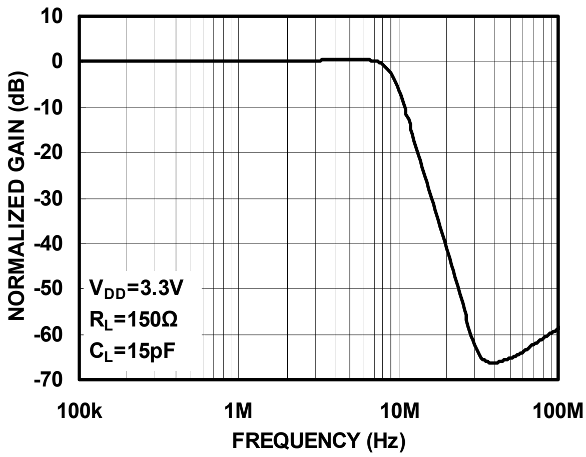


Figure3. Gain Vs. Frequency

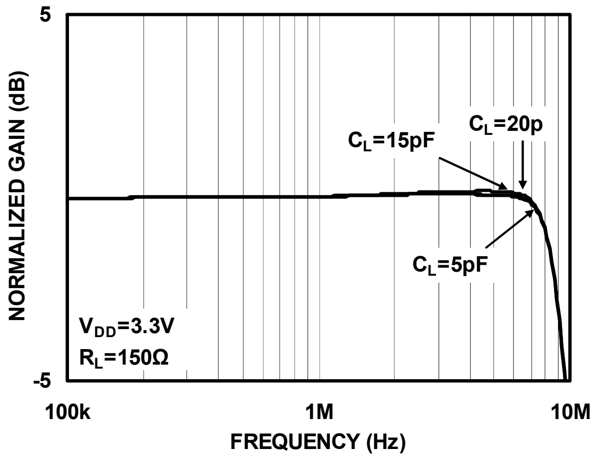


Figure4. Gain Vs. Frequency With C_{LOAD}

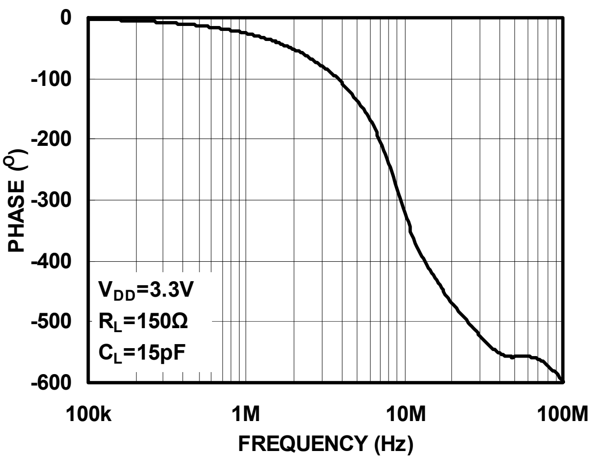


Figure5. Phase Vs. Frequency

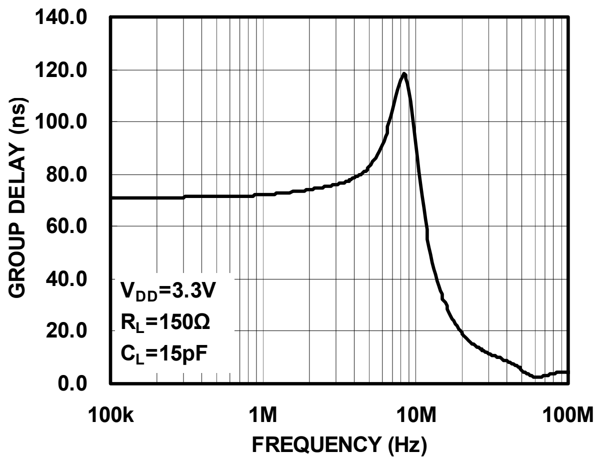


Figure6. Group Delay vs Frequency

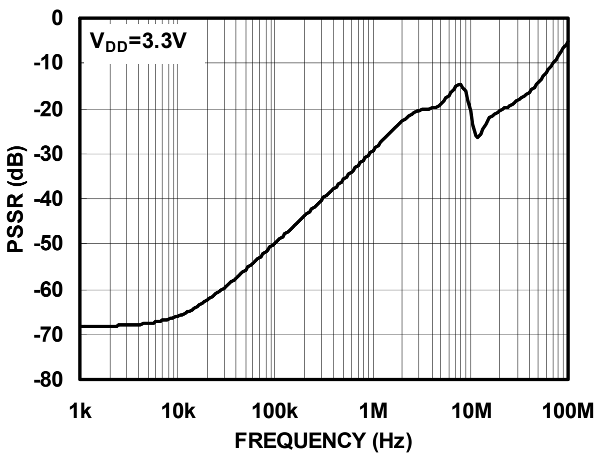


Figure7. PSRR Vs. Frequency

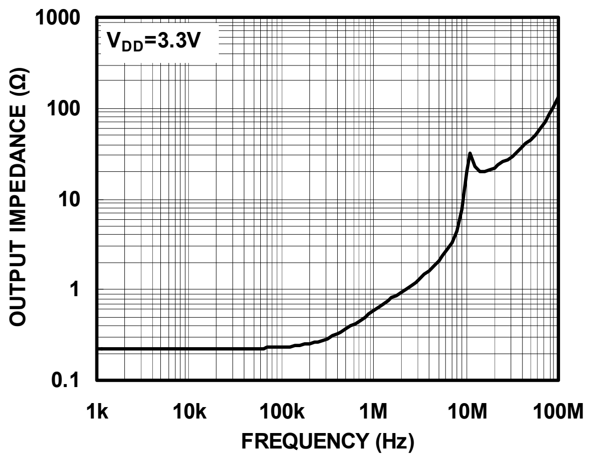


Figure8. Output Impedance Vs. Frequency

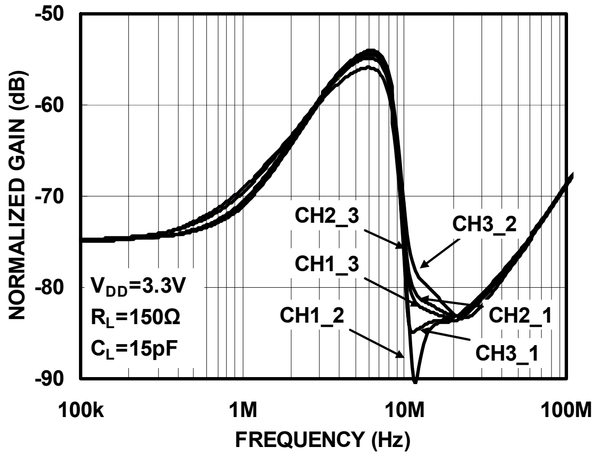


Figure9. Crosstalk Vs. Frequency

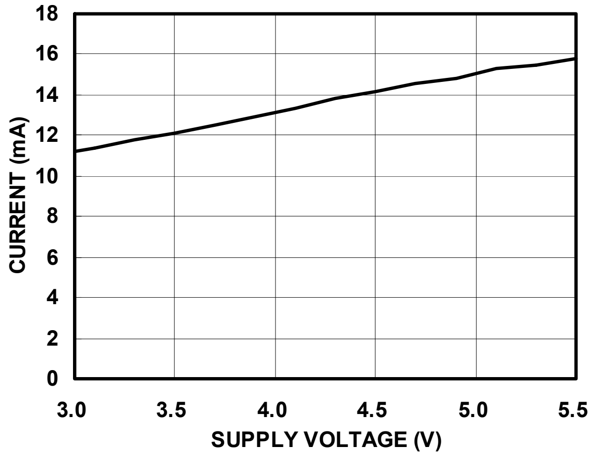


Figure10. Current Vs. Supply Voltage

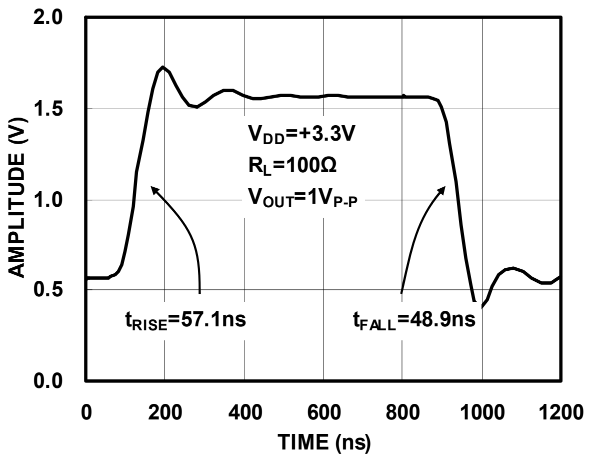


Figure11. Large-Signal Pulse Response Vs. Time

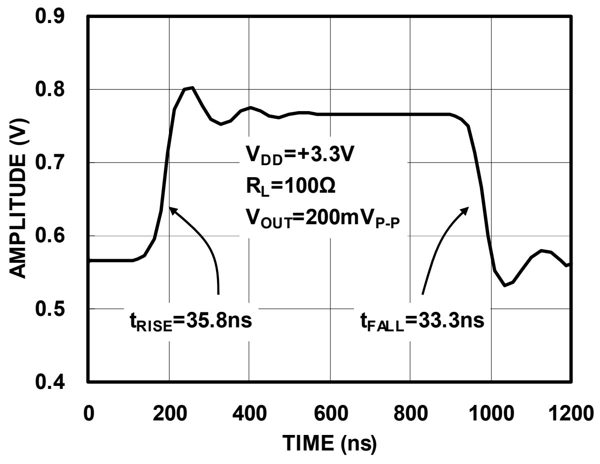


Figure12. Small-Signal Pulse Response Vs. Time

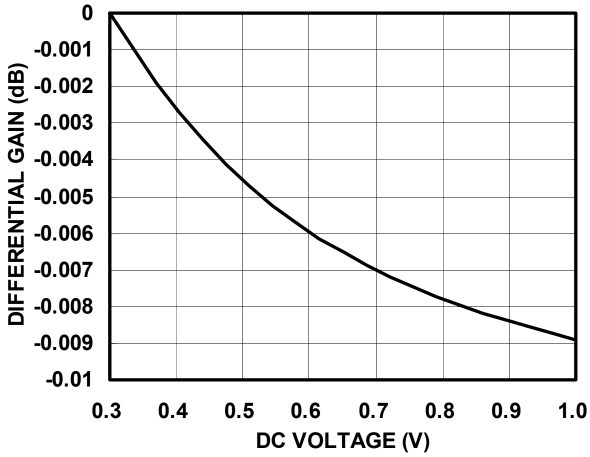


Figure13. Differential Gain(dG)

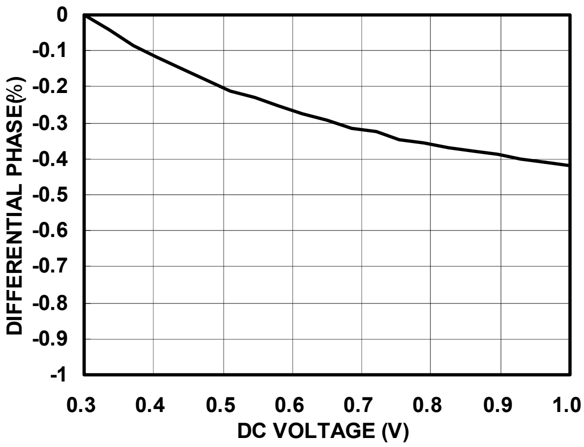


Figure14. Differential Phase(dP)

Application Information

The TPF113 is a single supply 3 channel rail-to-rail output amplifier achieving a -3dB bandwidth of around 9MHz and slew rate of about 38V/μs while demanding only 3.85mA(per channel) of supply current. This part is ideally suited for applications with specific micro power consumption and high bandwidth demands. As the performance characteristics above and the features described below, the TPF113 is designed to be very attractive for portable composite video applications.

Internal Sync Clamp

The typical embedded video DAC operates from a ground referenced single supply. This becomes an issue because the lower level of the sync pulse output may be at a 0V reference level to some positive level. The problem is presenting a 0V input to most single supply driven amplifiers will saturate the output stage of the amplifier resulting in a clipped sync tip and degrading the video image. A larger positive reference may offset the input above its positive range.

The TPF113 features an internal sync clamp and offset function to level shift the entire video signal to the best level before it reaches the input of the amplifier stage. These features are also helpful to avoid saturation of the output stage of the amplifier by setting the signal closer to the best voltage range.

The simplified block diagram of the TPF113 in Page-1.The AC coupled video sync signal is pulled negative by a current source at the input of the comparator amplifier. When the sync tip goes below the comparator threshold the output comparator is driven negative, The PMOS device turns on clamping sync tip to near ground level. The network triggers on the sync tip of video signal.

Droop Voltage and DC Restoration

Selection of the input AC-coupling capacitance is based on the system requirements. A typical sync tip width of a 64μs NTSC line is 4μs during which clamp circuit restores its DC level. In the remaining 60μs period, the voltage droops because of a small constant 2.0μA sinking current. If the AC-coupling capacitance is 0.1μF, the maximum droop voltage is about 1mV which is restored by the clamp circuit. The maximum pull-up current of the clamp circuit is 1.7mA. For a 4μs sync tip width and 0.1μF capacitor, the maximum restoration voltage is about 80mV.

The line droop voltage will increase if a smaller AC-coupling capacitance is used. For the same reason, if larger capacitance is used the line droop voltage will decrease. Table 1 is droop voltage and maximum restoration voltage of the clamp for typical capacitance.

Table 1. Maximum restoration voltage and droop voltage of Y and CVBS signals for different capacitance

CAP VALUE (nF)	DROOP IN 60μs (mV)	CHARGE IN 4μs (mV)
100	1.2	68
1,000	0.12	6.8

Low Pass Filter--Sallen Key

The Sallen Key is a classic low pass configuration. This provides a very stable low pass function, and in the case of the TPF113, a six-pole roll-off at around 9MHz. The six-pole function is accomplished with an RC low pass network placed in series with and before the Sallen Key.

Output Couple

TPF113 output could support both “AC Couple” and “DC Couple”, if use “AC Couple”, this capacitor is typically between 220-μF and 1000-μF, although 470-μF is common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document.

The TPF113 internal sync clamp makes it possible to DC couple the output to a video load, eliminating the need for any AC coupling capacitors, thereby saving board space and additional expense for capacitors. This makes the TPF113 extremely attractive for portable video applications. Additionally, this solution completely eliminates the issue of field tilt in the lower frequency. The trade off is greater demand of supply current. Typical load current for AC coupled is around 1mA, compared to typical 6.6mA used when DC coupling.

Output Drive Capability and Power Dissipation

With the high output drive capability of the TPF113, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area. The maximum power dissipation allowed in a package is determined according to Equation:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

Where：
T_{JMAX} = Maximum junction temperature
T_{AMAX} = Maximum ambient temperature
Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or: for sourcing:

$$PD_{MAX} = V_s \times I_{SMAX} + (V_s - V_{OUT}) \times \frac{V_{OUT}}{R_L}$$

Where：
V_S = Supply voltage
I_{SMAX} = Maximum quiescent supply current
V_{OUT} = Maximum output voltage of the application
R_{LOAD} = Load resistance tied to ground

By setting the two PDMAX equations equal to each other, we can solve the output current and RLOAD to avoid the device overheat.

Power Supply Bypassing Printed Circuit Board Layout

As with any modern operational amplifier, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor from VS+ to GND will suffice.

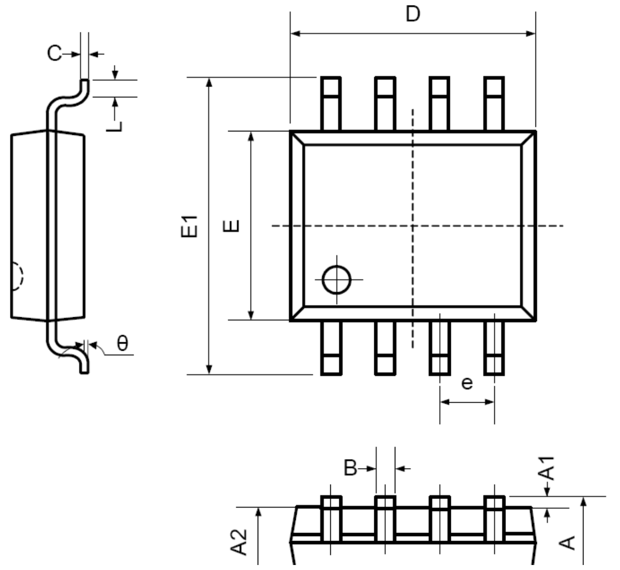
VIDEO FILTER DRIVER SELECTION GUIDE

P/N	Product Description	Channel	-3dB Bandwidth	Package
TPF110 /TPF110L	Low power, enable function and SAG correction, 1 channel 6th order 9MHz	1-SD	9MHz	SC70-5 SOT23-6
TPF113	Low power 3 channel, 6th-order 9MHz SD video filter	3-SD	9MHz	SO-8
TPF114	Low power 4 channel, 6th-order 9MHz SD video filter	4-SD	9MHz	MSOP-10 TSSOP-14
TPF116	Low power 4 channel, 6th-order 9MHz SD video filter for CVBS, SVIDEO	6-SD	9MHz	TSSOP-14
TPF123	3 channel 6th-order 13.5MHz, 960H/720H-CVBS video filter or Y'Pb'Pr 480P/576P video filter	3-ED	13.5MHz	SO-8
TPF133	Low power 3 channel, 6th-order 36MHz HD video filter	3-HD	36MHz	SO-8
TPF134	Low power 3 channel, 6th-order 36MHz HD video filter and 1 channel SD video filter	1-SD& 3-SD	9MHz 36MHz	MSOP-10 TSSOP-14
TPF136	Low power 3 channel, 6th-order 36MHz HD video filter and 3 channel SD video filter	3-SD& 3-HD	9MHz 36MHz	TSSOP-20

TPF143	Low power 3 channel, 6th-order 72MHz Full HD video filter	3-FHD	72MHz	SO-8
TPF144	Low power 3 channel, 6th-order 72MHz Full HD video filter and 1 channel SD video filter	1-SD& 3-FHD	9MHz 72MHz	MSOP-10 TSSOP-14
TPF146	Low power 3 channel, 6th-order 72MHz Full HD video filter and3 channel SD video filter	3-SD& 3-FHD	9MHz 72MHz	TSSOP-20
TPF153	Low power 3 channel, 6th-order 220MHz Full HD video filter	3-CH	220MHz	SO-8

Package Outline Dimensions

SOIC-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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