Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage	'4015 '4030 '4040	V_{DRM}	±8 ±15 ±25	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2) 2/10 µs (Telcordia GR-1089-CORE, 2/10 µs voltage wave shape) 8/20 µs (IEC 61000-4-5, combination wave generator, 1.2/50 voltage, 8/20 current) 10/160 µs (FCC Part 68, 10/160 µs voltage wave shape) 5/310 µs (ITU-T K.20/45/21, 10/700 µs voltage wave shape) 5/320 µs (FCC Part 68, 9/720 µs voltage wave shape) 10/560 µs (FCC Part 68, 10/560 µs voltage wave shape) 10/1000 µs (Telcordia GR-1089-CORE, 10/1000 µs voltage wave shape)		I_{TSP}	 ±150 ±120 ± 65 ± 45 ± 45 ± 35 ± 30	A
Non-repetitive peak on-state current (see Notes 1 and 2) 20 ms (50 Hz) full sine wave 16.7 ms (60 Hz) full sine wave 0.2 s 50 Hz/60 Hz a.c. 2 s 50 Hz/60 Hz a.c. 1000 s 50 Hz/60 Hz a.c.		I_{TSM}	 20 22 13 5 1.8	A
Initial rate of rise of current (2/10 waveshape)		di/dt	130	A/µs
Maximum junction temperature		T_{JM}	150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. Initially, the device must be in thermal equilibrium with T_J = 25 °C.
2. The surge may be repeated after the device returns to its initial conditions.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$				±5	µA
$V_{(BO)}$	Breakover voltage	di/dt = ±0.8 A/ms	'4015 '4030 '4040			±15 ±30 ±40	V
$V_{(BO)}$	Impulse breakover voltage	dv/dt = ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±5 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'4015 '4030 '4040			±34 ±50 ±63	V
$I_{(BO)}$	Breakover current	di/dt = ±0.8 A/ms				±0.8	A
I_D	Off-state current	V_D = ± 6 V V_D = ± 13 V V_D = ± 22 V	'4015 '4030 '4040			±2	µA
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±50			mA

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, V_D = 0	'4015		28	36	pF
			'4030		27	35	
			'4040		23	29	
		f = 1 MHz, V_d = 1 V rms, V_D = 1 V	'4015		25	33	
			'4030		24	31	
			'4040		20	26	
		f = 1 MHz, V_d = 1 V rms, V_D = 2 V	'4015		23	30	
			'4030		22	29	
			'4040		18	24	

Thermal Characteristics

Parameter		Test Conditions		Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 3)	SMA			125	°C/W
			SMB			120	
		265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C	SMA		60		
			SMB		55		

NOTE 3: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

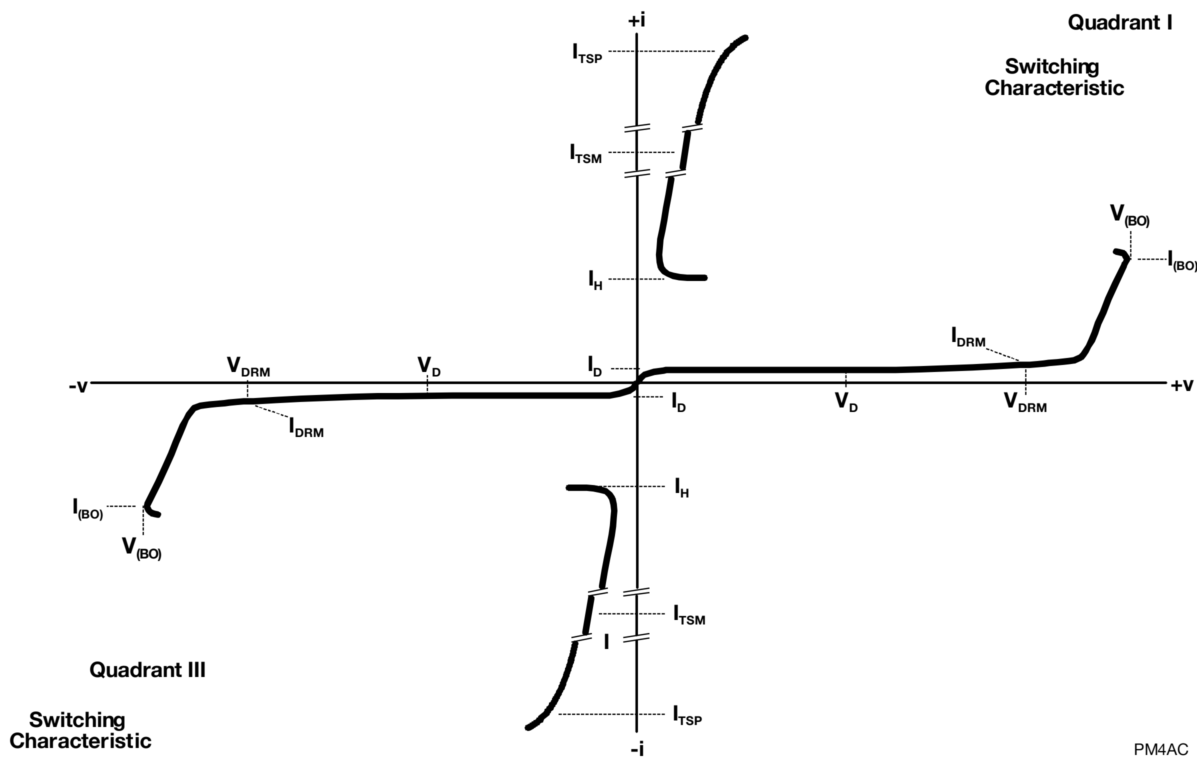


Figure 1. Voltage-Current Characteristic for T and R Terminals
All Measurements are Referenced to the R Terminal

Typical Characteristics

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

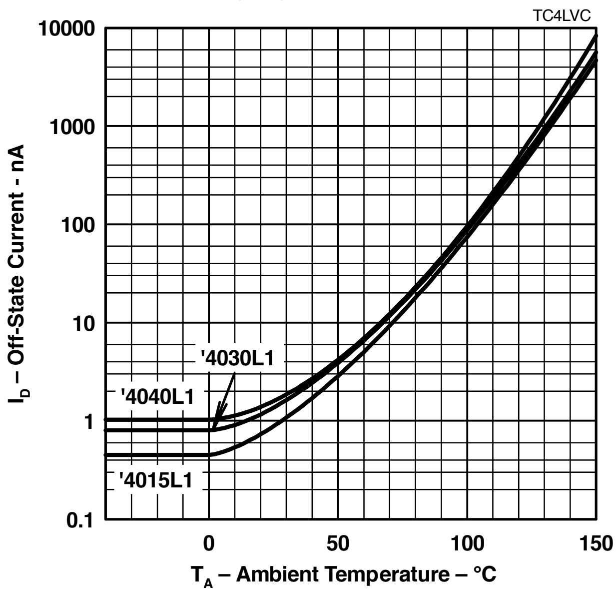


Figure 2.

NORMALIZED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

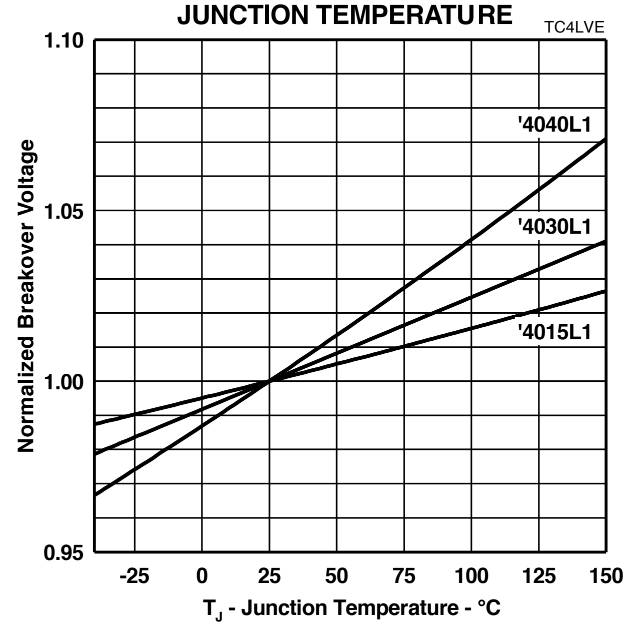


Figure 3.

ON-STATE CURRENT vs ON-STATE VOLTAGE

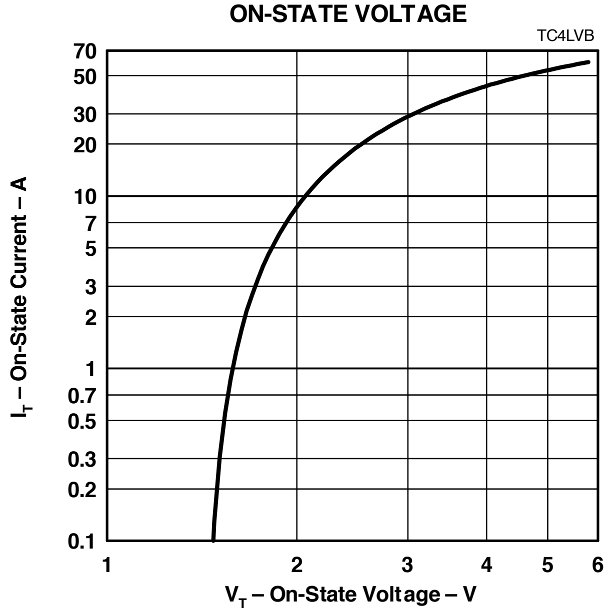


Figure 4.

NORMALIZED HOLDING CURRENT vs JUNCTION TEMPERATURE

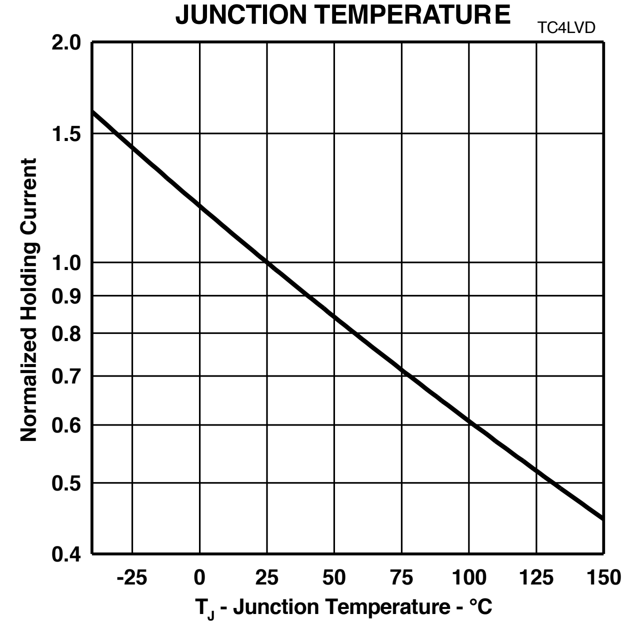


Figure 5.

Typical Characteristics

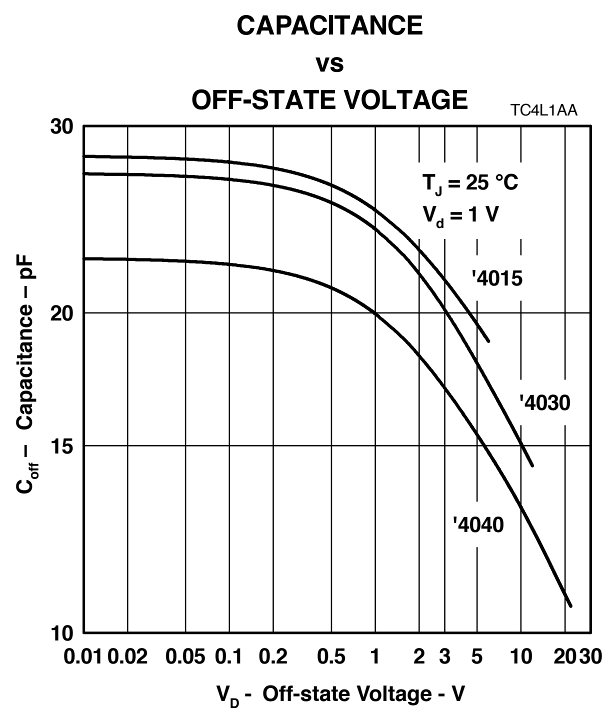


Figure 6.

Rating and Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT
vs
CURRENT DURATION

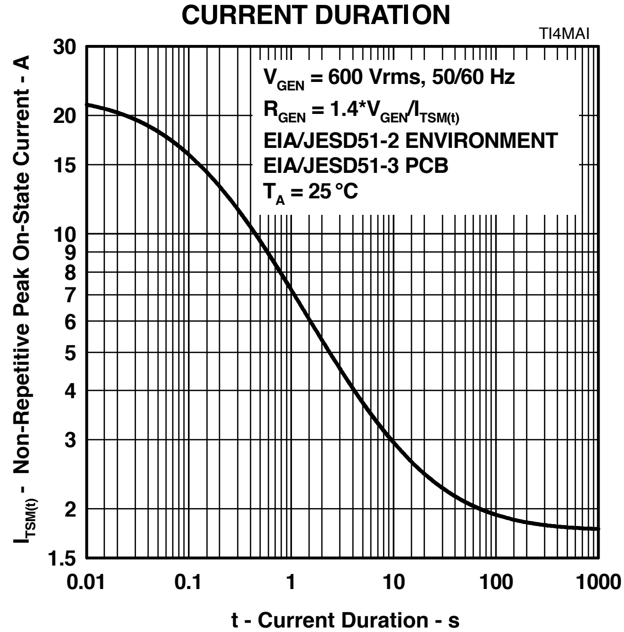


Figure 7.

V_{DRM} DERATING FACTOR
vs
MINIMUM AMBIENT TEMPERATURE

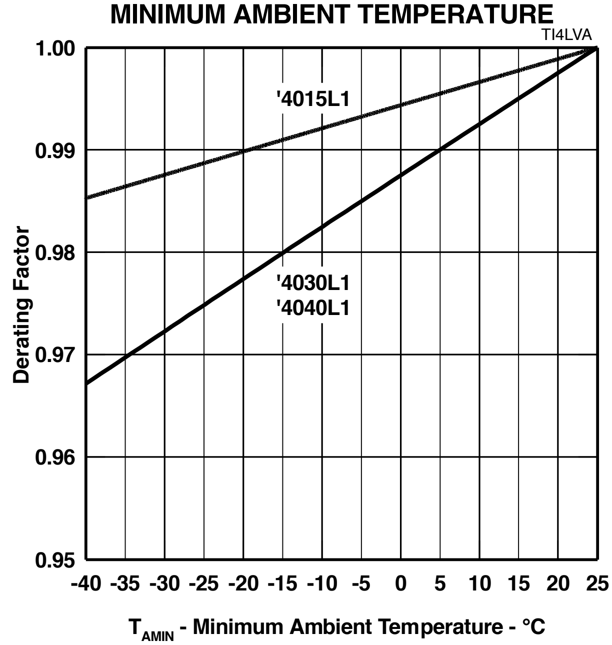


Figure 8.

APPLICATIONS INFORMATION

Transformer Protection

The inductance of a transformer winding reduces considerably when the magnetic core material saturates. Saturation occurs when the magnetizing current through the winding inductance exceeds a certain value. It should be noted that this is a different current to the transformed current component from primary to secondary. The standard inductance-current relationship is:

$$E = -\left(L\frac{di}{dt}\right)$$

where:
L = unsaturated inductance value in H
di = current change in A
dt = time period in s for current change di
E = winding voltage in V

Rearranging this equation and working large Δ changes to saturation gives the useful circuit relationship of:

$$E \; x \; \Delta t = L \; x \; \Delta i$$

A transformer winding volt-second value for saturation gives the designer an idea of circuit operation under overvoltage conditions. The volt-second value is not normally quoted, but most manufacturers should provide it on request. A 50 Vµs winding will support rectangular voltage pulses of 50 V for 1 µs, 25 V for 2 µs, 1 V for 50 µs and so on. Once the transformer saturates, primary to secondary coupling will be lost and the winding resistance, RW, shunts the overvoltage protector, Th1 - see Figure 9. This saturated condition is a concern for long duration impulses and a.c. fault conditions because the current capability of the winding wire may be exceeded. For example, if the on-state voltage of the protector is 1 V and the winding resistance is 0.2 Ω, the winding would bypass a current of 1/0.2 = 5 A, even though the protector was in the low voltage condition.

Figure 9. Transformer Saturation

Figure 10 shows a generic protection arrangement. Resistors R1 and R2, together with the overcurrent protection, prevent excessive winding current flow under a.c. conditions. Normally these resistors would only be needed for special cases, e.g. some T1/E1 designs. Alternatively, a split winding could be used with a single resistor connecting the windings. This resistor could be by-passed by a small capacitor to reduce signal attenuation.

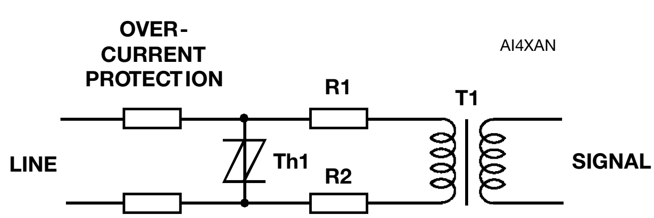


Figure 10. Transformer Winding Protection

Overcurrent protection upstream from the overvoltage protector can be fuse, PTC or thick film resistor based. For very high frequency circuits, fuse inductance due to spiral wound elements may need to be evaluated.

TISP® Device Voltage Selection

Normally, the working voltage value of the protector, V_{DRM}, would be chosen to be just greater than the peak signal amplitude over the equipment temperature range. This would give the lowest possible protection voltage, $V_{(BO)}$. This would minimize the peak voltage applied to the transformer winding and increase the time to core saturation.

In high frequency circuits, there are two further considerations. Low voltage protectors have a higher capacitance than high voltage protectors.

TISP® Device Voltage Selection (Continued)

So a higher voltage protector might be chosen specifically to reduce the protector capacitive effects on the signal.

Low energy short duration spikes will be clipped by the protector. This will extend the spike duration and the data loss time. A higher protector voltage will reduce the data loss time. Generally, this will not be a significant factor for inter-conductor protection.

However, clipping is significant for protection to ground, where there is continuous low-level a.c. common mode induction. In some cases the induced a.c. voltage can be over 10 V. Repetitive clipping at the induced a.c. peaks by the protector would cause severe data corruption. The expected a.c. voltage induced should be added to the maximum signal level for setting the protector V_{DRM} value.

2-Wire Digital Systems

Typical systems using a single twisted pair connection are: Integrated Services Digital Network (ISDN) and Pair Gain.

Signal level protection at the transformer winding is given by protectors Th3 and Th5. Typically these could be TISP4015L1 type devices with a 15 V voltage protection level.

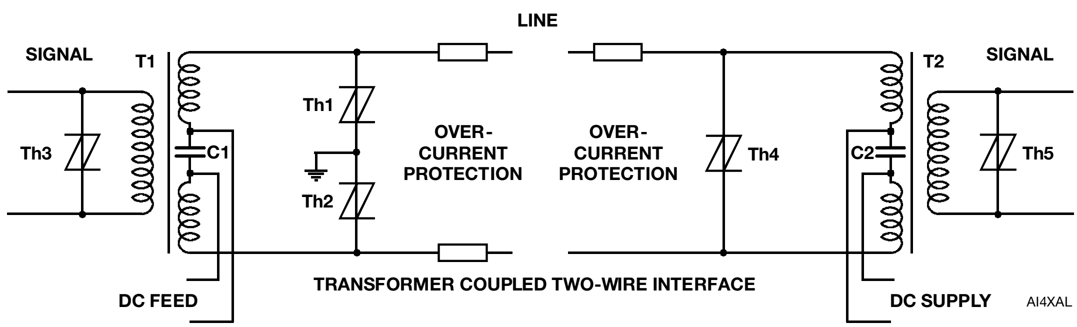


Figure 11. 2-Wire System

Two line protection circuits are given; one referenced to ground using Th1 and Th2 (left) and the other inter-wire using protector Th4 (right) - see Figure 11. For ISDN circuits compliant to ETSI ETR 080:1993, ranges 1 and 2 can be protected by the following device types: TISP4095M3, TISP4095H3, TISP3095H3 (combines Th1 and Th2) and TISP7095H3 (combines Th1, Th2 and Th4). Ranges 4 through 5 can be protected by: TISP4145M3, TISP4145H3, TISP3145H3 (combines Th1 and Th2) and TISP7145H3 (combines Th1, Th2 and Th4). Device surge requirement, H or M, will be set by the overcurrent protection components and the standards complied with. Protection of just the d.c. feed to ETSI ranges is covered in the TISP5xxxH3 data sheet.

When loop test voltages exceed the normal d.c. feed levels, higher voltage protectors need to be selected. For two terminal protectors, for levels up to 190 V (135 V rms) the TISP4250, H3 or M3, can be used and for 210 V (150 V rms) the TISP4290, H3 or M3, can be used.

In Pair Gain systems, the protector V_{DRM} is normally set by the d.c. feed value. The following series of devices have a 160 V working voltage at 25 °C: TISP4220M3, TISP4220H3, TISP3210H3 (combines Th1 and Th2) and TISP7210H3 (combines Th1, Th2 and Th4). These devices can be used on 150 V d.c. feed voltages down to an ambient temperature of -25 °C. Where the subscriber equipment may be exposed to POTS (Plain Old Telephone Service) voltage levels, protector Th4 needs a higher working voltage of about 275 V. Suitable device types are: TISP4350M3, TISP4350H3, TISP3350H3 (combines Th1 and Th2) and TISP7350H3 (combines Th1, Th2 and Th4).

The overcurrent protection for the overvoltage protector can be fuse, PTC or thick film resistor based. Its a.c. limiting capability should be less than the ratings of the intended overvoltage protector. Equipment complying with the year 2000 international K.20, K.21 and K.45 recommendations from the ITU-T, may be required to demonstrate protection coordination with the intended primary protector. Without adding series resistance, a simple series fuse overcurrent protection is likely to fail the equipment for this part of the recommendation.

If the d.c. feed consists of equal magnitude positive and negative voltage supplies, appropriately connected TISP5xxxH3 unidirectional protectors could replace Th1 and Th2.

4-Wire Digital Systems

A typical system using a two twisted pair connection is the High-bit-rate Digital Subscriber Line (HDSL) and the “S” interface of ISDN.

Figure 12 shows a generic two line system. HDSL tends to have ground referenced protection at both ends of the lines (Th1, Th2, Th3 and Th4). The ISDN “S” interface is often inside the premises and simple inter-wire protection is used at the terminating adaptor (Th7 and Th8). In all cases, signal protection, Th5, Th6, Th9 and Th10, can be TISP4015L1 type devices with a 15 V voltage protection level.

4-Wire Digital Systems (Continued)

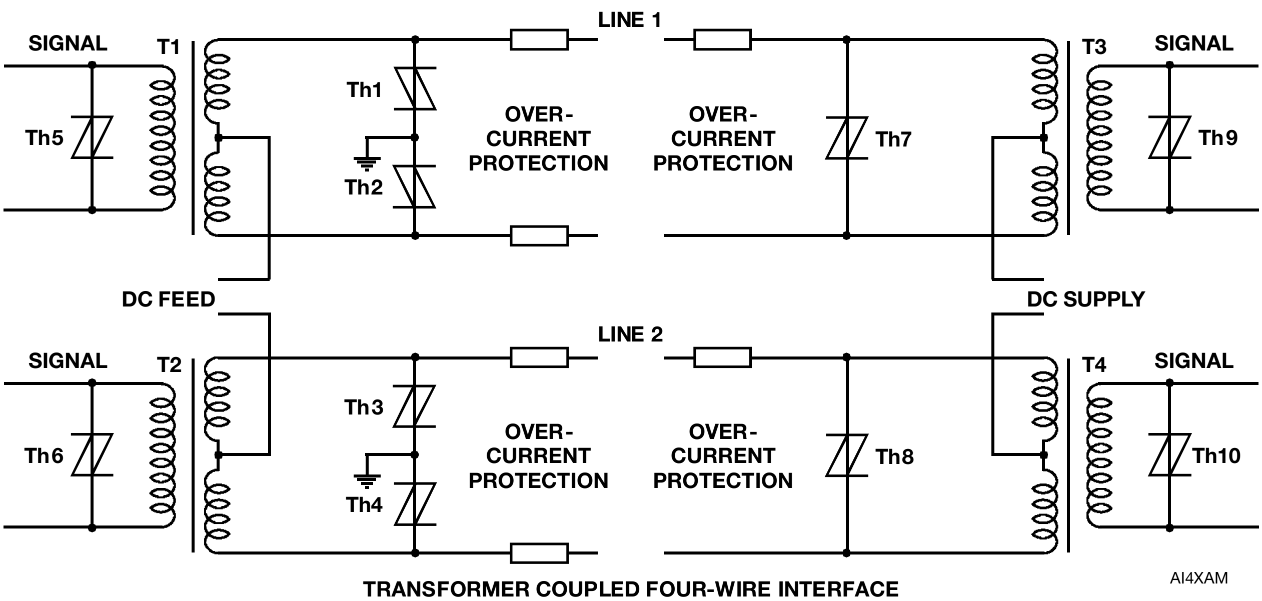


Figure 12. 4-Wire System

For an HDSL d.c. feed voltage of 180 V or less and operation down to an ambient of -25 °C, the following Th1, Th2, Th3 and Th4 protectors are suitable: TISP4250M3 or TISP4250H3, TISP3250H3 (combines Th1 and Th2 or Th3 and Th4) and TISP7250H3 (combines Th1, Th2 and Th7 or Th3, Th4 and Th8). Possible overcurrent protection components are covered in the 2-wire digital systems clause.

For ISDN interfaces powered with ±40 V (ETSI, ETS 300 012 1992) the following Th1, Th2, Th3 and Th4 protectors are suitable: TISP4070M3 or TISP4070H3 or TISP4070L3, TISP3070F3 or TISP3070H3 (combines Th1 and Th2 or Th3 and Th4) and TISP7070F3 or TISP7070H3 (combines Th1, Th2 and Th7 or Th3, Th4 and Th8). At the terminating adaptor, the Th7 and Th8 protectors do not "see" the d.c. feed voltage and should be selected to not clip the maximum signal level. Generally, the TISP40xxL1 series will be suitable.

Internal ISDN lines are not exposed to high stress levels and the chances of a.c. power intrusion are low (ETSI EN 300 386-2 1997). Accordingly, the equipment port protection needs are at a lower level than ports connected to outside lines.

Home Phone Networking

Using the existing house telephone wiring, home phone networking systems place the local network traffic in a high band above the POTS and ADSL (Asymmetrical Digital Subscriber Line) spectrum. Local network rates are 1 Mbps or more. To reject noise and harmonics, an in-line protection and 5 MHz to 10 MHz bandpass filter module is used for the equipment. These modules are available from magnetic component manufacturers (e.g. Bel Fuse Inc.) A typical circuit for the telephone line magnetics module is shown in Figure 13. Transformer T1 isolates the equipment from the house wiring. The isolated winding output is voltage limited by a very low-voltage protector, Th1. With a differential voltage of about 12 V peak to peak, the TISP4015L1 could be used for Th1. After filtering, connection is made to the differential transceiver of the processing IC.

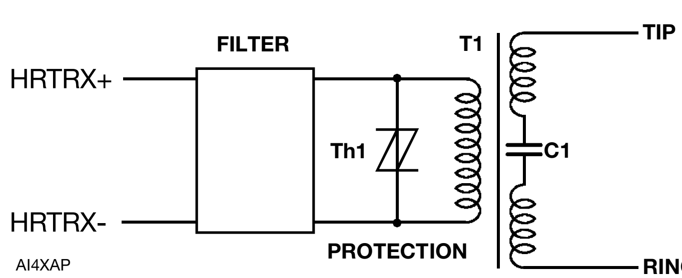
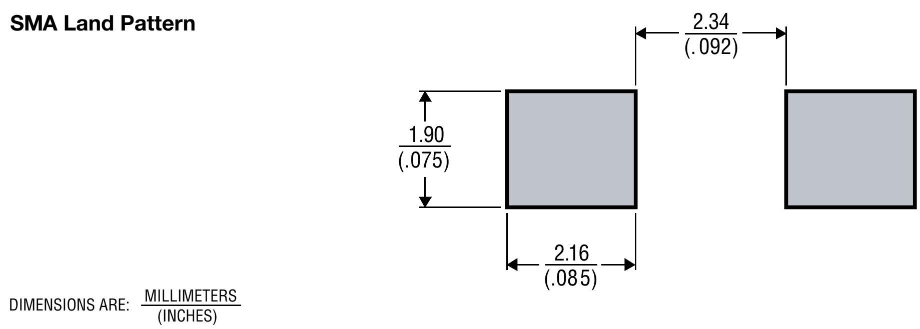


Figure 13. Home Phone Networking Isolation/filter/protection Circuit

MECHANICAL DATA

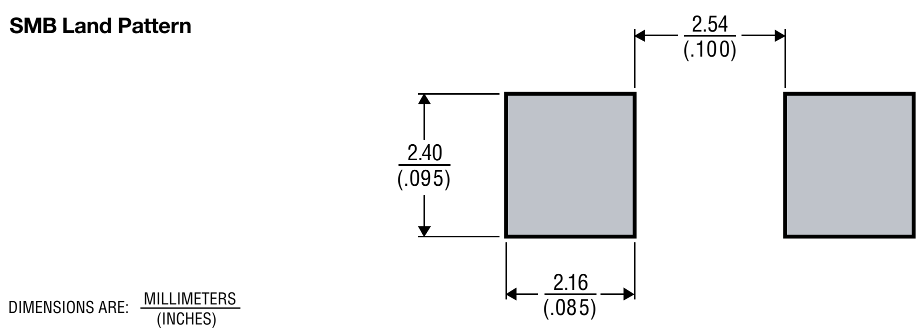
Recommended Printed Wiring Land Pattern Dimensions

SMA Land Pattern



MDXXBIC

SMB Land Pattern



MDXXBIB

Device Symbolization Code

Devices will be coded as below. As the device parameters are symmetrical, terminal 1 is not identified.

Device	Symbolization Code	Device	Symbolization Code
TISP4015L1AJ	4015L	TISP4015L1BJ	4015L1
TISP4030L1AJ	4030L	TISP4030L1BJ	4030L1
TISP4040L1AJ	4040L	TISP4040L1BJ	4040L1

Carrier Information

For production quantities, the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

Package	Carrier	Standard Quantity
SMA	Embossed Tape Reel Pack	5000
SMB		3000

AUGUST 1999 – REVISED JULY 2019

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