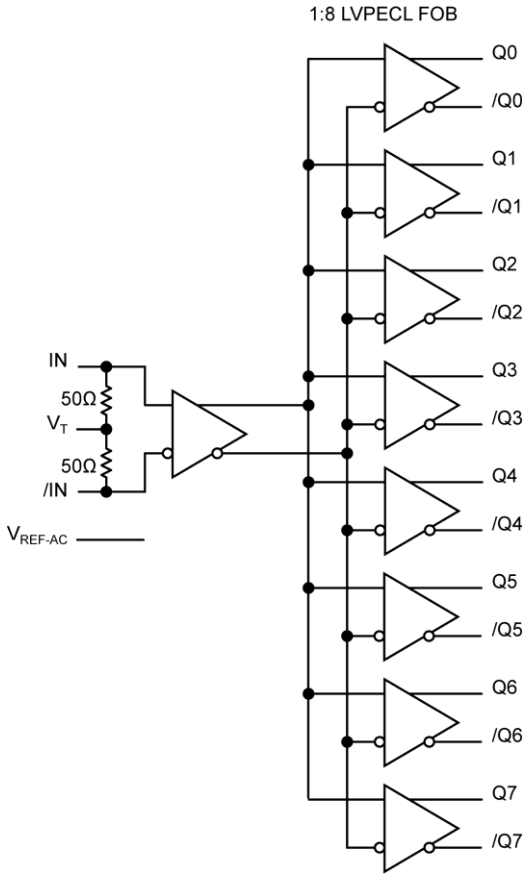
Typical Application



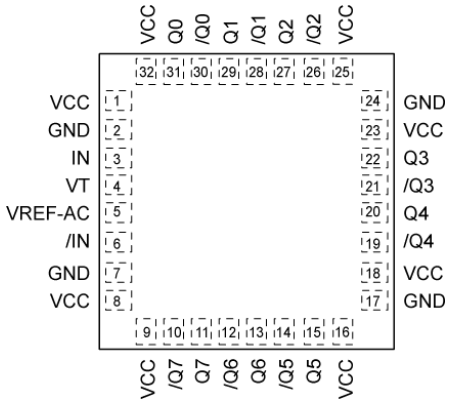
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89858UMG	QFN-32	Industrial	SY89858 with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89858UMGTR[2]	QFN-32	Industrial	SY89858 with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals Only.
2. Tape and Reel.

Pin Configuration



32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
3, 6	IN, /IN	Differential Input: This differential input accepts AC- or DC-coupled signals as small as 100mV (200mV$_{PP}$). Each pin of this pair internally terminates to a VT pin through 50□. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
4	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to this VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See the “Input Interface Applications” section for more details.
5	VREF-AC	Reference Voltage: This output biases to V_{CC}–1.2V (typical). It is used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01uF low ESR capacitor to V_{CC}. Maximum sink/source capability is 1.5mA.
1, 8, 9, 16, 18, 23, 25, 32	VCC	Positive Power Supply: Bypass with 0.1□F//0.01□F low ESR capacitors as close to the VCC pins as possible.
31, 30, 29, 28, 27, 26, 22, 21, 20, 19, 15, 14, 13, 12, 11, 10	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3, Q4, /Q4, Q5, /Q5, Q6, /Q6, Q7, /Q7	100k LVPECL Differential Outputs: Differential buffered output copy of the input signal. The LVPECL output swing is typically 800mV into 50Ω to V_{CC}–2V. Unused output pairs may be left floating with no impact on jitter. See “LVPECL Output” section.
2, 7, 17, 24	GND Exposed Pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .....–0.5V to +4.0V
Input Voltage (V_{IN}) .....–0.5V to V_{CC}
Termination Current
  Source or sink current on V_T ..... ±100mA
Reference Current[3]
  Source or sink current on V_{REF-AC}..... ±1.5mA
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge..... 100mA
Lead Temperature (soldering, 20 sec.) .....+260°C
Storage Temperature (T_s).....–65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC})..... +2.375V to +2.625V
  .....+3.0V to +3.6V
Ambient Temperature (T_A)..... –40°C to +85°C
Package Thermal Resistance[4]
QFN (θ_{JA})
  Still-Air ..... 35°C/W
QFN (ψ_{JB})
  Junction-to-Board ..... 20°C/W

DC Electrical Characteristics[5]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		95	150	mA
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)	Note 6	V_{CC} –1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 1b.	0.2			V
V_{T_IN}	IN-to-V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3V	V_{CC}–1.2V	V_{CC}–1.1V	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still air, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

LVPECL Outputs DC Electrical Characteristics[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C; R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	500	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1000	1600		mV

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[8]

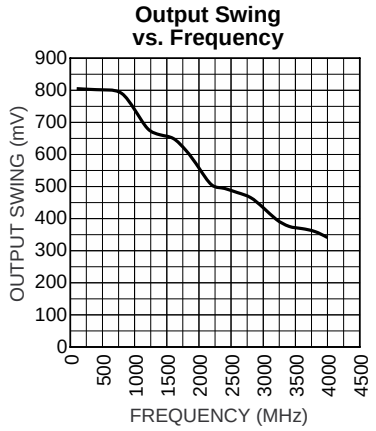
V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

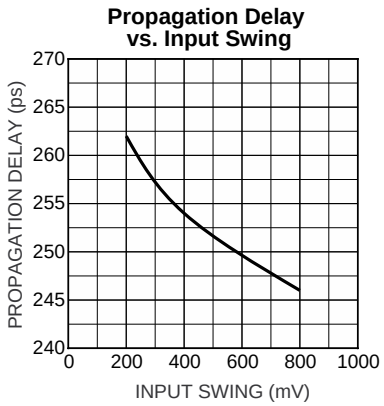
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ≥ 400mV	2.0	3.0		GHz
t_{PD}	Propagation Delay (IN-to-Q)		180	260	380	ps
T_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
T_{skew}	Output-to-Output Skew	Note 9			30	ps
	Part-to-Part Skew	Note 10			150	
t_{Jitter}	RMS Phase Jitter	Output = 25MHz Integration Range 12kHz – 20MHz		710		fs
t_R, t_F	Output Rise/Fall Time (20% to 80%)	At full output swing.	75	130	200	ps

Notes:

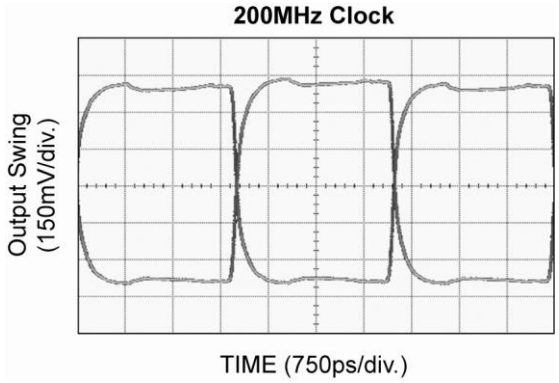
8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Output-to-output skew is measured between outputs under identical conditions.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Part-to-part skew includes variation in t_{pd}.

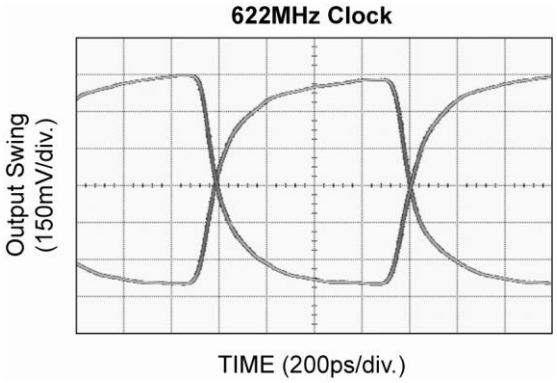
Typical Operating Characteristics

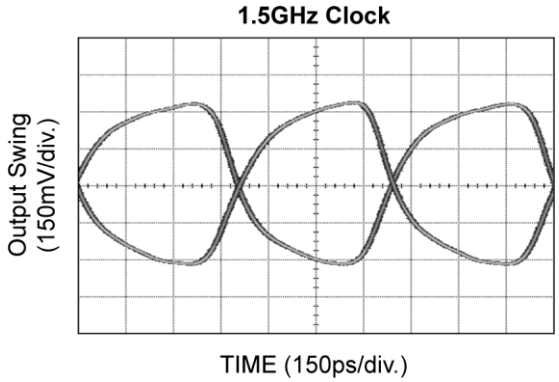


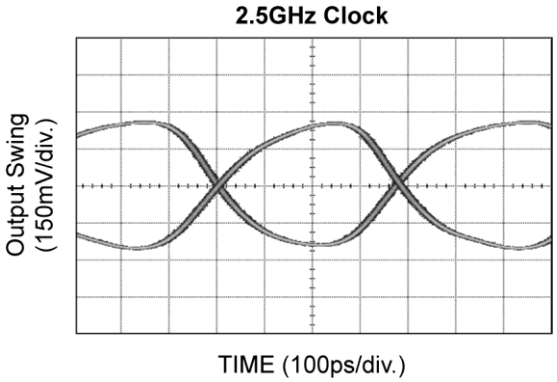


Functional Characteristics









Singled-Ended and Differential Swings

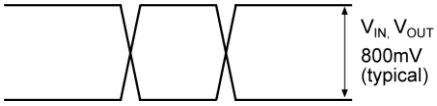


Figure 1a. Single-Ended Voltage Swing

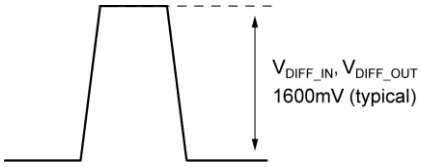
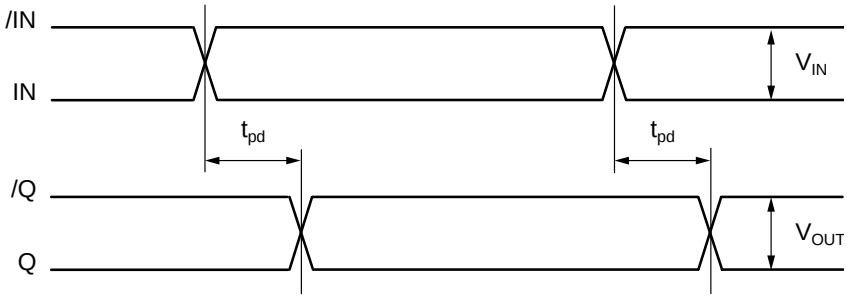


Figure 1b. Differential Voltage Swing

Timing Diagram



Input and Output Stages

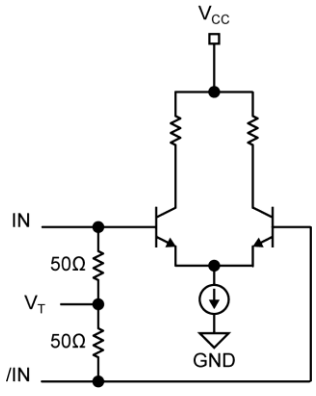


Figure 2a. Simplified Differential Input Stage

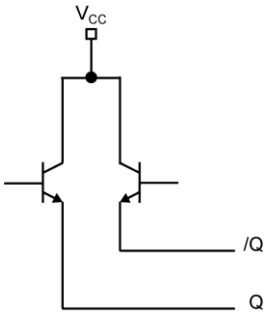


Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications

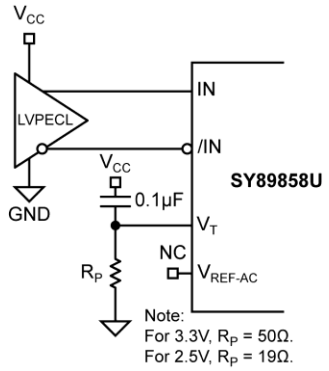


Figure 3a. LVPECL Interface (DC-Coupled)

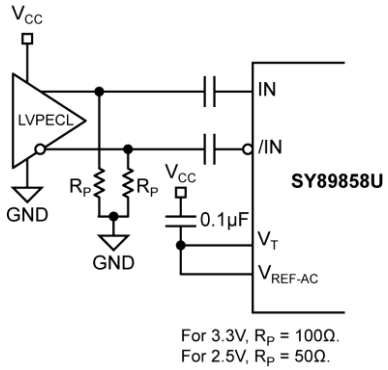
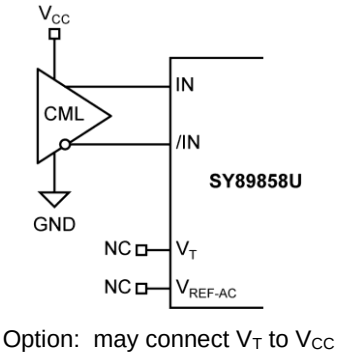


Figure 3b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

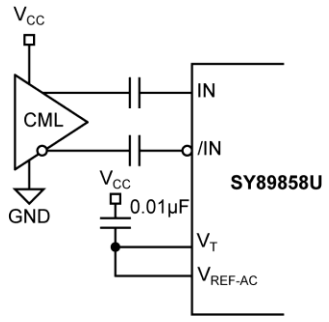


Figure 3d. CML Interface (AC-Coupled)

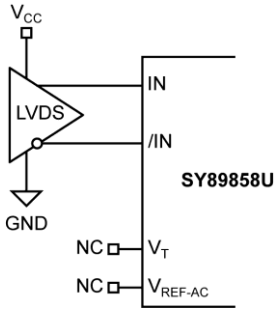


Figure 3e. LVDS Interface (DC-Coupled)

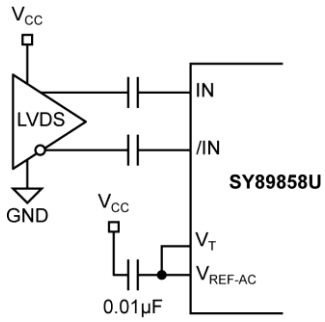


Figure 3f. LVDS Interface (AC-Coupled)

LVPECL Output Interface Applications

LVPECL has high input impedance, and very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques for terminating the LVPECL output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-resistor), and AC-coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

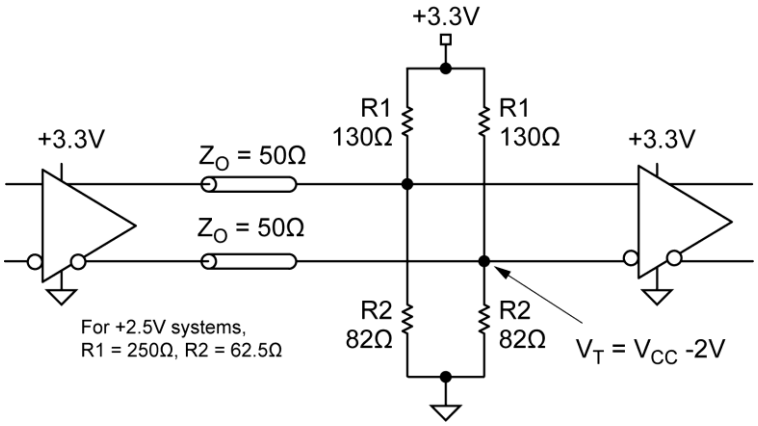


Figure 4a. Parallel Termination-Thevenin Equivalent

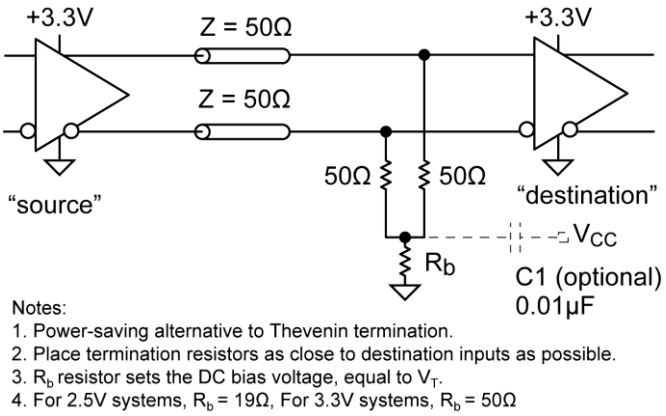
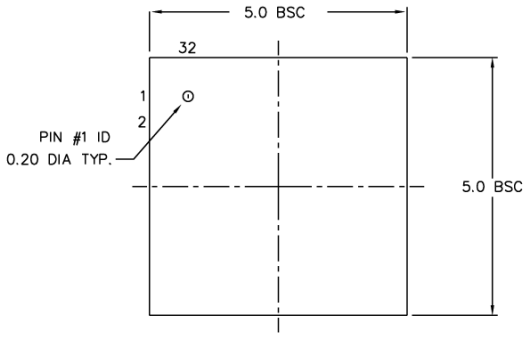


Figure 4b. Parallel Termination (3-Resistor)

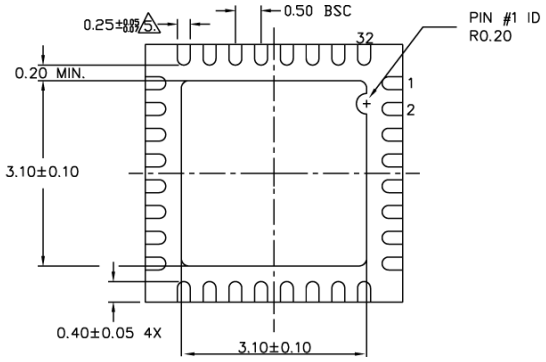
Related Product and Support Documentation

Part Number	Function	Datasheet Link
SY58032U	Ultra-Precision 1:8 LVPECL Fanout Buffer w/Internal Termination	www.micrel.com/product-info/products/sy58032u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

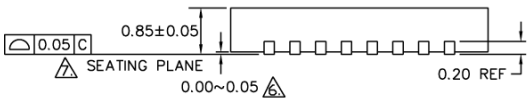
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin (5mm x 5mm)

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packaged before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management.

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