Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58610UMG	QFN-16	Industrial	610U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY58610UMGTR[2]	QFN-16	Industrial	610U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC Electricals only.

2. Tape and Reel.

Pin Configuration
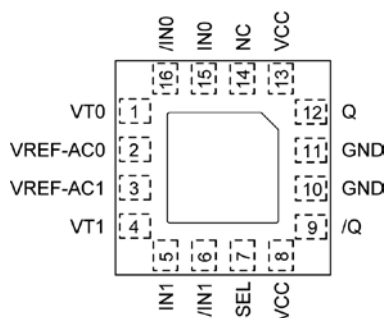
16-Pin QFN

Truth Table

SEL	Output
0	IN0 Selected
1	IN1 Selected

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" subsection.
2, 3	VREF-AC0, VREF-AC1	Reference Voltage: These outputs bias to V_{CC}–1.2V. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is ±0.5mA. See "Input Interface Applications" subsection.
5, 6 15, 16	IN1, /IN1 IN0, /IN0	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept DC-Coupled differential signals as small as 100mV (200mV$_{pp}$). Each pin of the pairs internally terminates with 50Ω to the corresponding VT pin. If the input swing falls below a certain threshold (typical 30mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. See "Input Interface Applications" subsection.
7	SEL	Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is V_{CC}/2.
8, 13	VCC	Positive Power Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V_{CC} pins as possible.
9, 12	/Q, Q	LVPECL Differential Output Pair: Differential buffered output copy of the selected input signal. The output swing is typically 800mV. Unused output pair may be left floating with no impact on jitter. See "LVPECL Output Termination" subsection.
10, 11	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
14	NC	No connect.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
LVPECL Output Current(I_{OUT})
    Continuous.. 50mA
    Surge 100mA
Current (V_T)
    Source or sink on VT pin .... ±100mA
Input Current
    Source or sink Current on (IN, /IN) .... ±50mA
Current (V_{REF})
    Source or sink current on V_{REF}-AC[4] .... ±0.5mA
Maximum operating Junction Temperature .... 125°C
Lead Temperature (soldering, 20sec.) .... 260°C
Storage Temperature (T_s) .... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) .... +2.375V to +3.60V
Ambient Temperature (T_A) .... –40°C to +85°C
Package Thermal Resistance[3]
    QFN
        Still-air (θ_{JA}) .... 60°C/W
        Junction-to-board (ψ_{JB}) .... 33°C/W

DC Electrical Characteristics[5]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		2.375	2.5	2.625	V
			3.0	3.3	3.6	
I_{CC}	Power Supply Current	No load, max. V_{CC}		40	50	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN, Note 7	V_{CC}-1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)	IN, /IN	0.2		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	see Figure 3a, Note 6	0.1		1.0	V
V_{DIFF_IN}	Differential Input Voltage Swing (|IN - /IN|)	see Figure 3b	0.2			V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{REF-AC}	AC Reference Voltage		V_{CC}-1.3		V_{CC}-1.0	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.

4. Due to the limited drive capability, use for input of the same package only.

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

6. V_{IN} (max) is specified when V_T is floating.

7. V_{IH} (min) not lower than 1.2V.

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LVPECL Outputs DC Electrical Characteristics[7]

V_{CC} = +2.5V ±5% or +3.3V ±10%, R_L = 50Ω to V_{CC}-2V; T_A = −40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	Q0, /Q0, Q1, /Q1	V_{CC}-1.145		V_{CC} -0.895	V
V_{OL}	Output LOW Voltage	Q0, /Q0, Q1, /Q1	V_{CC}-1.945		V_{CC}-1.695	V
V_{OUT}	Output Voltage Swing	See Figure 3a	550	800	950	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 3b	1100	1600		mV

LVTTL/CMOS DC Electrical Characteristics[70]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = −40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		30	µA
I_{IL}	Input LOW Current		-300			µA

Notes:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[8]

V_{CC} = +2.5V ±5% or +3.3V ±10%, R_L = 50Ω to V_{CC}-2V; Input $t_R/t_F \leq$ 300ps, T_A = −40°C to +85°C, unless otherwise stated.

Symbol	Parameter		Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency		NRZ Data	3.2			Gbps
			V_{OUT} > 400mV Clock	2.5	3		GHz
t_{PD}	Propagation Delay IN-to-Q		V_{IN}: 100mV-200mV	180	340	470	ps
			V_{IN}: >200mV	140	290	370	ps
	SEL-to-Q			150		450	ps
t_{Skew}	Input-to-Input Skew		Note 9, 10		5	20	ps
	Part-to-Part Skew		Note 11			150	ps
t_{Jitter}	Data	Random Jitter	Note 12			1	ps_{RMS}
		Deterministic Jitter	Note 13			10	ps_{PP}
	Clock	Cycle-to-Cycle Jitter	Note 14			1	ps_{RMS}
		Total Jitter	Note 15			10	ps_{PP}
t_R, t_F	Output Rise/Fall Times (20% to 80%)		At full output swing.	40	100	130	ps
	Duty Cycle		Differential I/O	47		53	%

Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.

9   Input-to-input skew is the time difference between the two inputs to one output, under identical input transitions.

10 Input-to-Input Skew is included in IN-to-Q propagation delay.

11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature, same transition edge, and no skew at the edges at the respective inputs.

12. Random jitter is measured with a K28.7 pattern, measured at ≤ f_{MAX}.

13. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}−1 PRBS pattern.

14. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = T_n − T_{n+1}$, where T is the time between rising edges of the output signal.

15. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^12 output edges will deviate by more than the specified peak-to-peak jitter value.

Functional Description

Fail-Safe Input (FSI)

The input includes a special fail-safe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below $100mV_{PK}$ ($200mV_{PP}$), typically $30mV_{PK}$. Maximum frequency of the SY58610U is limited by the FSI function.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, such that the voltage swing across the input pair is less than 100mV, the FSI function will eliminate a metastable condition and latch the outputs to the last valid state. No ringing and no undetermined state will occur at the output under these conditions. The output recovers to normal operation once the input signal returns to a valid state with a swing greater than 100mV.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to "Typical Operating Characteristics" for detailed information.

Timing Diagrams
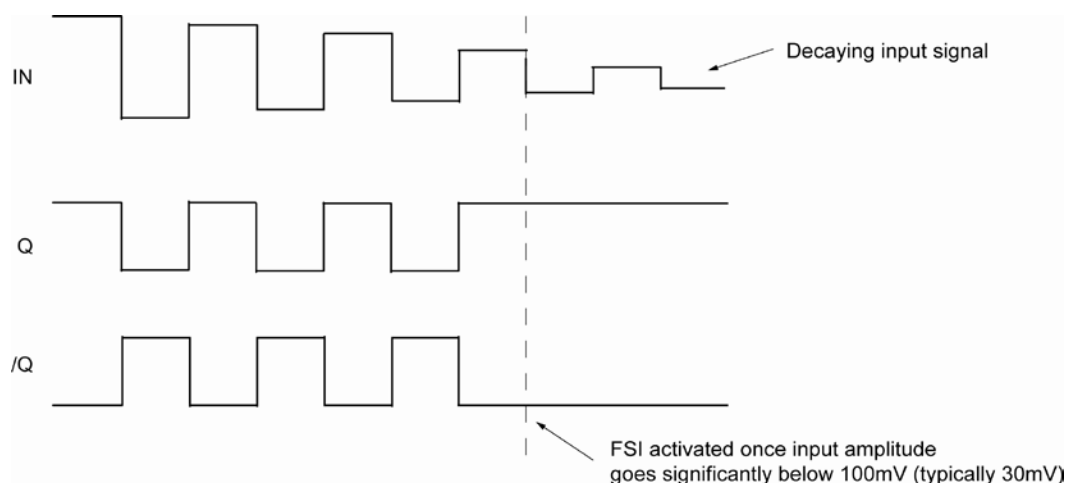
Figure 1a. Fail Safe Feature
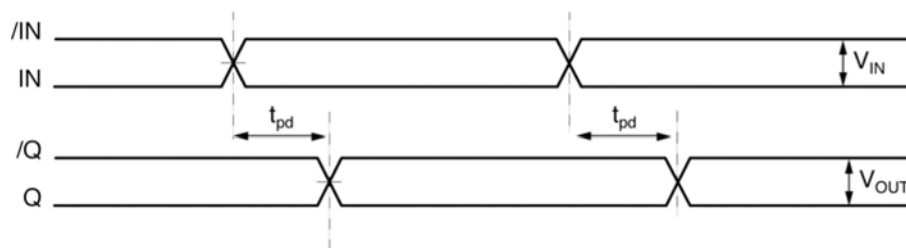
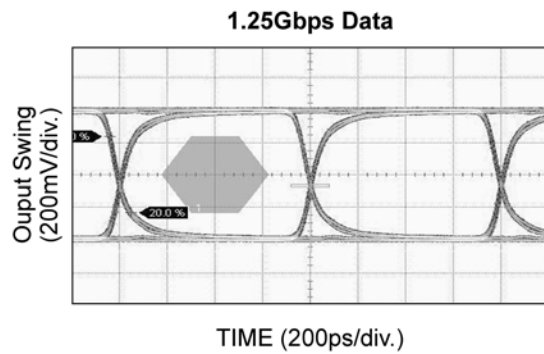**Figure 1b. Propagation Delay IN-to-Q**
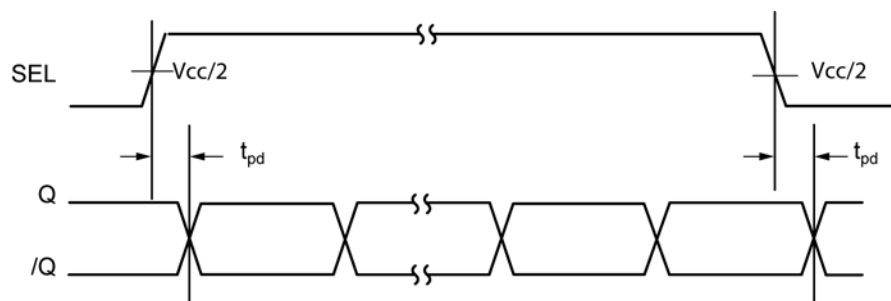
Figure 1c. Propagation Delay SEL-to-Q

Typical Characteristics

V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV, R_L = 50Ω to V_{CC}-2V, T_A = 25°C, unless otherwise stated.
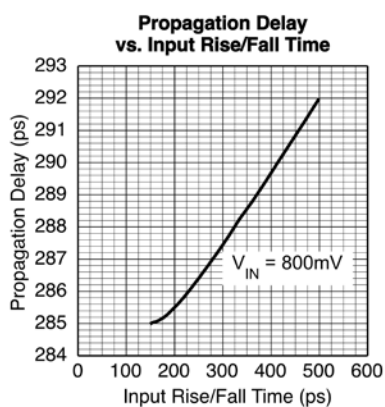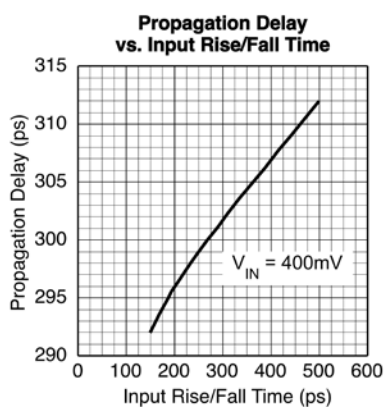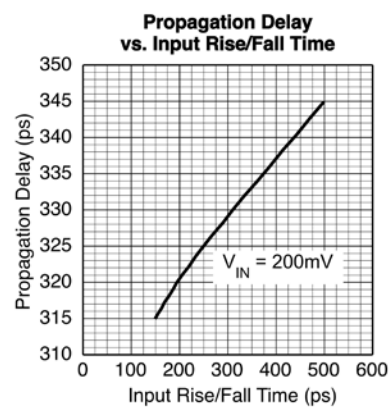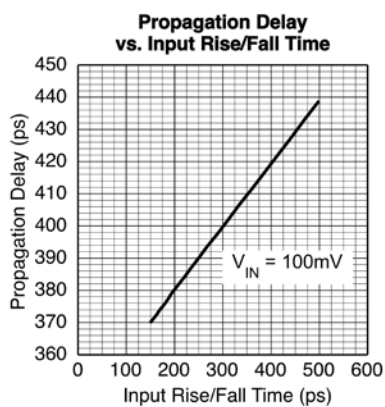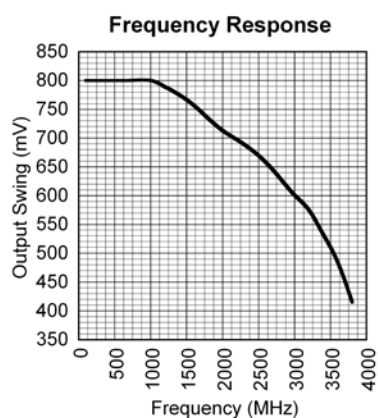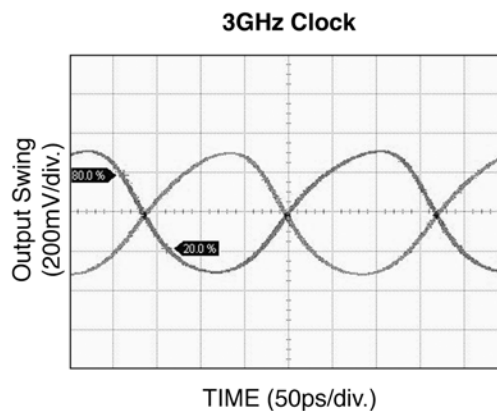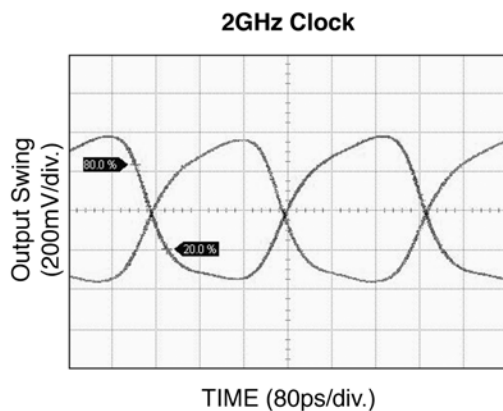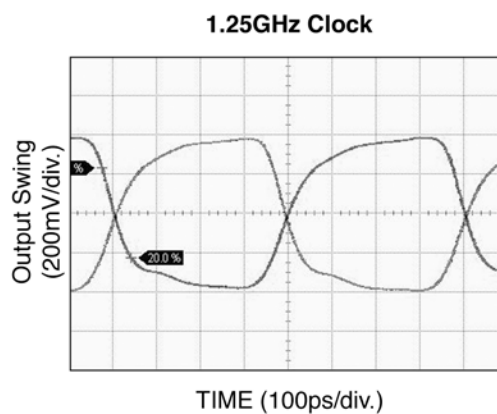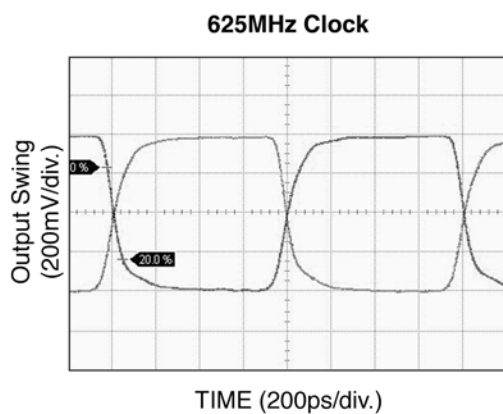
Functional Characteristics

V_{CC} = 3.3V, GND = 0V, V_{IN} = 400mV, R_L = 50Ω to V_{CC}-2V, T_A = 25°C, unless otherwise stated.

1.25Gbps Data

TIME (200ps/div.)

2.5Gbps Data

TIME (100ps/div.)

3.2Gbps Data

TIME (80ps/div.)

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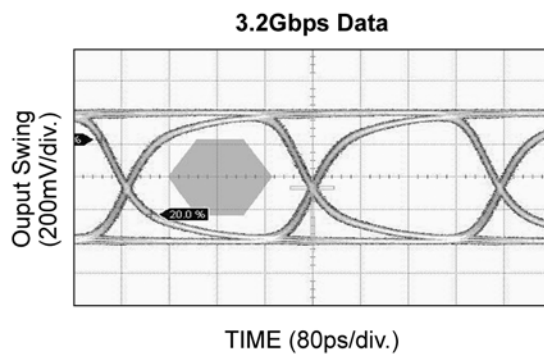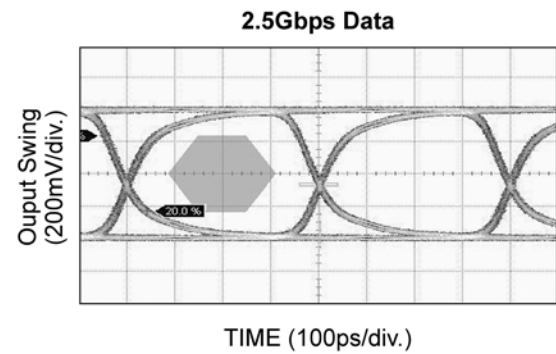
Functional Characteristics (continued)

V_{CC} = 3.3V, GND = 0V, V_{IN} = 400mV, R_L = 50Ω to V_{CC}-2V, T_A = 25°C, unless otherwise stated.

625MHz Clock

Output Swing (200mV/div.)

TIME (200ps/div.)

1.25GHz Clock

Output Swing (200mV/div.)

TIME (100ps/div.)

2GHz Clock

Output Swing (200mV/div.)

TIME (80ps/div.)

3GHz Clock

Output Swing (200mV/div.)

TIME (50ps/div.)

Input and Output Stage
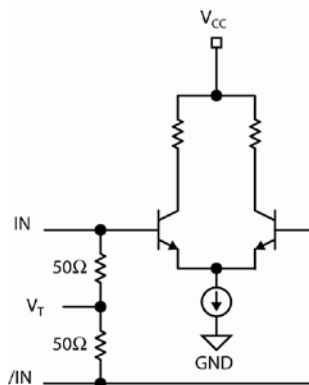
Figure 2a. Simplified Differential Input Buffer
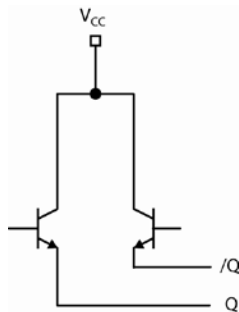
Figure 2b. Simplified LVPECL Output Buffer

Single-Ended and Differential Swings
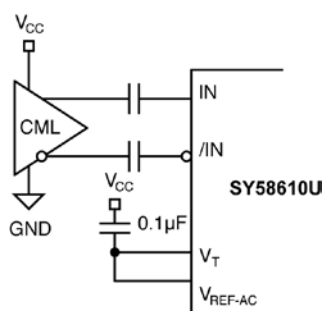

Figure 3a. Single-Ended Voltage Swing
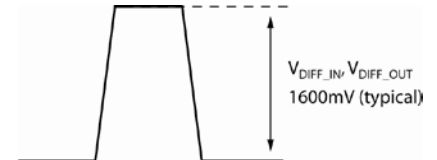
Figure 3b. Differential Voltage Swing
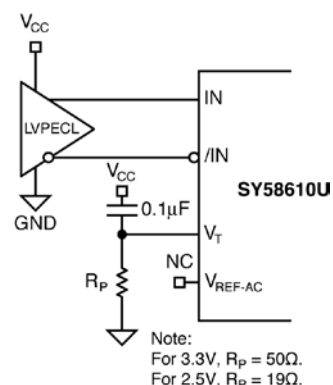
Input Interface Applications
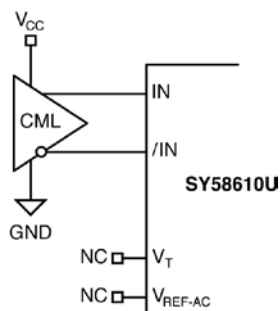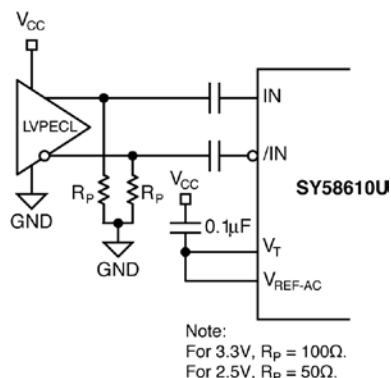

**Figure 4a. CML Interface
(DC-Coupled)**
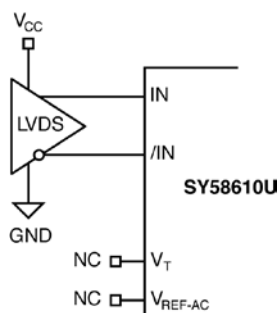
Option: May connect V_T to V_{CC}

**Figure 4b. CML Interface
(AC-Coupled)**

**Figure 4c. LVPECL Interface
(DC-Coupled)**


**Figure 4d. LVPECL Interface
(AC-Coupled)**

Figure 4e. LVDS Interface

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LVPECL Output Termination

LVPECL output has very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω - controlled impedance transmission lines. There are several techniques in terminating the LVPECL output, as shown in Figures 5a and 5b.

For 2.5V system:
R1=250Ω, R2=62.5Ω
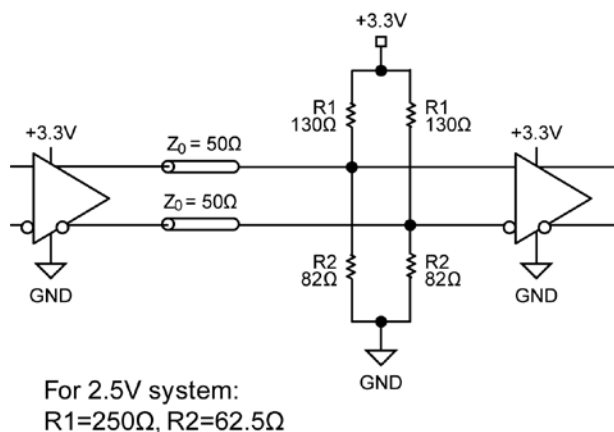
Figure 5a. Parallel Termination-Thevenin Equivalent

For 2.5V system: R1 = 19Ω.
For 3.3V system: R1 = 50Ω.
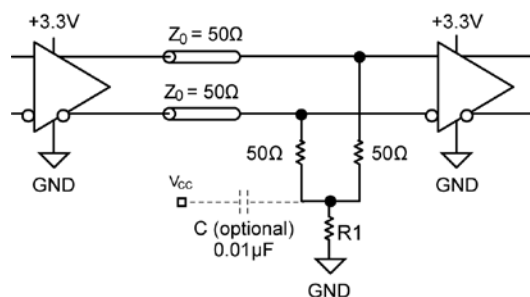
**Figure 5b. Three-Resistor "Y-Termination"**

Related Product and Support Documents

Part Number	Function	Data Sheet Link
SY58609U	4.25Gbps Precision, CML 2:1 MUX with Internal Termination and Fail Safe Input	http://www.micrel.com/_PDF/HBW/sy58609u.pdf
SY58611U	3.2Gbps Precision, LVDS 2:1 MUX with Internal Termination and Fail Safe Input	http://www.micrel.com/_PDF/HBW/sy58611u.pdf
HBW Solutions	New Products and Termination Application Notes	http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml

Package Information
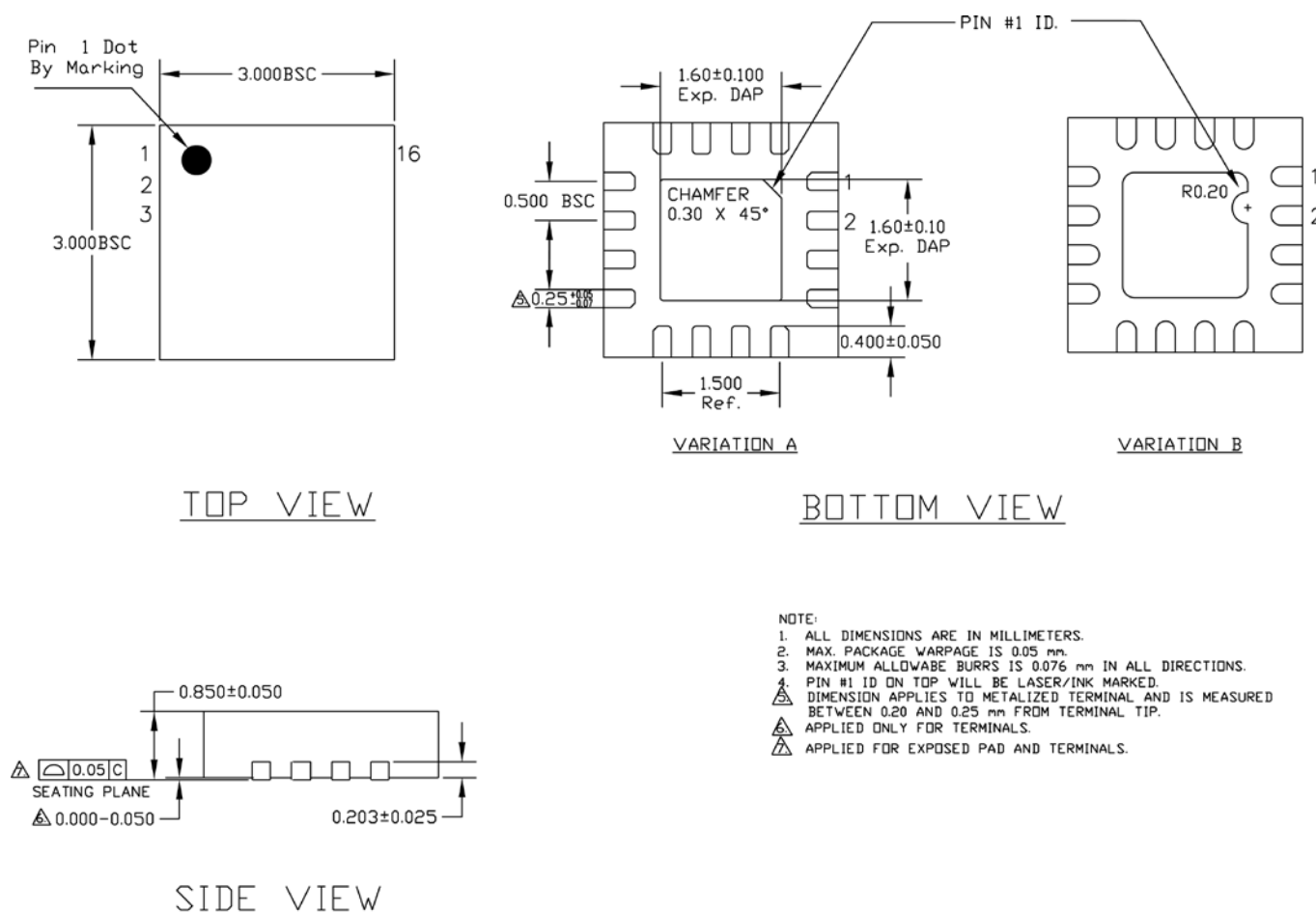
16-Pin (3mm x 3mm) QFN

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