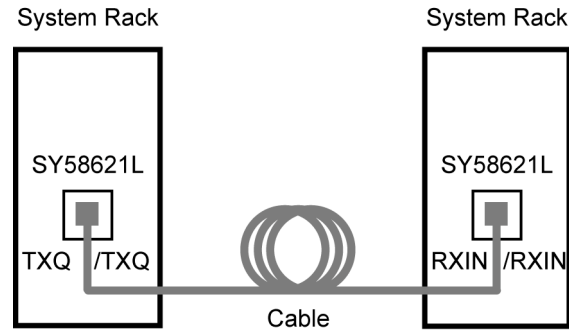
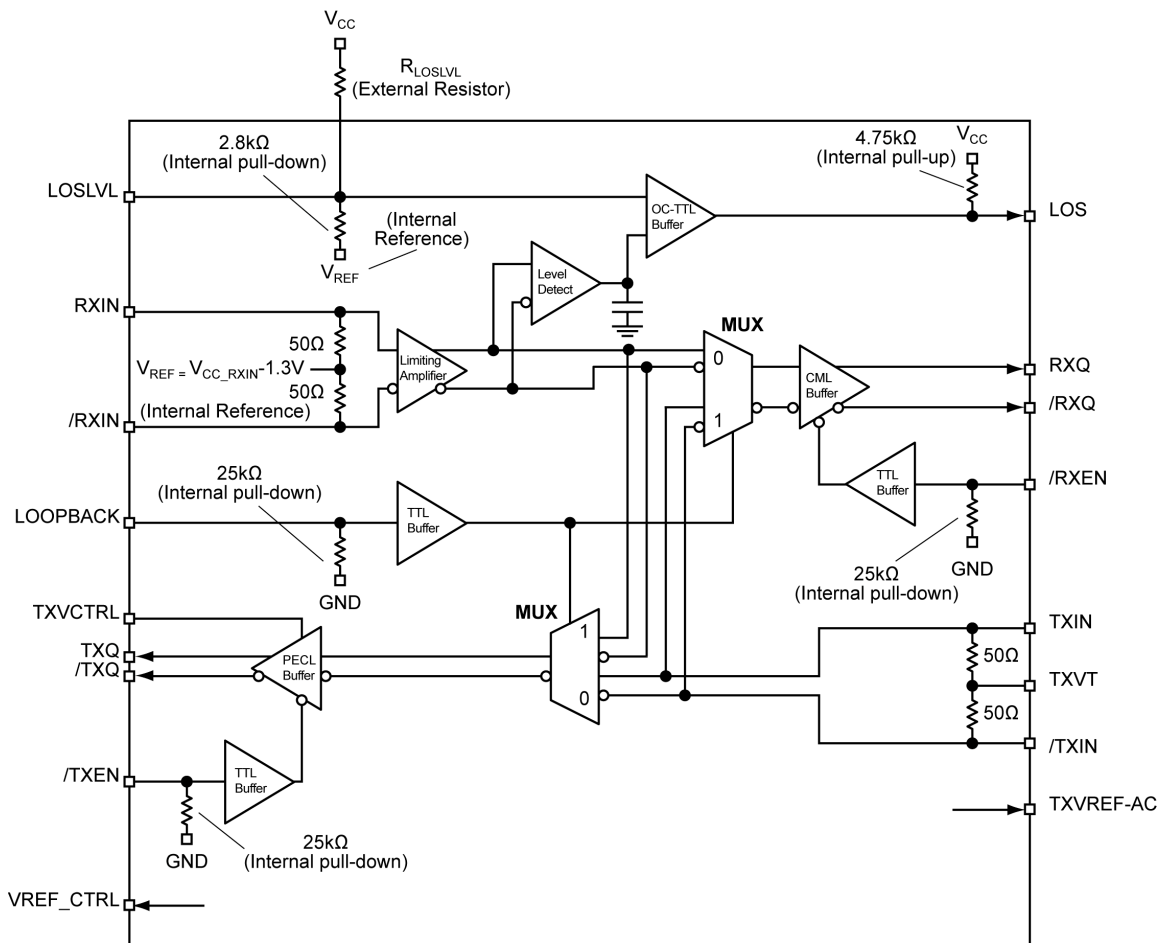


Typical Applications



Functional Block Diagram



Note:

It is recommended that $R_{LOS_{LVL}} \leq 10k\Omega$. See the "Typical Operating Characteristics" section for more details.

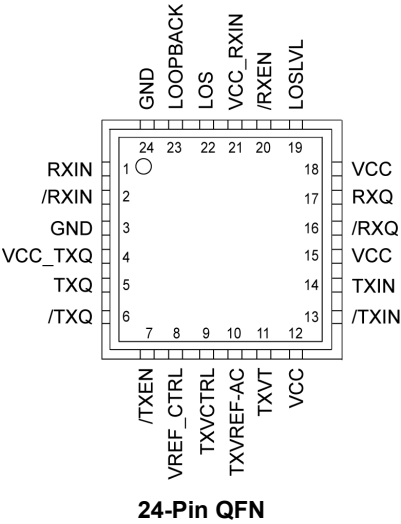
Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|-----------------------------|--------------|-----------------|--------------------------------------|-------------------|
| SY58621LMG | QFN-24 | Industrial | 621L with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY58621LMGTR ⁽²⁾ | QFN-24 | Industrial | 621L with Pb-Free bar-line indicator | NiPdAu Pb-Free |

Notes:

- 1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
- 2. Tape and Reel.

Pin Configuration



Pin Description

Inputs

| Pin Number | Pin Name | Pin Description |
|------------|-------------|---|
| 23 | LOOPBACK | LOOPBACK Mode Control. TTL/CMOS control input. LOOPBACK is an active HIGH signal used to control the LOOPBACK MUX. LOOPBACK is internally connected to a 25k Ω pull-down resistor and will default to a LOW state if left open. $V_{TH} = V_{CC}/2$. |
| 20 | /RXEN | Receiver Output Control. TTL/CMOS control input. /RXEN is an active LOW signal used to enable the receiver outputs. /RXEN is internally connected to a 25k Ω pull-down resistor and will default to a LOW state if left open. $V_{TH} = V_{CC}/2$. |
| 1, 2 | RXIN, /RXIN | Receiver Differential Input. Input accepts AC differential signals as small as 10mV (20mV _{PP}). Each pin internally terminates to $V_{CC_RXIN} - 1.3V$ (internal voltage reference) through 50 Ω . Input will default to an indeterminate state if left open. See figure 6b. |
| 7 | /TXEN | Transmitter Output Control. TTL/CMOS control input. /TXEN is an active LOW signal used to enable the transmitter output. /TXEN is internally connected to a 25k Ω pull-down resistor and will default to a LOW state if left open. $V_{TH} = V_{CC}/2$. |
| 14, 13 | TXIN, /TXIN | Transmitter Differential Input. Input accepts AC- or DC-coupled differential signals as small as 100mV (200mV _{PP}). Each pin terminates to the TXVT pin through 50 Ω . Note that this input will default to an indeterminate state if left open. See figure 6a. |
| 9 | TXVCTRL | Transmitter Output Swing Control. Input that controls the output amplitude of the transmitter. The operating range of the control input is from V_{REF_CTRL} (max swing) to V_{CC} (min swing). Control of the output swing can be obtained by using a variable resistor between V_{REF_CTRL} and V_{CC_TXQ} through a wiper driving TXVCTRL. Setting TXVCTRL to V_{CC_TXQ} sets the output swing to min swing. Refer to the "Interface Applications" and "Output Stage" sections for more details. |
| 11 | TXVT | Input Termination Center-Tap. Each side of the transmitter differential input pair terminates to the TXVT pin. The TXVT pin provides a center-tap to a termination network for maximum interface flexibility. Refer to the "Input Stage" section for more details. |

Outputs

| Pin Number | Pin Name | Pin Description |
|------------|-----------|--|
| 22 | LOS | Loss-of-Signal Output. TTL-compatible output with internal 4.75k Ω pull-up resistor. Loss-of-Signal asserts to logic HIGH when the receiver input amplitudes fall below the threshold set by LOSLVL. |
| 19 | LOSLVL | RX Loss-of-Signal Level Set. A resistor (R_{LOSLVL}) connected between LOSLVL and V_{CC} sets the threshold for the data input amplitude at which the LOS output is asserted. Default is max sensitivity. LOSLVL is used to set the Loss-of-Signal (LOS) voltage. It is internally connected to a 2.8k Ω pull-down resistor to an internal V_{REF} voltage source. See "Typical Operating Characteristics," and "Application Implementation" sections for more details. |
| 17, 16 | RXQ, /RXQ | Receiver Differential Output. Output is CML compatible. Refer to the "Truth Table" and "Output Stage" sections for more details. Unused output pair may be left open. The output is designed to drive 400mV (800mV _{PP}) into 50 Ω to V_{CC} or 100 Ω across the pair. |
| 5, 6 | TXQ, /TXQ | Transmitter differential Variable Swing Output. Output is LVPECL-compatible. Please refer to the "Truth Table" section for details. Unused output pair may be left open. Each output is designed to drive 80mV (min) to 800mV (typ) into 50 Ω to V_{CC} -2V depending on TXVCTRL. |
| 8 | VREF_CTRL | Transmitter Output Reference Voltage. Output biases to V_{CC_TXQ} -1.3V. Connecting V_{REF_CTRL} to TXVCTRL sets the transmitter output swing to max swing. |
| 10 | TXVREF-AC | Transmitter Input Reference Voltage. This output biases to V_{CC} -1.3V. It is used when AC coupling the transmitter input. For AC-coupled applications, connect TXVREF-AC to the TXVT pin and bypass with a 0.01 μ F low ESR capacitors to V_{CC} . See "Input Stage" section for more details. Maximum sink/source current is ± 1.5 mA. |

Power Pins

| Pin Number | Pin Name | Pin Description |
|------------|---------------------|--|
| 3, 24 | GND, Exposed Pad | Ground. GND pins and exposed pad must be connected to the same ground plane. |
| 12, 15, 18 | VCC | 3.3V $\pm 10\%$ Positive Power Supply. Bypass with 0.1 μ F//0.01 μ F low ESR capacitors and place as close to each V_{CC} pins as possible. Power pins are not connected internally and must be connected to the same power supply externally. |
| 21 | VCC_RXIN | 3.3V $\pm 10\%$ Receive Input Power Supply. Bypass with 0.1 μ F//0.01 μ F low ESR capacitors and place as close to the V_{CC_RXIN} pin as possible. Power pins are not connected internally and must be connected to the same power supply externally. |
| 4 | VCC_TXQ | 3.3V $\pm 10\%$ Output Transmit Power Supply. Bypass with 0.1 μ F//0.01 μ F low ESR capacitors and place as close to the V_{CC_TXQ} pin as possible. Power pins are not connected internally and must be connected to the same power supply externally. |

Truth Table

| LOOPBACK | RXQ | TXQ |
|----------|------|------|
| 0 | RXIN | TXIN |
| 1 | TXIN | RXIN |

Absolute Maximum Ratings⁽¹⁾**Supply Voltage**(V_{CC}, V_{CC_TXQ}, V_{CC_RXIN}).....-0.5V to +4.0V**Input Voltage**LOSLVL..... V_{REF} -1.2V to V_{CC}LOOPBACK.....-0.5V to V_{CC}/TXEN, /RXEN.....-0.5V to V_{CC}TXVCTRL..... VREF_CTRL -1.2V to V_{CC}TXIN, /TXIN.....-0.5V to V_{CC}**LVPECL Output Current (I_{OUT})**

TXQ, /TXQ

Continuous.....±50mA

Surge.....±100mA

Source or Sink Current on

TXVT.....±100mA

LOS.....±5mA

RXQ, /RXQ.....±25mA

RXIN, /RXIN.....±10mA

TXIN, /TXIN.....±50mA

TXVREF-AC, VREF-CTRL.....±2mA

Lead Temperature (soldering, 20sec.)..... 260°C

Storage Temperature (T_s)..... -65°C to +150°C**DC Electrical Characteristics⁽⁴⁾**T_A = -40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------------|-----------------------|-------------------------------|-----|-----|-----|-------|
| V _{CC} | Power Supply | | 3 | 3.3 | 3.6 | V |
| V _{CC_TXQ} | Transmit Power Supply | | 3 | 3.3 | 3.6 | V |
| V _{CC_RXIN} | Receive Power Supply | | 3 | 3.3 | 3.6 | V |
| I _{CC} | Power Supply Current | No load, max. V _{CC} | | 100 | 150 | mA |

Receiver Input DC Electrical CharacteristicsV_{CC_RXIN} = 3.3V ±10%; T_A = -40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------------|--|-----------------------------|-------------------------------|-------------------------------|-------------------------------|-------|
| R _{IN} | Input Resistance (RXIN to VREF) | | 45 | 50 | 55 | Ω |
| R _{DIFF_IN} | Input Resistance (RXIN to /RXIN) | | 90 | 100 | 110 | Ω |
| V _{IN} | Input Voltage Swing (RXIN, /RXIN) | See Figure 5a AC-coupled | 10 | | 900 | mV |
| V _{DIFF_IN} | Differential Input Voltage Swing RXIN - /RXIN | See Figure 5b AC-coupled | 20 | | 1800 | mV |
| V _{REF} | Internal Reference Voltage | | V _{CC_RXIN} -1.48 | V _{CC_RXIN} -1.32 | V _{CC_RXIN} -1.16 | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Receiver Output DC Electrical Characteristics

$V_{CC} = 3.3V \pm 10\%$, $R_L = 100\Omega$ across the outputs; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|---|--|------------------|------------------|----------|----------|
| V_{OH} | Output HIGH Voltage (RXQ, /RXQ) | $R_L = 50\Omega$ to V_{CC} | $V_{CC} - 0.020$ | $V_{CC} - 0.010$ | V_{CC} | V |
| V_{OUT} | Output Voltage Swing (RXQ, /RXQ) | See Figure 5a | 325 | 400 | 500 | mV |
| V_{DIFF_OUT} | Differential Output Voltage Swing (RXQ, /RXQ) | See Figure 5b | 650 | 800 | 1000 | mV |
| R_{OUT} | Single-Ended Output Impedance | | 45 | 50 | 55 | Ω |
| R_{DIFF_OUT} | Differential Output Impedance | | 90 | 100 | 110 | Ω |
| V_{OFFSET} | Differential Output Offset | $R_L = 50\Omega$ to V_{CC} , limiting mode | -140 | | +140 | mV |

Transmitter Input DC Electrical Characteristics

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------|--|---------------|-----------------|----------------|----------------|----------|
| R_{IN} | Input Resistance (TXIN to TXVT) | | 45 | 50 | 55 | Ω |
| R_{DIFF_IN} | Differential Input Resistance (TXIN to /TXIN) | | 90 | 100 | 110 | Ω |
| V_{IH} | Input HIGH Voltage (TXIN, /TXIN) | | 1.2 | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (TXIN, /TXIN) | | 0 | | $V_{IH} - 0.1$ | V |
| V_{IN} | Input Voltage Swing (TXIN, /TXIN) | See Figure 5a | 0.1 | | V_{CC} | V |
| V_{DIFF_IN} | Differential Input Voltage Swing TXIN - /TXIN | See Figure 5b | 0.2 | | | V |
| V_{T_IN} | TXIN, /TXIN to VT | | | | 1.28 | V |
| V_{TXVREF_AC} | Output Reference Voltage | | $V_{CC} - 1.4$ | $V_{CC} - 1.3$ | $V_{CC} - 1.3$ | V |
| V_{REF_CTRL} | Output Reference Voltage | | $V_{CC} - 1.4$ | $V_{CC} - 1.3$ | $V_{CC} - 1.3$ | V |
| $V_{TXVCTRL}$ | Input Voltage (TXVCTRL) | | V_{REF_CTRL} | | V_{CC} | V |

Transmitter Output DC Electrical Characteristics

$V_{CC_TXQ} = 3.3V \pm 10\%$, $R_L = 50\Omega$ to $V_{CC_TXQ} - 2V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|---|--|-----------------------|-----------------------|-----------------------|-------|
| V_{OH} | Output HIGH Voltage (TXQ, /TXQ) | | $V_{CC_TXQ} - 1.145$ | $V_{CC_TXQ} - 1.020$ | $V_{CC_TXQ} - 0.895$ | V |
| V_{OL} | Output LOW Voltage (TXQ, /TXQ) | TXVCTRL = V_{REF_CTRL} | $V_{CC_TXQ} - 1.945$ | $V_{CC_TXQ} - 1.820$ | $V_{CC_TXQ} - 1.695$ | V |
| | | TXVCTRL = V_{CC_TXQ} | | $V_{CC_TXQ} - 1.100$ | | V |
| V_{OUT} | Output Voltage Swing (TXQ, /TXQ) | TXVCTRL = V_{REF_CTRL} See Figure 5a | 550 | 800 | | mV |
| | | TXVCTRL = V_{CC_TXQ} See Figure 5a | | 80 | | mV |
| V_{DIFF_OUT} | Differential Output Voltage Swing (TXQ, /TXQ) | TXVCTRL = V_{REF_CTRL} See Figure 5b | 1100 | 1600 | | mV |
| | | TXVCTRL = V_{CC_TXQ} See Figure 5b | | 160 | | mV |

LVTTTL/CMOS INPUT DC Control Electrical Characteristics⁽⁵⁾

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|------------------------|--------------------------|-----|-----|-----|---------|
| V_{IL} | /TXEN, /RXEN, LOOPBACK | | | | 0.8 | V |
| V_{IH} | /TXEN, /RXEN, LOOPBACK | | 2 | | | V |
| I_{IL} | /TXEN, /RXEN, LOOPBACK | $I_{IL}@V_{IN} = 0.5V$ | 0 | | 50 | μA |
| I_{IH} | /TXEN, /RXEN, LOOPBACK | $I_{IH}@V_{IN} = V_{CC}$ | | | 300 | μA |

Note:

5. /TXEN, /RXEN, and LOOPBACK have an internal pull-down 25k Ω resistor.

LOS DC Electrical Characteristics

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------------|----------------------------|--|------------------|-----|----------|------------------|
| V_{LOSLVL} | LOSLVL Voltage Range | | V_{REF} | | V_{CC} | V |
| V_{OH} | Output HIGH Voltage | Source 100 μ A; $V_{CC} \geq 3.3V$ | 2.4 | | | V |
| V_{OL} | Output LOW Voltage | Sink 2mA | | | 0.5 | V |
| VSR | LOS Sensitivity Range | | 7 | | 35 | mV _{PP} |
| LOS _{AL} | Low LOS Assert Level | $R_{\text{LOSLVL}} = 10\text{k}\Omega$ 2 ⁷ -1 Data Pattern, Note 7 | | | | |
| | | 622Mbps | | 15 | | mV |
| | | 3.2Gbps | | 10 | | mV |
| LOS _{DL} | Low LOS De-assert Level | $R_{\text{LOSLVL}} = 10\text{k}\Omega$ 2 ⁷ -1 Data Pattern, Note 7 | | | | |
| | | 622Mbps | | 20 | | mV |
| | | 3.2Gbps | | 15 | | mV |
| HYS _L | Low LOS Hysteresis | $R_{\text{LOSLVL}} = 10\text{k}\Omega$, limiting mode 2 ⁷ -1 Data Pattern, Note 6 and 7 | | | | |
| | | 622Mbps | | 3 | | dB |
| | | 3.2Gbps | | 5.5 | | dB |
| LOS _{AM} | Medium LOS Assert Level | $R_{\text{LOSLVL}} = 5\text{k}\Omega$ 2 ⁷ -1 Data Pattern, Note 7 | | | | |
| | | 622Mbps | | 20 | | mV |
| | | 3.2Gbps | | 15 | | mV |
| LOS _{DM} | Medium LOS De-assert Level | $R_{\text{LOSLVL}} = 5\text{k}\Omega$ 2 ⁷ -1 Data Pattern, Note 7 | | | | |
| | | 622Mbps | | 30 | | mV |
| | | 3.2Gbps | | 25 | | mV |
| HYS _M | Medium LOS Hysteresis | $R_{\text{LOSLVL}} = 5\text{k}\Omega$, limiting mode 2 ⁷ -1 Data Pattern, Note 6 and 7 | | | | |
| | | 622Mbps | | 4 | | dB |
| | | 3.2Gbps | | 5.5 | | dB |
| LOS _{AH} | High LOS Assert Level | $R_{\text{LOSLVL}} = 1\text{k}\Omega$ 2 ⁷ -1 Data Pattern, Note 7 | | | | |
| | | 622Mbps | | 35 | | mV |
| | | 3.2Gbps | | 30 | | mV |
| LOS _{DH} | High LOS De-assert Level | $R_{\text{LOSLVL}} = 1\text{k}\Omega$ 2 ⁷ -1 Data Pattern, Note 7 | | | | |
| | | 622Mbps | | 60 | | mV |
| | | 3.2Gbps | | 55 | | mV |
| HYS _H | High LOS Hysteresis | $R_{\text{LOSLVL}} = 1\text{k}\Omega$, limiting mode 2 ⁷ -1 Data Pattern, Note 6 and 7 | | | | |
| | | 622Mbps | | 5 | | dB |
| | | 3.2Gbps | | 5.5 | | dB |

Notes:

6. Hysteresis is defined as: $20\text{Log}_{10} \left(\frac{SD_AssertVoltage}{SD_De-assertVoltage} \right) \text{dB}$.

7. See the "Typical Operating Characteristics" section for more details on R_{LOSLVL} and its associated LOS assert and de-assert amplitudes for a 2⁷-1 PRBS data pattern. See the "PRBS Discussion" section for more details on the 2⁷-1 PRBS data pattern.

AC Electrical Characteristics⁽⁸⁾

$V_{CC} = V_{CC_TXQ} = V_{CC_RXIN} = 3.3V \pm 10\%$, Receiver Load: $R_L = 100\Omega$ across the outputs. Transmitter Load: $R_L = 50\Omega$ to $V_{CC_TXQ} - 2V$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

Receiver and Transmitter

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------|---------------------------|-----------|-----|-----|---------|-------------------|
| t_{JITTER} | Deterministic Jitter (DJ) | Note 9 | | | Note 13 | ps _{PP} |
| | Random Jitter (RJ) | Note 10 | | 0.7 | 5 | ps _{RMS} |
| | Crosstalk-Induced Jitter | Note 11 | | | 1.2 | ps _{RMS} |

Receiver

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------------------|---------------------------------------|---|-------|-----|-----|---------------|
| f_{MAX} | Maximum Operating Frequency | $V_{RXIN} \geq 10\text{mV}$ (20mV _{PP}) | 3.2 | | | Gbps |
| BW | -3dB | $V_{RXIN} \geq 10\text{mV}$ (20mV _{PP}) | | 2.5 | | GHz |
| S_{21} | Single-Ended Gain | Linear mode | | 32 | | dB |
| $A_{V(DIFF)}$ | Differential Voltage Gain | Linear mode | | 38 | | dB |
| t_r, t_f | Output Rise/Fall Time (20% to 80%) | Limiting mode | | 60 | 120 | ps |
| LOS Frequency Range | LOS Operating Frequency Range | Note 12 | 0.622 | | 3.2 | Gbps |
| t_{OFF} | LOS De-assert Time | | | 0.1 | 0.5 | μs |
| t_{ON} | LOS Assert Time | | | 0.2 | 0.5 | μs |

Transmitter

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------|---------------------------------------|---|-----|-----|-----|-------|
| f_{MAX} | Maximum Operating Frequency | $V_{TXIN} \geq 100\text{mV}$ (200mV _{PP}) | 3.2 | | | Gbps |
| BW | -3dB | $V_{REF_CTRL} \leq V_{TXCTRL} \leq V_{CC_TXQ}$ | | 2 | | GHz |
| t_r, t_f | Output Rise/Fall Time (20% to 80%) | $V_{TXVCTRL} = V_{REF_CTRL}$ | | 100 | 160 | ps |

Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Deterministic jitter is measured with both K28.5 and $2^{23}-1$ PRBS data-pattern, measured at $<f_{MAX}$. $V_{IN} = 10\text{mV}$ (20mV_{PP}) RX, 100mV (200mV_{PP}) TX. See the "PRBS Discussion" section for more details on the K28.5 and $2^{23}-1$ PRBS data pattern.
10. Random jitter is measured with a K28.7 character pattern, measured at $<f_{MAX}$. $V_{IN} = 10\text{mV}$ (20mV_{PP}) RX, 100mV (200mV_{PP}) TX. See the "PRBS Discussion" section for more details on the K28.7 PRBS data pattern.
11. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.
12. LOS is guaranteed to be chatter-free at $f_{MAX} \geq 622\text{Mbps}$ or $f_{MAX} \geq 311\text{MHz}$ with $V_{RXIN} \geq 10\text{mV}$ (20mV_{PP}) with a 2^7-1 PRBS data pattern.
13. Contact factory for limits.

Detailed Description

Receiver

The receiver AC-coupled differential input distributes data to 3.2Gbps with signals as small as 10mV (20mV_{PP}) or as large as 900mV (1.8V_{PP}). The receiver input features an internal 50Ω input termination connected to an internal reference which optimizes the inputs for AC-coupled signals. Input signals are linearly amplified with 38dB of differential gain and the output signal is limited to 400mV (800mV_{PP}).

The receiver output buffer features 50Ω source termination resistors and a current source that provides 400mV (800mV_{PP}) swing into 50Ω termination. The output buffers terminates to standard CML loads (100Ω across the output pair or equivalent). See the "Output Stage Receiver" section for more details.

Transmitter

The transmitter differential input includes Micrel's unique, patented 3-pin input termination architecture that directly interfaces to any (AC- or DC-coupled) differential signal as small as 100mV (200mV_{PP}) without any termination resistor network in the signal path.

The transmitter output buffer terminates to standard LVPECL loads ($R_L = 50_{\Omega}$ to $V_{CC_TXQ} - 2V$). The output buffer is a special variable swing LVPECL buffer controlled by TXVCTRL. The output buffer features emitter follower output that provides 80mV (160mV_{PP}) to 800mV (1.6V_{PP}) swing into 50_Ω transmission lines. See the next section and Figures 1a and 1b for more details on how to control the variable output swing feature.

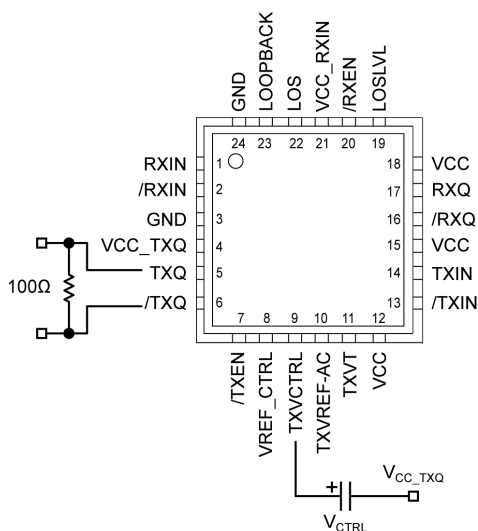


Figure 1a. Voltage Source Implementation

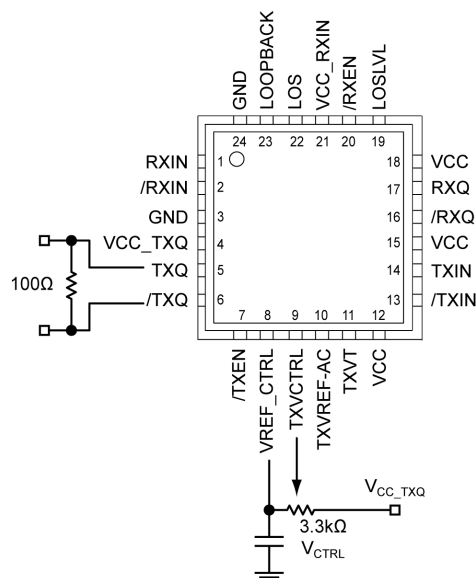


Figure 1b. Alternative Implementation

Transmitter PECL Variable-Swing Output Buffer

- Connecting V_{REF_CTRL} to TXVCTRL sets the transmitter output buffer to maximum swing
- Setting TXVCTRL to V_{CC_TXQ} , sets the transmitter output buffer to minimum swing
- Control of the transmitter output swing buffers can be obtained by using a variable resistor connected between V_{REF_CTRL} and V_{CC_TXQ} with a wiper connected to TXVCTRL as shown in Figure 1b

Receiver LOS

The SY58621L features a chatter-free Loss-of-Signal (LOS) TTL compatible output with an internal 4.75kΩ pull-up resistor. LOS circuitry monitors the input receiver signal and asserts a signal when the input signal falls below the threshold set by the programmable LOS level set pin (LOSLVL). When the amplitude of the receiver input signal falls below the threshold, LOS is asserted HIGH with a response time of ~0.2μs. LOS can be fed into /RXEN to maintain output stability by disabling the output during a Loss-of-Signal condition. Figure 2a and 2b shows the LOS connection to /RXEN. When /RXEN is HIGH, the output signal RXQ is held LOW and /RXQ is held HIGH. Typically, 2dB of LOS hysteresis is adequate to prevent the receiver output from chattering. LOS operation is optimized for data rates ≥ 622 Mbps with an input receiver amplitude of at least 10mV (20mV_{PP}). Due to the long time constant in slower data rates below 622Mbps, the SY58621L LOS function does not guarantee chatter-free operation for low amplitude signals.

LOSLVL sets the threshold of the LOS input amplitude detection. Connecting an external resistor, R_{LOSLVL} ,

between VCC and LOSLVL sets the input amplitude. LOS detection trip-point by setting up a voltage divider between VCC and V_{REF} (an internal voltage source set at $V_{CC}-1.3V$), since there is a $2.8k\Omega$ internal resistor connected between LOSLVL and V_{REF} . The input voltage range of LOSLVL ranges from V_{CC} to V_{REF} . See the “Functional Block Diagram” section and Figures 2a and 2b, to see how R_{LOSLVL} sets up a voltage divider between VCC and V_{REF} . See the “LOS Output DC Electrical Characteristics” table and “Typical Operating Characteristics” section to see how different R_{LOSLVL} values affect LOS sensitivity.

connected to VCC with a wiper connected to LOSLVL, as shown in Figure 2b

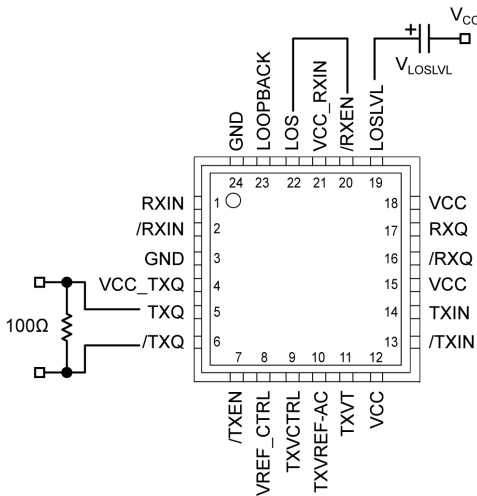


Figure 2a. Voltage Source Implementation

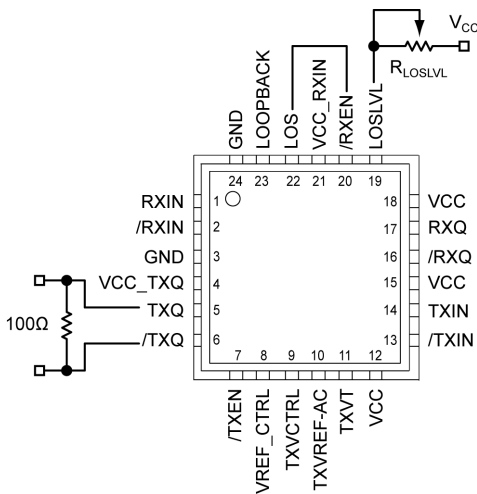


Figure 2b. Alternative Implementation

LOS Output

- Connecting the input /RXEN to the LOS output as shown in Figures 2a and 2b, maintains receiver output stability under a Loss-of-Signal condition
- Sensitivity of the LOS signal can be programmed using the LOSLVL input by using a variable resistor

- $\geq 2\text{dB}$ hysteresis is insured if $R_{\text{LOSLVL}} \leq 10\text{k}\Omega$
- LOS is guaranteed chatter-free at $f \geq 622\text{Mbps}$ (311MHz)

Hysteresis

The SY58621L provides a minimum of 2dB of LOS hysteresis, see the Figure 3 for more details.

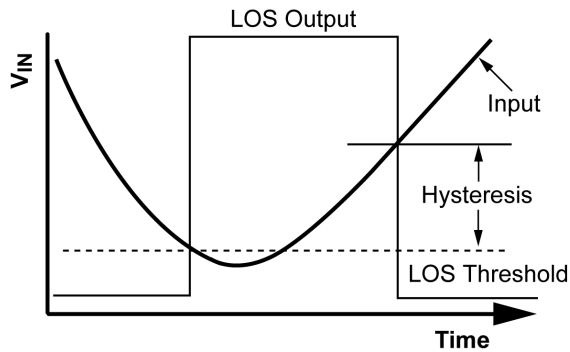


Figure 3. LOS Hysteresis Assert/De-assert

Hysteresis is defined as: $20\text{Log}_{10}\left(\frac{SD_AssertVoltage}{SD_De-assertVoltage}\right)dB$.

Loopback

To support diagnostic system testing, the SY58621L features a loopback test mode, activated by setting LOOPBACK to logic HIGH. Loopback mode enables an internal loopback path from the transmitter input to the receiver output and supports the full 3.2Gbps data rate throughput.

Crosstalk

The SY58621L features a patent-pending isolation between the receiver and transmitter channels. The following guide lines can be used to minimize on layout induced crosstalk:

1. Ground Stripping

Ground stripping is an effective method to reduce crosstalk. Ground stripping involves running a ground trace between the receiver and transmitter channels.

2. Vertical and Horizontal Traces

Another way to reduce crosstalk is to route the receiver and transmitter channels on separate layers with an embedded ground or power supply layer between the layers. When routing the traces on different layers, run the receiver traces horizontal to the transmitter traces and route the transmitter traces vertical to the receiver traces.

PRBS Discussion

LOS Testing

The LOS function is tested with a 2^7-1 PRBS (Pseudo Random Bit Stream) data-pattern. A PRBS data-pattern of 2^7-1 is used because it is a good approximation to an 8b10b-encoded NRZ data stream. 8b10b encodes 8 bits of data and replaces it with 10 bits of symbol. The extra bits are added to improve transition density and the BER (Bit Error Rate) of the system.

Deterministic Jitter Testing and the K28.5 Pattern

The K28.5 (11000001010011111010) and $2^{23}-1$ PRBS data-patterns are used to characterize DJ because both data patterns have lower spectral frequency content which provides a best approximation to scrambled NRZ data streams.

Random Jitter Testing and the K28.7 Pattern

The K28.7 (1111100000...) data pattern is used to measure RJ since the pattern is free of DJ. In addition, because the K28.7 data-pattern can be used to compare the T_N (N^{TH} period) to the T_0 (1st period), low frequency jitter components can be accumulated.

Power Supply Filtering

Although the SY58621L is fully differential, it is recommended that the power supplies are filtered as shown in Figure 4.

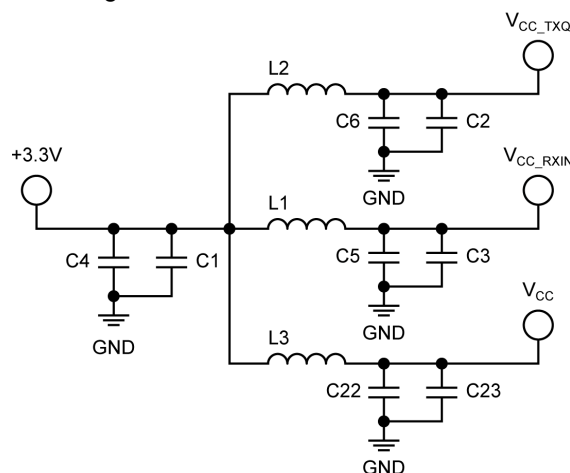


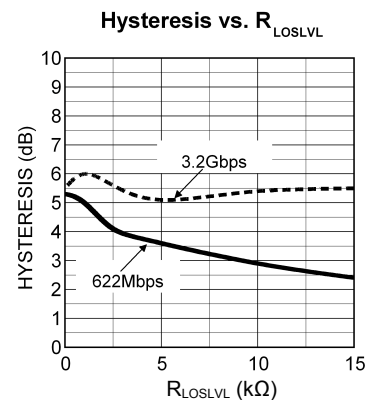
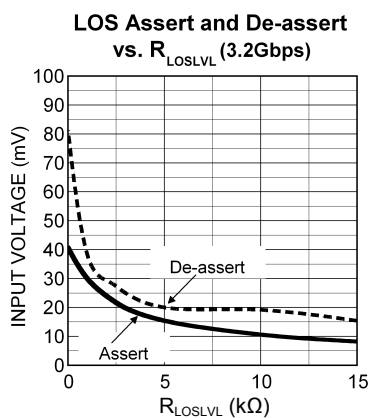
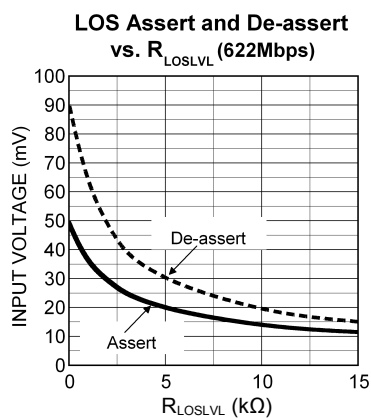
Figure 4. Power Supply Filtering Scheme

| Item | Description |
|-----------------|-----------------------------|
| C1, C2, C3, C23 | 0.1μF Capacitor |
| C4, C5, C6, C22 | 0.01μF Capacitor |
| L1, L2, L3 | 1.2μH Ferrite Bead Inductor |

Table 1. Bill of Materials

Typical Operating Characteristics

$V_{CC} = V_{CC_TXQ} = V_{CC_RXIN} = 3.3V \pm 10\%$, Receiver: $R_L = 100\Omega$ across the outputs. Transmitter: $R_L = 50\Omega$ to V_{CC_TXQ} $-2V$; $T_A = 25^\circ C$, unless otherwise stated.



Single-Ended and Differential Swings



Figure 5a. Single-Ended Voltage Swing

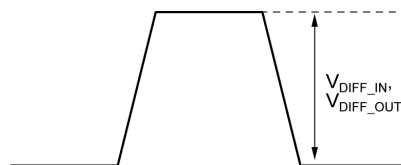


Figure 5b. Differential Voltage Swing

Input Stage

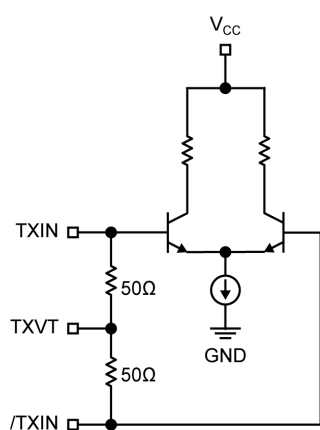


Figure 6a. TX Simplified Differential Input Stage

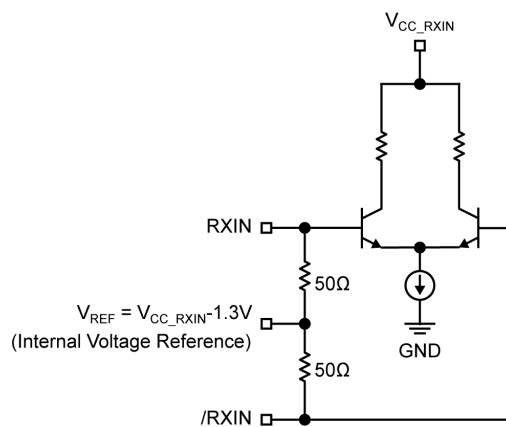
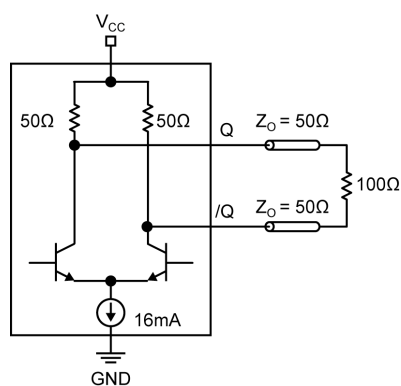


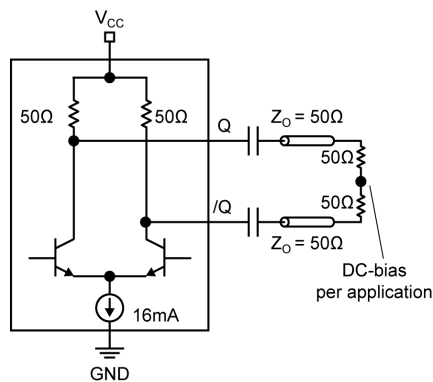
Figure 6b. RX Simplified Differential Input Stage

Output Stage

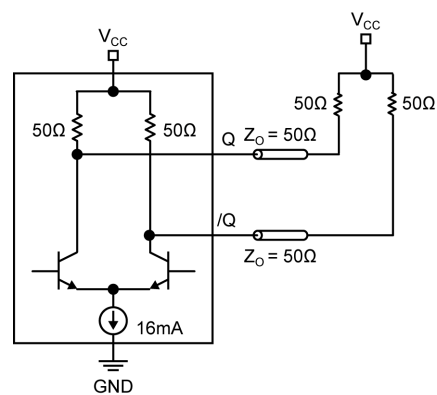
Receiver



**Figure 7a. Receiver CML
DC-Coupled Output**



**Figure 7b. Receiver CML
AC-Coupled Output**



**Figure 7c. Receiver CML
DC-Coupled Output (50Ω to V_{CC})**

Transmitter

The transmitters output is a variable swing LVPECL open emitter driver. LVPECL has very low output (open emitter) impedance, and small signal swing which result in low EMI.

LVPECL is ideal for driving 50Ω and 100Ω-controlled impedance transmission lines. There are several techniques for terminating the LVPECL output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-Resistor), and AC-Coupled Termination. Unused output pairs may be left floating. However, the unused half of a single-ended output must be terminated, or balanced.

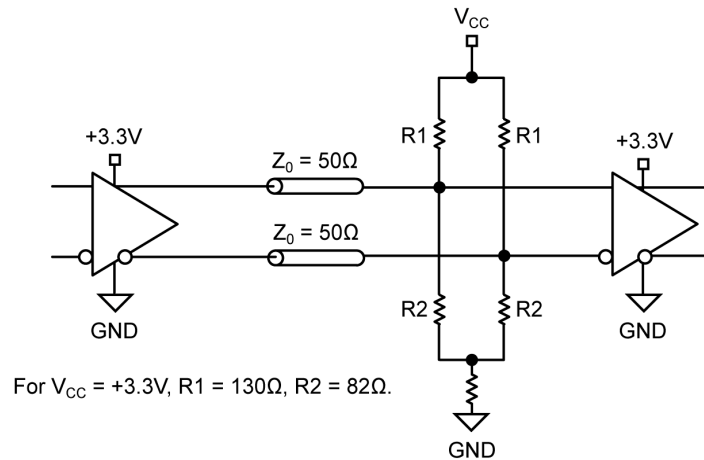


Figure 8a. Parallel Thevenin-Equivalent Termination

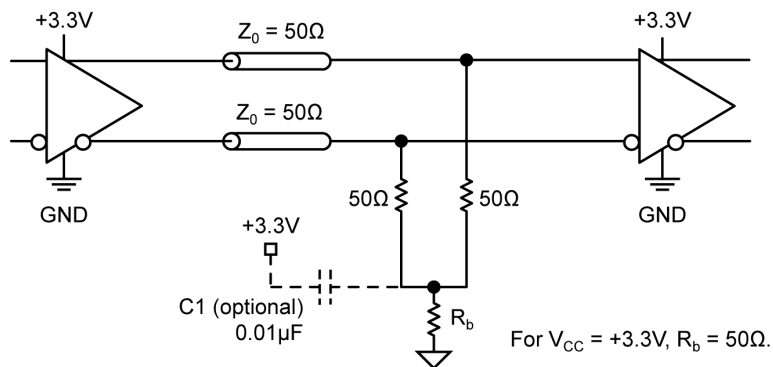


Figure 8b. Parallel Termination – 3-Resistors

Figure 9a. LVPECL Interface (TX DC-Coupled/RX AC-Coupled)

Figure 9a shows the LVPECL interface configuration. The transmitter (TX) is DC-coupled, and the receiver (RX) is AC-coupled. The TXIN and /TXIN pins are connected to the LVPECL driver output. The TXVT pin is connected to the TXVREF-AC pin. The TXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The TXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The RXIN and /RXIN pins are connected to the LVPECL receiver input. The RXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The RXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The power supply V_{CC} is connected to the V_{CC} pin, and GND is connected to the GND pin. The input signal V_{IN} is connected to the TXIN pin, with V_{IN} ≥ 10mV (20mV_{pp}).

Figure 9b. LVPECL Interface (TX AC-Coupled/RX AC-Coupled)

Figure 9b shows the LVPECL interface configuration with both TX and RX AC-coupled. The TXIN and /TXIN pins are connected to the LVPECL driver output. The TXVT pin is connected to the TXVREF-AC pin. The TXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The TXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The RXIN and /RXIN pins are connected to the LVPECL receiver input. The RXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The RXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The power supply V_{CC} is connected to the V_{CC} pin, and GND is connected to the GND pin. The input signal V_{IN} is connected to the TXIN pin, with V_{IN} ≥ 10mV (20mV_{pp}).

Figure 9c. CML Interface (TX DC-Coupled/RX AC-Coupled)

Figure 9c shows the CML interface configuration. The transmitter (TX) is DC-coupled, and the receiver (RX) is AC-coupled. The TXIN and /TXIN pins are connected to the CML driver output. The TXVT pin is connected to the TXVREF-AC pin. The TXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The TXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The RXIN and /RXIN pins are connected to the CML receiver input. The RXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The RXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The power supply V_{CC} is connected to the V_{CC} pin, and GND is connected to the GND pin. The input signal V_{IN} is connected to the TXIN pin, with V_{IN} ≥ 10mV (20mV_{pp}).

Figure 9d. CML Interface (TX AC-Coupled/RX AC-Coupled)

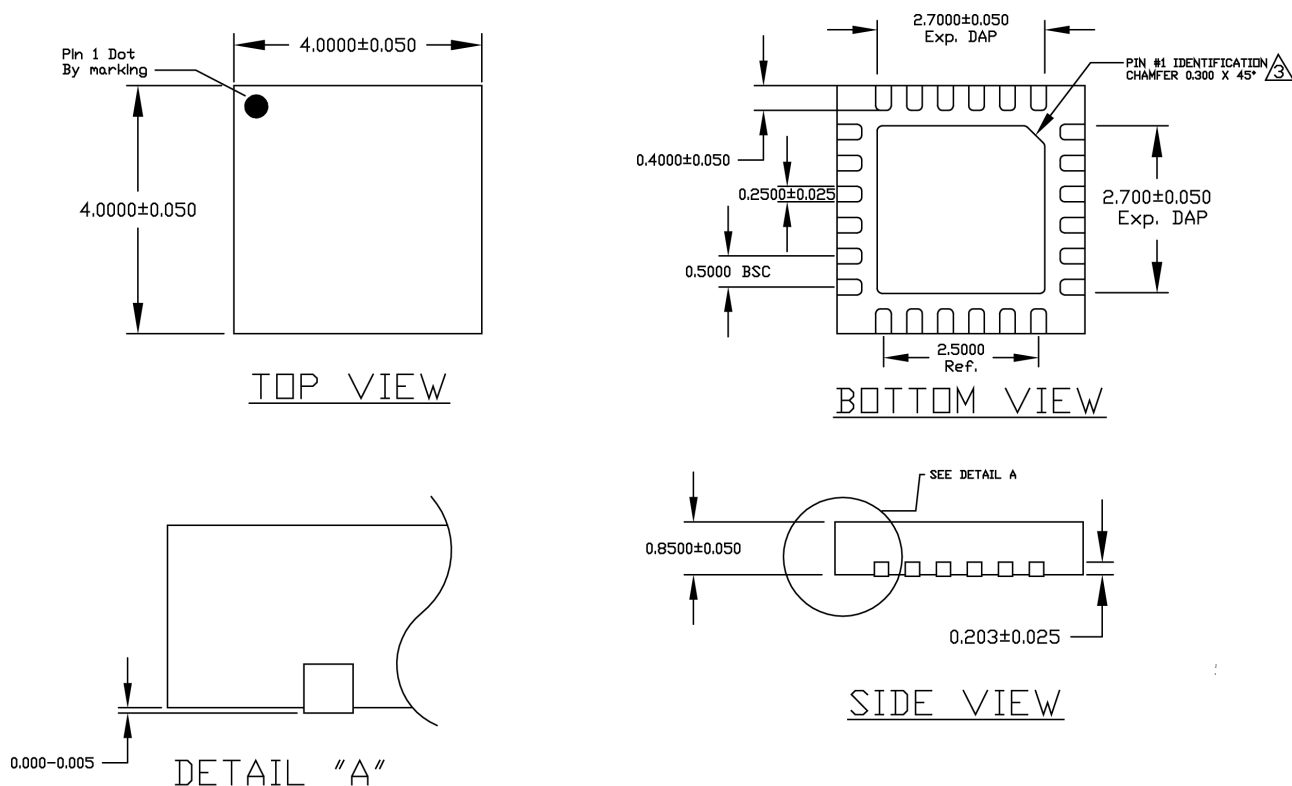
Figure 9d shows the CML interface configuration with both TX and RX AC-coupled. The TXIN and /TXIN pins are connected to the CML driver output. The TXVT pin is connected to the TXVREF-AC pin. The TXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The TXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The RXIN and /RXIN pins are connected to the CML receiver input. The RXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The RXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The power supply V_{CC} is connected to the V_{CC} pin, and GND is connected to the GND pin. The input signal V_{IN} is connected to the TXIN pin, with V_{IN} ≥ 10mV (20mV_{pp}).

Figure 9e. LVDS Interface (TX DC-Coupled/RX AC-Coupled)

Figure 9e shows the LVDS interface configuration. The transmitter (TX) is DC-coupled, and the receiver (RX) is AC-coupled. The TXIN and /TXIN pins are connected to the LVDS driver output. The TXVT pin is connected to the TXVREF-AC pin. The TXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The TXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The RXIN and /RXIN pins are connected to the LVDS receiver input. The RXVREF-AC pin is connected to a 0.01 μF capacitor to ground. The RXVREF-DC pin is connected to a 0.01 μF capacitor to ground. The power supply V_{CC} is connected to the V_{CC} pin, and GND is connected to the GND pin. The input signal V_{IN} is connected to the TXIN pin, with V_{IN} ≥ 10mV (20mV_{pp}).

| Part Number | Function | Data Sheet Link |
|---------------|---|--|
| SY58620L | Precision 4.25Gbps CML Transceiver with Integrated Loopback | www.micrel.com/product-info/products/sy58620l.shtml |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

Package Information



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin QFN

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