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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	49	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	31	A
$I_{DM}^{(1)}$	Drain current (pulsed)	196	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	358	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 49$ A, $di/dt = 400$ A/ μs , peak $V_{DS} < V_{(BR)DSS}$, $V_{DD} = 400$ V
3. $V_{DS} \leq 520$ V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$R_{thj-case}$	Thermal resistance junction-case max	0.35	$^\circ\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50$ V)	1300	mJ

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650 \text{ V}$ $V_{DS} = 650 \text{ V}$, $T_C = 125^\circ\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			± 10	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2	3	4	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$, $I_D = 24.5 \text{ A}$		0.049	0.062	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$	-	3900	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{rss}	Reverse transfer capacitance		-	2.8	-	pF
$C_{o(\text{er})}^{(1)}$	Equivalent Output Capacitance	$V_{GS} = 0$, $V_{DS} = 0$ to 520 V	-	838	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz}$ open drain	-	4.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 520 \text{ V}$, $I_D = 49 \text{ A}$, $V_{GS} = 10 \text{ V}$, (see Figure 15)	-	93	-	nC
Q_{gs}	Gate-source charge		-	16	-	nC
Q_{gd}	Gate-drain charge		-	40	-	nC

1. C_{oss} eq. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

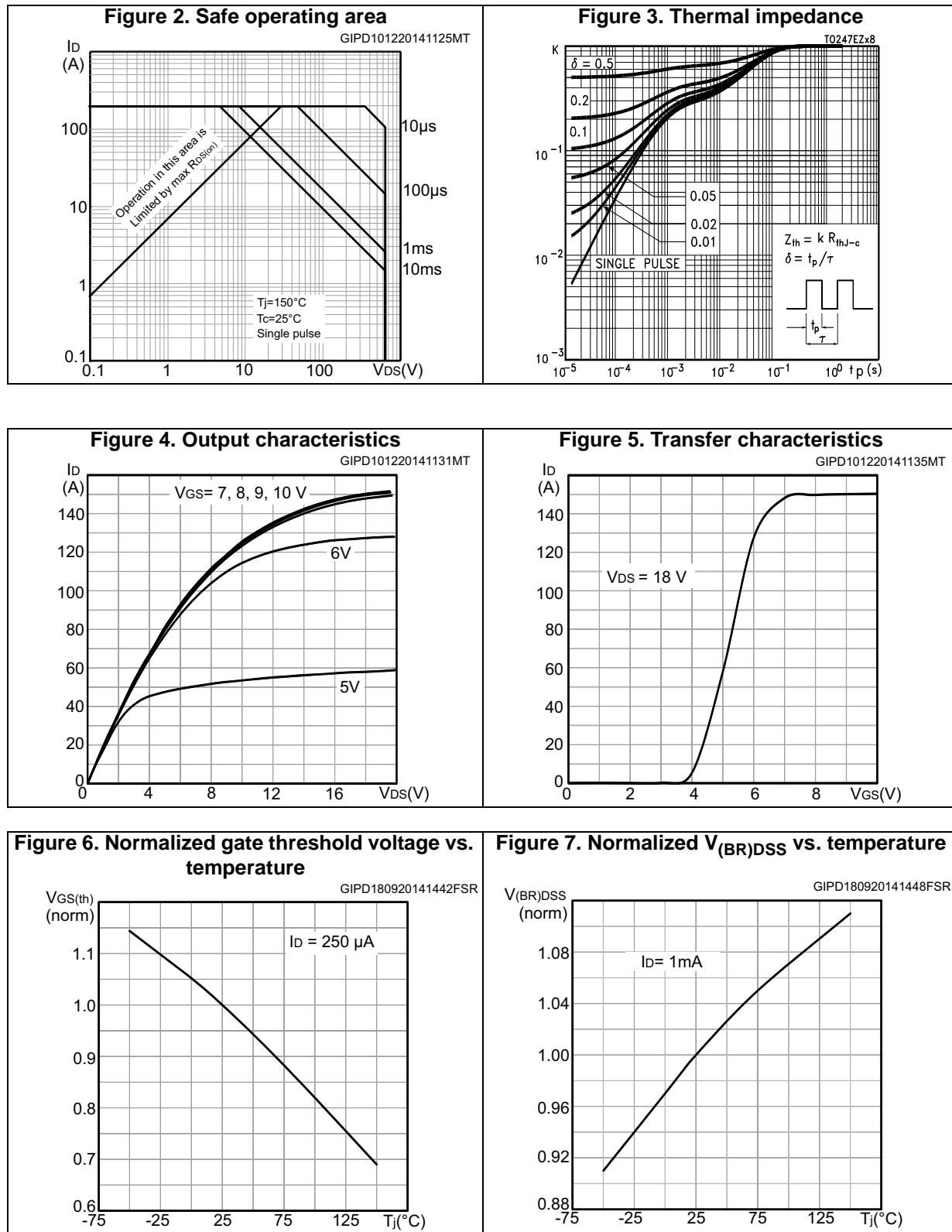
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 \text{ V}$, $I_D = 24.5 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 16 and Figure 19)	-	19	-	ns
t_r	Rise time		-	27.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	146	-	ns
t_f	Fall time		-	13	-	ns

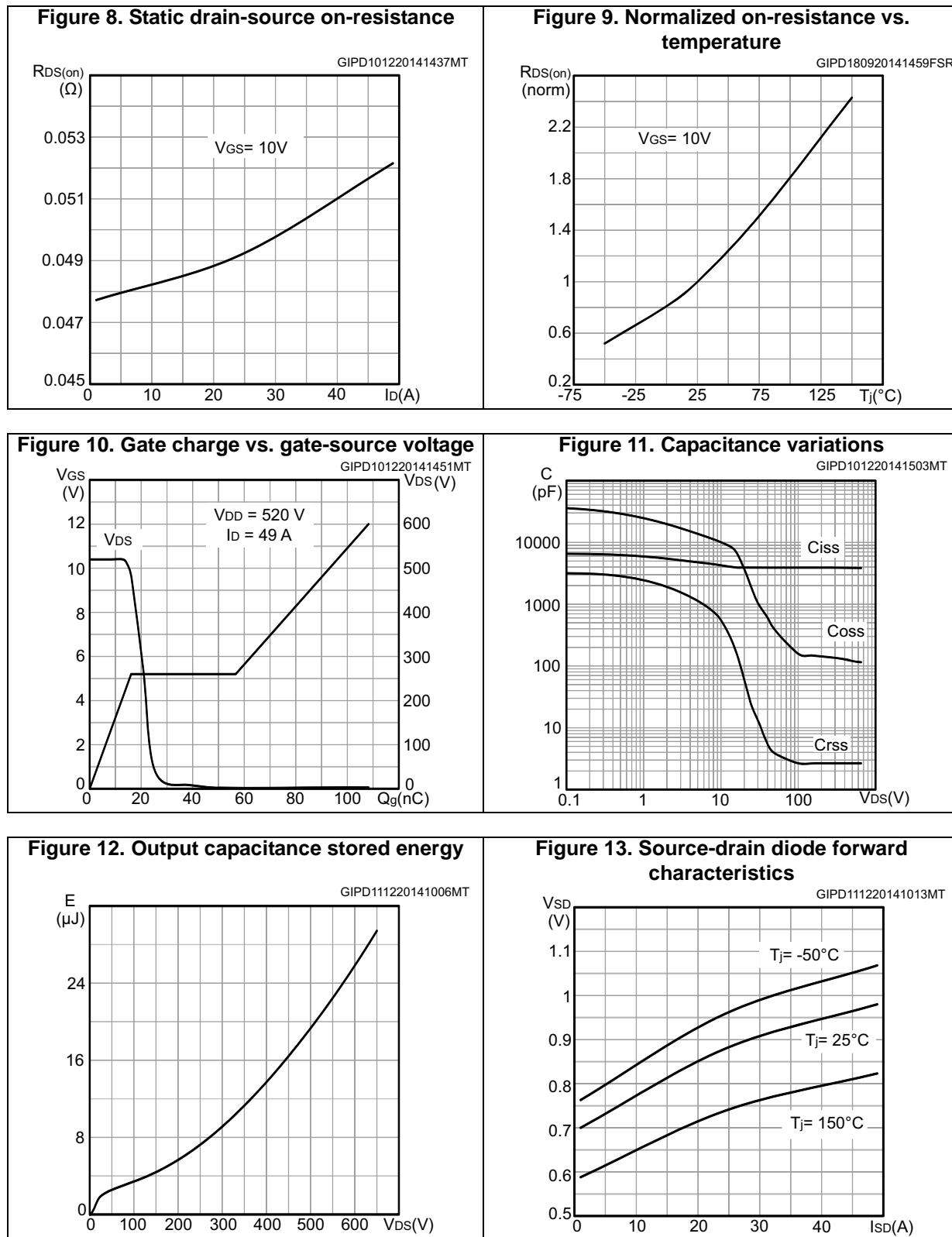
Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		49	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		196	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 49 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 49 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 16)	-	554		ns
Q_{rr}	Reverse recovery charge		-	13.5		μC
I_{RRM}	Reverse recovery current		-	49.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 49 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 19)	-	688		ns
Q_{rr}	Reverse recovery charge		-	18		μC
I_{RRM}	Reverse recovery current		-	52		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

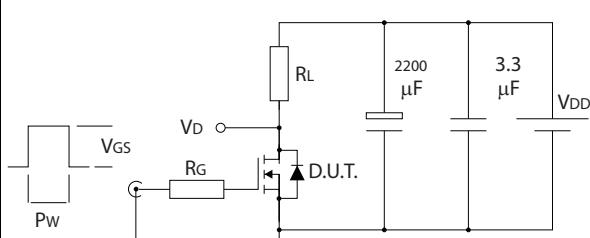
2.1 Electrical characteristics (curves)





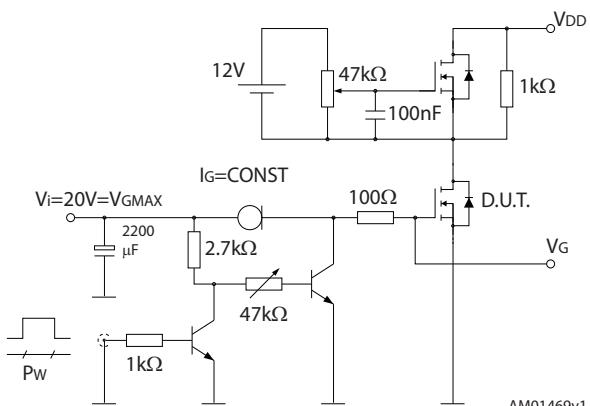
3 Test circuits

Figure 14. Switching times test circuit for resistive load



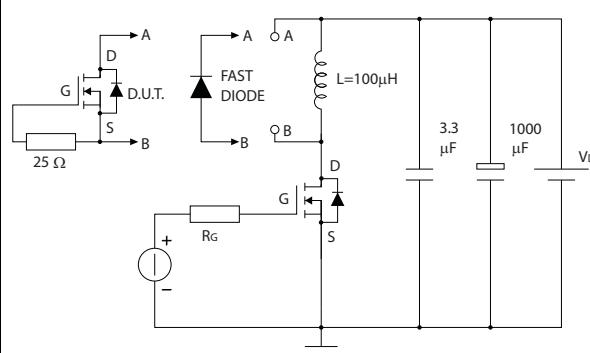
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Figure 15. Gate charge test circuit



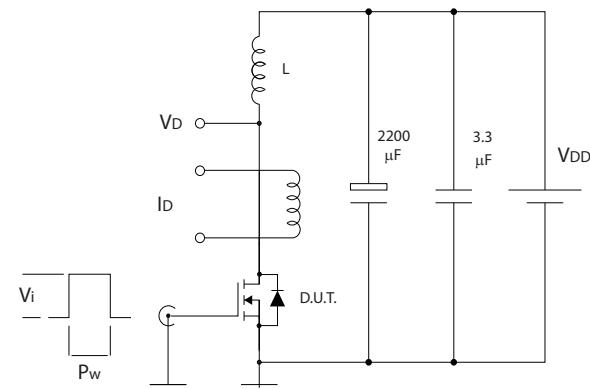
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Figure 16. Test circuit for inductive load switching and diode recovery times



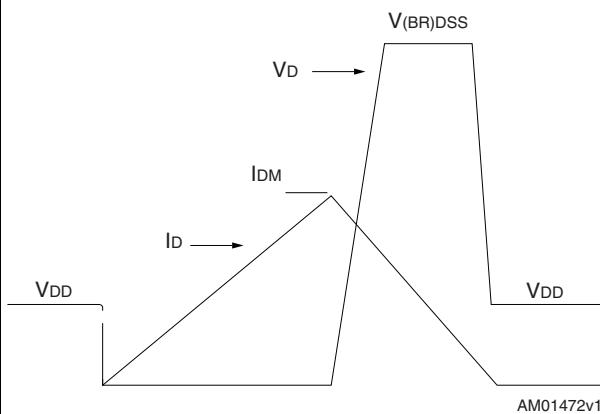
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Figure 17. Unclamped inductive load test circuit



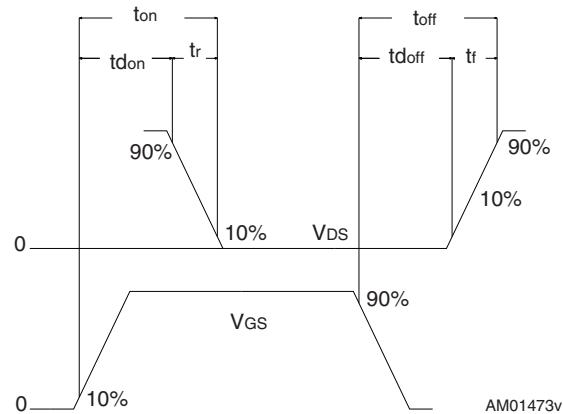
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Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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4.1 TO-247, STW56N65M2

Figure 20. TO-247 drawing

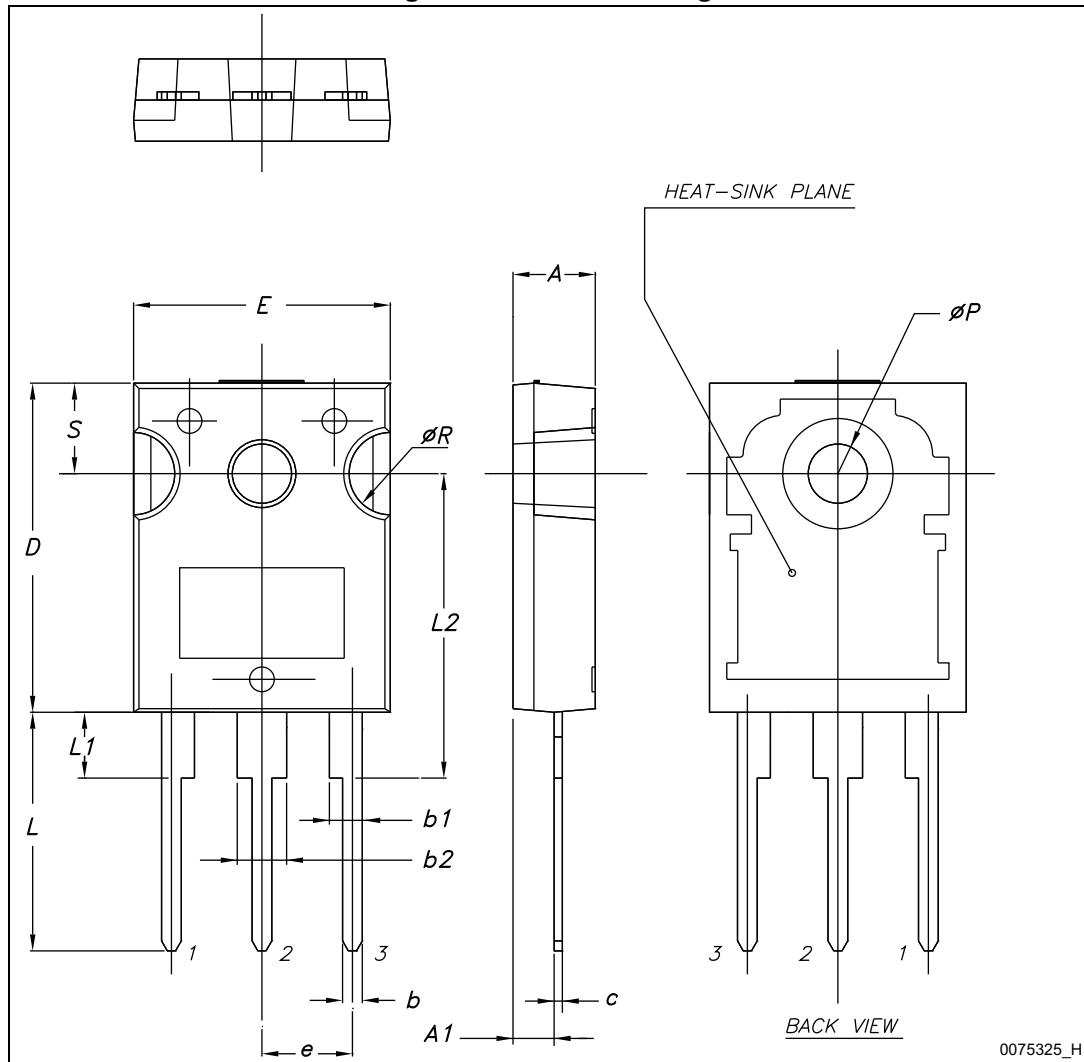


Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Dec-2014	1	Initial release.

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