## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{CC}$ ..... 7V
BST ..... 13.2V
BST-SWN ..... 7V
SWN ..... -1V to 7V
GH ..... -0.3V to BST +0.3V
GH-SWN ..... 7V
All Other Pins ..... -0.3V to $V_{CC}$ +0.3V

Peak Output Current < 10µs
GH, GL ..... 2A

Operating Temperature Range
SP6120C ..... 0°C to +70°C
SP6120E ..... -40°C to +85°C
Junction Temperature, $T_J$ ..... +125°C
Storage Temperature Range ..... -65°C to +150°C
Power Dissipation
Lead Temperature (soldering 10 sec) ..... +300°C
ESD Rating ..... 2kV HBM

## ELECTRICAL CHARACTERISTICS

Unless otherwise specified: 3.0V < $V_{CC}$ <5.5V, 3.0V < BST < 13.2V, $R_{OSC}$ = 18.7kΩ, $C_{COMP}$ = 0.1µF, $C_{SS}$ = 0.1µF, ENABLE = 3V, CGH = CGL = 3.3nF, $V_{FB}$ = 1.25V, ISP = ISN = 1.25V, SWN = GND = PGND = 0V, -40°C < $T_{AMB}$ <85°C (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **QUIESCENT CURRENT** | | | | | |
| $V_{CC}$ Supply Current | No Switching | - | 0.95 | 1.8 | mA |
| $V_{CC}$ Supply Current (Disabled) | ENABLE = 0V | - | 5 | 20 | µA |
| BST Supply Current | No Switching, $V_{BST}$ = $V_{CC}$<br>No Switching, $V_{CC}$ = 5V, $V_{BST}$ = 10V | -<br>- | 1<br>100 | 20<br>150 | µA<br>µA |
| **ERROR AMPLIFIER** | | | | | |
| Error Amplifier Transconductance | | | 600 | | µs |
| COMP Sink Current | $V_{FB}$ = 1.35V, COMP = 0.5V, No Faults | 15 | 35 | 65 | µA |
| COMP Source Current | $V_{FB}$ = 1.15V, COMP = 1.6V | 15 | 35 | 65 | µA |
| COMP Output Impedence | | | 3 | | MΩ |
| $V_{FB}$ Input Bias Current | | - | 60 | 100 | nA |
| **REFERENCE** | | | | | |
| Error Amplifier Reference | Trimmed with Error Amp in Unity Gain | 1.238 | 1.250 | 1.262 | V |
| $V_{FB}$ 3% Low Comparator | | | 3 | | %$V_{REF}$ |
| $V_{FB}$ 3% High Comparator | | | 3 | | %$V_{REF}$ |
| **OSCILLATOR & DELAY PATH** | | | | | |
| Oscillator Frequency | | 270 | 300 | 330 | kHz |
| Oscillator Frequency #2 | $R_{OSC}$ = 10.2kΩ | 450 | 500 | 550 | kHz |
| Duty Ratio | Loop In Control -100% DC possible | | 95 | | % |
| $R_{OSC}$ Voltage | Information Only - Moves with Oscillator Trim | | 0.65 | | V |
| Minimum GH Pulse Width | $V_{CC}$ > 4.5V, Ramp up COMP Voltage > 0.6V until GH starts Switching | | 120 | 250 | ns |

## ELECTRICAL CHARACTERISTICS

Unless otherwise specified: 3.0V < $V_{CC}$ <5.5V, 3.0V < BST < 13.2V, $R_{OSC}$ = 18.7kΩ, $C_{COMP}$ = 0.1μF, $C_{SS}$ = 0.1μF, ENABLE = 3V, CGH = CGL = 3.3nF, $V_{FB}$ = 1.25V, ISP = ISN = 1.25V, SWN = GND = PGND = 0V, -40°C < $T_{AMB}$ <85°C (Note 1)

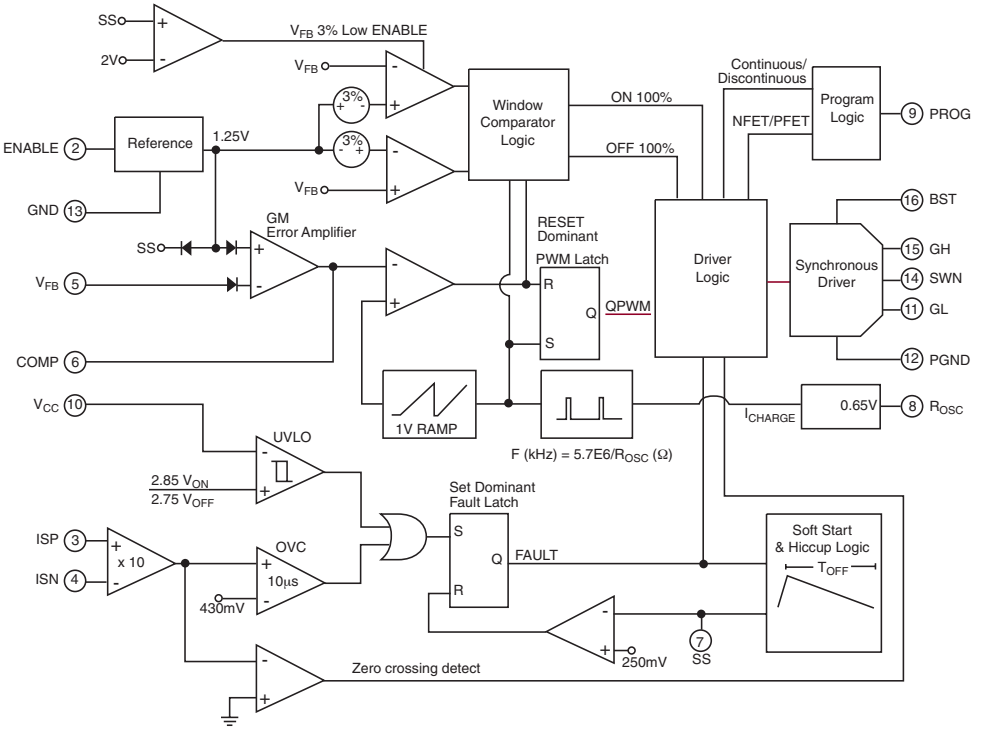
| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **SOFTSTART** | | | | | |
| SS Charge Current | $V_{SS}$ = 1.5V | 25 | 50 | 70 | μA |
| SS Discharge Current | $V_{SS}$ = 1.5V | 2 | 5 | 7 | μA |
| COMP Discharge Current | $V_{COMP}$ = 0.5V, Fault Initiated | 200 | 500 | - | μA |
| COMP Clamp Voltage | $V_{FB}$ < 1.0V, VSS = 2.5V | 2.0 | 2.4 | 2.8 | V |
| SS Ok Threshold | | 1.7 | 2.0 | 2.2 | V |
| SS Fault Reset | | 0.2 | 0.25 | 0.3 | V |
| SS Clamp Voltage | | 2.0 | 2.4 | 2.8 | V |
| **OVER CURRENT & ZERO CURRENT COMPARATORS** | | | | | |
| Over Current Comparator Threshold Voltage | Rail to Rail Common Mode Input | 32 | 43 | 54 | mV |
| ISN, ISP Input Bias Current | | - | 60 | 250 | nA |
| Zero Current Comparator Threshold | VISP - VISN | | 2 | | mV |
| **UVLO** | | | | | |
| $V_{CC}$ Start Threshold | | 2.75 | 2.85 | 2.95 | V |
| $V_{CC}$ Stop Threshold | | 2.65 | 2.75 | 2.9 | V |
| **ENABLE** | | | | | |
| Enable Threshold | ON<br>OFF | <br>0.65 | | 1.45 | <br>V |
| Enable Pin Source Current | | 0.6 | 4 | 9 | μA |
| **GATE DRIVER** | | | | | |
| GH Rise Time | $V_{CC}$ > 4.5V | - | 40 | 110 | ns |
| GH Fall Time | $V_{CC}$ > 4.5V | - | 40 | 110 | ns |
| GL Rise Time | $V_{CC}$ > 4.5V | - | 40 | 110 | ns |
| GL Fall Time | $V_{CC}$ > 4.5V | - | 40 | 110 | ns |
| GH to GL Non-Overlap Time | $V_{CC}$ > 4.5V | 0 | 60 | 140 | ns |
| GL to GH Non-Overlap Time | $V_{CC}$ > 4.5V | 0 | 60 | 140 | ns |
| $V_{BST}$ OK Threshold | $V_{CC}$ = 3.0V, FB=1.15V, Search GL High<br>$V_{CC}$ = 5.5V, FB=1.15V, Search GL High | 4.0<br>7.3 | 4.8<br>7.8 | 5.0<br>8.3 | V<br>V |
| Forced GL ON | $V_{BST}$ < $V_{BST}$ OK Threshold, FB =1.15V | 200 | 350 | 650 | ns |

**Note 1:** Specifications to -40°C are guaranteed by design, characterization and correlation with statistical process control.

## PIN DESCRIPTION

| NAME | FUNCTION | PIN NUMBER |
|---|---|---|
| 1 | N/C | No Connection |
| 2 | ENABLE | TTL compatible input with internal 4uA pullup. Floating or Venable> 1.5V will enable the part, Venable < 0.65V disables part. |
| 3 | ISP | Current Sense Positive Input: Rail to Rail Input for Over-Current Detection, 43mV threshold with 10μs (typ) response time. |
| 4 | ISN | Current Sense Negative Input: Rail to Rail input for Over-Current Detection. |
| 5 | $V_{FB}$ | Feedback Voltage Pin: Inverting input of the error amplifier and serves as the output voltage feedback point for the buck converter. The output voltage is sensed and can be adjusted through an external resistor divider. |
| 6 | COMP | Error Amplifier Compensation Pin: A lead lag network is typically connected to this pin to compensate the feedback loop. This pin is clamped by the SS voltage and is limited to 2.8V maximum. |
| 7 | SS | Soft Start Programming Pin: This pin sources 50μA on start-up. A 0.01μF to 1μF capacitor on this pin is typically enough capacitance to soft start a power supply. In addition, hiccup mode timing is controlled by this pin through the 5μA discharge current. The SS voltage is clamped to 2.7V maximum. |
| 8 | $R_{OSC}$ | Frequency Programming Pin: A resistor to ground is used to program frequency. Typical values - 18,700Ω, 300kHz; 10,200Ω, 500kHz. |
| 9 | PROG | Programming Pin:<br>PROG = GND; MODE = NFET/CONTINOUS<br>PROG = 68kΩ to GND; MODE = NFET/DISCONTINOUS<br>PROG = VCC; MODE = PFET/CONTINOUS<br>PROG = 68kΩ to VCC; MODE = PFET/DISCONTINOUS |
| 10 | $V_{CC}$ | I.C. Supply Pin: ESD structures also hooked to this pin. Properly bypass this pin to PGND with a low ESL/ESR ceramic capacitor. |
| 11 | GL | Synchronous FET Driver: 1nF/20ns typical drive capability. |
| 12 | PGND | Power Ground Pin: Used for Power Stage. Connect Directly to GND at I.C. pins for optimal performance. |
| 13 | GND | Ground Pin: Main ground pin for I.C. |
| 14 | SWN | Switch Node Reference: High side MOSFET driver reference. Can also be tied to GND for low voltage applications. |
| 15 | GH | HIgh Side MOSFET Driver: Can be NFET or PFET depending on Program Mode. 1nF/20ns typical drive capability. Maximum voltage rating is referenced to SWN. |
| 16 | BST | High Side Driver Supply Pin. When $V_{BST}$ is less than $V_{BST}$ OK Threshold, GL is forced to turn on for at least 300ns. This is intended for enough time to charge the BST capacitor. |

## BLOCK DIAGRAM




## APPLICATION SCHEMATIC

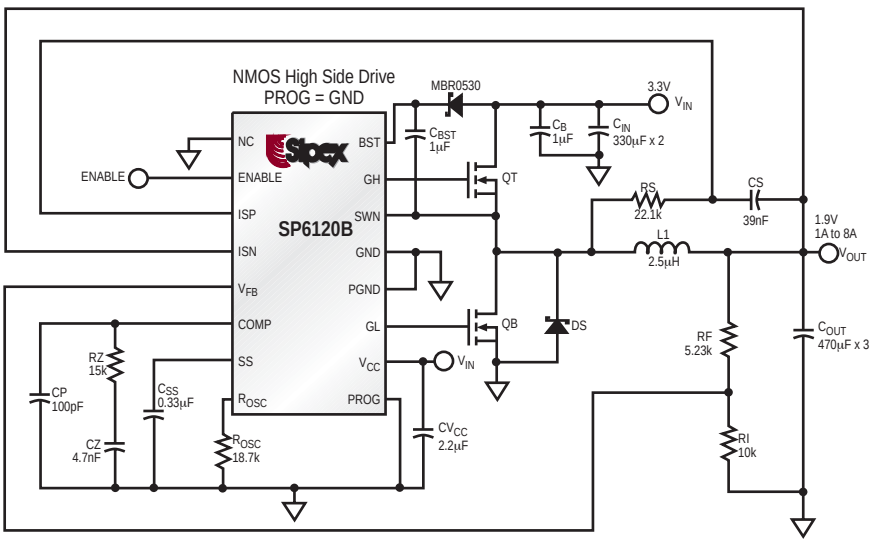



*Figure 1. Schematic 3.3V to 1.9V Power Supply*

QT, QB = FAIRCHILD FDS6690A
L1 = PANASONIC ETQP6F2R5SFA
DS = STMICROELECTRONICS STPS2L25U

$C_{IN}$ = SANYO 6TPB330M
$C_{OUT}$ = SANYO 4TPB470M

## Typical Performance Characteristics

Refer to circuit in Figure 1 with $V_{IN}$ = 3.3V; $V_{OUT}$ = 1.9V, $R_{OSC}$ = 18.7kΩ, and $T_{AMB}$ = +25°C unless otherwise noted.

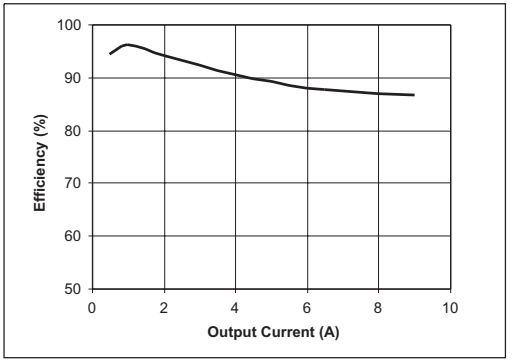



*Figure 2. Efficiency vs. Output Current*

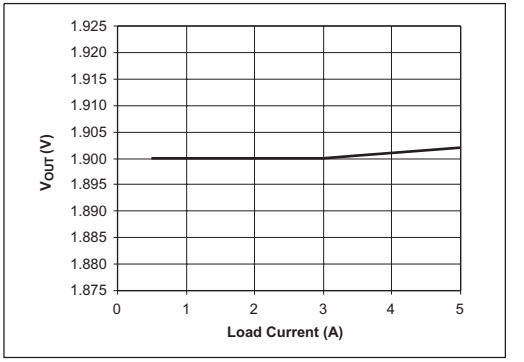



*Figure 3. Load Regulation*

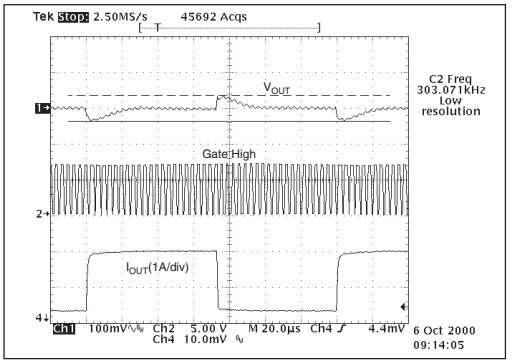



*Figure 4. Load Step Response: 0.4A to 2A*

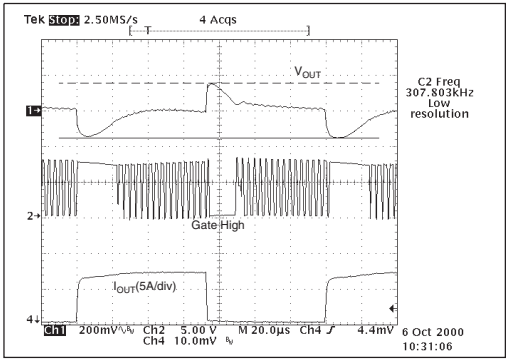



*Figure 5. Load Step Response: 0.4A to 7A*

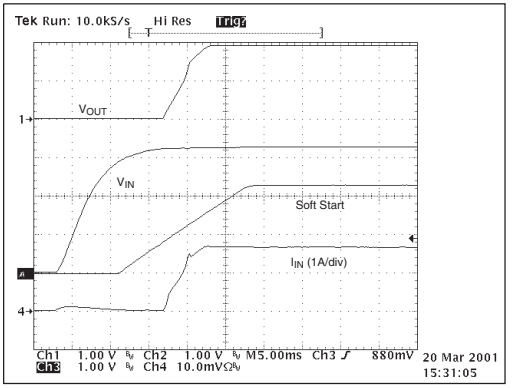



*Figure 6. Start-Up Response: 5A Load*

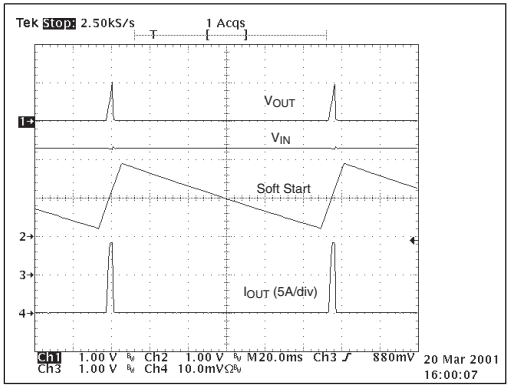



*Figure 7. Overcurrent: 9A Load*

## Typical Performance Characteristics

Unless otherwise specified: $V_{CC}$ = BST = ENABLE = 3.3V, $R_{OSC}$ = 18.7kΩ, $C_{COMP}$ = 0.1µF, $C_{SS}$ = 0.1µF, CGH = CGL = 3.3nF, $V_{FB}$ = 1.25V, ISP = ISN = 1.25V, SWN = GND = PGND = 0V, $T_{AMB}$ = 25°C.

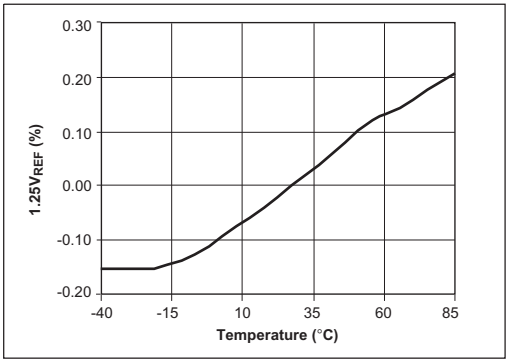



*Figure 8. Error Amplifier Reference vs. Temperature*

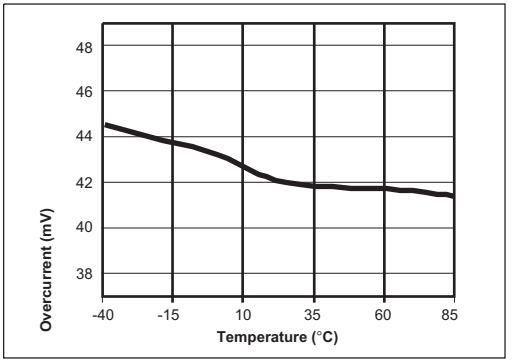



*Figure 9. Overcurrent Comparator Threshold Voltage vs. Temperature*

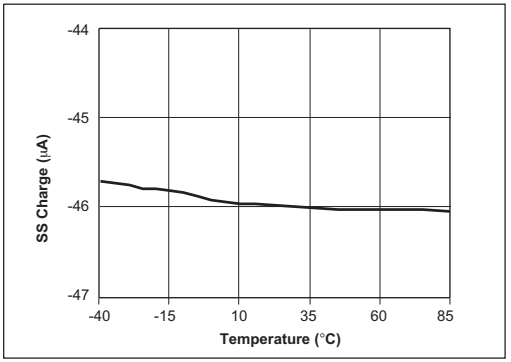



*Figure 10. SS Charge Current vs. Temperature with $V_{SS}$ = 1.5V*

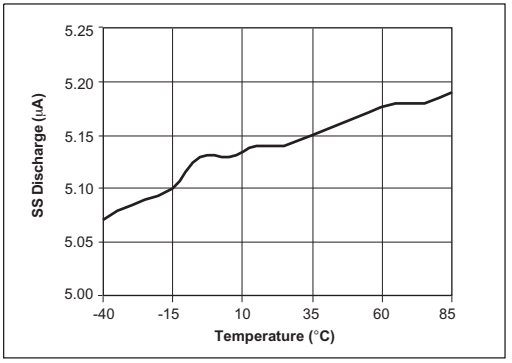



*Figure 11. SS Discharge Current vs. Temperature with $V_{SS}$ = 1.5V*

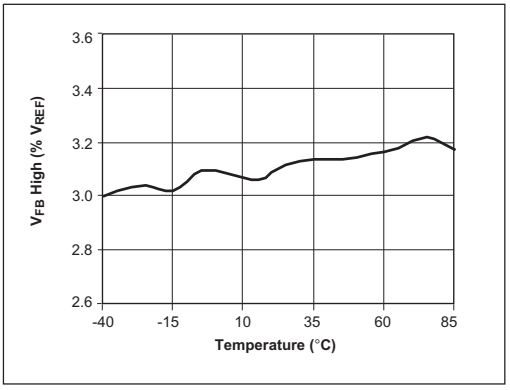



*Figure 12. $V_{FB}$ 3% High Comparator vs. Temperature*

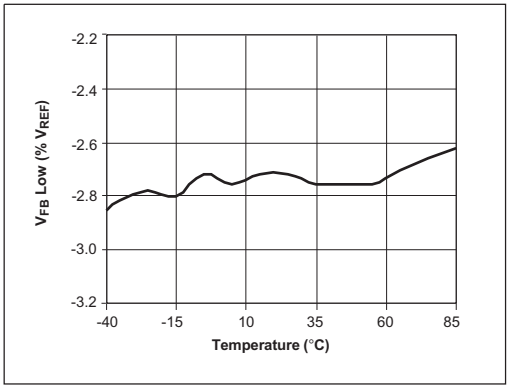



*Figure 13. $V_{FB}$ 3% Low Comparator vs. Temperature*

## Typical Performance Characteristics

Unless otherwise specified: $V_{CC}$ = BST = ENABLE = 3.3V, $R_{OSC}$ = 18.7k, $C_{COMP}$ = 0.1µF, $C_{SS}$ = 0.1µF, CGH = CGL = 3.3nF, $V_{FB}$ = 1.25V, ISP = ISN = 1.25V, SWN = GND = PGND = 0V, $T_{AMB}$ = 25°C.

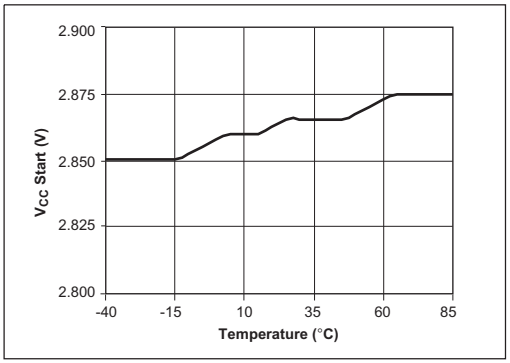



*Figure 14. $V_{CC}$ Start Threshold vs. Temperature*

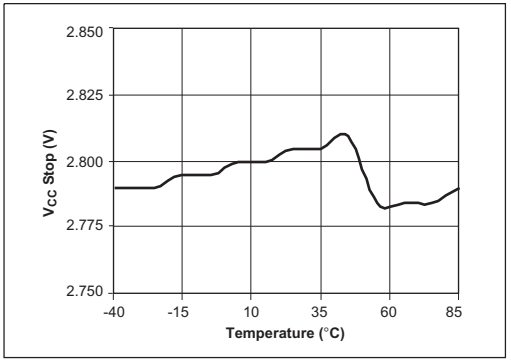



*Figure 15. $V_{CC}$ Stop Threshold vs. Temperature*

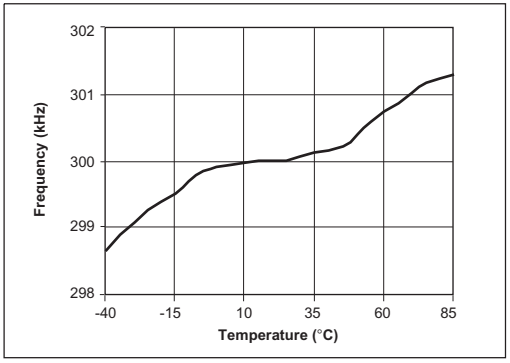



*Figure 16. Oscillator Frequency vs. Temperature*

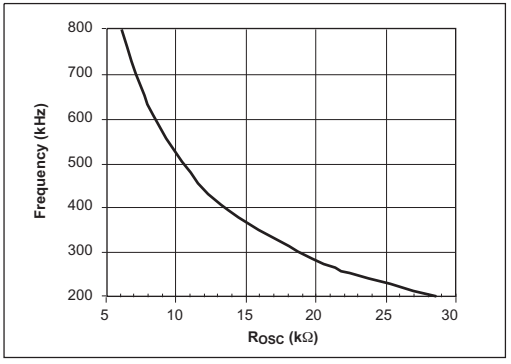



*Figure 17. Oscillator Frequency vs. $R_{OSC}$ with $V_{CC}$ = 5V and CGH = CGL = Open.*

## THEORY OF OPERATION

### General Overview

The SP6120B is a constant frequency, voltage mode PWM controller for low voltage, DC/DC step down converters. It has a main loop where an external resistor ($R_{OSC}$) sets the frequency and the driver is controlled by the comparison of an error amp output (COMP) and a 1V ramp signal. The error amp has a transconductance of 600µS, an output impedance of 3 MΩ, an internal pole at 2 MHz and a 1.25V reference input. Although the main control loop is capable of 0% and 100% duty cycle, its response time is limited by the external component selection. Therefore, a secondary loop, including a window comparator positioned 3% above and below the reference, has been added to insure fast response to line and load transients. A unique "Ripple & Frequency Independent" algorithm, added to the secondary loop, insures that the window comparator does not interfere with the main loop during normal operation. In addition to receiving driver commands from the main and secondary loops, the Driver Logic is also controlled by the Programming Logic, Fault Logic and Zero Crossing Comparator. The Programming Logic tells the Driver Logic whether the controller is using a PFET or NFET high side driver as well as whether the controller is operating in continuous or discontinuous mode. The Fault Logic holds the high and low side drivers off if $V_{CC}$ dips below 2.75V, if an over current condition exists, or if the part is disabled through the ENABLE pin. The Zero Crossing Comparator turns the lower driver off

## General Overview: continued

if the conduction current reaches zero and the Driver Logic has made an attempt to turn the lower driver on and the Programming Logic is set for discontinuous mode. Lastly, the 4Ω drivers have internal gate non-overlap circuitry and are designed to drive MOSFETs associated with converter designs in the 5A to 10A range. Typically the high side driver is referenced to the SWN pin; further improving the efficiency and performance of the converter.

## ENABLE

Low quiescent mode or "Sleep Mode" is initiated by pulling the ENABLE pin below 650mV. The ENABLE pin has an internal 4µA pull-up current and does not require any external interface for normal operation. If the ENABLE pin is driven from a voltage source, the voltage must be above 1.45V in order to guarantee proper "awake" operation. Assuming that $V_{CC}$ is above 2.85V, the SP6120B transitions from "Sleep Mode" to "Awake Mode" in about 20µs to 30µs and from "Awake Mode" to "Sleep Mode" in a few microseconds. SP6120B quiescent current in sleep mode is 20µA maximum. During Sleep Mode, the high side and low side MOSFETs are turned off and the COMP and SS pins are held low.

## Bootstrap Circuit

When SP6120B is programmed to drive a high side N channel MOSFET, a bootstrap circuit is required to generate a voltage higher than $V_{IN}$ to fully enhance the top MOSFET. A typical bootstrap only requires a capacitor and diode shown as $C_{BST}$ and $D_{BST}$ in the application circuit on the front page. When the bottom MOSFET $Q_B$ is turned on, $D_{BST}$ is forward biased and charges the $C_{BST}$ close to $V_{IN}$. When the top MOSFET turn on, the switch node swings to the $V_{IN}$ voltage. Now the voltage at the BST pin is $2*V_{IN}$ and $D_{BST}$ is reverse biased. The BST pin voltage powers the high side MOSFET driver, and thus the GH output goes up to $2*V_{IN}$ to provide a $V_{DS}$ equal to $V_{IN}$.

Under certain conditions, the bottom MOSFET may not turn on long enough to replenish $C_{BST}$ voltage. Therefore, when the top MOSFET turns on, the BST pin may not be high enough to fully enhance the switch. To prevent this operation, SP6120B monitors the BST pin voltage in reference to the $V_{CC}$ voltage. When the BST pin voltage is less than $V_{BST}$ OK threshold, the controller forces the GL to turn on for MINIMUM GL ON at the end of the switching cycle. This provides enough time to recharge the $C_{BST}$ and ensures the proper operation of the bootstrap circuit.

## UVLO

Assuming that the ENABLE pin is either pulled high or floating, the voltage on the $V_{CC}$ pin then determines operation of the SP6120B. As $V_{CC}$ rises, the UVLO block monitors $V_{CC}$ and keeps the high side and low side MOSFETs off and the COMP and SS pins low until $V_{CC}$ reaches 2.85V. If no faults are present, the SP6120B will initiate a soft start when $V_{CC}$ exceeds 2.85V. Hysteresis (about 100mV) in the UVLO comparator provides noise immunity at start-up.

## Soft Start

*(see figures on next page)*

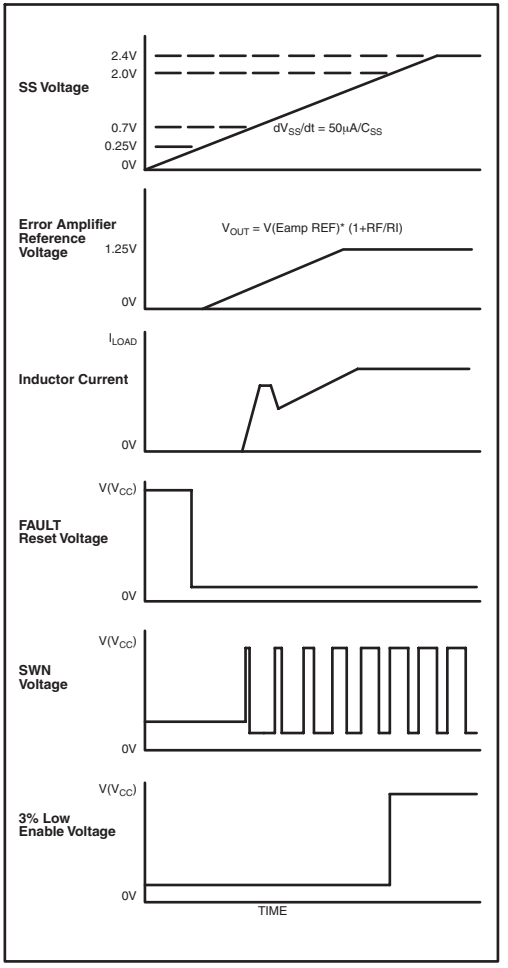
Soft start is required on step-down controllers to prevent excess inrush current through the power train during start-up. Typically this is managed by sourcing a controlled current into a programming capacitor (on the SS pin) and then using the voltage across this capacitor to slowly ramp up either the error amp reference or the error amp output (COMP). The control loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady-state duty cycle as the output voltage increases to its regulated value. As a result of controlling the inductor volt*second product during start-up, inrush current is also controlled.

The presence of the output capacitor creates extra current draw during start-up. Simply stated, $dV_{OUT}/dt$ requires an average sustained current in the output capacitor and this current must be considered while calculating peak inrush current and over current thresholds. Since the SP6120B ramps up the error amp reference voltage, an expression for the output capacitor current can be written as:

$$IC_{OUT} = (C_{OUT}/C_{SS}) * (V_{OUT}/1.25) * 50\mu A$$

As the figure shows, the SS voltage controls a variety of signals. First, provided all the external fault conditions are removed, the fault latch is reset and the SS cap begins to charge. When the SS voltage reaches around 0.3V, the error amp reference begins to track the SS voltage while maintaining the 0.3V differential. As the SS voltage reaches 0.7V, the driver begins to switch the high side and low side MOSFETs with narrow pulses in an effort to keep the converter output regulated. As the error amp reference ramps upward, the driver pulses widen until a steady state value is reached. The "bump" in the inductor current transfer curve is indicative of excess charge current incurred due to the finite propagation delay of the controller. When the SS voltage reaches 2.0V, the secondary loop including the 3% window comparator is enabled. Lastly, the SS voltage is clamped at 2.4V, ending the soft start charge cycle.



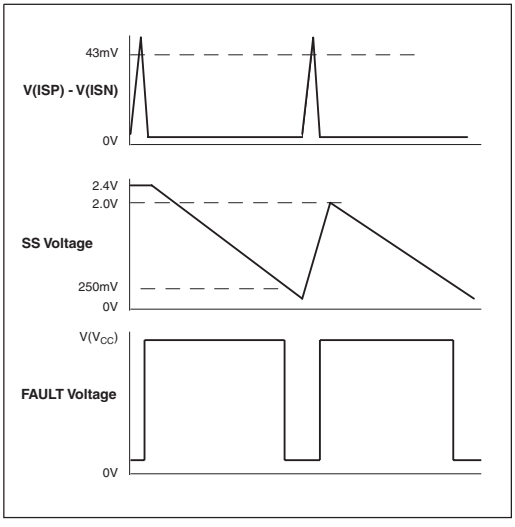

## Hiccup Mode

When the converter enters a fault mode, the driver holds the high side and low side MOSFETs off for a finite period of time. Provided the part is enabled, this time is set by the discharge of the SS capacitor. The discharge time is roughly 10 times the charge interval thereby giving the power supply plenty of time to cool during an over current fault. The driver off-time is predominantly determined by the discharge time. Restart will occur just like a normal soft start cycle.

However, if a fault occurs during the soft start charge cycle, the FAULT latch is immediately set, turning off the high side and low side MOSFETs. The MOSFETs remain off during the remainder of the charge cycle and subsequent discharge cycle of the SS capacitor. Again, provided there are no external fault conditions, the FAULT latch will be reset when the SS voltage reaches 250 mV.

## Over Current Protection

The SP6120B over current protection scheme is designed to take advantage of three popular detection schemes: Sense Resistor, Trace Resistor or Inductor Sense. Because the detection threshold is only 43mV, both trace resistor and inductor sense become attractive protection schemes. The inductor sense scheme adds no additional dc loss to the converter and is an excellent alternative to Rdson based schemes;



### Over Current Protection: continued

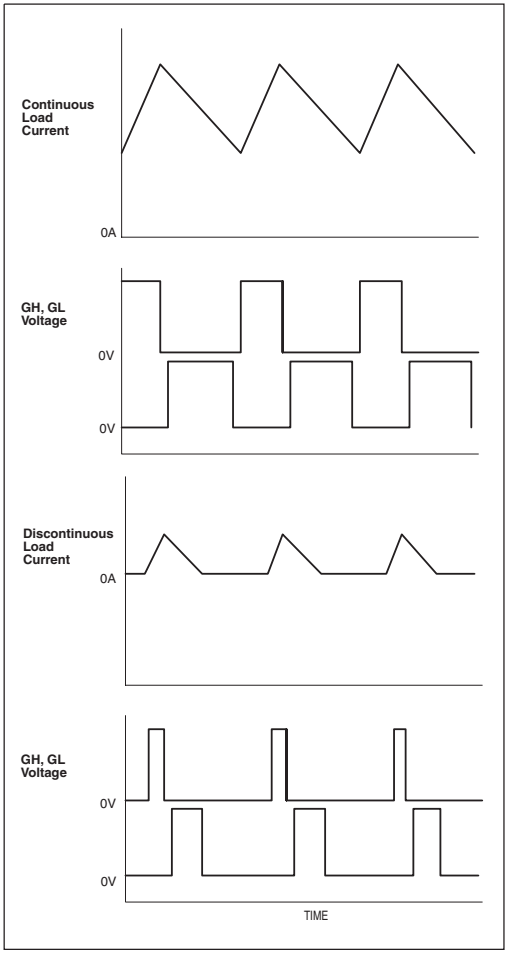
providing continuous current sensing and flexible MOSFET selection. An internal, 10µs filter conditions the over current signal from transients generated during load steps. In addition, because the over current inputs, ISP and ISN, are capable of rail to rail operation, the SP6120B provides excellent over current protection during conditions where $V_{IN}$ approaches $V_{OUT}$.

### Zero Crossing Detection

In some applications, it may be undesirable to have negative conduction current in the inductor. This situation happens when the ripple current in the inductor is higher than the load current. Therefore, the SP6120B provides an option for "discontinuous" operation. If the Program Logic (see next section) is set for discontinuous mode, then the Driver Logic looks at the Zero Crossing Comparator and the state of the lower gate driver. If the low side MOSFET was "on" and V(ISP)-V(ISN) < 0 then the low side MOSFET is immediately turned off and held off until the high side MOSFET is turned "on". When the high side MOSFET turns "on" , the Driver Logic is reset. The following figures show continuous and discontinuous operation for a converter with an NFET high side MOSFET.

### Discontinuous vs. Continuous Mode

The discontinuous mode is used when better light load efficiency is desired, for example in portable applications. Additionally, for power supply sequencing in some applications the DC-DC converter output is pre-charged to a voltage through a switch at start-up, and discontinuous operation would be required to prevent reverse inductor current from discharging the pre-charge voltage. The continuous mode is preferable for lower noise and EMI applications since the discontinuous mode can cause ringing of the switch node voltage when it turns both switches off. Another example where continuous mode could be required is one where the inductor has an extra winding used for an over-winding regulator and thus continuous conduction is necessary to produce this second output voltage.




### Program Logic

The Program pin (PROG) of the SP6120B adds a new level of flexibility to the design of DC/DC converters. A 10µA current flows either into or out of the Program pin depending on the initial potential presented to the pin. If no resistor is present, the Program Logic simply looks at the potential on the pin, sets the mode to "continuous" and programs NFET or PFET high side drive accordingly. If the 68kΩ resistor is present, the voltage drop across the resistor signals the SP6120B to put the Driver Logic in "discontinuous" mode. With one pin and a 68kΩ resistor, the SP6120B can be configured for a variety of operating modes:

| PROGRAM LOGIC TRUTH TABLE | | |
|---|---|---|
| PROGRAM PIN | NFET OR PFET | MODE |
| Short to GND | NFET | Continuous |
| 68 kΩ to GND | NFET | Discontinuous |
| Short to $V_{CC}$ | PFET | Continuous |
| 68 kΩ to $V_{CC}$ | PFET | Discontinous |

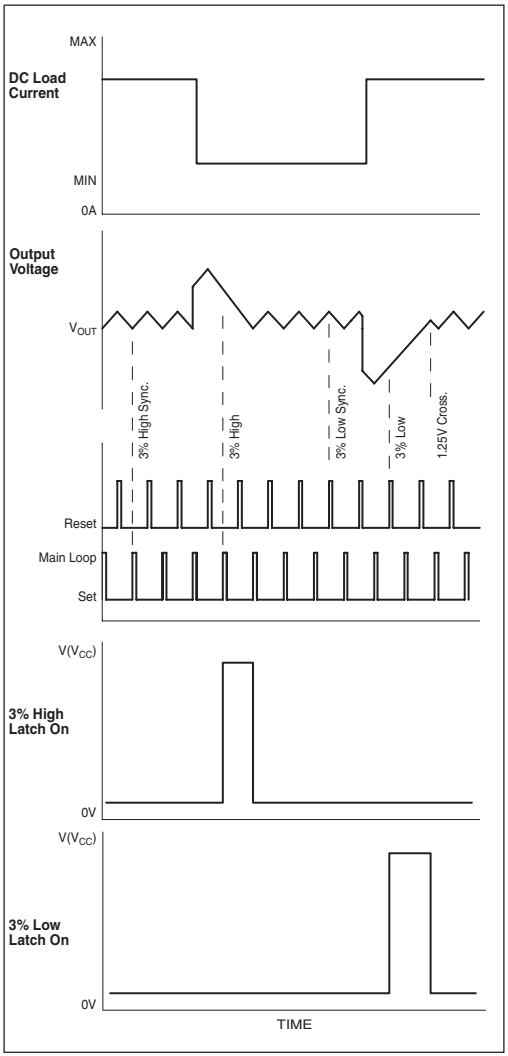
The NFET/PFET programmability is for the high side MOSFET. When designing DC/DC converters, it is not always obvious when to use an NFET with a charge pump or a simple PFET for the high side MOSFET. Often, the controller has to be changed, making performance evaluations difficult. This difficulty is worsened by the limited availability of true low voltage controllers. In addition, by also programming the mode, continuous or discontinuous, switch mode power designs that are successful in bus applications can now find homes in portable applications.

### Secondary Loop (3% Window Comparator)

DSP, microcontroller and microprocessor applications have very strict supply voltage requirements. In addition, the current requirements to these devices can change drastically. Linear regulators, typically the workhorse for DC/DC step-down, do a great job managing accuracy and transient response at the expense of efficiency. On the other hand, PWM switching regulators typically do a great job managing efficiency at the expense of output ripple and line/load step response. The trick in PWM controller design is to emulate the transient response of the linear regulator.

Of course improving transient response should be transparent to the power supply designer. Very often this is not the case. Usually the very circuitry that improves the controllers transient response adversely interferes with the main PWM loop or complicates the board level design of the power converter.

The SP6120B handles line/load transient response in a new way. First, a window comparator detects whether the output voltage is above or below the regulated value by 3%. Then, a proprietary "Ripple & Frequency Independent" algorithm synchronizes the output of the window comparator with the peak and valley of the inductor current waveform. 3% low detection is synchronized with inductor current peak; 3% high detection is synchronized with the inductor current valley. However, in order to eliminate any additional loops, the current peak and valley are determined by the edges associated with the on-time in the main loop. The set pulse corresponding to the start of an on-time indicates a



## Secondary Loop (3% Window Comparator): continued

current valley and the reset pulse corresponding to the end of an on-time indicates a current peak. In effect, the main loop determines the status of the secondary loop.

Notice that the output voltage appears to coast toward the regulated value during periods where the main loop would be telling the drivers to switch. It is during this interval that the 3% window comparator has taken control away from the main loop. The main loop regains control only if the output voltage crosses through its regulated value. Also notice where the 3% comparator takes over. The output voltage is considered "high" only if the trough of the ripple is above 3%. The output voltage is considered "low" only if the peak of the ripple is below 3%. By managing the secondary loop in this fashion, the SP6120B can improve the transient response of high performance power converters without causing strange disturbances in low to moderate performance systems.

## Driver Logic

Signals from the PWM latch (QPWM), Fault latch (FAULT), Program Logic, Zero Crossing Comparator, and 3% Window Comparators all flow into the Driver Logic. The following is a truth table for determining the state of the GH and GL voltages for given inputs:

DRIVER LOGIC TRUTH TABLE

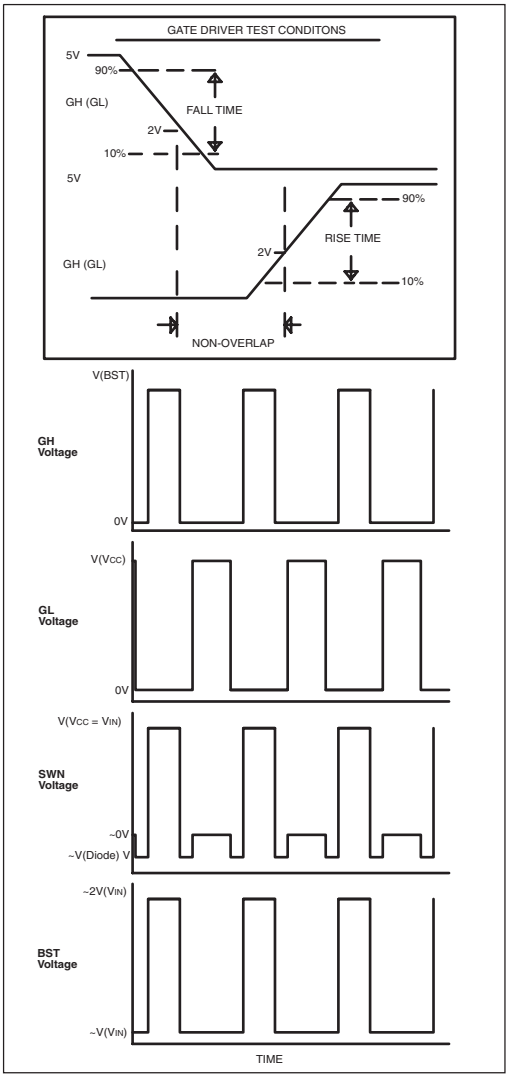
| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| FAULT | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| QPWM or 3% COMP | X | X | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| NFET/PFET | N | P | N | P | N | P | N | P | N | P |
| CONT/DISC | X | X | X | X | C | C | D | D | D | D |
| ZERO CROSS | X | X | X | X | X | X | 0 | 0 | 1 | 1 |
| GH | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| GL | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

The QPWM and 3% Comparators are grouped together because 3% Low is the same as QPWM = 1 and 3% High is the same as QPWM = 0.

## Output Drivers

The driver stage consists of one high side, 4Ω driver, GH and one low side, 4Ω, NFET driver, GL. As previously stated, the high side driver can be configured to drive a PFET or an NFET high side switch. The high side driver can also be configured as a switch node referenced driver. Due to voltage constraints, this mode is mandatory for 5V, single supply, high side NFET applications. The following figure shows typical driver waveforms for the 5V, high side NFET design.

As with all synchronous designs, care must be taken to ensure that the MOSFETs are properly chosen for non-overlap time, peak current capability and efficiency.



## APPLICATIONS INFORMATION

### Inductor Selection

There are many factors to consider in selecting the inductor including cost, efficiency, size and EMI. In a typical SP6120B circuit, the inductor is chosen primarily for value, saturation current and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. Low inductor values provide the smallest size, but cause large ripple currents, poor efficiency and more output capacitance to smooth out the larger ripple current. The inductor must also be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. A good compromise between size, loss and cost is to set the inductor ripple current to be within 20% to 40% of the maximum output current.

The switching frequency and the inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN(\max)} - V_{OUT})}{V_{IN(\max)}\, F_S\, K_r\, I_{OUT(\max)}}$$

where:

$F_S$ = switching frequency

$K_r$ = ratio of the ac inductor ripple current to the maximum output current

The peak to peak inductor ripple current is:

$$I_{PP} = \frac{V_{OUT}(V_{IN(\max)} - V_{OUT})}{V_{IN(\max)}\, F_S\, L}$$

Once the required inductor value is selected, the proper selection of core material is based on peak inductor current and efficiency requirements.

The core material must be large enough not to saturate at the peak inductor current

$$I_{PEAK} = I_{OUT(\max)} + \frac{I_{PP}}{2}$$

and provide low core loss at the high switching frequency. Low cost powdered iron cores have a gradual saturation characteristic but can introduce considerable ac core loss, especially when the inductor value is relatively low and the ripple current is high. Ferrite materials, on the other hand, are more expensive and have an abrupt saturation characteristic with the inductance dropping sharply when the peak design current is exceeded. Nevertheless, they are preferred at high switching frequencies because they present very low core loss and the design only needs to prevent saturation. In general, ferrite or molypermalloy materials are better choice for all but the most cost sensitive applications.

The power dissipated in the inductor is equal to the sum of the core and copper losses. To minimize copper losses, the winding resistance needs to be minimized, but this usually comes at the expense of a larger inductor. Core losses have a more significant contribution at low output current where the copper losses are at a minimum, and can typically be neglected at higher output currents where the copper losses dominate. Core loss information is usually available from the magnetic vendor.

The copper loss in the inductor can be calculated using the following equation:

$$P_{L(Cu)} = I^2_{L(RMS)}\, R_{WINDING}$$

where $I_{L(RMS)}$ is the RMS inductor current that can be calculated as follows:

$$I_{L(RMS)} = I_{OUT(max)}\sqrt{1 + \frac{1}{3}\left(\frac{I_{PP}}{I_{OUT(max)}}\right)^2}$$

### Output Capacitor Selection

The required ESR (Equivalent Series Resistance) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage do not exceed the tolerance limits expected on the output voltage. During an output load transient, the output capacitor must supply all the additional current demanded by the load until the SP6120B adjusts the inductor current to the new value. Therefore the capacitance must be large

enough so that the output voltage is held up while the inductor current ramps up or down to the value corresponding to the new load current. Additionally, the ESR in the output capacitor causes a step in the output voltage equal to the ESR value multiplied by the change in load current. Because of the fast transient response and inherent 100% and 0% duty cycle capability provided by the SP6120B when exposed to output load transient, the output capacitor is typically chosen for ESR, not for capacitance value.

The output capacitor's ESR, combined with the inductor ripple current, is typically the main contributor to output voltage ripple. The maximum allowable ESR required to maintain a specified output voltage ripple can be calculated by:

$$R_{ESR} \leq \frac{\Delta V_{OUT}}{I_{PP}}$$

where:

$\Delta V_{OUT}$ = peak to peak output voltage ripple
$I_{PP}$ = peak to peak inductor ripple current

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP}\,(1-D)}{C_{OUT} F_S}\right)^2 + (I_{PP} R_{ESR})^2}$$

where:

$F_S$ = switching frequency
$D$ = duty cycle
$C_{OUT}$ = output capacitance value

Recommended capacitors that can be used effectively in SP6120B applications are: low-ESR aluminum electrolytic capacitors, OS-CON capacitors that provide a very high performance/size ratio for electrolytic capacitors and low-ESR tantalum capacitors. AVX TPS series and Kemet T510 surface mount capacitors are popular tantalum capacitors that work well in SP6120B applications. POSCAP from Sanyo is a solid electrolytic chip capacitor that has low ESR and high capacitance. For the same ESR value, POSCAP has lower profile compared with tantalum capacitor.

### Input Capacitor Selection

The input capacitor should be selected for ripple current rating, capacitance and voltage rating. The input capacitor must meet the ripple current requirement imposed by the switching current. In continuous conduction mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle $V_{OUT}/V_{IN}$. Most of this current is supplied by the input bypass capacitors. The RMS value of input capacitor current is determined at the maximum output current and under the assumption that the peak to peak inductor ripple current is low, it is given by:

$$I_{CIN(rms)} = I_{OUT(max)} \sqrt{D(1 - D)}$$

The worse case occurs when the duty cycle D is 50% and gives an RMS current value equal to $I_{OUT}/2$. Select input capacitors with adequate ripple current rating to ensure reliable operation.

The power dissipated in the input capacitor is:

$$P_{CIN} = I^2_{CIN(rms)} R_{ESR(CIN)}$$

This can become a significant part of power losses in a converter and hurt the overall energy transfer efficiency.

The input voltage ripple primarily depends on the input capacitor ESR and capacitance. Ignoring the inductor ripple current, the input voltage ripple can be determined by:

$$\Delta V_{IN} = I_{out(\max)} R_{ESR(CIN)} + \frac{I_{OUT(MAX)} V_{OUT} (V_{IN} - V_{OUT})}{F_S C_{IN} V_{IN}^2}$$

The capacitor type suitable for the output capacitors can also be used for the input capacitors. However, exercise extra caution when tantalum capacitors are considered. Tantalum capacitors are known for catastrophic failure when exposed to surge current, and input capacitors

are prone to such surge current when power supplies are connected 'live' to low impedance power sources. Certain tantalum capacitors, such as AVX TPS series, are surge tested. For generic tantalum capacitors, use 2:1 voltage derating to protect the input capacitors from surge fall-out.

### MOSFET Selection

The losses associated with MOSFETs can be divided into conduction and switching losses. Conduction losses are related to the on resistance of MOSFETs, and increase with the load current. Switching losses occur on each on/off transition when the MOSFETs experience both high current and voltage. Since the bottom MOSFET switches current from/to a paralleled diode (either its own body diode or a Schottky diode), the voltage across the MOSFET is no more than 1V during switching transition. As a result, its switching losses are negligible. The switching losses are difficult to quantify due to all the variables affecting turn on/off time. However, the following equation provides an approximation on the switching losses associated with the top MOSFET driven by SP6120B.

$$P_{SH(\max)} = 12 C_{rss} V_{IN(\max)} I_{OUT(\max)} F_S$$

where

$C_{rss}$ = reverse transfer capacitance of the top MOSFET

Switching losses need to be taken into account for high switching frequency, since they are directly proportional to switching frequency. The conduction losses associated with top and bottom MOSFETs are determined by:

$$P_{CH(\max)} = R_{DS(ON)} I_{OUT(\max)}{}^2 D$$

$$P_{CL(\max)} = R_{DS(ON)} I_{OUT(\max)}{}^2 (1 - D)$$

where

$P_{CH(max)}$ = conduction losses of the high side MOSFET

$P_{CL(max)}$ = conduction losses of the low side MOSFET

$R_{DS(ON)}$ = drain to source on resistance.

The total power losses of the top MOSFET are the sum of switching and conduction losses. For synchronous buck converters of efficiency over 90%, allow no more than 4% power losses for high or low side MOSFETs. For input voltages of 3.3V and 5V, conduction losses often dominate switching losses. Therefore, lowering the $R_{DS(ON)}$ of the MOSFETs always improves efficiency even though it gives rise to higher switching losses due to increased $C_{rss}$.

Top and bottom MOSFETs experience unequal conduction losses if their on time is unequal. For applications running at large or small duty cycle, it makes sense to use different top and bottom MOSFETs. Alternatively, parallel multiple MOSFETs to conduct large duty factor.

$R_{DS(ON)}$ varies greatly with the gate driver voltage. The MOSFET vendors often specify $R_{DS(ON)}$ on multiple gate to source voltages ($V_{GS}$), as well as provide typical curve of $R_{DS(ON)}$ versus $V_{GS}$. For 5V input, use the $R_{DS(ON)}$ specified at 4.5V $V_{GS}$. At the time of this publication, vendors, such as Fairchild, Siliconix and International Rectifier, have started to specify $R_{DS(ON)}$ at $V_{GS}$ less than 3V. This has provided necessary data for designs in which these MOSFETs are driven with 3.3V and made it possible to use SP6120B in 3.3V only applications.

Thermal calculation must be conducted to ensure the MOSFET can handle the maximum load current. The junction temperature of the MOSFET, determined as follows, must stay below the maximum rating.

$$T_{J(\max)} = T_{A(\max)} + \frac{P_{MOSFET(\max)}}{R_{\theta JA}}$$

where

$T_{A(max)}$ = maximum ambient temperature

$P_{MOSFET(max)}$ = maximum power dissipation of the MOSFET

$R_{\Theta JA}$ = junction to ambient thermal resistance.

$R_{\Theta JA}$ of the device depends greatly on the board layout, as well as device package. Significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. For example, in a SO-8 package, placing

two 0.04 square inches copper pad directly under the package, without occupying additional board space, can increase the maximum power from approximately 1 to 1.2W. For DPAK package, enlarging the tap mounting pad to 1 square inches reduces the $R_{\Theta}JA$ from 96°C/W to 40°C/W.

### Schottky Diode Selection

When paralleled with the bottom MOSFET, an optional Schottky diode can improve efficiency and reduce noises. Without this Schottky diode, the body diode of the bottom MOSFET conducts the current during the non-overlap time when both MOSFETs are turned off. Unfortunately, the body diode has high forward voltage and reverse recovery problem. The reverse recovery of the body diode causes additional switching noises when the diode turns off. The Schottky diode alleviates these noises and additionally improves efficiency thanks to its low forward voltage. The reverse voltage across the diode is equal to input voltage, and the diode must be able to handle the peak current equal to the maximum load current.

The power dissipation of the Schottky diode is determined by

$$P_{DIODE} = 2V_F I_{OUT} T_{NOL} F_S$$

where

$T_{NOL}$ = non-overlap time between GH and GL.

$V_F$ = forward voltage of the Schottky diode.

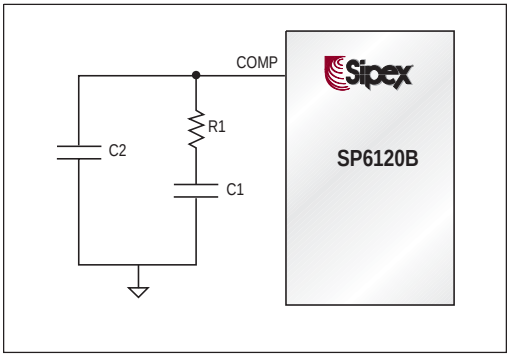



***Figure 18. The RC network connected to the COMP pin provides a pole and a zero to control loop.***

### Loop Compensation Design

The goal of loop compensation is to manipulate loop frequency response such that its gain crosses over 0db at a slope of –20db/dec. The SP6120B has a transconductance error amplifier and requires the compensation network to be connected between the COMP pin and ground, as shown in Figure 18.

The first step of compensation design is to pick the loop crossover frequency. High crossover frequency is desirable for fast transient response, but often jeopardize the system stability. Since the SP6120B is equipped with 3% window comparator that takes over the control loop on transient, the crossover frequency can be selected primarily to the satisfaction of system stability. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by:

$$f_{Z(ESR)} = \frac{1}{2\pi C_{OUT} R_{ESR}}$$

Crossover frequency of 20kHz is a sound first try if low ESR tantalum capacitors or poscaps are used at the output. The next step is to calculate the complex conjugate poles contributed by the LC output filter,

$$f_{P(LC)} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

The open loop gain of the whole system can be divided into the gain of the error amplifier, PWM modulator, buck converter, and feedback resistor divider. In order to crossover at the selected frequency fco, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. In the RC network shown in Figure 18, the product of R1 and the error amplifier transconductance determines this gain. Therefore, R1 can be determined from the following equation that takes into account the typical error amplifier transconductance, reference voltage and PWM ramp built into the SP6120B.

$$R_1 = \frac{1300 V_{OUT} f_{CO} f_{Z(ESR)}}{V_{IN} f_{P(LC)}^2}$$

In Figure 18, R1 and C1 provides a zero $f_{Z1}$ which needs to be placed at or below $f_{P(LC)}$. If $f_{Z1}$ is made equal to $f_{P(LC)}$ for convenience, the value of C1 can be calculated as

$$C_1 = \frac{1}{2\pi f_{P(LC)} R_1}$$

The optional C2 generates a pole $f_{P1}$ with R1 to cut down high frequency noise for reliable operation. This pole should be placed one decade higher than the crossover frequency to avoid erosion of phase margin. Therefore, the value of the C2 can be derived from

$$C_2 = \frac{1}{20\pi f_{CO} R_1}$$

Figure 19 illustrates the overall loop frequency response and frequency of each pole and zero. To fine-tune the compensation, it is necessary to physically measure the frequency response using a network analyzer.

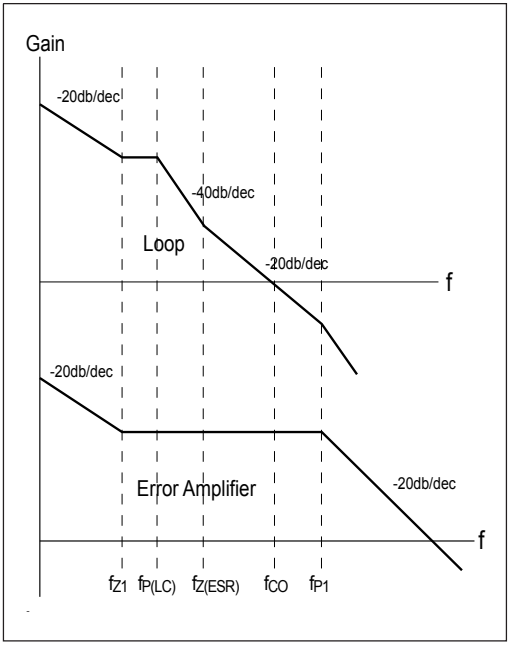



***Figure 19. Frequency response of a stable system and its error amplifier.***

## Current Sense

The SP6120B allows sensing current using the inductor, PCB trace or current-sense resistor. Inductor-sense utilizes the voltage drop across the ESR of the inductor, while PCB trace and current-sense resistor introduce additional resistance in series with the inductor. The resistance of the sense element determines the overcurrent protection threshold as follows,

$$I_{LIM} = \frac{43mV}{R_{SEN}}$$

$R_{SEN}$ = current-sense resistance which can be implemented as ESR of the inductor, trace or discrete resistor.

The maximum power dissipation on the current-sense element is:

$$P_{SEN} = I_{OUT(\max)}{}^2 R_{SEN}$$

For the inductor-sense scheme shown in the application circuit, $R_S$ and $C_S$ are used to replicate the signal across the ESR of the inductor. $R_S$ and $C_S$ can be looked at as a low pass filter whose output represents the DC differential voltage between the switch node and the output. At steady state, this voltage happens to be the output current times the ESR of the inductor. In addition, if the following relationship is satisfied,

$$\frac{L}{ESR} = R_S C_S$$

the output of the RsCs filter represents the exact voltage across the ESR, including the ripple. Since the SP6120B's hiccup overcurrent protection scheme is intended to safeguard sustained overload conditions, the DC portion of the current signal is more of interest. Therefore, designing the $R_S C_S$ time constant higher than L/ESR provides reliable current sense against any premature triggering due to noise or any transient conditions. Pick Rs between 10k and 100k, and Cs can be determined by:

$$C_S = 2 \frac{L}{ESR} \frac{1}{R_S}$$

Here the time constant of $R_S C_S$ is twice the value of L/ESR.

In some applications, it may be desirable to extend the current sense capability of a given $R_{SEN}$ element (usually the inductor ESR) be-

yond the limit set by the 43mV threshold.

A straight forward way to do this would be to add a resistor $R_{S2}$ in parallel with $C_S$, creating a voltage divider with $R_S$. This changes the relationship with $R_S$ and $C_S$ to be

$$C_S = 2\frac{L}{ESR}\frac{1}{R_S // R_{S2}}$$

Using a voltage divider across the inductor, the new relationship becomes:

$$I_{LIM} = \frac{43mV}{ESR}\frac{R_S + R_{S2}}{R_{S2}}$$

To calculate $R_{S2}$, the formula becomes

$$R_{S2} = R_S \left( \frac{I_{LIM} ESR}{43mV} - 1 \right)$$

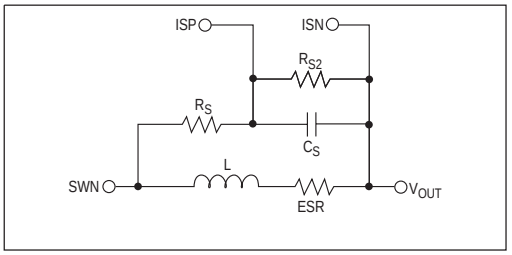



*Figure 20: Current Sensing*

## Output Voltage Programming

As shown in Figure 21(A), the voltage divider connecting to the $V_{FB}$ pin programs the output voltage according to

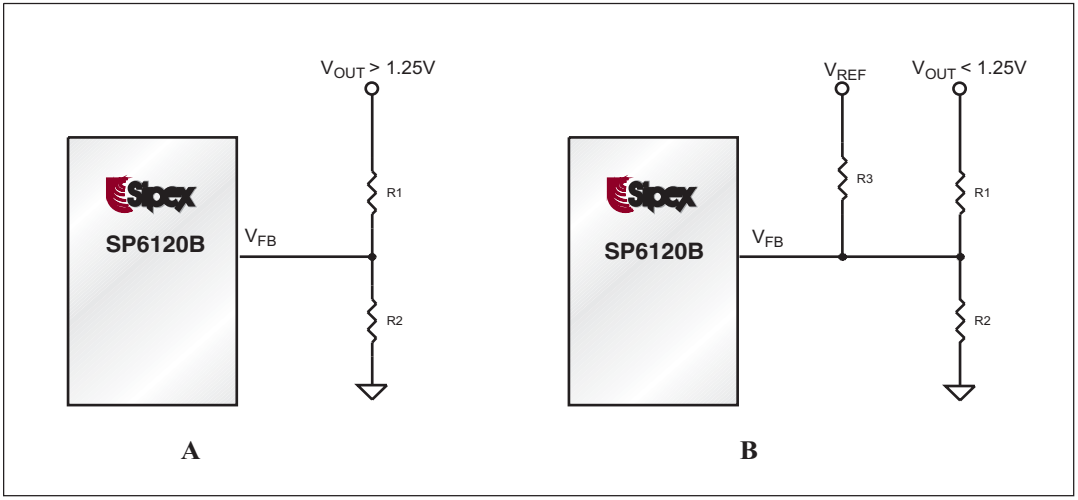
$$V_{OUT} = 1.25\left(1 + \frac{R_1}{R_2}\right)$$

where 1.25V is the internal reference voltage. Select R2 in the range of 10k to 100k, and R1 can be calculated using

$$R_1 = \frac{R_2(V_{OUT} - 1.25)}{1.25}$$

For output voltage less than 1.25V, a simple circuit shown in Figure 21(B) can be used in which $V_{REF}$ is an external voltage reference greater than 1.25V. For simplicity, use the same resistor value for R1 and R2, then R3 is determined as follows,

$$R_3 = \frac{(V_{REF} - 1.25)R_1}{2.5 - V_{OUT}}$$




***Figures 21(A), a voltage divider connected to the $V_{FB}$ pin programs the output voltageand 21(B), a simple circuit using one external voltage reference programs the output voltages to less than 1.25V.***

## Layout Guideline

PCB layout plays a critical role in proper function of the converters and EMI control. In switch mode power supplies, loops carrying high di/dt give rise to EMI and ground bounces. The goal of layout optimization is to identify these loops and minimize them. It is also crucial on how to connect the controller ground such that its operation is not affected by noise. The following guideline should be followed to ensure proper operation.

1. A ground plane is recommended for minimizing noises, copper losses and maximizing heat dissipation.

2. Connect the ground of feedback divider, compensation components, oscillator resistor and soft-start capacitor to the GND pin of the IC. Then connect this pin as close as possible to the ground of the output capacitor.

3. The $V_{CC}$ bypass capacitor should be right next to the Vcc and GND pin.

4. The traces connecting to feedback resistor and current sense components should be short and far away from the switch node, and switching components.

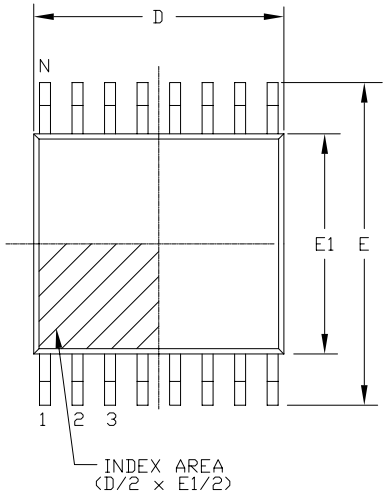
5. Connect the PGND pin close to the source of the bottom MOSFET, and the SWN pin to the source of the top MOSFET. Minimize the trace between GH/GL and the gates of the MOSFETs. All of these requirements reduce the impedance driving the MOSFETs. This is especially important for the bottom MOSFET that tends to turn on through its miller capacitor when the switch node swings high.

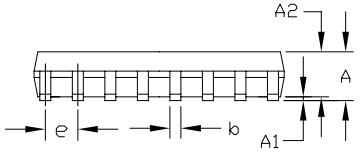
6. Minimize the loop composed of input capacitors, top/bottom MOSFETs and Schottky diode, This loop carries high di/dt current. Also increase the trace width to reduce copper losses.

7. Maximize the trace width of the loop connecting the inductor, output capacitors, Schottky diode and bottom MOSFET.

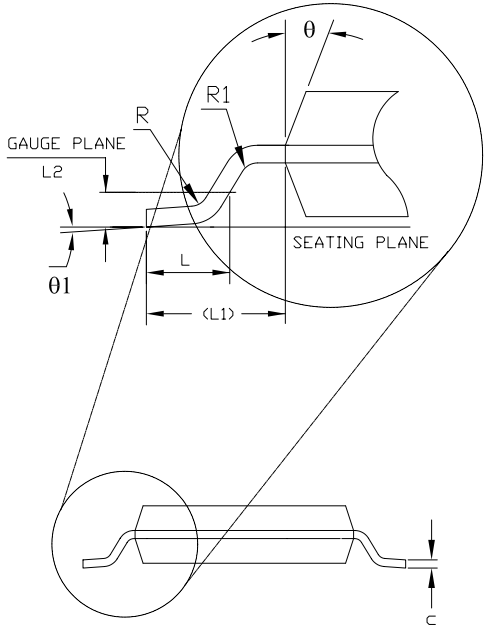
| REVISION HISTORY | | | |
|---|---|---|---|
| REV. | DISCRIPTION | DATE | APP'D |
| A | DRAWING ORIGINATION | 04/19/06 | JL |

Top View




Side View




Front View

| 16 Pin TSSOP JEDEC MO-153 Variation AB | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | — | 0.30 | 0.007 | — | 0.012 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| E | 6.40 BSC | | | 0.252 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.09 | — | — | 0.035 | — | — |
| R1 | 0.09 | — | — | 0.035 | — | — |
| θ | 12° REF | | | 12° REF | | |
| θ1 | 0° | — | 8° | 0° | — | 8° |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.200 |
| N | 16 | | | 16 | | |

| | | |
|---|---|---|
| Solved by Sipex | SIPEX CORPORATION | |
| | 16 PIN TSSOP PACKAGE OUTLINE | |
| Packaging Approval: | Drawing No: 16-PIN TSSOP | |
| By: JL / Date: 04/19/06 | Revision: A | Sheet: 1 OF 1 |

## ORDERING INFORMATION

| Model | Operating Temperature Range | Package Type |
|---|---|---|
| SP6120BCY | 0˚C to +70˚C | 16-Pin TSSOP |
| SP6120BCY/TR | 0˚C to +70˚C | 16-Pin TSSOP |
| SP6120BEY | -40˚C to +85˚C | 16-Pin TSSOP |
| SP6120BEY/TR | -40˚C to +85˚C | 16-Pin TSSOP |

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP6120BEY/TR = standard; SP6120BEY-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 2500 for TSSOP.

For further assistance:

Email: Sipexsupport@sipex.com

WWW Support page: http://www.sipex.com/content.aspx?p=support

Sipex Application Notes: http://www.sipex.com/applicationNotes.aspx

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