

## **PROTECTION PRODUCTS**

# Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	$P_{pk}$	300	Watts
Operating Temperature	T <sub>J</sub>	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

# Electrical Characteristics (T=25°C)

SMDA05C-8									
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units			
Reverse Stand-Off Voltage	V <sub>RWM</sub>				5	V			
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 1mA	6			V			
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5V, T=25°C			20	μΑ			
Clamping Voltage	V <sub>c</sub>	$I_{pp} = 1A, t_p = 8/20 \mu s$			9.8	V			
Peak Pulse Current	I <sub>PP</sub>	t <sub>p</sub> = 8/20μs			17	А			
Junction Capacitance	C <sub>j</sub>	Between I/O Pins and Ground V <sub>R</sub> = OV, f = 1MHz			350	pF			

SMDA12C-8									
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units			
Reverse Stand-Off Voltage	V <sub>RWM</sub>				12	V			
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 1mA	13.3			V			
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 12V, T=25°C			1	μΑ			
Clamping Voltage	V <sub>c</sub>	$I_{pp} = 1A, t_p = 8/20 \mu s$			19	V			
Peak Pulse Current	I <sub>PP</sub>	t <sub>p</sub> = 8/20µs			12	Α			
Junction Capacitance	C <sub>j</sub>	Between I/O Pins and Ground V <sub>R</sub> = OV, f = 1MHz			120	pF			



## **PROTECTION PRODUCTS**

# Electrical Characteristics (Continued)

SMDA15C-8									
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units			
Reverse Stand-Off Voltage	V <sub>RWM</sub>				15	V			
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 1mA	16.7			V			
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 15V, T=25°C			1	μΑ			
Clamping Voltage	V <sub>c</sub>	$I_{pp} = 1A, t_p = 8/20 \mu s$			24	V			
Peak Pulse Current	I <sub>PP</sub>	t <sub>p</sub> = 8/20μs			10	А			
Junction Capacitance	C <sub>j</sub>	Between I/O Pins and Ground V <sub>R</sub> = OV, f = 1MHz			75	pF			

SMDA24C-8										
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units				
Reverse Stand-Off Voltage	V <sub>RWM</sub>				24	V				
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 1mA	26.7			V				
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 24V, T=25°C			1	μΑ				
Clamping Voltage	V <sub>c</sub>	$I_{pp} = 1A, t_p = 8/20 \mu s$			43	V				
Peak Pulse Current	I <sub>PP</sub>	t <sub>p</sub> = 8/20μs			5	А				
Junction Capacitance	C <sub>j</sub>	Between I/O Pins and Ground V <sub>R</sub> = OV, f = 1MHz			50	pF				

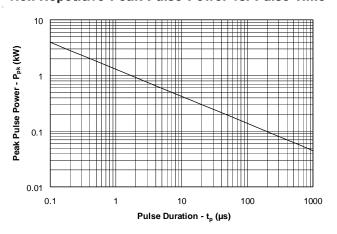




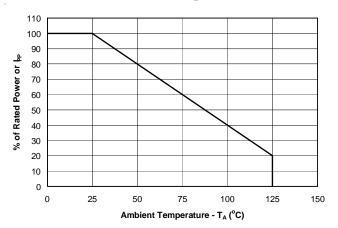
### PROTECTION PRODUCTS

### Typical Characteristics

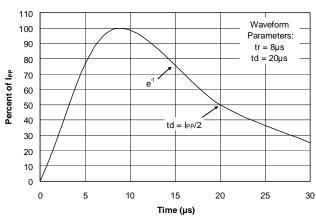
### Non-Repetitive Peak Pulse Power vs. Pulse Time



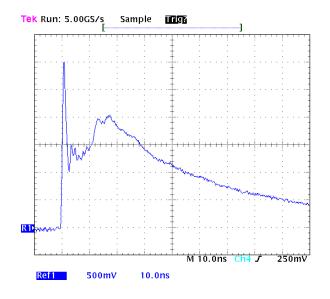
### **Power Derating Curve**



#### **Pulse Waveform**



### ESD Pulse Waveform (IEC 61000-4-2)



### IEC 61000-4-2 Discharge Parameters

Level	First Peak Current	Peak Current at 30 ns	Peak Current at 60 ns	Test Voltage (Contact	Test Voltage (Air
	(A)	(A)	(A)	Discharge) (kV)	Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15





### PROTECTION PRODUCTS

### **Applications Information**

### **Device Connection for Protection of Eight Data Lines**

The SMDAxxC-8 is designed to protect up to 8 data or I/O lines. They are bidirectional devices and may be used on lines where the signal polarities are above and below ground.

The SMDAxxC-8 TVS arrays employ a monolithic structure. Therefore, the working voltage ( $V_{\text{RWM}}$ ) and breakdown voltage ( $V_{\text{BR}}$ ) specifications apply to the differential voltage between any two data line pins. For example, the SMDA24C-8 is designed for a maximum voltage excursion of  $\pm 12V$  between any two data lines.

The device is connected as follows:

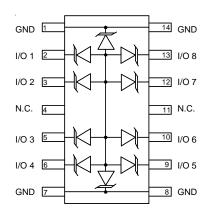
• Pins 2, 3, 5, 6, 9, 10, 12 and 13 are connected to the lines that are to be protected. Pins 1, 7, 8, and 14 are connected to ground. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces. Pins 4 and 11 are not connected.

# Circuit Board Layout Recommendations for Suppression of ESD.

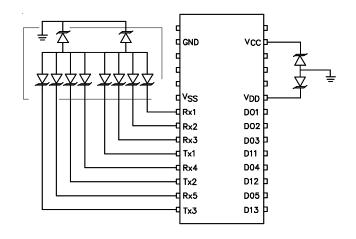
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

### **Circuit Diagram**



**Connection Diagram** 

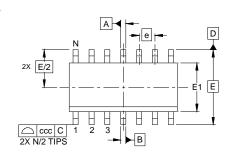


#### **Matte Tin Lead Finish**

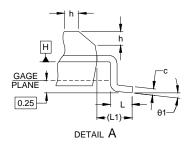
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

### PROTECTION PRODUCTS

### Outline Drawing - SO-14







	DIMENSIONS								
DIM	11	NCHE	S	MILLIMETERS					
ווועו	MIN	MOM	MAX	MIN	NOM	MAX			
Α	.053	-	.069	1.35	-	1.75			
A1	.004	-	.010	0.10	-	0.25			
A2	.049	-	.065	1.25	-	1.65			
b	.012	-	.020	0.31	-	0.51			
С	.007 -		.010	0.17	-	0.25			
D	.337	.341	.344	8.55	8.65	8.75			
E1	.150	.150 .154		3.80	3.90	4.00			
E	.2	236 BS	С	6.00 BSC					
е	.0	)50 BS	С	1.27 BSC					
h	.010	-	.020	0.25	-	0.50			
L	.016	.028	.041	0.40	0.72	1.04			
L1		(.041)		(1.04)					
N	14			14					
θ1	0°	-	8°	0°	-	8°			
aaa	.004			0.10					
bbb	.010			0.25					
DDD									

#### NOTES:

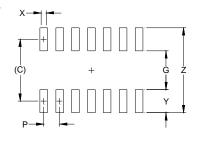
aaa C

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

A2 A

- 2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
- 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 4. REFERENCE JEDEC STD MS-012, VARIATION AB.

# Land Pattern - SO-14



	DIMENSIONS								
DIM	INCHES	MILLIMETERS							
С	(.205)	(5.20)							
G	.118	3.00							
Р	.050	1.27							
X	.024	0.60							
Υ	.087	2.20							
Z	.291	7.40							

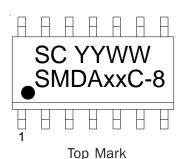
#### NOTES

- THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
  CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
  COMPANY'S MANUFACTURING GUIDELINES ARE MET.
- 2. REFERENCE IPC-SM-782A, RLP NO. 302A.



### PROTECTION PRODUCTS

### Marking

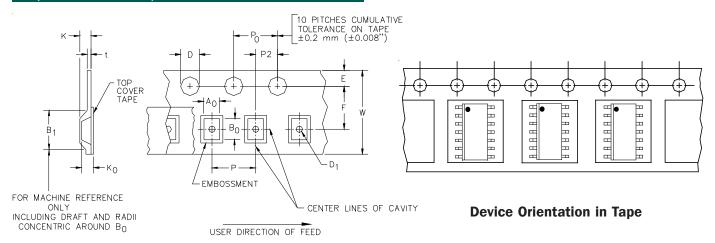


YYWW = Date Code

# Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
SMDA05C-8.TBT	Pb Free	500	7 inch
SMDA12C-8.TBT	Pb Free	500	7 inch
SMDA15C-8.TBT	MDA15C-8.TBT Pb Free 500		7 inch
SMDA24C-8.TBT	Pb Free	500	7 inch
SMDA05C-8.T	Pb Free	56/Tube	N/A
SMDA12C-8.T	Pb Free	56/Tube	N/A
SMDA15C-8.T	Pb Free	56/Tube	N/A
SMDA24C-8.T	Pb Free	56/Tube	N/A

# Tape and Reel Specification



A0	ВО	ко		
6.50 +/-0.30 mm	9.50 +/-0.30 mm	2.10 +/-0.15 mm		

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	Р	PO	P2	T(MAX)	W
16 mm	12.1 mm	1.5 + 0.1 mm - 0.0 mm )	0.5 mm ±0.05	1.750±.10 mm	7.5±0.10 mm	6.5 mm	8.0±0.1 mm	4.0±0.1 mm	2.0±0.01 mm	0.4 mm	16.0 mm ± 0.3 mm





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# Contact Information

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