ABSOLUTE MAXIMUM RATINGS (all voltages referenced to GND = 0 V)			
Parameter		**Limit**	**Unit**
V_{CC}, PV_{CC}		- 0.3 to 15	V
BOOT, PHASE		- 0.3 to 55	
BOOT to PHASE		- 0.3 to 15	
Storage Temperature		- 40 to 150	°C
Operating Junction Temperature		125	
Power Dissipation[a]	SO-8	770	mW
Thermal Impedance (Θ_{JA})[b]		130	°C/W

Notes:
a. Device Mounted with all leads soldered or welded to PC board.
b. Derate 7.7 mW/°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (all voltages referenced to GND = 0 V)		
Parameter	**Limit**	**Unit**
V_{CC}	10.8 to 13.2	V
V_{LX}	48	
C_{BOOT}	100 nF to 1 µF	
BOOT to PHASE	8	V
Operating Temperature Range	- 40 to 85	°C

SPECIFICATIONS[a]							
Parameter	**Symbol**	**Test Conditions Unless Specified** V_{CC} = 12 V, V_{BOOT} - V_{PHASE} = 8 V, T_A = - 40 °C to 85 °C		**Min.**[a]	**Typ.**[b]	**Max.**[a]	**Unit**
Power Supplies							
Supply Voltage	V_{DD}			10.8		13.2	V
Quiescent Current	I_{CCQ}	PWM non-switching			5.6	9.5	mA
Supply Current	I_{DD}	f_{PWM} = 100 kHz, C_{LOAD} = 3 nF	SiP41109		12.5		
			SiP41110		11.0		
Tristate (Shutdown) Current	I_{CCT}	PWM = open			850	1200	µA
Reference Voltage							
Break-Before-Make	V_{BBM}				2.5		V
PWM Input							
Input High	V_{IH}			4.0		V_{DD}	V
Input Low	V_{IL}					1.0	
Bias Current	I_B	PWM 5 V or 0 V			± 600	± 1000	µA
Tristate Threshold High	V_{TSH}			3.0			V
Tristate Threshold Low	V_{TSL}					2.0	
Tristate Holdoff Timeout[c]	t_{TST}				240		ns
Bootstrap Diode							
Forward Voltage	V_F	I_F = 40 mA, T_A = 25 °C		0.70	0.85	1.0	V

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SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V_{CC} = 12 V, V_{BOOT} - V_{PHASE} = 8 V, T_A = - 40 °C to 85 °C		Limits Min.[a]	Limits Typ.[b]	Limits Max.[a]	Unit
MOSFET Drivers							
High-Side Drive Current[c]	$I_{PKH(source)}$	V_{BOOT} - V_{PHASE} = 8 V			0.8		A
	$I_{PKH(sink)}$				1.0		
Low-Side Drive Current[c]	$I_{PKL(source)}$	V_{PVCC} = 8 V	SiP41110		0.9		
	$I_{PKL(sink)}$				1.2		
	$I_{PKL(source)}$	V_{PVCC} = 12 V	SiP41109		1.4		
	$I_{PKL(sink)}$				1.8		
High-Side Driver Impedance	$R_{DH(source)}$	V_{BOOT} - V_{PHASE} = 8 V, PHASE = GND			2.3	4.2	Ω
	$R_{DH(sink)}$				1.9	3.5	
Low-Side Driver Impedance	$R_{DL(source)}$	V_{PVCC} = 8 V	SiP41110		2.9	5.2	
	$R_{DL(sink)}$				1.3	2.4	
	$R_{DL(source)}$	V_{PVCC} = 12 V	SiP41109		2.4	4.3	
	$R_{DL(sink)}$				1.2	2.2	
High-Side Rise Time	t_{rH}	10 % - 90 %, V_{BOOT} - V_{PHASE} = 8 V, C_{LOAD} = 3 nF			45		ns
High-Side Fall Time	t_{fH}				35		
High-Side Rise Time Bypass		10 % - 90 %, V_{BOOT} - V_{PHASE} = 12 V, C_{LOAD} = 3 nF			45		
High-Side Fall Time Bypass					35		
High-Side Propagation Delay[c]	$t_{d(off)H}$	See Timing Waveforms			15		
	$t_{d(on)H}$				15		
Low-Side Rise Time	t_{rL}	10 % to 90 %, V_{BOOT} - V_{PHASE} = 8 V, C_{LOAD} = 3 nF	SiP41110		40		
		10 % to 90 %, V_{BOOT} - V_{PHASE} = 12 V, C_{LOAD} = 3 nF	SiP41109		40		
Low-Side Fall Time	t_{fL}	10 % to 90 %, V_{BOOT} - V_{PHASE} = 8 V, C_{LOAD} = 3 nF	SiP41110		30		
		10 % to 90 %, V_{BOOT} - V_{PHASE} = 12 V, C_{LOAD} = 3 nF	SiP41109		30		
Low-Side Propagation Delay	$t_{d(off)L}$	See Timing Waveforms			15		
	$t_{d(on)L}$				15		
PHASE Timer							
PHASE Falling Timeout[c]	t_{PHASE}				380		ns
PV_{CC} Regulator							
Output Voltage	PV_{CC}			7.6	8	8.4	V
Output Current	I_{PVCC}				80	100	mA
Current Limit	I_{LIM}	V_{DRV} = 0 V		120	200	280	
Line Regulation	LNR	V_{CC} = 10.8 V to 13.2 V			0.05	0.5	%/V
Load Regulation	LDR	5 mA to 80 mA			0.1	1.0	%
PV_{CC} Regulator UVLO							
PV_{CC} Rising	V_{UVLO2}				6.7	7.2	V
PV_{CC} Falling					6.4	6.9	
Hysteresis	Hyst			100	300	500	mV
High-Side Undervoltage Lockout							
Threshold	V_{UVHS}	Rising or falling		2.5	3.35	4.0	V
V_{CC} Undervoltage Lockout							
Threshold	V_{UVLO1}			5.0	5.3	5.6	V
Power on Reset Time	POR				2.5		ms
Thermal Shutdown							
Temperature	T_{SD}	Temperature rising			165		°C
Hysteresis	T_H	Temperature ralling			25		

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at V_{CC} = 12 V unless otherwise noted.

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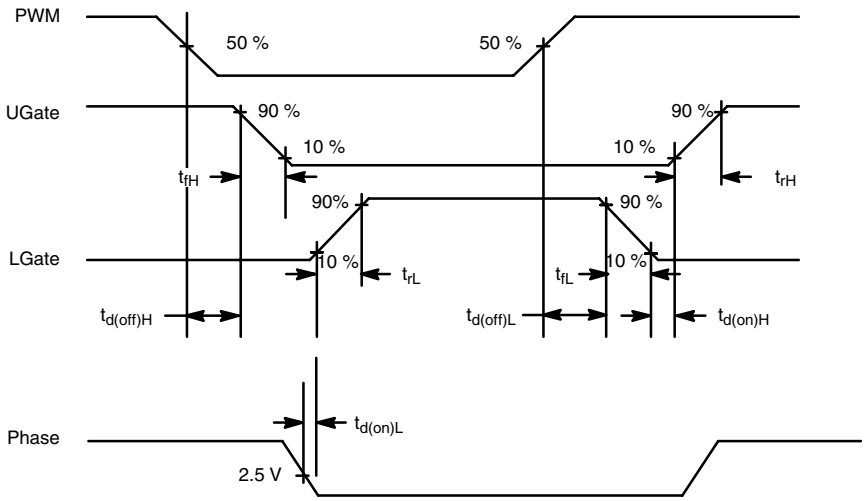
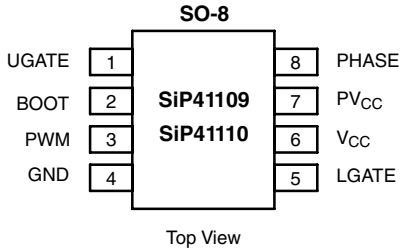
TIMING WAVEFORMS



PIN CONFIGURATION AND TRUTH TABLE



TRUTH TABLE

PWM	UGATE	LGATE
L	L	H
L	H	L
Tri-State	L	L

ORDERING INFORMATION

Part Number	Temperature Range	Marking
SiP41109DY-T1-E3	- 40 °C to 85 °C	41109
SiP41110DY-T1-E3		41110
Eval Kit	**Temperature Range**	
SiP41109DB	- 40 °C to 85 °C	
SiP41110DB		

PIN DESCRIPTION

Pin Number	Name	Function
1	UGATE	8 V high-side MOSFET gate drive
2	BOOT	Bootstrap supply for high-side driver. The bootstap capacitor is connected between BOOT and PHASE.
3	PWM	Input signal for the MOSFET drivers and tri-state enable
4	GND	Ground
5	LGATE	Synchronous or low-side MOSFET gate drive
6	V_{CC}	12 V supply. Connect a bypass capacitor ≥ 1 µF from here to ground
7	PV_{CC}	8 V voltage regulator Output. Connect a bypass capacitor ≥ 1 µF from here to ground
8	PHASE	Connection to source of high-side MOSFET, drain of the low-side MOSFET, and the inductor

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FUNCTIONAL BLOCK DIAGRAM

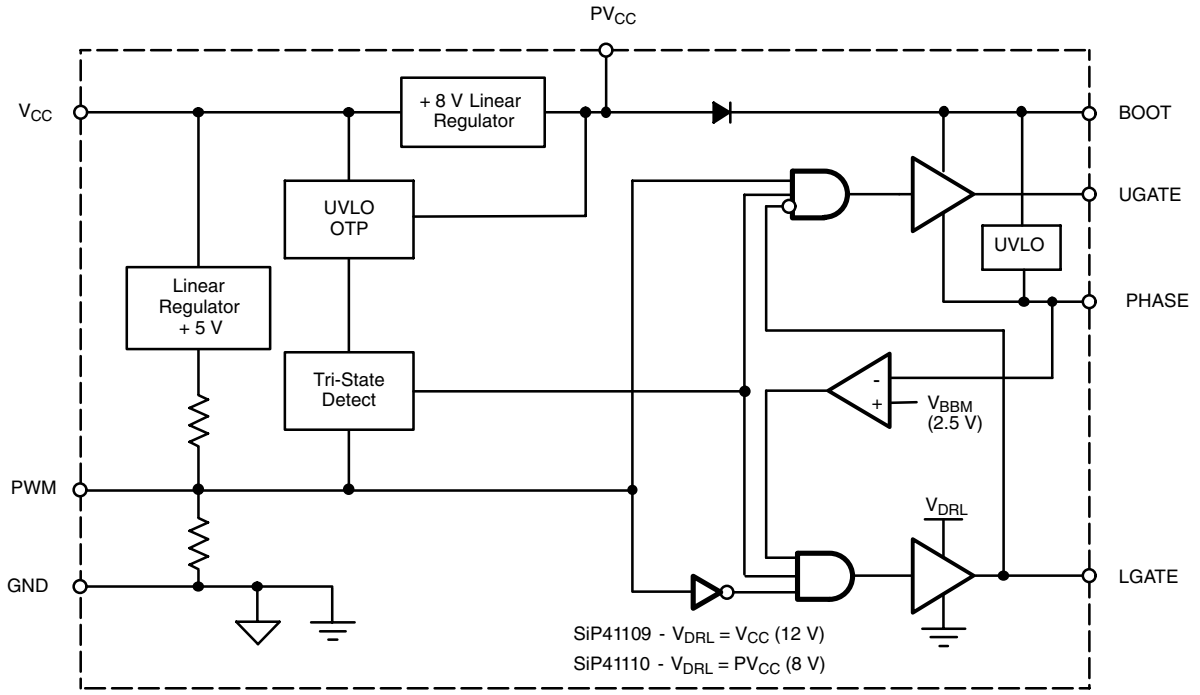

Figure 1.

DETAILED OPERATION

PWM/Tri-State Enable

The PWM pin controls the switching of the external MOSFETs. The driver logic operates in a noninverting configuration. The PWM input stage should be driven by a signal with fast transition times, like those provided by a PWM controller or logic gate, (< 200 ns). The PWM input functions as a logic input and is not intended for applications where a slow changing input voltage is used to generate a switching output when the input switching threshold voltage is reached.

Shutdown

The SiP41109/41110 enters shutdown mode when the signal driving PWM enters the tri-state window for more than 240 ns. The shutdown state is removed when the PWM signal moves outside the tri-state window. If the PWM is left open, the pin is held to 2.5 V by an internal voltage divider, thus forcing the tri-state condition.

Low-Side Driver

In the SiP41109, the low-side driver voltage is supplied by V_{CC}. In the SiP41110, the low-side driver voltage is supplied by PV_{CC}. During shutdown, LGATE is held low.

High-Side Driver

The high-side driver is isolated from the substrate to create a floating high-side driver so that an N-channel MOSFET can be used for the high-side switch. The high-side driver voltage is supplied by PV_{CC}. The voltage is maintained by a floating bootstrap capacitor, which is continually recharged by the switching action of the output. During shutdown UGATE is held low.

Gate Drive Voltage (PV_{CC}) Regulator

An integrated 80 mA, 8 V regulator supplies voltage to the PV_{CC} pin and it current limits at 200 mA typical when the output is shorted to ground. A capacitor (1 µF minimum) must be connected to the PV_{CC} pin to stabilize the regulator output. The voltage on PV_{CC} is supplied to the integrated bootstrap diode. PV_{CC} is used to recharge the bootstrap capacitor and powers the SiP41110 low-side driver. PV_{CC} pin can be externally connected to V_{CC} to bypass the 8 V regulator and increase high-side gate drive to 12 V. If the PV_{CC} pin is connected to V_{CC} the system voltage should not exceed 43 V.

Bootstrap Circuit

The internal bootstrap diode and an external bootstrap capacitor supply voltage to the BOOT pin. An integrated bootstrap diode replaces the external diode normally needed

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for the bootstrap circuit; only a capacitor is necessary to complete the bootstrap circuit. The bootstrap capacitor is sized according to

$C_{BOOT} = (Q_{GATE}/(\Delta V_{BOOT} - V_{PHASE})) \times 10$

where Q_{GATE} is the gate charge needed to turn on the high-side MOSFET and ΔV_{BOOT} - PHASE is the amount of droop allowed in the bootstrapped supply voltage when the high-side MOSFET is driven high. The bootstrap capacitor value is typically 0.1 µF to 1 µF. The bootstrap capacitor voltage rating must be greater than V_{CC} + 12 V to withstand transient spikes and ringing.

Shoot-Through Protection

The external MOSFETs are prevented from conducting at the same time during transitions. Break-before-make circuits monitor the voltages on the PHASE pin and the LGATE pin and control the switching as follows: When the signal on PWM goes low, UGATE will go low after an internal propagation delay. After the voltage on PHASE falls below 2.5 V by the inductor action, the low-side driver is enabled and LGATE goes high after some delay. When the signal on PWM goes high, LGATE will go low after an internal propagation delay. After the voltage on LGATE drops below 2.5 V the high-side driver is enabled and UGATE will go high after an internal propagation delay. If PHASE does not drop below 2.5 V within 380 ns after UGATE goes low, LGATE is forced high until the next PWM transition.

V_{CC} Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1 µF ceramic capacitor as close as practical between the V_{CC} and GND pins.

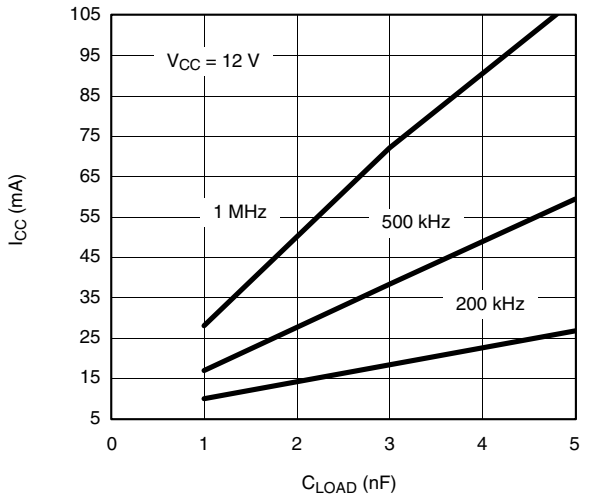
Undervoltage Lockout

Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces LGATE and UGATE to low when V_{CC} is below its specified voltage. A separate UVLO forces UGATE low when the voltage between BOOT and PHASE is below the specified voltage.

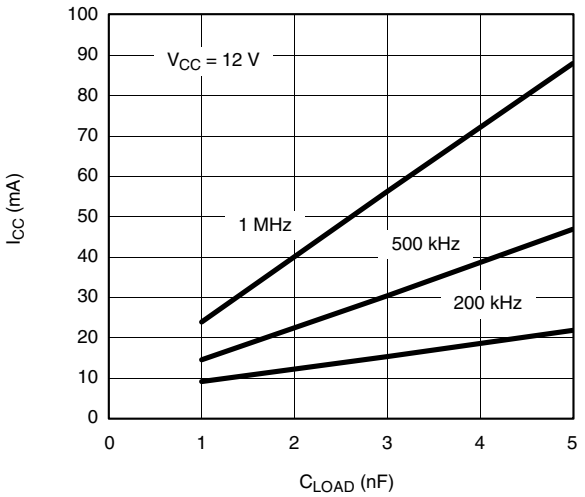
Thermal Protection

If the die temperature rises above 165 °C, the thermal protection disables the drivers. The drivers are re-enabled after the die temperature has decreased below 140 °C.

TYPICAL CHARACTERISTICS



I_{CC} vs. C_{LOAD} vs. Frequency (SiP41109)



I_{CC} vs. C_{LOAD} vs. Frequency (SiP41110)

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TYPICAL WAVEFORMS

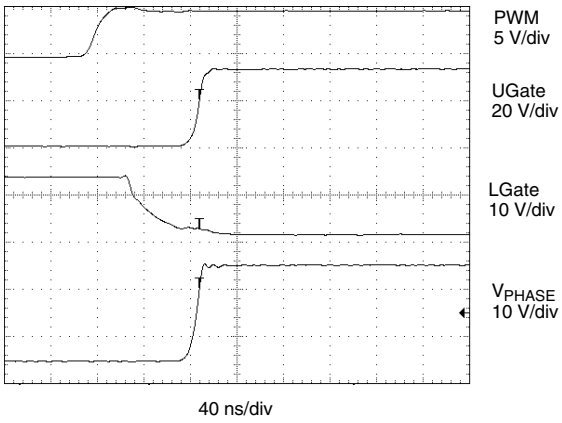

Figure 2. PWM Signal vs. HS Gate, LS Gate and PHASE (Rising)

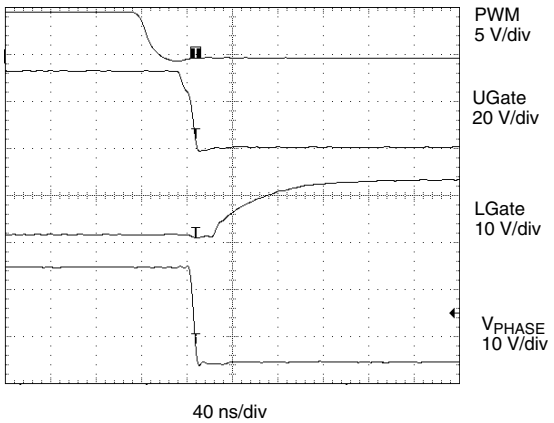

Figure 3. PWM Signal vs. HS Gate, LS Gate and PHASE (Falling)

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