TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Electrical Specifications

T_A = –40 to +125 ºC (typical specified at 25 ºC), VDD = 3 V (±10%) to 5 V (±10%), f = 400 kHz, unless specified

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage (V_{DD})		2.7	—	5.5	V
Supply Current	Fully enabled, input frequency = 1 MHz	—	4	7	mA
Undervoltage Lockout (V_{UVLO})		2.1	2.3	2.5	V
Undervoltage Lockout Hysteresis (V_{HYST})		—	100	—	mV
Logic Input HIGH Level	MODE, R1, R2, R3, R4 inputs (TTL compatible)	2.0	—	—	V
Logic Input LOW Level		—	—	0.8	V
Reset Time (t_R)	Time for 5% initial accuracy	150	—	—	ns
Reset Time Resistor Range[1]		15	—	2500	kΩ
R1, R2, R3, R4 Input Rise Time (t_{RR})		—	—	30	ns
R1, R2, R3, R4 Input Fall Time (t_{FR})		—	—	30	ns
Measurement Watchdog Timeout (t_{WD})		30	50	80	µs
Series Input Resistance	Measured from IIN to IOUT	—	1.3	—	mΩ
Series Inductance	Measured from IIN to IOUT	—	2	—	nH
Input/Output Delay[1]	OUT, OUT1, OUT2 delay relative to input	—	150	200	ns
Start-Up Self-Cal Delay (t_{CAL})[1]	Time from VDD = V_{UVLO} + V_{HYST} to cal complete	—	150	200	µs
Input Common Mode Voltage Range (dc) [1]	4x4 mm QFN	1000	—	—	V_{RMS}
	SOIC-20	5000	—	—	V_{RMS}
Operating Input Frequency Range (f)[1]		50	—	1000	kHz
DC Power Supply Rejection Ratio		—	40	—	db
Sensitivity @ VDD = 3 V	Si8501/11/17	—	404	—	mV/A
	Si8502/12/18	—	202	—	mV/A
	Si8503/13/19	—	101	—	mV/A
Sensitivity @ VDD = 5 V	Si8501/11/17	—	392	—	mV/A
	Si8502/12/18	—	196	—	mV/A
	Si8503/13/19	—	98	—	mV/A

Notes:
1. Guaranteed by design and/or characterization.
2. Maximum output load is not recommended to exceed 200 pF and 5 kΩ.
3. Production tested at 400 kHz (50% duty cycle) at VDD = 3.3 V.
4. See "2.4. Total Measurement Error" on page 11 for more information.

Table 1. Electrical Specifications (Continued)

T_A = –40 to +125 ºC (typical specified at 25 ºC), VDD = 3 V (±10%) to 5 V (±10%), f = 400 kHz, unless specified

Parameter	Conditions	Min	Typ	Max	Unit
OUT, OUT1, OUT2 Offset Voltage (V_{OUTMIN})	Current flow from I_{IN} to I_{OUT} = 0	—	50	—	mV
V_{OUT} Slew Rate[1,2]	OUT, OUT1, OUT2 load = 5K || 50 pF	—	50	—	V/µs
OUT, OUT1, OUT2 Output Resistance		20	—	130	Ω
Total Measurement Error (%) (–40 to 125 ºC Temp Range)	20% of full scale[3,4] (all devices)	–30	—	+30	%
	100% of full scale[3,4]	–10	—	+10	%

Notes:
1. Guaranteed by design and/or characterization.
2. Maximum output load is not recommended to exceed 200 pF and 5 kΩ.
3. Production tested at 400 kHz (50% duty cycle) at VDD = 3.3 V.
4. See "2.4. Total Measurement Error" on page 11 for more information.

Table 2. Regulatory Information[1] (SOIC-20 Only)

CSA
The Si85xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
VDE[2]
The Si85xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
UL
The Si85xx is certified under UL1577 component recognition program. For more details, see File E257455.

Notes:
1. All 5.0 kV_{RMS} rated devices are production tested to ≥6.0 kV_{RMS} for 1 sec. For more information, see "6. Ordering Guide" on page 26.
2. Pending.

Table 3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			SOIC-20	
Minimum Air Gap (Clearance)	L(1O1)		7.6 min	mm
Minimum External Tracking (Creepage)	L(1O2)		7.6 min	mm
Minimum Internal Gap (Internal Clearance)			0.2	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	V
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	1.4	pF
Input Capacitance[2]	C_I		4.0	pF

Notes:
1. To determine resistance and capacitance, the Si85xx is converted into a 2-terminal device. Pins 1–10 are shorted together to form the first terminal and pins 11–20 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 4. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Conditions	Specification
		SOIC-20
Basic Isolation Group	Material Group	IIIa
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 400 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 600 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 1000 V_{RMS}	I-III

Table 5. IEC 60747-5-2 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic	Unit
			SOIC-20	
Maximum Working Insulation Voltage	V_{IORM}		1414	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2652	V peak
Transient Overvoltage	V_{IOTM}	t = 60 s	8000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	W

Note: The Si85xx is suitable for basic and reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si85xx provides a climate classification of 40/125/21. Note that the Si85xx is compliant with the IEC60747-5-2 but neither certified nor inspected to IEC60747-5-2. The Si85xx is compliant, certified, and factory-inspected to IEC60950.

Table 6. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	SOIC-20	Unit
Case Temperature	T_S		150	°C
Safety Input Current	I_S	θ_{JA} = 85, V_{DD} = 5.5 V, IIN to IOUT = 20 A, T_J = 150 °C, T_A = 25 °C	30	A
Device Power Dissipation[2]	P_D		0.9	W

Notes:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 1.
2. The Si85xx is tested with V_{DD} = 5.5 V, T_J = 150 ºC, C_L = 15 pF, and with an input current from IIN to IOUT equal to 20 Amps at 500 kHz (duty cycle = 50%).

Table 7. Thermal Characteristics

Parameter	Symbol	Test Condition	SOIC-20	4x4 mm QFN	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}		85	55	°C/W

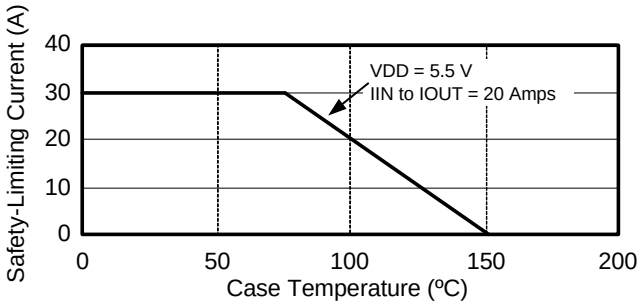

Figure 1. SOIC-20 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 8. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Units
Storage temperature	T_{STG}	–65	—	+150	°C
Ambient temperature under bias	T_A	–40	—	+125	°C
Junction Temperature	T_J	—	—	150	°C
Supply voltage	V_{DD}	—	—	5.75	V
Voltage on any pin with respect to ground (not including IIN, IOUT)	V_{IN}	–0.5	—	VDD + 0.5	V
Output Current Drive	L_O	—	—	10	mA
Lead solder temperature (10 s)		—	—	260	ºC
Maximum Input Current Rate of Change		—	—	1000	A/µs
Maximum Peak AC Input Current Limit		—	—	200	A
Thermal Limit (DC Current)[2]		—	—	30	A
Maximum Isolation Voltage (QFN)		—	—	1400	V_{RMS}
Maximum Isolation Voltage (SOIC-20)		—	—	6000	V_{RMS}
ESD (CDM)	JEDEC (JESD22-C101C)	–1.5		+1.5	kV
ESD (HBM)	JEDEC (JESD22-A114E)	–2500		+2500	V
ESD (MM)	JEDEC (JESD22-A115A)	–250		+ 250	V

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Refer to “AN329: Extending the Full-Scale Range of the Si85xx” for more information.

2. Functional Overview

The Si85xx ac current sensor family of products mimics the functionality of traditional current transformer (CT) circuits with burden resistor, diode, and output filter, but offers enhanced performance and added capabilities. These devices use inductive current sensing and on-board signal conditioning electronics to generate a 2 V full-scale output signal proportional to the ac current flowing from the IIN to the IOUT terminals. As shown in Figures 2 and 3, current flowing through the metal package slug induces a signal in the pickup coil on the Si85xx die. This signal is applied to the input of an integrator that reconstructs the ac current flowing from IIN to IOUT. Onboard circuitry provides cycle-by-cycle integrator reset and temperature and offset voltage compensation to achieve initial measurement accuracy to within ±5%.

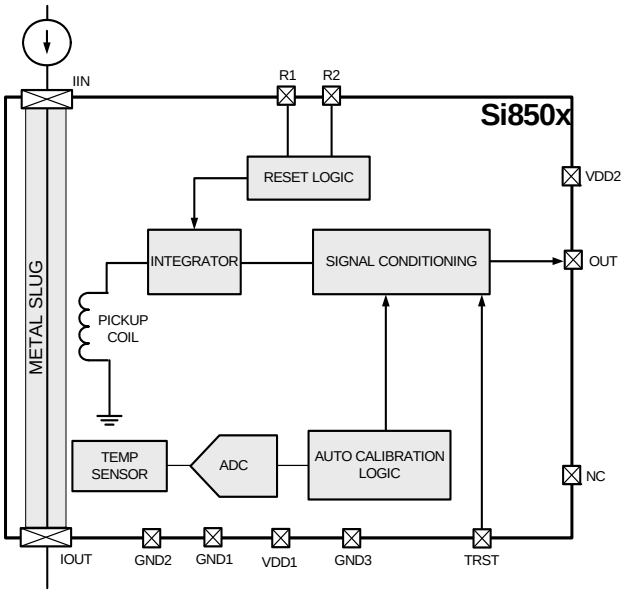

Figure 2. Si850x (Single Output) Block Diagram

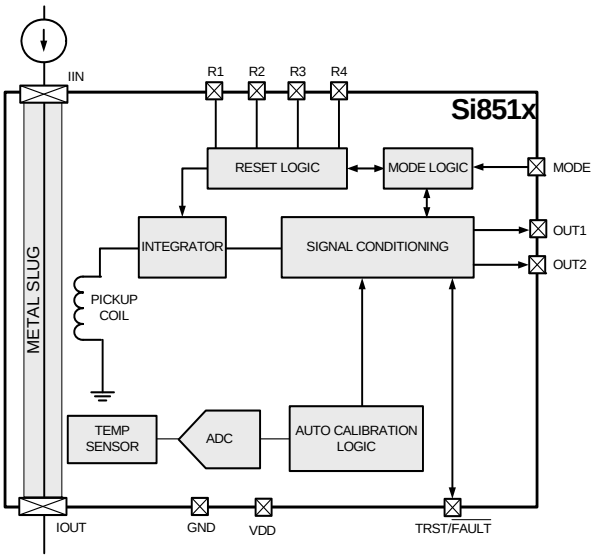

Figure 3. Si851x (Ping Pong Output) Block Diagram

The Si85xx is superior to other current sensing approaches and benefits the system in a number of ways:

- **Small size:** With its 4x4 mm footprint and 1 mm height (QFN package option), the Si85xx is among the smallest current sensors available.
- **Large output signal:** The nominal 2.0 V full-scale output swing offers superior noise immunity versus other current sensing technologies.
- **Low loss:** The Si85xx adds only 1.3 mΩ (at 25 °C) to the sensing path, making it one of the lowest-loss current sensors available. Low 2 nH primary series inductance is 2,000 times lower compared to a CT and results in significantly less ringing.
- **High precision:** All versions are available with an initial maximum error of ±5% of reading; one of the most accurate current sensors available.
- **Ping-Pong output mode (Si851x):** Alternately routes the current measurements from each side of a full-bridge circuit to separate output pins for comparison, which is very useful for transformer flux balancing applications. Eliminates a second CT in a full-bridge application.
- **Leading edge noise suppression:** Filters out reflected noise due to long reverse recovery time of output rectifier. Eliminates the need for external leading edge blanking circuit.
- **High common-mode voltage:** The Si85xx offers a minimum of 1,000 V_{RMS} (for QFN package) or 5 kV_{RMS} (for SOIC package) of common-mode voltage range (or isolation), making it useful over a very wide voltage range.

- **$\overline{\text{FAULT}}$ output (Si8517/8/9):** Goes low when external reset timing is in error.
- **Ease-of-use:** Other than conventional power and grounding techniques, no special board layout considerations are required. Built-in timing interface circuits allow already-available system switching signals to be used for reset with no external circuits required.

2.1. Under Voltage Lockout (UVLO)

UVLO is provided to prevent erroneous operation during device start-up and shutdown or when VDD is significantly below the specified operating range. The Si85xx is in UVLO state when VDD ≤ V_{UVLO} (Figure 4). During UVLO, the output(s) are held at minimum value regardless of the amount of current flowing from IIN to IOUT, and signals on integrator reset inputs R1–R4 are ignored. The Si85xx exits UVLO when VDD ≥ (V_{UVLO} + V_{HYST}).

2.2. Device Startup

Upon exit from UVLO, the Si85xx performs a voltage offset and temperature self-calibration cycle. During this time, output(s) are held at minimum value and reset inputs (R1-R4) are ignored. The reset inputs are enabled at the end of the self-calibration cycle, and an integrator reset cycle is initiated on the first occurrence of active signals on R1–R4. A current measurement is initiated immediately after the completion of the integrator reset cycle, and the resulting current waveforms appear on the output pins. This "reset-measure-reset" pattern repeats throughout steady-state operation.

2.3. Integrator Reset and Current Measurement

The Si85xx measures current flowing from the IIN to IOUT terminals. Current is allowed to flow in the opposite direction, but will not be measured (OUT1 and OUT 2 remain at their minimum values during reverse current flow. Reverse current flow will not damage the Si85xx).

To achieve the specified accuracy, the integrator capacitor must be discharged (reset) for time period t_R prior to the start of every measurement cycle. This cycle-by-cycle reset is implemented by connecting existing system gate control signals to the R1–R4 inputs in a way that resets the integrator when no current is flowing from IIN to IOUT. To achieve rated accuracy, the reset cycle must be completed prior to the start of the measurement cycle. For maximum flexibility, integrator reset operation can be configured in one of two ways:

Option 1: The start and duration of reset is determined by the states of the timing signals applied to R1–R4.

Option 2: The timing signals applied to R1–R4 trigger the start of reset, and the duration of the reset is determined by an onboard programmable reset timer.

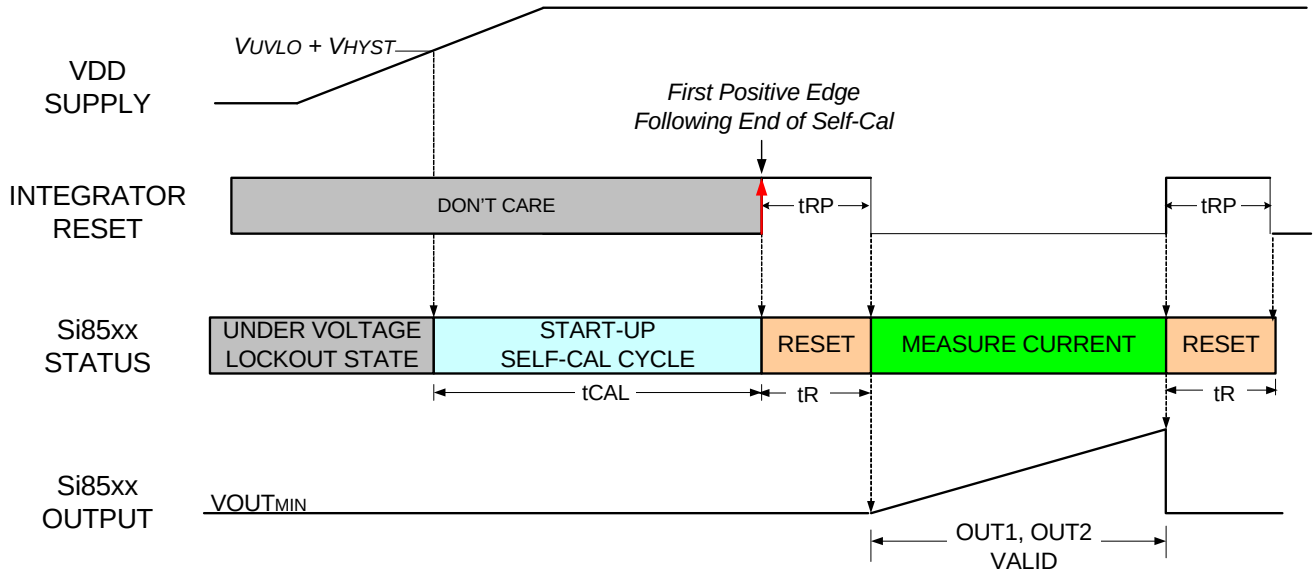

Figure 4. Si85xx Startup and Control Timing

Integrator reset Option 1 is selected by connecting T_{RST} to VDD. In this mode, the Si85xx is held in reset as long as the signals on R1–R4 satisfy the logic equations of Table 11. It is typically used in applications where the gate drivers are external to the system controller IC (the gate driver delay ensures reset is completed prior to the start of measurement).

Reset Option 2 is selected by connecting a timing resistor (R_{TRST} in Figure 5) from the TRST input to ground. It is typically used in applications where the gate drivers are on-board the controller. In this mode, the on-chip reset timer is triggered when the signals on R1–R4 satisfy the logic equations in Table 11. Once triggered, the timer maintains integrator in reset for time duration t_R as programmed by the value of resistor R_{TRST}. The user must select the value of resistor R_{TRST} to terminate the reset cycle prior to the start of measurement under worst-case timing conditions. Note that values of t_R below the specified value in "1. Electrical Specifications" on page 4 results in increased integrator output offset error and increased output noise on V_{OUT}. Moreover, t_R's time is summarized by the following equation (see Table 9):

$$t_R = 10\ ns/k\Omega$$

where values of R_{TRST} that produce a reset time less than 150 ns ($R_{TRST} \leq 15\ k\Omega$) should not be used.

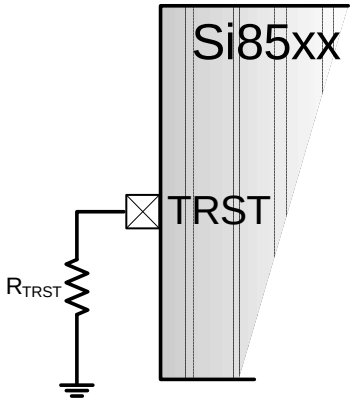

Figure 5. Programming Reset Time (t_R)

Table 9. Typical Reset Time vs. R_{TRST} Resistance

R_{TRST}	Reset Time (t_R)
15 kΩ	150 ns
100 kΩ	1 µs
1 MΩ	9 µs
2.2 MΩ	20 µs

2.4. Total Measurement Error

The Si85xx's absolute accuracy is affected by the following factors:

- Ambient operating temperature
- VDD supply voltage
- Time

Table 10 includes a composite of all environmental and operating conditions that can ultimately affect the absolute measurement accuracy of the Si85xx. The total worst-case accuracy at full scale can be estimated by the sum of the initial accuracy (up to ±5%) plus aging (up to ±1.5%) and supply variations (up to ±3.5%). For example, the total measurement error expected for a device operating at a given V_{DD} supply of 5 V (±10%) is 10% if the device is operated over a temperature range of –40 to 125 °C for up to 10 years. If the temperature range is limited to 0 to 85 °C, the measurement error can be improved by up to 2%. See Figure 6 for details.

Table 10. Total Measurement Error Contributors

Error Contributor	% Error Added
Initial error @ given V_{DD} ±10%, 25 °C	±5%
Temperature variation –40 to 125 °C	±3.5%
Aging (10 years)	±1.5%

2.5. Effect of Temperature on Accuracy

Offset voltage present at the Si85xx output terminals (output offset voltage) is calibrated out each time VDD is applied to the Si85xx; so, its error contribution is minimized when the temperature at which calibration occurred is at or near the steady-state operating temperature of the Si85xx. For example, applying VDD at 25 °C (offset cal is performed) and operating at 85 °C will result in a larger offset error than operating at 50 °C. The effect of this error is summarized in Figure 6. The chart is referenced to 25 °C. If the Si85xx is powered up at 25 °C and then operated at 125 °C with no auto-calibration performed (i.e., the power is not cycled at 125 °C, which causes an auto-calibration), a 3% measurement error can be expected.

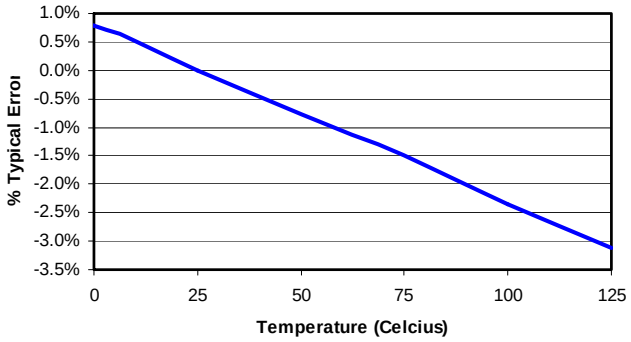

Figure 6. Differential Temperature Calibration Error

Figure 7 shows the Si85xx thermal characteristics of the on-chip sense resistance over the temperature range of –40 to +125 °C. Series inductance is constant at 2 nH (max) across this same temperature range.

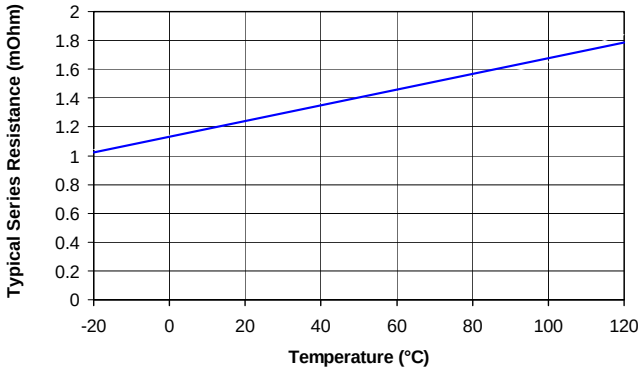

Figure 7. Series Resistance Thermal Characteristics

2.6. Leading Edge Noise Suppression

High-amplitude spikes on the leading edge of the primary switching waveforms can cause the PWM latch to be erroneously reset at the start of the switching cycle when operating in current mode control. To prevent this problem, leading edge blanking is commonly used to disable the current comparator during the early portion of the primary-side switching cycle. The Si85xx eliminates leading-edge noise spikes by including them in the signal integration. As shown in the output waveform of Figure 8 (Si8502 waveform measured directly on OUT pin with no external filter), noise present in the input waveform is eliminated without the use of blanking.

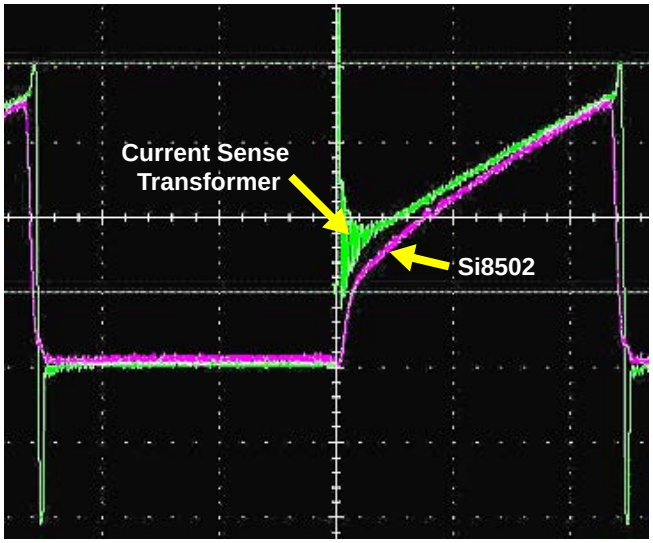

Figure 8. Leading-Edge Noise Suppression Waveforms (200 kHz, 9.3 A Load)

2.7. $\overline{\text{FAULT}}$ Output

The $\overline{\text{FAULT}}$ output (Si8517/8/9) guards against Si85xx output signal errors caused by missing reset cycles. $\overline{\text{FAULT}}$ is asserted when a measurement cycle exceeds the internal watchdog timer times limit of t_{WD}. $\overline{\text{FAULT}}$ can be used to alert a local microcontroller or digital power controller of a current sense failure or to initiate a system shutdown. To detect faults, tie a 200 kΩ resistor from TRST/$\overline{\text{FAULT}}$ to VDD.

2.8. Safe Operating Limits

The Si85xx is a very robust current sensor. Its maximum input current rate of change is limited to 1000 A/µs. The maximum peak ac input current limit is 200 A. The thermal limit or continuous dc current flow limit is 30 A. Exceeding these limits may cause long-term reliability issues. Refer to “AN329: Extending the Full-Scale Range of the Si85xx” for more information.

3. Application Information

3.1. Board Layout

The Si85xx is connected in the series path of the current to be measured. The Si85xx must be located as far as possible from transformer and other magnetic field sources. Like other analog components, the Si85xx should be powered from a low-noise dc source and, preferably, to a low-noise analog ground plane. Recommended bypass capacitors are 1 µF in parallel with a 0.1 µF, positioned as close to the Si85xx as possible. *When using the Si850x (single output versions), all three ground pins MUST be connected to the same ground point, and both VDD1 and VDD2 pins MUST be tied to the VDD system power supply.*

3.2. Layout Requirements

The Si85xx requires special layout techniques to ensure proper operation (see Figures 9 and 10). Due to the close proximity of the current-carrying slug and current sensor silicon, magnetic coupling between the current-carrying slug and the silicon can form a ground loop causing the output voltage to be 0 V even though current is flowing through the slug. To eliminate any such coupling issues, a red fly-wire VDD trace (see Figures 9 and 10) should be implemented in the layout. For the SOIC package, the red fly-wire trace should be approximately 3.5 mm from the center edge of the package intersecting approximately in the center of the package (see Figure 9). For the QFN package, the red fly-wire should be approximately in the center of the package (see Figure 10). Standard wire thicknesses for 10 mA current-carrying capabilities should be used. Moreover, note that the fly-wire trace should be completely under the ground plane since this will also reduce coupling.

Regarding isolation voltage requirements, the trace does not need to follow the lead frame and bonding traces exactly, as long as the net magnetic flux is close to zero. The goal here is to keep the magnetic coupling small and, at the same time, keep the isolation distance large. Moreover, to ensure that the layout meets the design's required creepage and clearance requirements, the VDD trace should be placed on one of the inner layers or even the back side of the board. For example, one can lay out the return VDD trace on the other side of the PCB so the PCB itself can help to provide high isolation voltage.

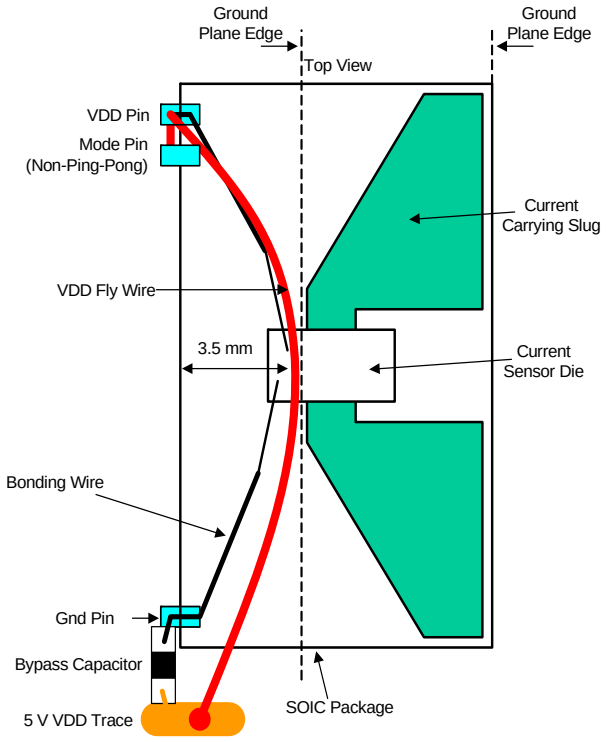

Figure 9. SOIC Layout Requirements

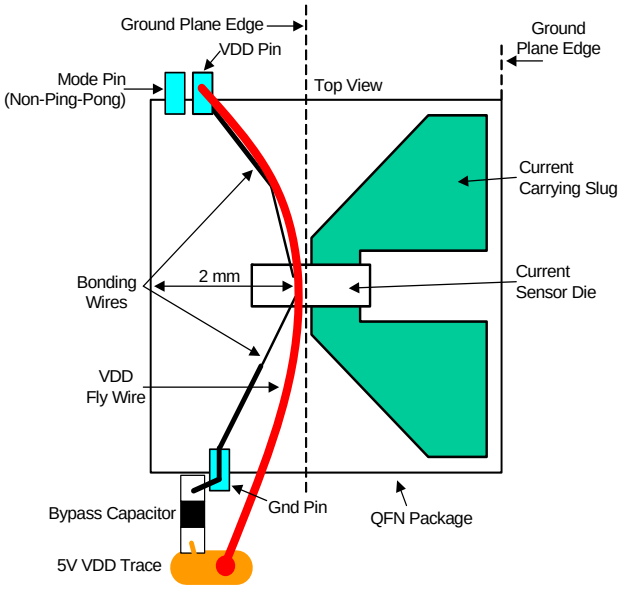

Figure 10. QFN Layout Requirements

3.3. Device Configuration

Configuring the Si85xx involves the following steps:

1. Selecting an output mode
2. Configuring integrator reset timing
3. Setting integrator reset time t_R

3.3.1. Device Selection

The Si85xx family offers three output modes: Single output (Si850x), and 2 and 4-Wire Ping Pong (Si851x). The Si851x products can be configured to operate in all three of these output modes.

The Si850x products operate ONLY in Single output mode. Most half-wave and single-phase applications require only Single output mode and will typically use the Si850x.

In Single output mode, output current always appears on the OUT pin (Si850x) or the OUT1 pin (Si851x). A single integrator reset signal is typically sufficient when operating in this mode.

Ping-Pong mode routes the current waveform to two different output pins on alternate measurement cycles. It is useful in full-wave and push-pull topologies where external circuitry can be used to monitor and/or control transformer flux balance. *(Section "3. Application Information" on page 13 shows design examples using both output modes in various power topologies.)*

2-wire Ping-Pong mode is useful mainly in non-overlapping two-phase buck converters but may also be used in full-bridge applications. In this output mode, reset inputs R1 and R2 are used, and input R3 is grounded. Measured current appears on OUT1 when R1 is high and on OUT2 when R2 is high as shown in the full-bridge timing example of Figures 11 and 12.

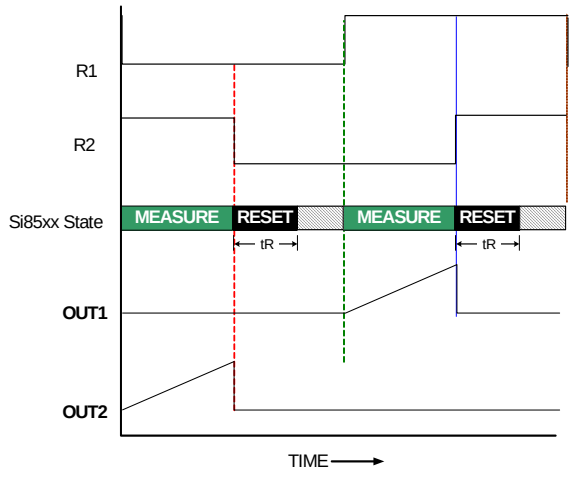

Figure 11. Two-Phase Buck Timing Example A

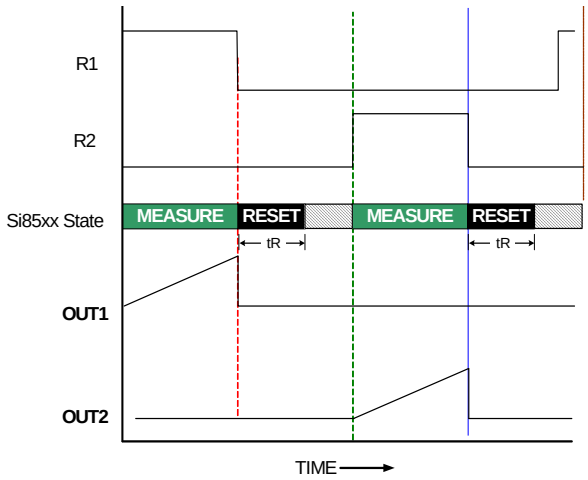

Figure 12. Full-Bridge Timing Example B

4-Wire Ping-Pong mode is recommended for full-bridge applications over 2-wire because it uses all four inputs, making the reset function tolerant to single-point signal failures. In 4-Wire Ping-Pong mode, current appears on OUT2 when R1 is high and R2 is low, and appears on OUT1 when R3 is high and R4 is low as shown in the full-bridge timing example of Figure 13. Table 11 shows the states of the Mode and R4 inputs that select each output, and the resulting reset logic functions and truth tables.

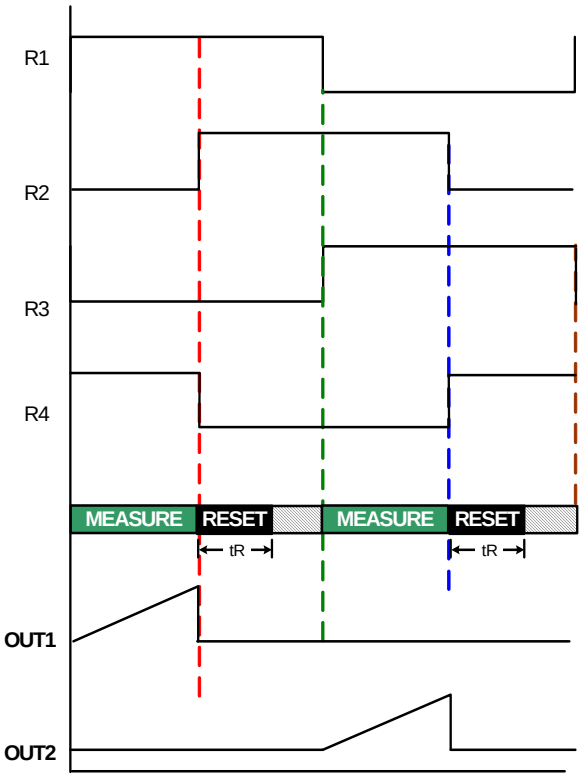

Figure 13. Full-Bridge Timing Example C

3.3.2. Selecting Reset Timing Signals

Reset timing signals should be chosen to meet the following conditions:

- Satisfy reset time t_R
- Not overlap integrator reset into the desired measurement period
- Not violate reset watchdog timeout period t_{WD}

3.3.3. Configuring Integrator Reset

Per Section “2. Functional Overview”, the integrator must be reset (zeroed) prior to the start of each measurement cycle to achieve specified measurement accuracy. This reset must be synchronized with the system switch timing signals to ensure that current is measured during the appropriate time; so, the Si85xx integrator reset circuitry uses system timing as its reference. Timing signals connect to reset inputs R1 through R4 where built-in logic functions allow the user to choose the conditions that cause an integrator reset event. *Important Note: reset inputs R1–R4 are rated to a maximum input voltage of VDD. External resistor dividers must be used when connecting driver output signals to R1–R4 that swing beyond VDD.*

As shown in Table 11, the Si850x integrator reset logic is a simple XOR gate where reset is maintained (or triggered, depending on use of the TRST input) when states of reset inputs R1 and R2 are not equal.

Figure 14 shows the logic for the Si851x products, where any one of three reset logic functions can cause integrator reset. The output mode (Si851x) is determined by the states of the Mode and R4 inputs, as shown in Table 11.

Table 11. Si85xx Output and Reset Mode Summary

Output Mode	MODE	R4	R3	R2	R1	Reset State[1]	Reset Logic Expression
Single-Ended[2]	1	0	0	0	0	0	RESET = XOR[R1, (R2|R3)]
				0	1	1	
				1	0	1	
				1	1	0	
			1	0	0	1	
				0	1	0	
				1	0	1	
				1	1	0	
2-Wire Ping Pong	1	1	0	0	0	1	RESET = XNOR[R1,(R2|R3)]
				0	1	0	
				1	0	0	
				1	1	1	
4-Wire Ping Pong	0	0	0	0	0	0	RESET = (R1&R2)|(R3&R4)
				0	1	0	
				1	0	0	
				1	1	1	
			1	0	0	0	
				0	1	0	
				1	0	0	
				1	1	1	
		1	0	0	0	0	
				0	1	0	
				1	0	0	
				1	1	1	
			1	0	0	1	
				0	1	1	
				1	0	1	
				1	1	1	

Notes:
1. Device is in reset when Reset State = 1.
2. For Si850x devices, RESET = XOR [R1, R2].

As explained in Section “2.3. Integrator Reset and Current Measurement”, the signals applied to R1–R4 can control integrator reset in real time (Option 1), or they can trigger a reset event of programmable duration (Option 2). Referring to Figure 14, reset timing is exclusively a function of the signals applied to R1–R4 when TRST is tied to VDD.

If not connected to VDD, the reset timer is enabled, and TRST *must* be connected through a resistor to ground to set the reset duration (t_R). Note that the reset timer is retriggerable and generates a timed integrator discharge pulse whenever the reset logic output transitions from low to high.

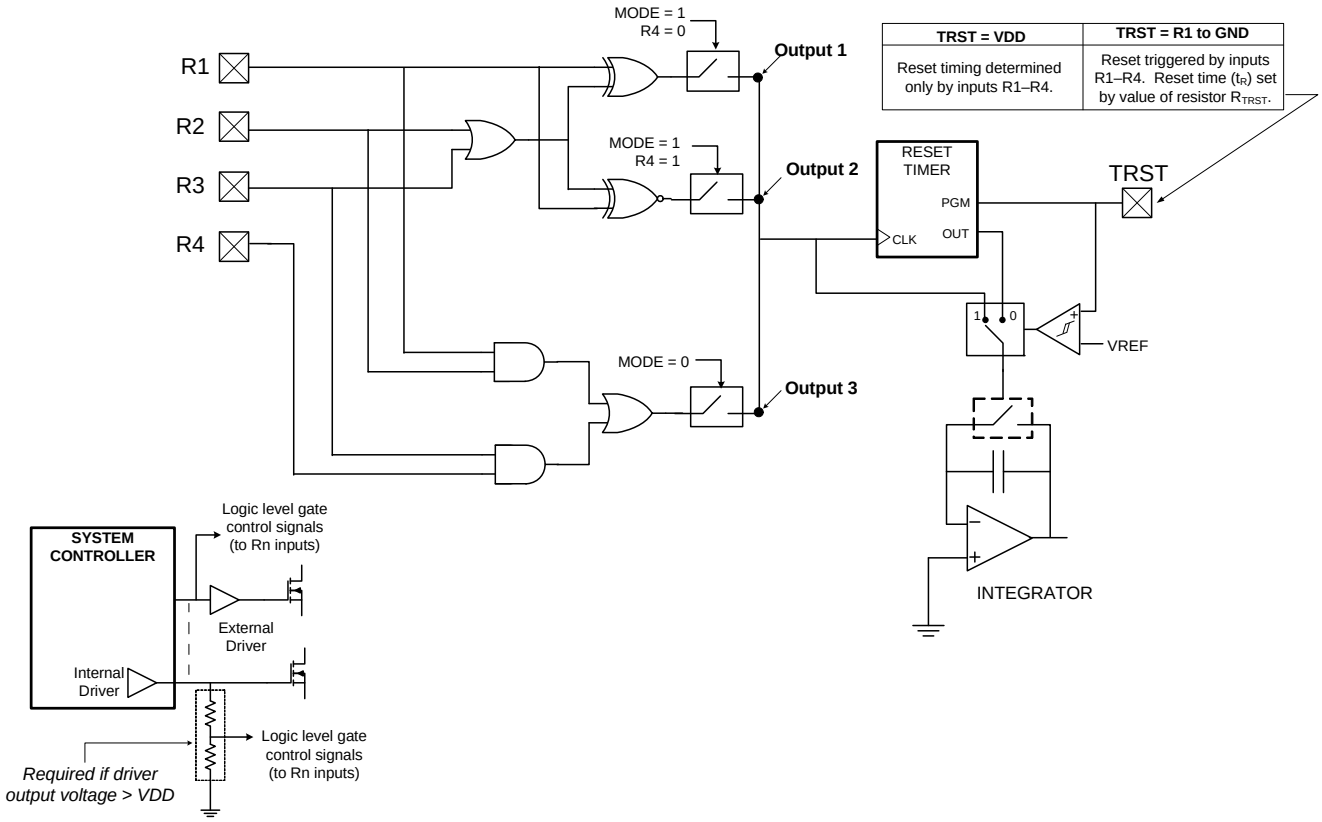

Figure 14. Si851x Integrator Reset Logic

3.3.4. Setting Reset Time t_R

The programmable reset timer is triggered when the states of the signals applied to R1–R4 cause the associated logic expression in Table 11 to go high (transition to the TRUE state).

Because this timer is re-triggerable, R1–R4 must remain TRUE for the duration of the desired t_R as shown in Figure 15. Should R1–R4 transition FALSE during t_R, integrator reset will be immediately halted, resulting in lower measurement accuracy due to higher integrator offset error.

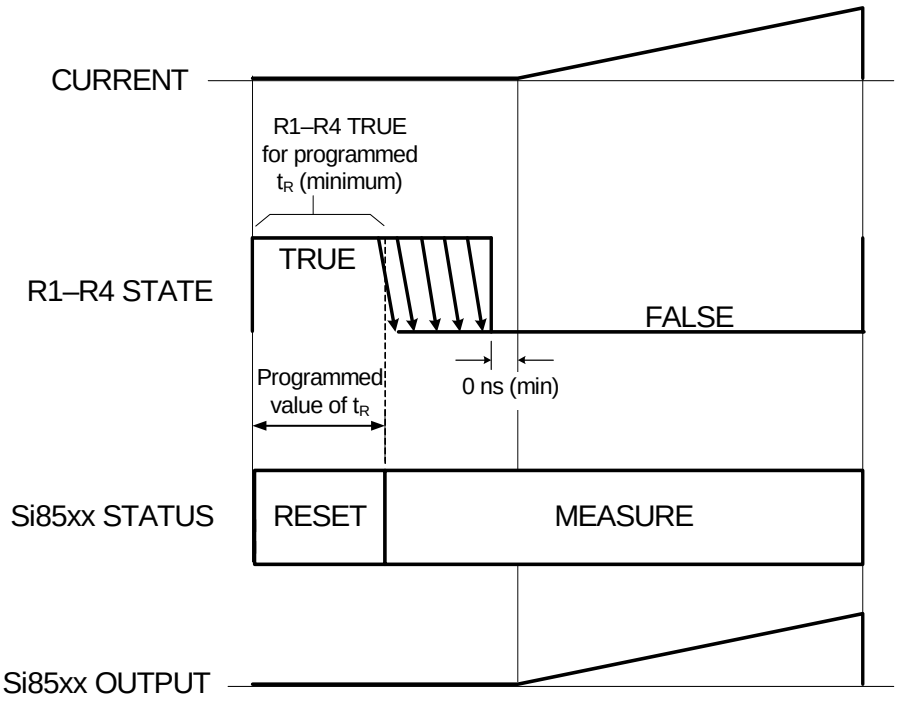

Figure 15. Correct t_R Programming Using Resistor from TRST Input to Ground

3.3.5. Measurement Watchdog Timer and $\overline{\text{FAULT}}$ Output

A built-in watchdog timer disables measurement and holds OUT or OUT1 and OUT2 at their minimum values when the time between integrator resets exceeds the $\overline{\text{FAULT}}$ Detect Time. The output signal from this watchdog is available on the $\overline{\text{FAULT}}$ output pin (Si8517/8/9 only).

Figure 16 illustrates two means of entering a fault condition. Either fault condition 1 or 2 occurs when the reset period exceeds the $\overline{\text{FAULT}}$ Detect Time, which ranges from 30 to 80 µs due process variations. The fault condition ends when the next logic reset cycle begins.

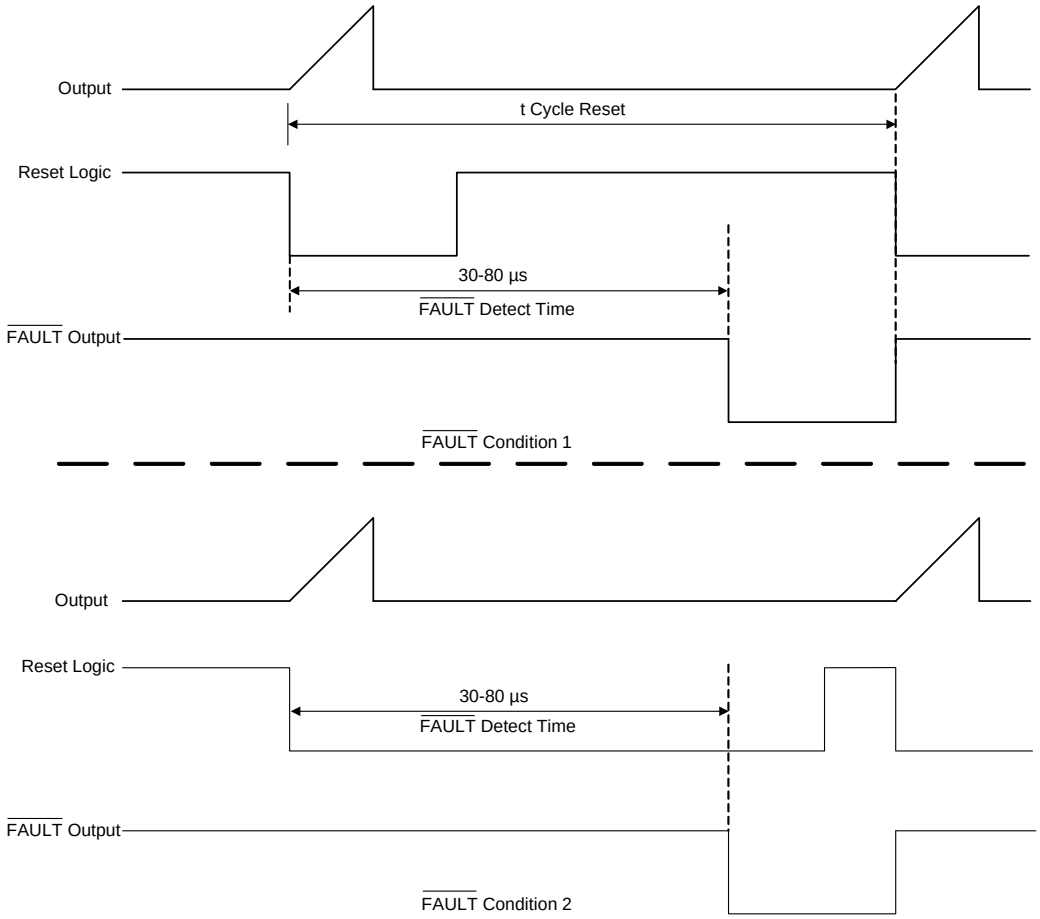

Figure 16. Measurement Watchdog Timer Operation

3.3.6. Output Over-Range

The Si85xx can be over-ranged by more than 100% with no adverse effects. For instance, if the Si8512 (a 10 A nominal full-scale device) has a 15 A peak current applied, then the output voltage (OUT) will be 3 V (assuming VDD = 5 V). If a 10 A peak current is applied, then the output returns to the nominal 2 V output. The head room of OUT is VDD–1.4 V. Figure 17 illustrates the head room limitation of the Si85xx versus supply.

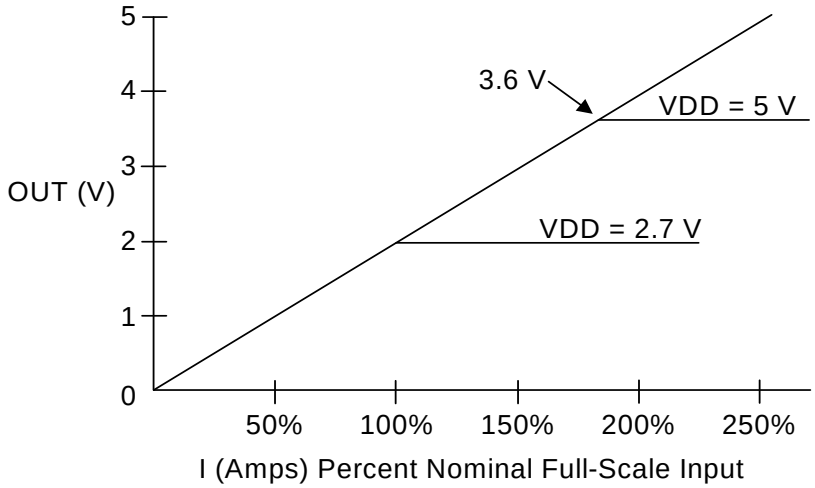

Figure 17. Headroom Limitation

3.4. Single-Phase Buck Converter Example

In this example, the Si850x is configured to operate in a single-phase synchronous buck converter (Figure 18). This converter has a PWM frequency of 1 MHz and a maximum duty cycle of 80%.

This is an example of a half-wave application that can be addressed with Single-Ended output mode. The PWM period is calculated to be $1/10^{-6}$ = 1.0 µs, and the worst-case value, t_R, is 0.2 x 1.0 x 10^{-6} = 200 ns at 80% maximum duty cycle (R_{TRST} = 20 kΩ).

In this example, the current measurement is made when the buck switch is on; so, PH2 is chosen as the reset signal by connecting PH2 to R1 and grounding R2. The PH2 signal can be obtained at the input of the driver external to the PWM controller or the output of the controller's internal driver (through a resistor divider if the driver output swings beyond the device VDD range).

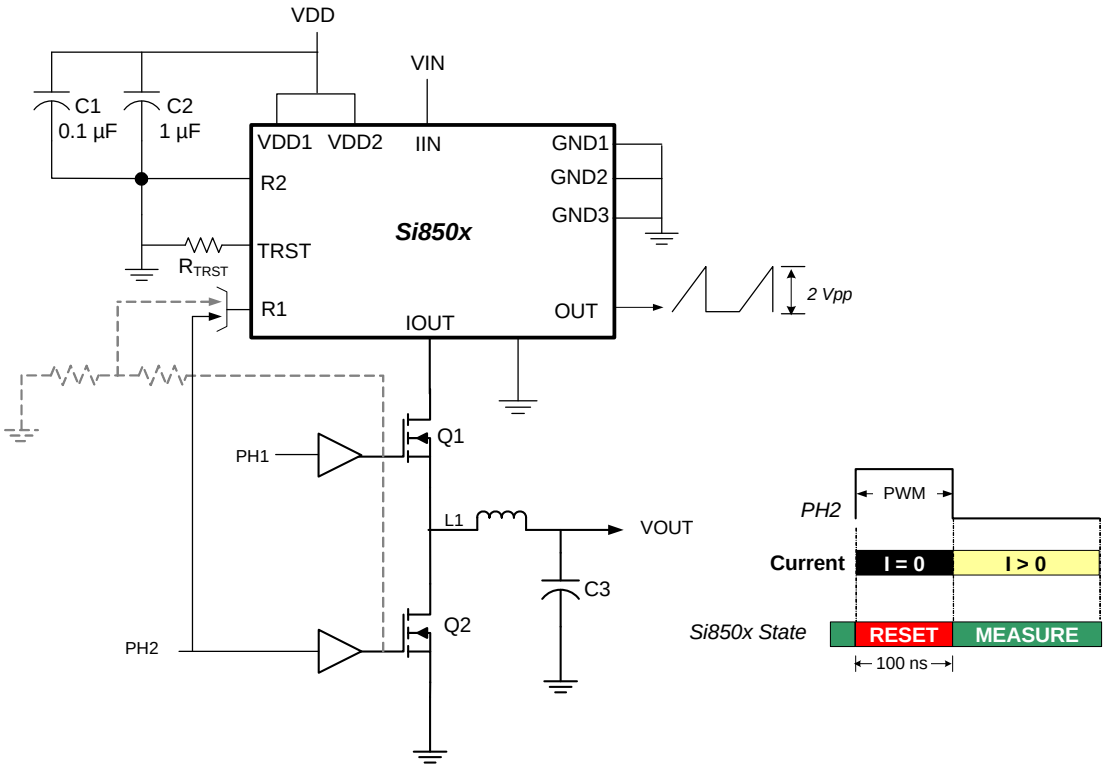

Figure 18. Si850x Single-Phase Buck Converter

3.5. Full-Bridge Converter Example

The full-bridge circuit of Figure 19 uses an Si851x configured in 4-Wire Ping-Pong output mode. The switching frequency of this phase-shifted full-bridge is 150 kHz, and the maximum control phase overlap is 70%.

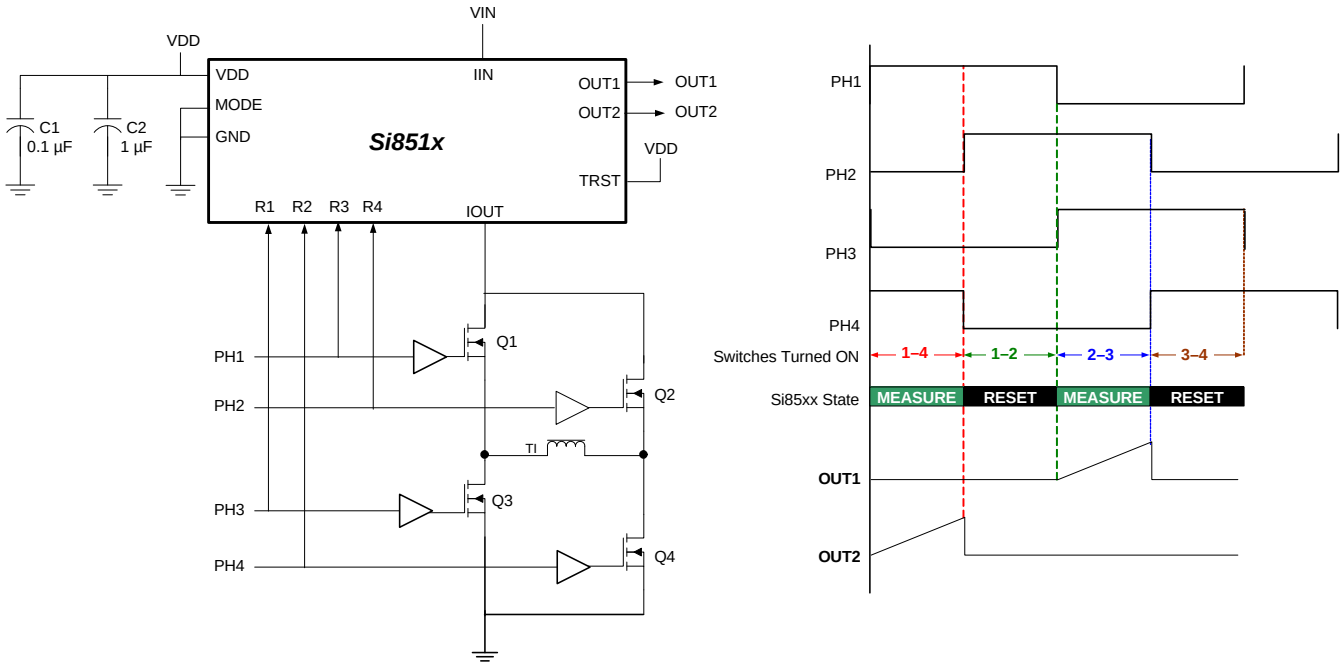

Figure 19. Full-Bridge Converter

Given the 150 kHz switching frequency (duty cycle fixed at 50%), the equivalent period is $1/150 \times 10^3 = 6.6$ µs. At 70% maximum overlap, this equates to a worst-case t_R value of $0.3 \times 6.6 \times 10^{-6} = 1.98$ µs. The default value for t_R can, therefore, be used and is selected by connecting TRST to VDD. As shown in the timing diagram of Figure 19, integrator reset occurs when current circulates between Q1 and Q2 and between Q3 and Q4 (i.e. when current is not being sourced from VIN). The external driver delay ensures reset is complete prior to the start of measurement.

3.6. Push-Pull Converter Example

The Push-Pull converter of Figure 20 uses 2-Wire Ping Pong output mode. As shown in the timing diagram, the integrator reset occurs when the inputs of both the PH1 and PH2 drivers are low. As shown, TRST is connected to VDD, selecting the default value of t_R (250 ns). Assuming an 80% maximum duty cycle, this value of t_R would deliver specified accuracy over a PWM frequency range of 50 to 400 kHz. Frequencies above 400 kHz would require the selection of a lower t_R value by connecting a resistor from TRST to ground.

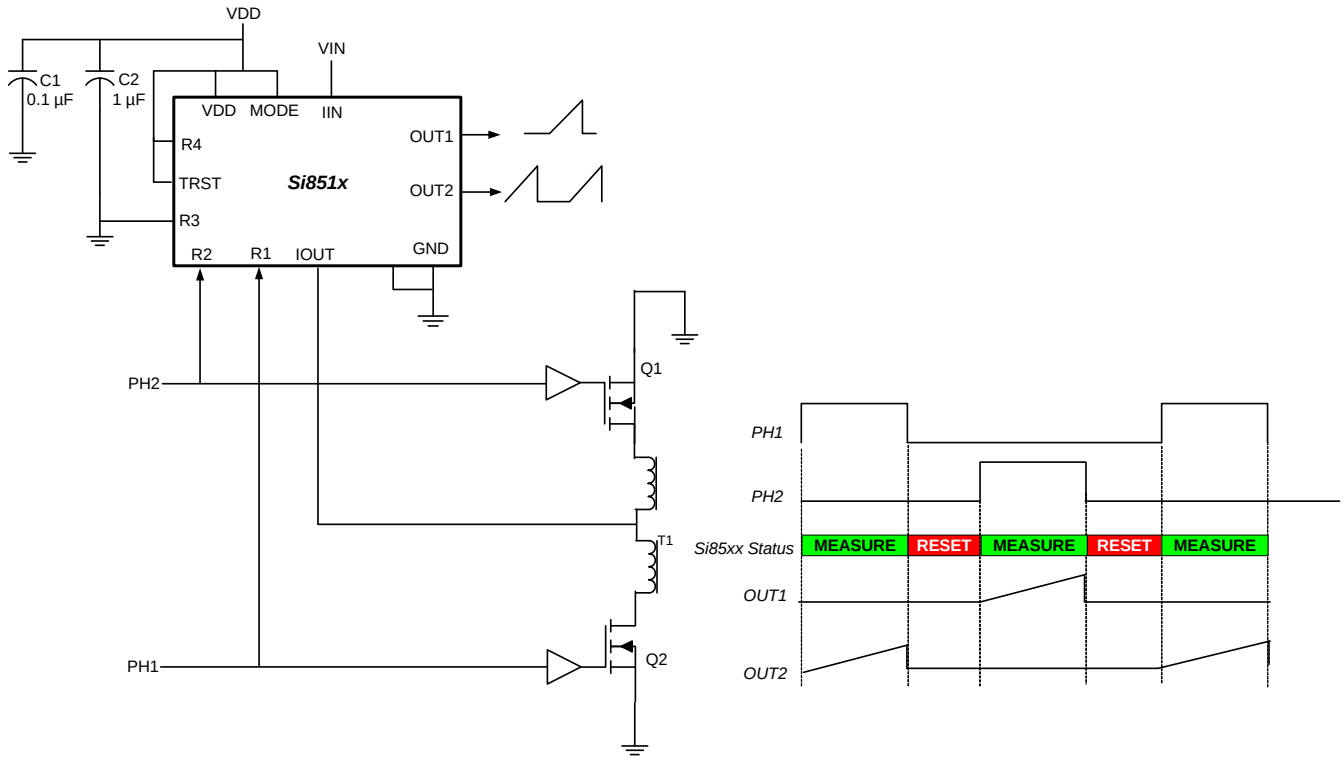

Figure 20. Push-Pull Example Using Default t_R Value

4. Pin Descriptions—12-Pin QFN

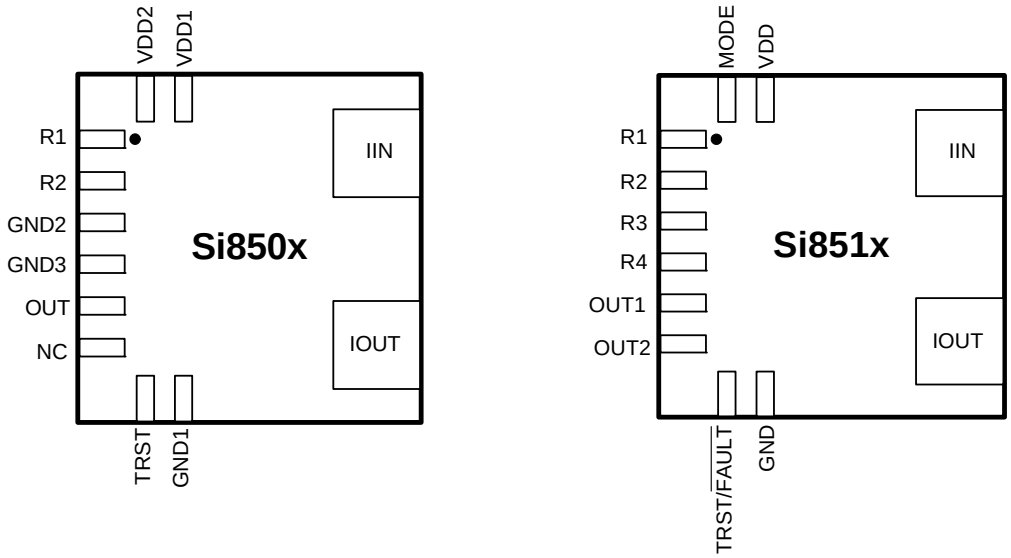

Figure 21. Example Pin Configurations

Table 12. Si85xx Family Pin Descriptions

Pin#	Si850x Pin Name	Description	Si851x Pin Name	Description
1	R1	Integrator reset input 1	R1	Integrator reset input 1
2	R2	Integrator reset input 2	R2	Integrator reset input 2
3	GND2	Ground	R3	Integrator reset input 3
4	GND3		R4	Integrator reset input 4
5	OUT	Output	OUT1	Output in single-ended output mode, or one of two outputs in Ping-Pong mode.
6	NC	No connect	OUT2	Second of two Ping-Pong mode outputs
7	TRST	Reset time control	TRST	Reset time control
8	GND1	Ground	GND	Ground
9	IOUT	Current output terminal	IOUT	Current output terminal
10	IIN	Current input terminal	IIN	Current input terminal
11	VDD1	Power supply input	VDD	Power supply input
12	VDD2		MODE	Mode control input

5. Pin Descriptions—20-Pin SOIC

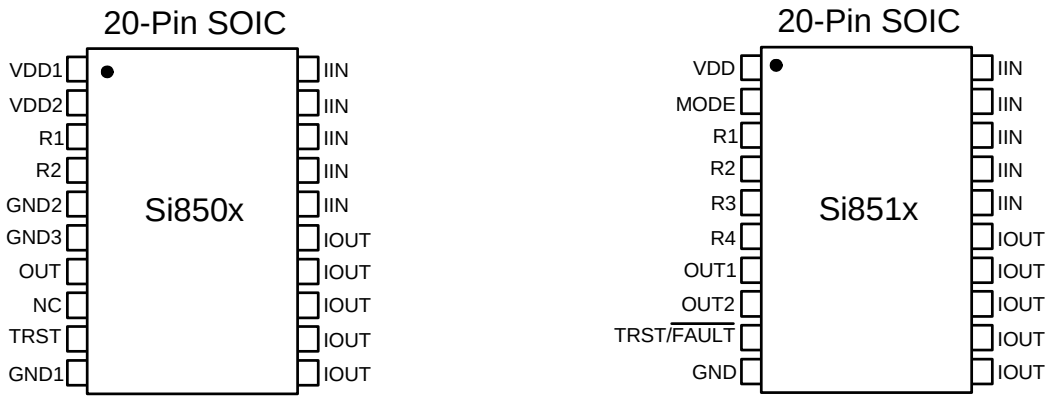

Figure 22. Example Pin Configurations

Table 13. Si85xx Family Pin Descriptions

Pin#	Si850x Pin Name	Description	Si851x Pin Name	Description
1	VDD1	Power supply input	VDD	Power supply input
2	VDD2		MODE	Mode control input
3	R1	Integrator reset input 1	R1	Integrator reset input 1
4	R2	Integrator reset input 2	R2	Integrator reset input 2
5	GND2	Ground	R3	Integrator reset input 3
6	GND3		R4	Integrator reset input 4
7	OUT	Output	OUT1	Output in single-ended output mode, or one of two outputs in Ping-Pong mode.
8	NC	No connect	OUT2	Second of two Ping-Pong mode outputs
9	TRST	Reset time control	TRST	Reset time control
10	GND1	Ground	GND	Ground
11–15	IOUT	Current output terminal	IOUT	Current output terminal
16–20	IIN	Current input terminal	IIN	Current input terminal

6. Ordering Guide

New OPNs	Full Scale Current (A)	Initial Accuracy %[1]	Temp Range	Pin 7 Function	Isolation Rating	Output Mode	Package[2]	Old Obsolete OPNs[3] (Previously Specified with ±5% Accuracy and –40C to +85 °C)	Old Obsolete OPNs[3] (Previously Specified with ±20% Accuracy)
Si8501-C-IM	5	5%	–40 to 125 °C	Integrator Reset Programming Time Input	1 kV_{RMS}	Single	QFN-12	Si8501-C-GM	Si8504-C-IM
Si8502-C-IM	10							Si8502-C-GM	Si8505-C-IM
Si8503-C-IM	20							Si8503-C-GM	Si8506-C-IM
Si8501-C-IS	5				5 kV_{RMS}		SOIC-20	New package offering	
Si8502-C-IS	10								
Si8503-C-IS	20								
Si8511-C-IM	5				1 kV_{RMS}	Ping-Pong	QFN-12	Si8511-C-GM	Si8514-C-IM
Si8512-C-IM	10							Si8512-C-GM	Si8515-C-IM
Si8513-C-IM	20							Si8513-C-GM	Si8516-C-IM
Si8511-C-IS	5				5 kV_{RMS}		SOIC-20	New package offering	
Si8512-C-IS	10								
Si8513-C-IS	20								
Si8517-C-IM	5			FAULT Output	1 kV_{RMS}		QFN-12	Si8517-C-GM	—
Si8518-C-IM	10							Si8518-C-GM	
Si8519-C-IM	20							Si8519-C-GM	
Si8517-C-IS	5				5 kV_{RMS}		SOIC-20	New Package Offering	
Si8518-C-IS	10								
Si8519-C-IS	20								

Notes:

1. See "2.4. Total Measurement Error" on page 11 for more information.
2. All packages are RoHS-compliant. Moisture Sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry classification, and peak solder temperature.
3. Since the initial accuracy for all devices is now specified as ±5%, Si8504/5/6 and Si8514/15/16 OPNs have been replaced with Si8501/2/3 and Si8511/12/13 OPNs, respectively.

7. Package Outline—12-Pin QFN

Figure 23 illustrates the package details for the Si85xx. Table 14 lists the values for the dimensions shown in the illustration.

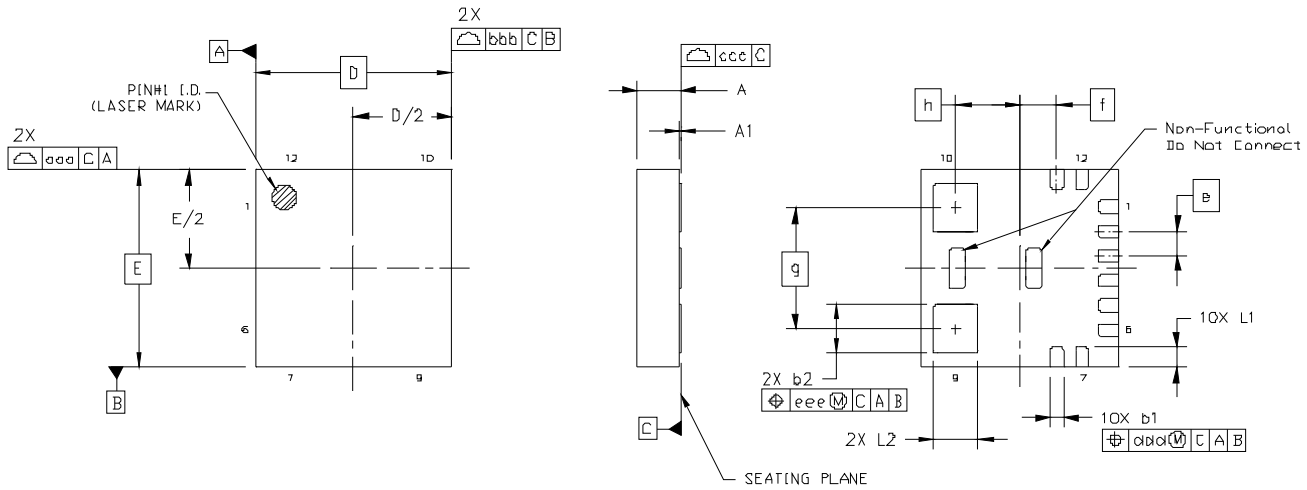

Figure 23. 12-Pin QFN Package Diagram

Table 14. QFN-12 Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.03	0.05
b1	0.20	0.25	0.30
b2	0.95	1.00	1.05
D	4.00 BSC.		
e	0.50 BSC.		
E	4.00 BSC.		
f	0.75 BSC.		
g	2.45 BSC.		
h	1.30 BSC.		
L1	0.35	0.40	0.45
L2	0.85	0.90	0.95
aaa	0.05		
bbb	0.05		
ccc	0.08		
ddd	0.10		
eee	0.10		

Notes:
1. All dimensions shown are in millimeters (mm).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

8. Recommended PCB Land Pattern (12-Pin QFN)

Figure 24 illustrates the PCB land pattern details for the 12-pin QFN package. Table 15 lists the values for the dimensions shown in the illustration.

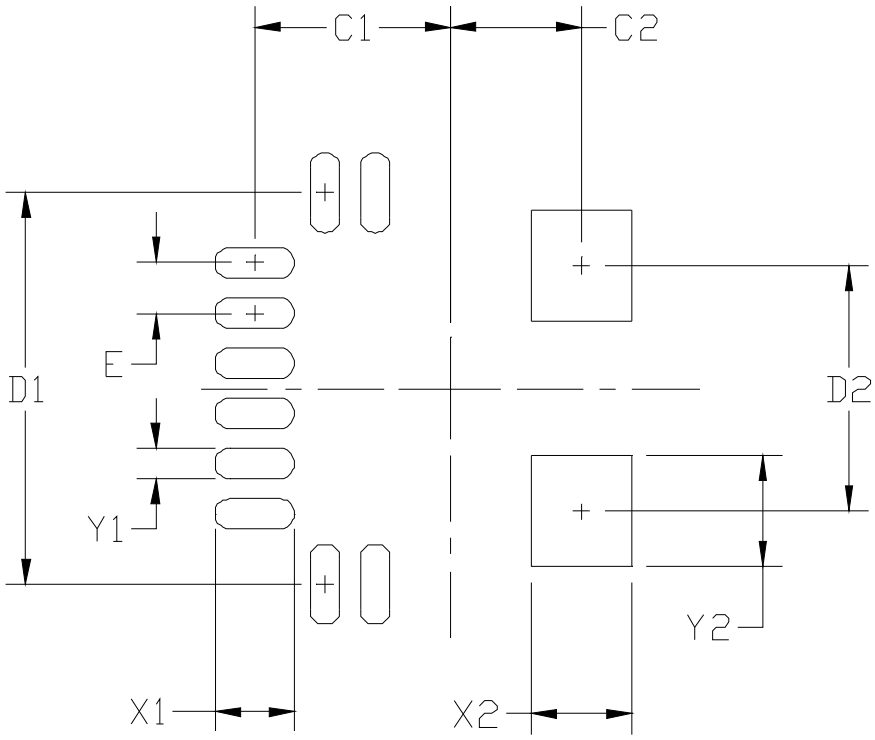

Figure 24. 12-Pin QFN PCB Land Pattern

Table 15. 12-Pin QFN PCB Land Pattern Dimensions

Dimension	mm
C1	1.95
C2	1.30
D1	3.90
D2	2.45
E	0.50
X1	0.80
X2	1.00
Y1	0.30
Y2	1.10

Notes:
1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Package Outline: Wide Body SOIC

Figure 25 illustrates the package details for the wide-body SOIC package. Table 16 lists the values for the dimensions shown in the illustration.

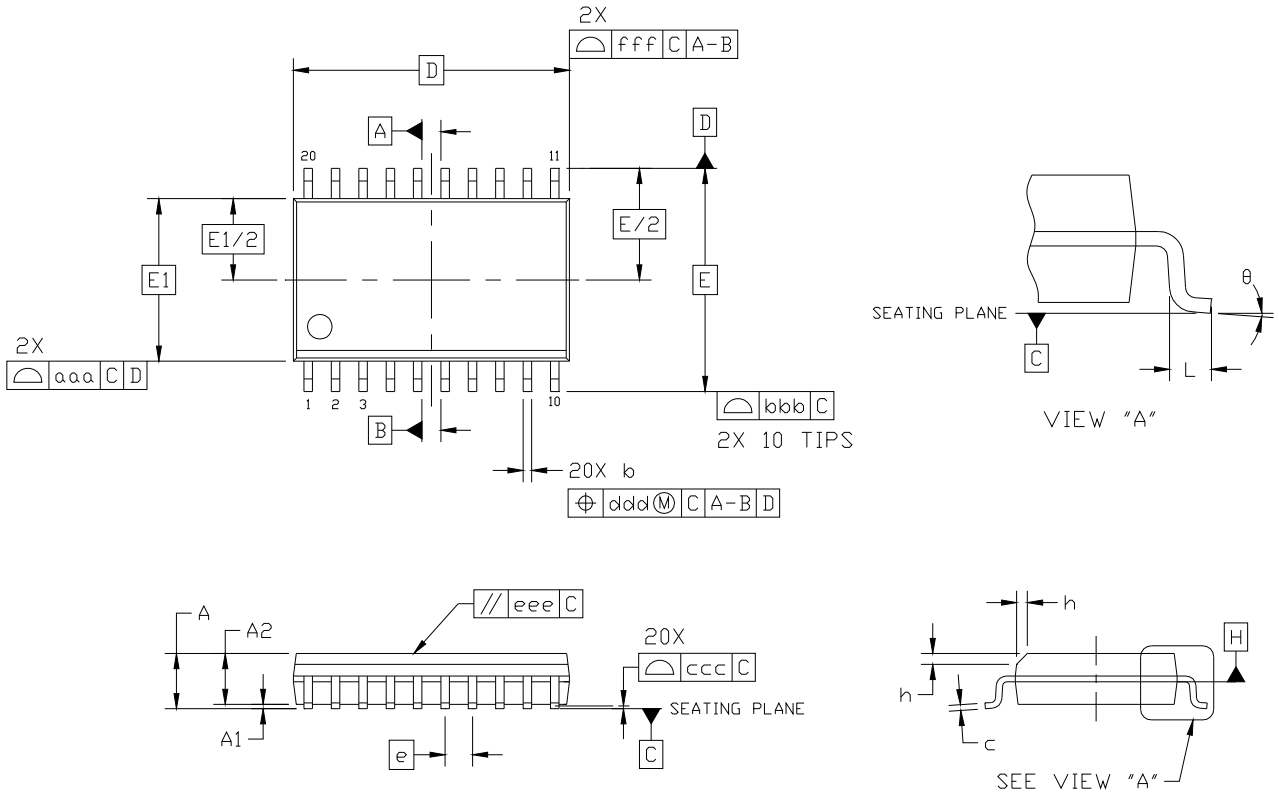

Figure 25. 20-Pin Wide Body SOIC

Table 16. 20-Pin Wide Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	12.80 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AC.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

10. Recommended PCB Land Pattern (20-Pin SOIC)

Figure 26 illustrates the PCB land pattern details for the 20-pin SOIC package. Table 17 lists the values for the dimensions shown in the illustration.

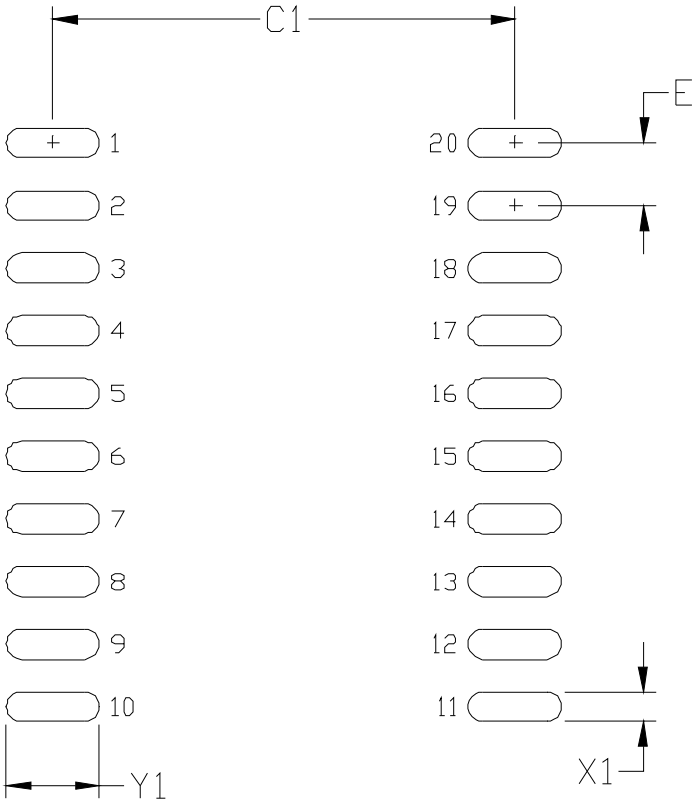

Figure 26. 20-Pin SOIC PCB Land Pattern

Table 17. 20-Pin SOIC PCB Land Pattern Dimensions

Dimension	mm
C1	9.40
E	1.27
X1	0.60
Y1	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

11. Top Marking (QFN)

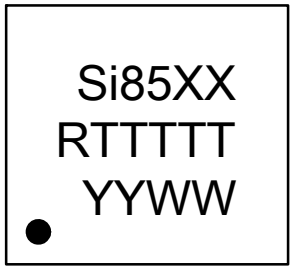

Figure 27. QFN Top Marking

Table 18. Top Marking Explanation

Line 1 Marking:	Device Part Number	Si85XX: Where XX = 01, 02, 03, 11, 12, 13, 17, 18, 19
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	Circle Bottom-Left Justified	Pin 1 Identifier
	YY = Year WW = Work Week	Corresponds to the year and work week of the assembly build date.

12. Top Marking (SOIC)

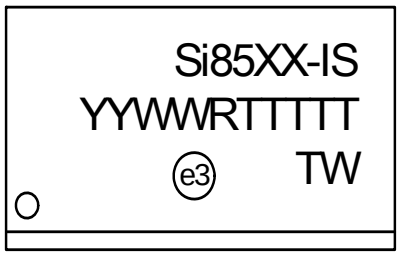

Figure 28. SOIC Top Marking

Table 19. Top Marking Explanation

Line 1 Marking:	Device Part Number	Si85XX-IS Where XX = 01, 02, 03, 11, 12, 13, 17, 18, 19
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated Table 1, “Electrical Specifications,” on page 4.
- Added 20-pin wide-body SOIC package option.
- Updated "6. Ordering Guide" on page 26.
  - All devices are now specified to ±5% initial accuracy.
  - All devices are now specified for operation over –40 to +125 °C temperature range. All ordering part numbers have been updated to reflect this (i.e. previous “-GM” and “-GS” part number suffixes have been replaced with “-IM” and “-IS” suffixes).
- Added sections “8. Recommended PCB Land Pattern (12-Pin QFN)” and “10. Recommended PCB Land Pattern (20-Pin SOIC)”.

Revision 0.2 to Revision 0.21

- Added reference to IEC61010, IEC60601 on page 1.
- Updated "6. Ordering Guide" on page 26.
- Added Top Marking sections.

Revision 0.21 to Revision 0.3

- Updated Table 2 on page 5.
  - Production test voltage is $\geq$ 6.0 kV_{RMS}.
- Added “2.5. Effect of Switching Frequency on Accuracy” on page 11.
- Added Figure 6, “Full-Scale Output Accuracy vs. Frequency,” on page 11.
- Updated "3.2. Layout Requirements" on page 13.
  - Added layout recommendations for QFN.
- Added Figure 10, “QFN Layout Requirements,” on page 13.

Revision 0.3 to Revision 0.4

- Updated Table 8 on page 8.
  - Added junction temperature spec.
- Removed Figure 6, “Full-Scale Output Accuracy vs. Frequency,” on page 11.
- Updated Figures 9 and 10 on page 13.
- Updated Table 11 on page 16.
  - Updated notes.
- Updated Top Marks.
  - Added revision description.

NOTES:

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