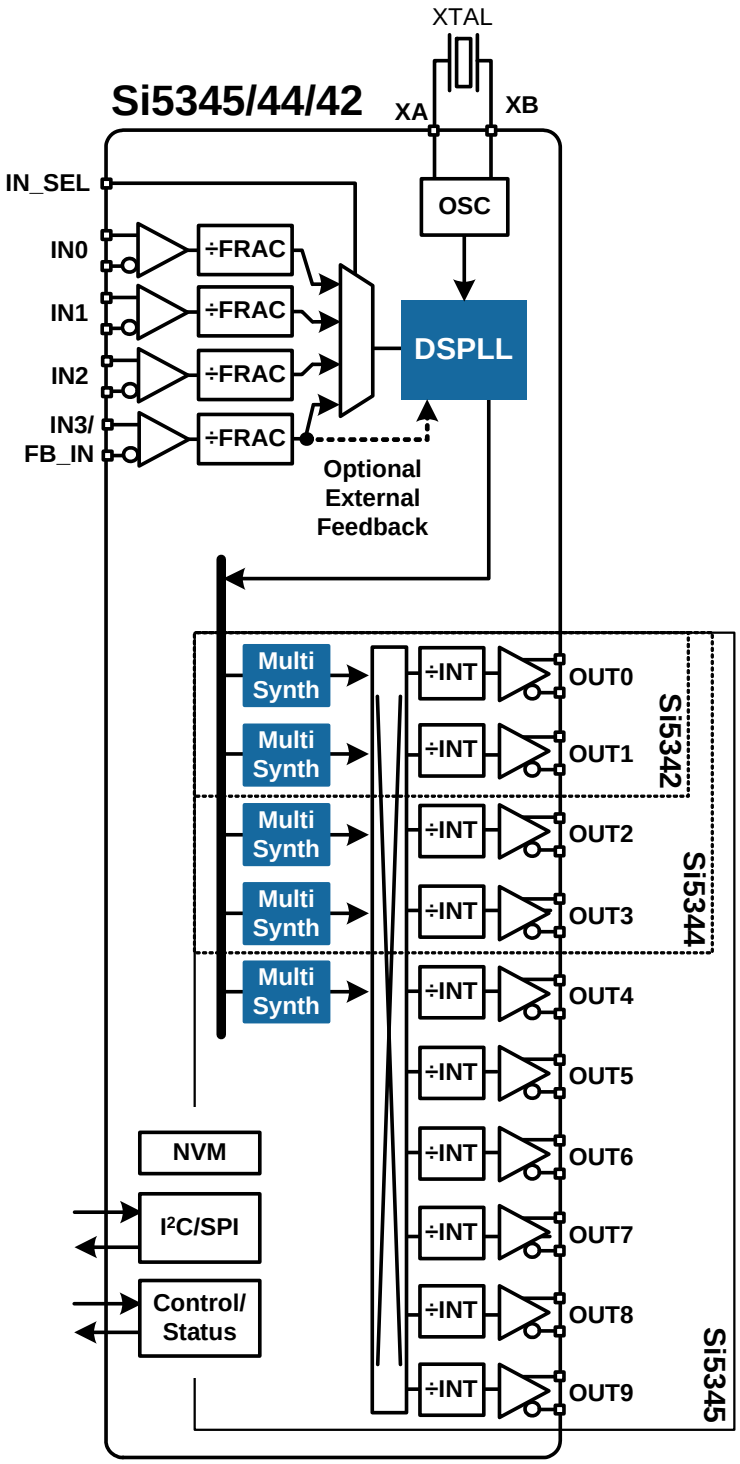
Functional Block Diagram



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1. Typical Application Schematic

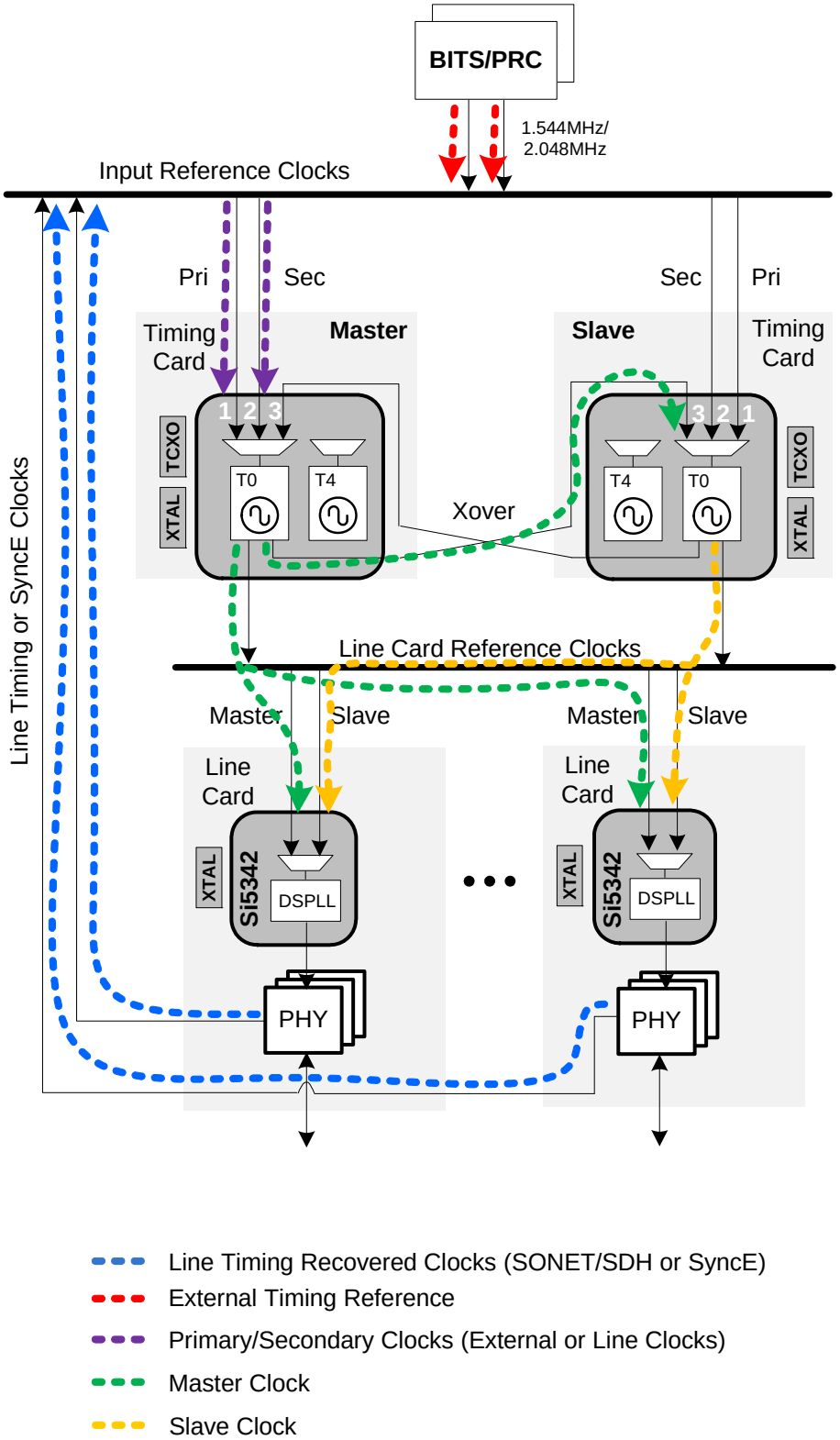


Figure 1. Using The Si5342 in a Typical Line Card Application

2. Electrical Specifications

Table 1. Recommended Operating Conditions*

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%,T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Clock Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

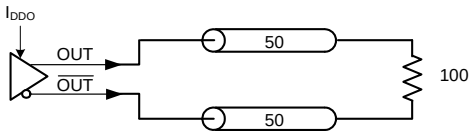
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Core Supply Current	I_{DD}	Si5345, Si5344, Si5342	Notes 1,2,3	—	125	170	mA
	I_{DDA}			—	115	125	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[4] @ 156.25 MHz		—	23	25	mA
		LVDS Output[4] @ 156.25 MHz		—	16	18	mA
		3.3 V LVCMOS[5] output @ 156.25 MHz		—	19	26	mA
		2.5 V LVCMOS[5] output @ 156.25 MHz		—	15	19	mA
		1.8 V LVCMOS[5] output @ 156.25 MHz		—	11	13	mA
Total Power Dissipation	P_d	Si5345	Note 1,6	—	885	1000	mW
		Si5344	Note 2,6	—	746	—	mW
		Si5342	Note 3,6	—	645	—	mW

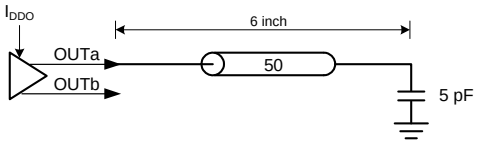
Notes:

1. Si5345 test configuration: 10x 3.3 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5344 test configuration: 4x 3.3 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Si5342 test configuration: 2x 3.3 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
4. Differential outputs terminated into an AC coupled 100 Ω load.
5. LVCMOS outputs measured into a 6 inch 50 Ω PCB trace with 5 pF load.

Differential Output Test Configuration



LVCMOS Output Test Configuration



6. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 3. Input Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Differential or Single-Ended - AC Coupled (IN0/$\overline{IN0}$, IN1/$\overline{IN1}$, IN2/$\overline{IN2}$, IN3/$\overline{IN3}$, FB_IN/$\overline{FB\_IN}$)						
Input Frequency Range	f_{IN_DIFF}		0.008	—	750	MHz
Voltage Swing	V_{IN}	f_{in} < 400 MHz	100	—	1000	mVpp_se
		600 MHz < f_{in} < 800 MHz	225	—	1000	mVpp_se
		f_{in} > 800 MHz	375	—	1000	mVpp_se
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2	—	pF
LVCMOS - DC Coupled (IN0, IN1, IN2, IN3)						
Input Frequency	f_{IN_CMOS}		0.008	—	250	MHz
Input Voltage	V_{IL}		–0.2	—	0.18	V
	V_{IH}		0.70	—	—	V
Slew Rate[1, 2]	SR		400	—	—	V/µs
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (applied to XA/XB)						
REFCLK Frequency	f_{IN_REF}	Frequency range for best output jitter performance	48	—	54	MHz
		TCXO frequency for SyncE applications. Jitter performance may be reduced	—	40	—	MHz
Input Voltage Swing	V_{IN}		350	—	1600	mVpp_se
Slew rate[1, 2]	SR	Imposed for best jitter performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Notes:

1. Imposed for jitter performance
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 – 0.2) \times V_{IN\_Vpp\_se}) / SR$
3. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.
4. A programmable internal divider (P_{REF}) is available to help support REFCLK frequencies up to 200 MHz.

Table 4. Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5345 Control Input Pins (I2C_SEL, IN_SEL[1:0], $\overline{\text{RST}}$, $\overline{\text{OE}}$, A1, SCLK, A0/$\overline{\text{CS}}$, FINC, FDEC)						
Input Voltage	V_{IL}		–0.1	—	0.3 x V_{DDIO}*	V
	V_{IH}		0.7 x V_{DDIO}*	—	3.6	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RST	50	—	—	ns
Si5344/42 Control Input Pins (I2C_SEL, IN_SEL[1:0], $\overline{\text{RST}}$, $\overline{\text{OE}}$, A1, SCLK, A0/$\overline{\text{CS}}$)						
Input Voltage	V_{IL}		–0.1	—	0.3 x V_{DDIO}*	V
	V_{IH}		0.7 x V_{DDIO}*	—	3.6	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RST	50	—	—	ns
***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.						

Table 5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency	f_{OUT}			0.0001	—	800	MHz
Duty Cycle	DC	f < 400 MHz		48	—	52	%
		400 MHz < f < 800 MHz		45	—	55	%
Output-Output Skew	T_{SK}	Differential Output		—	80	100	ps
OUT-$\overline{OUT}$ Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	—	100	ps
Output Voltage Swing[1]	**Normal Swing Mode**						
	V_{OUT}	V_{DDO} = 3.3 V or 2.5 V or 1.8 V	LVDS	370	470	570	mVpp_se
			LVPECL	650	820	1050	
	High Swing Mode						
	V_{OUT}	V_{DDO} = 3.3 V or 2.5 V or 1.8 V	LVDS	310	420	530	mVpp_se
		V_{DDO} = 3.3 V or 2.5 V	LVPECL	590	830	1060	
Common Mode Voltage[1,2,3] (100 Ω load line-to-line)	**Normal Swing or High Swing Modes**						
	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.12	1.23	1.34	V
			LVPECL	1.90	2.0	2.13	
		V_{DDO} = 2.5 V	LVPECL LVDS	1.17	1.23	1.30	
Rise and Fall Times (20% to 80%)	t_R/t_F	Normal Swing Mode		—	170	220	ps
		High Swing Mode		—	250	320	

Note:

1. Normal swing mode, high swing mode, Vswing and Cmode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently.
2. Not all combinations of voltage swing and common mode voltages settings are possible. See the Si5345/44/42 Family Reference Manual for details.
3. Common mode voltage min/max variation = ±4% from typical value
4. Driver output impedance depends on selected output mode (Normal, High).
5. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.

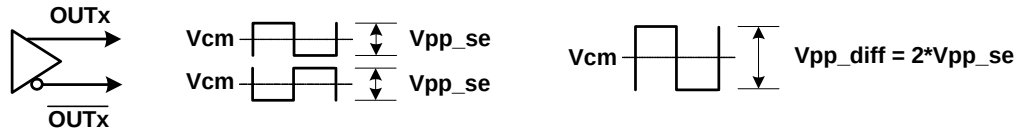


Table 5. Differential Clock Output Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Differential Output Impedance[4]	Z_O	Normal Swing Mode	—	100	—	Ω
		High Swing Mode	—	Hi-Z	—	Ω
Power Supply Noise Rejection[5]	PSRR	**Normal Swing Mode**				
		10 kHz sinusoidal noise	—	–93	—	dB
		100 kHz sinusoidal noise	—	–93	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–79	—	
		High Swing Mode				
		10 kHz sinusoidal noise	—	–98	—	dB
		100 kHz sinusoidal noise	—	–95	—	
		500 kHz sinusoidal noise	—	–84	—	
		1 MHz sinusoidal noise	—	–76	—	
Output-output Crosstalk	XTALK	Measured spur from adjacent output	—	–73	—	dB

Note:

1. Normal swing mode, high swing mode, Vswing and Cmode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently.
2. Not all combinations of voltage swing and common mode voltages settings are possible. See the Si5345/44/42 Family Reference Manual for details.
3. Common mode voltage min/max variation = ±4% from typical value
4. Driver output impedance depends on selected output mode (Normal, High).
5. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.

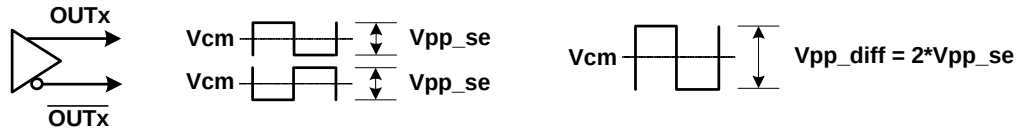


Table 6. LVCMOS Clock Output Specifications

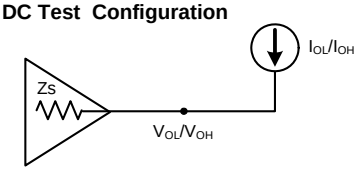
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency				0.0001	—	250	MHz
Duty Cycle	DC	f < 400 MHz		47	—	53	%
		400 MHz < f < 800 MHz		45	—	55	%
Output-to-Output Skew	T_{SK}			—	—	100	ps
Output Voltage High[1,2,3]	V_{OH}	**V_{DDO} = 3.3 V**					
		CMOS1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		CMOS2	I_{OH} = –12 mA		—	—	
		CMOS3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		CMOS1	I_{OH} = –6 mA	V_{DDO} x 0.85	—	—	V
		CMOS2	I_{OH} = –8 mA		—	—	
		CMOS3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		CMOS1	I_{OH} = –3 mA	V_{DDO} x 0.85	—	—	V
		CMOS2	I_{OH} = –4 mA		—	—	
		CMOS3	I_{OH} = –5 mA		—	—	

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are CMOS1, CMOS2, CMOS3.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the DC test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed.

DC Test Configuration



AC Test Configuration

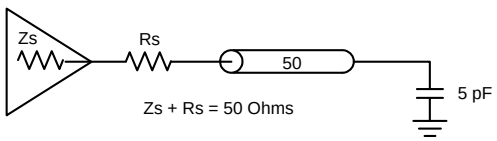
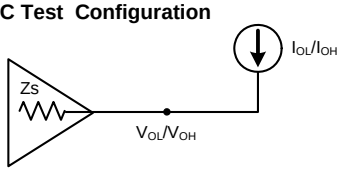


Table 6. LVCMOS Clock Output Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Voltage Low[1,2,3]	V_{OL}	**V_{DDO} = 3.3 V**					
		CMOS1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		CMOS2	I_{OL} = 12 mA	—	—		
		CMOS3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		CMOS1	I_{OH} = –6 mA	—	—	V_{DDO} x 0.15	V
		CMOS2	I_{OL} = 8 mA	—	—		
		CMOS3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		CMOS1	I_{OH} = –3 mA	—	—	V_{DDO} x 0.15	V
		CMOS2	I_{OH} = –4 mA	—	—		
		CMOS3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3 V		—	360	—	ps
		VDDO = 2.5 V		—	420	—	ps
		VDDO = 1.8 V		—	280	—	ps

Notes:
1. Driver strength is a register programmable setting and stored in NVM. Options are CMOS1, CMOS2, CMOS3.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the DC test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed.

DC Test Configuration



AC Test Configuration

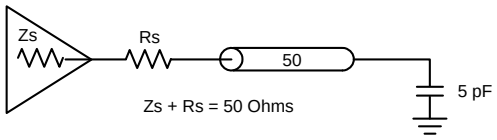


Table 7. Output Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5345 Status Output Pins ($\overline{\text{LOL}}$, $\overline{\text{INTR}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}* x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}* x 0.15	V
Si5344 Status Output Pins ($\overline{\text{INTR}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}* x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}* x 0.15	V
Si5344 Status Output Pins ($\overline{\text{LOL}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V
Si5342 Status Output Pins ($\overline{\text{INTR}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[1] x 0.75	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}* x 0.15	V
Si5342 Status Output Pins ($\overline{\text{LOL}}$, $\overline{\text{LOS0}}$, $\overline{\text{LOS1}}$, $\overline{\text{LOS2}}$, $\overline{\text{LOS3}}$, $\overline{\text{LOS\_XAXB}}$)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V

***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.

Table 8. Performance Characteristics
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	—	ms
PLL Lock Time	t_{ACQ}	With Fastlock enabled	—	160	—	ms
Output Delay Adjustment	t_{DELAY}	f_{VCO} = 14 GHz	—	0.28	—	ps
	t_{RANGE}		—	±9.14	—	ns
POR to Serial Interface Ready	t_{RDY}		—	—	10	ms
PLL Loop Bandwidth	f_{BW}		0.1	—	4000	Hz
Jitter Peaking	J_{PK}		—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter modulation = 10 Hz	—	23	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}		—	—	2.5	ns
Pull-in Range	ω_P		—	500	—	ppm
Input-to-Output Delay	$t_{IODELAY}$	Input-to-output delay is consistent after every power-up	—	2	—	ns
	t_{ZDELAY}	In Zero Delay Mode. Measured from INx to OUTx using a differential connection. Assumes delay from OUTx to FB_IN = 0.	—	100	—	ps
RMS Jitter Performance*	J_{GEN}	12 kHz to 20 MHz	—	0.125	—	ps

***Note:** Jitter generation test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL, loop bandwidth = 100 Hz. Does not include jitter from input clock.

Table 9. I²C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Units
			Standard Mode 100 kbps		Fast Mode 400 kbps		
SCL Clock Frequency	f_{SCL}		0	100	0	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		5.0	—	—	—	µs
Data set-up time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

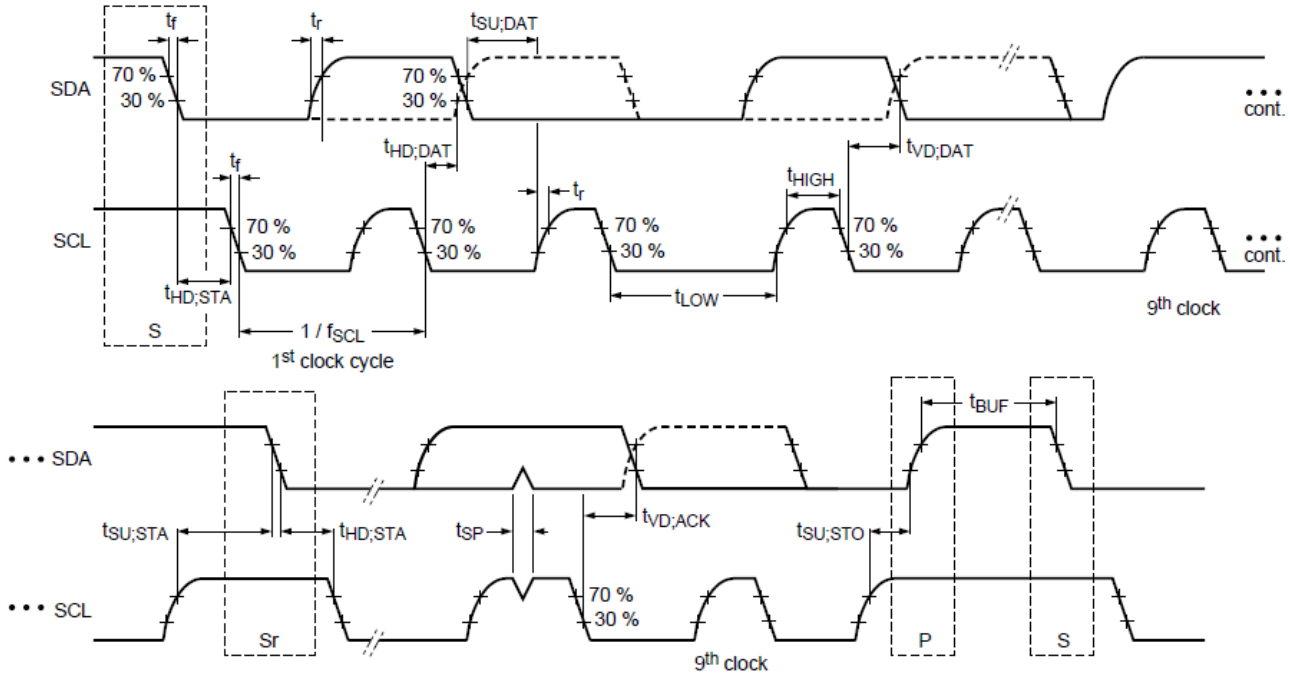


Figure 2. I²C Serial Port Timing Standard and Fast Modes

Table 10. SPI Timing Specifications

(V_{DD} = 1.8 V ±5%, or 3.3 V ±5%, V_{DD33} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Rise & Fall Time	Tr/Tf	—	—	10	ns
SCLK High & Low Time	T_{HL}				
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	12.5	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	12.5	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-State	T_{D3}	—	—	12.5	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	25	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Rise	T_{H1}	25	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	12.5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	12.5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	50	—	—	ns

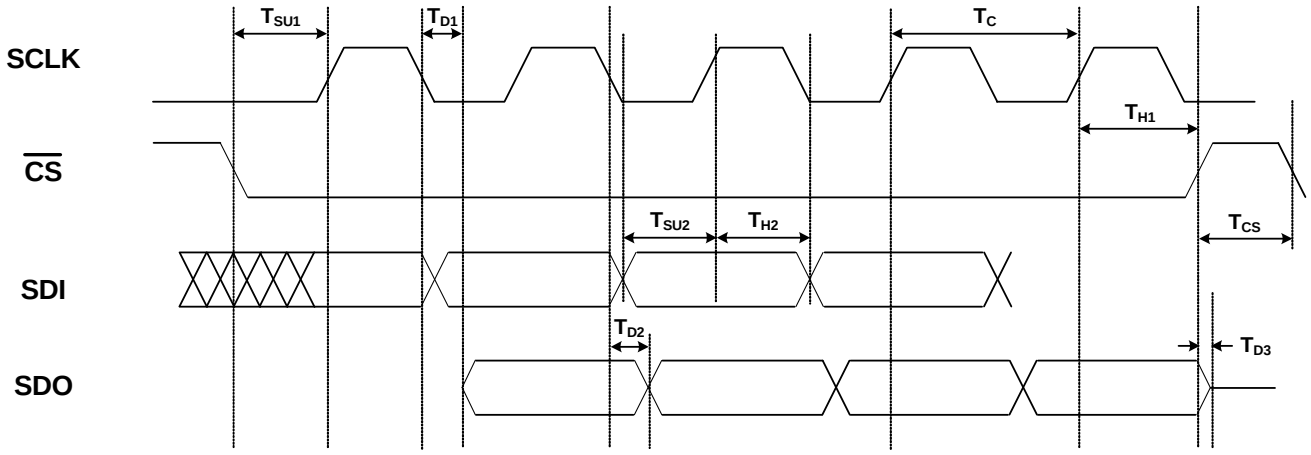


Figure 3. SPI Serial Interface Timing

Table 11. Crystal Specifications[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency Range	f_{XTAL}	Frequency range for best jitter performance	48	—	54	MHz
Load Capacitance	C_L		—	8	—	pF
Shunt Capacitance	C_O		—	—	2	pF
Crystal Drive Level	d_L		—	—	200	µW
Equivalent Series Resistance	r_{ESR}	Refer to the Si5345/44/42 Family Reference Manual to determine ESR				

Notes:
1. The Si5345/44/42 is designed to work with crystals that meet the specifications in Table 11.
2. Refer to the Si5345/44/42 Family Reference Manual for recommended 48 to 54 MHz crystals. Crystal frequencies from 24.97 to 54.06 MHz are supported, but jitter performance is best from 48 to 54 MHz.

Table 12. Thermal Characteristics

Parameter	Symbol	Test Condition*	Value	Units
Si5345-64QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	θ_{JC}		9.5	
Thermal Resistance Junction to Board	θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	
Si5344, Si5342-44QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.4	
Thermal Resistance Junction to Case	θ_{JC}		10.9	
Thermal Resistance Junction to Board	θ_{JB}		9.3	
	Ψ_{JB}		9.2	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	
***Note:** Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.				

Table 13. Absolute Maximum Ratings[1,2,3,4]

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	IN0 – IN3/FB_IN	–0.85 to 3.8	V
	V_{I2}	$\overline{\text{IN}}$_SEL1, IN_SEL0, $\overline{\text{RST}}$, $\overline{\text{OE}}$, I2C_SEL, FIN$\overline{\text{C}}$, FDEC, SDI, SCLK, A0/$\overline{\text{CS}}$, A1	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Temperature Range	T_{STG}		–55 to 150	°C
Junction Temperature	T_{JCT}		–55 to 150	°C
Soldering Temperature (Pb-free profile)[5]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[5]	T_P		20–40	s

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. Moisture sensitivity level is MSL2.
5. The device is compliant with JEDEC J-STD-020.

3. Detailed Block Diagrams

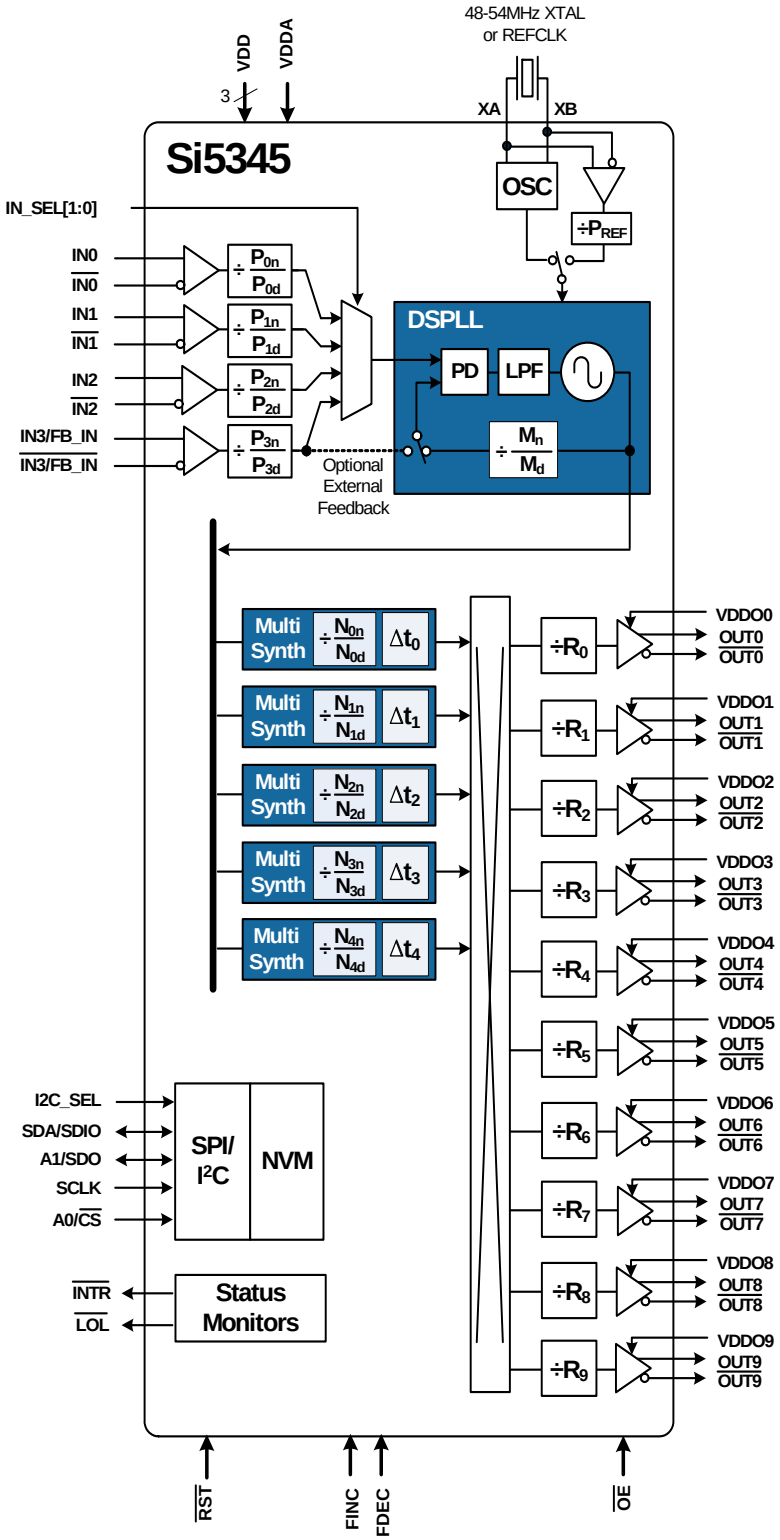


Figure 4. Si5345 Block Diagram

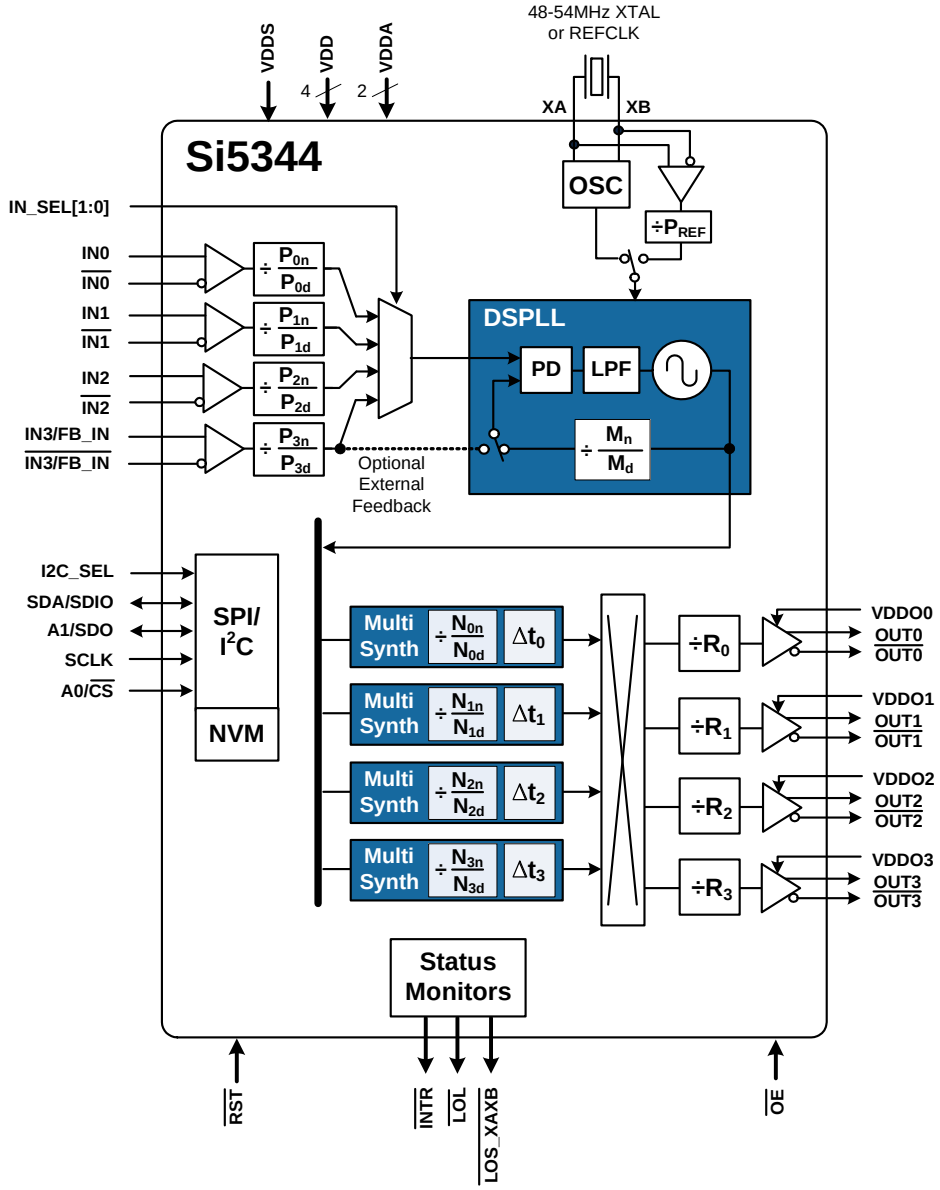


Figure 5. Si5344 Block Diagram

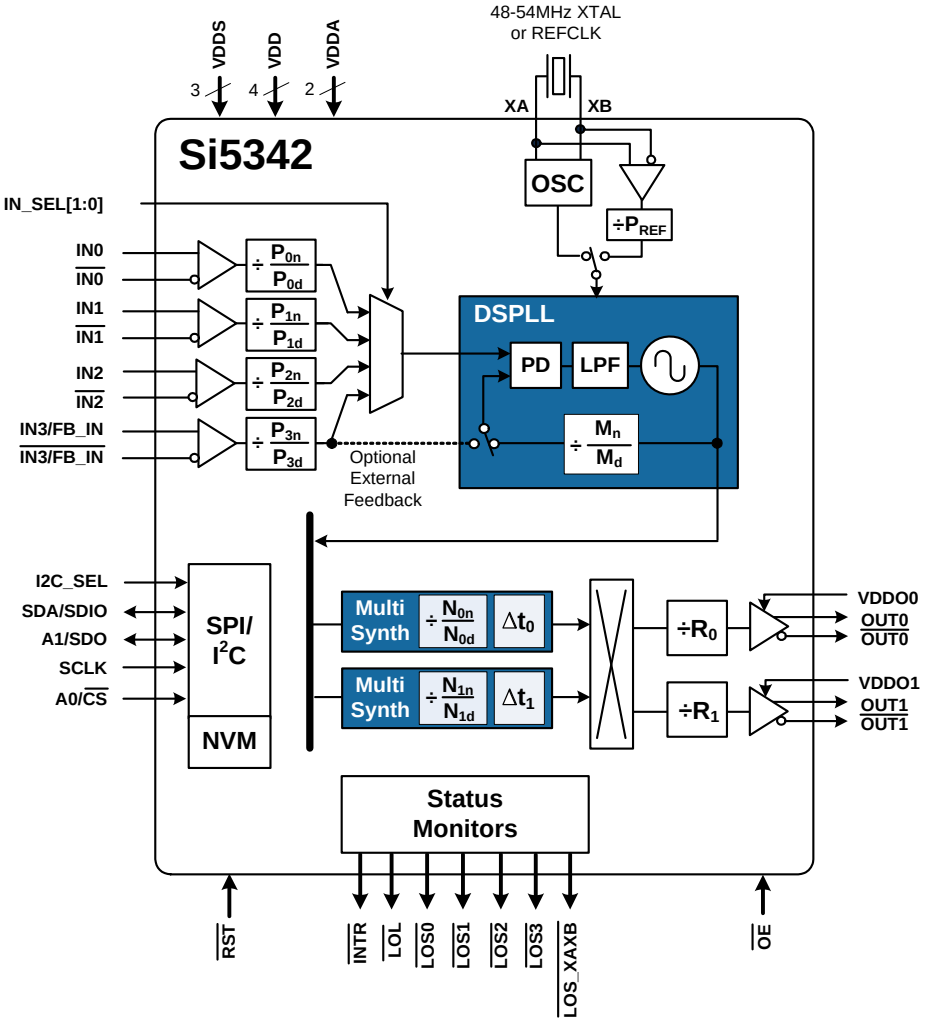


Figure 6. Si5342 Block Diagram

4. Functional Description

The Si5345 consist of a DSPLL which is responsible for input frequency multiplication (M) and jitter attenuation. Fractional input dividers (P) allow the DSPLL to perform hitless switching between input clocks (INx) that are fractionally related. Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode. The high-performance MultiSynth dividers (N) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the MultiSynth generated frequencies to any of the outputs. Additional integer division (R) determines the final output frequency.

4.1. Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (P_n/P_d), fractional frequency multiplication (M_n/M_d), fractional output MultiSynth division (N_n/N_d), and integer output division (R_n) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

4.2. DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

4.2.1. Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings of in the range of 100 Hz to 4 kHz are available for selection. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

4.3. Modes of Operation

Once initialization is complete the DSPLL operates in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in Figure 7. The following sections describe each of these modes in greater detail.

4.3.1. Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits including the serial interface will be restored to their initial state. A hard reset is initiated using the $\overline{\text{RST}}$ pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

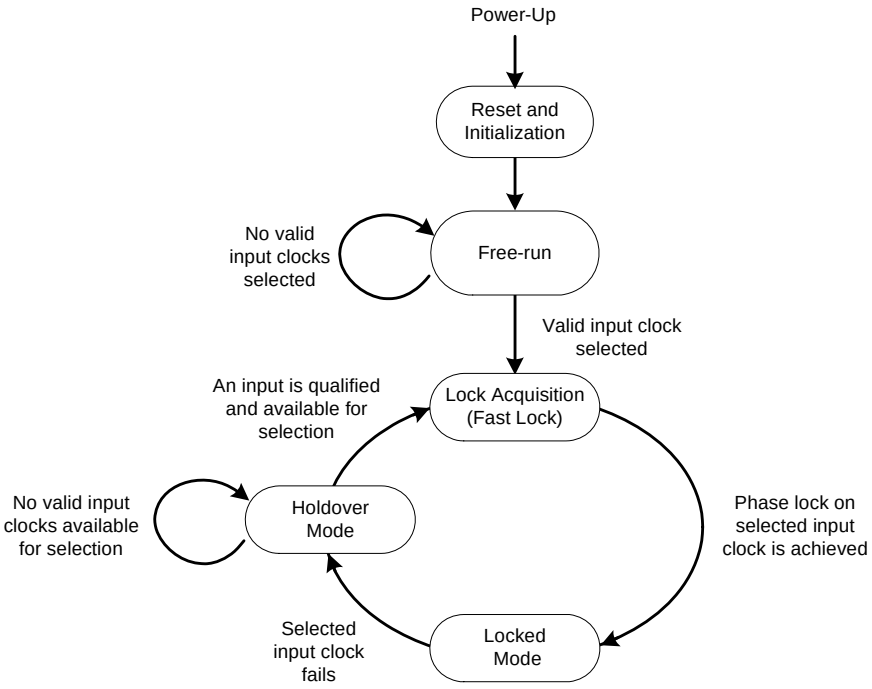


Figure 7. Modes of Operation

4.3.2. Freerun Mode

The DSPLL will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes.

4.3.3. Lock Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.3.4. Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point any XTAL frequency drift will not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See section 4.7.4 for more details on the operation of the loss of lock circuit.

4.3.5. Holdover Mode

The DSPLL will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while the locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in Figure 8. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

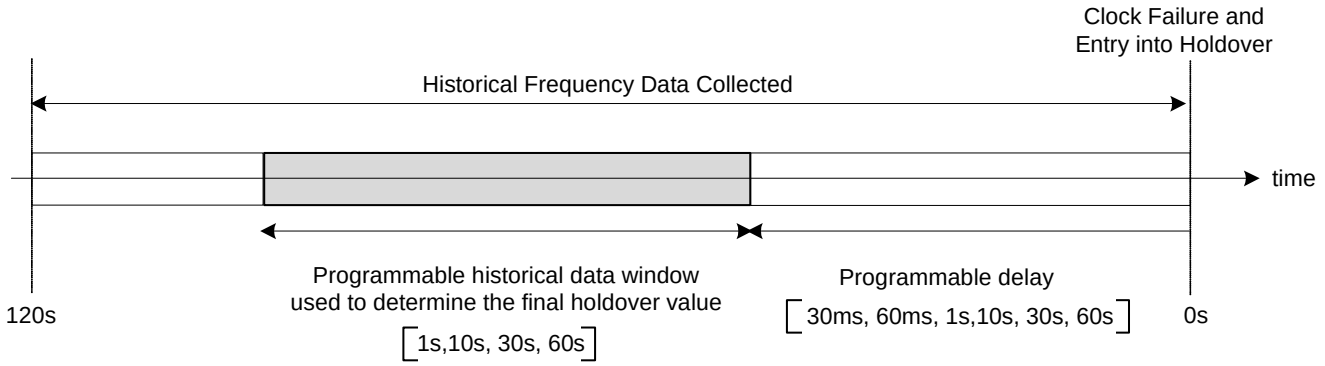


Figure 8. Programmable Holdover Window

When entering holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL bandwidth, the Fastlock bandwidth, or an artificial linear ramp rate selectable from 0.75 ppm/s up to 40 ppm/s. These options are register programmable.

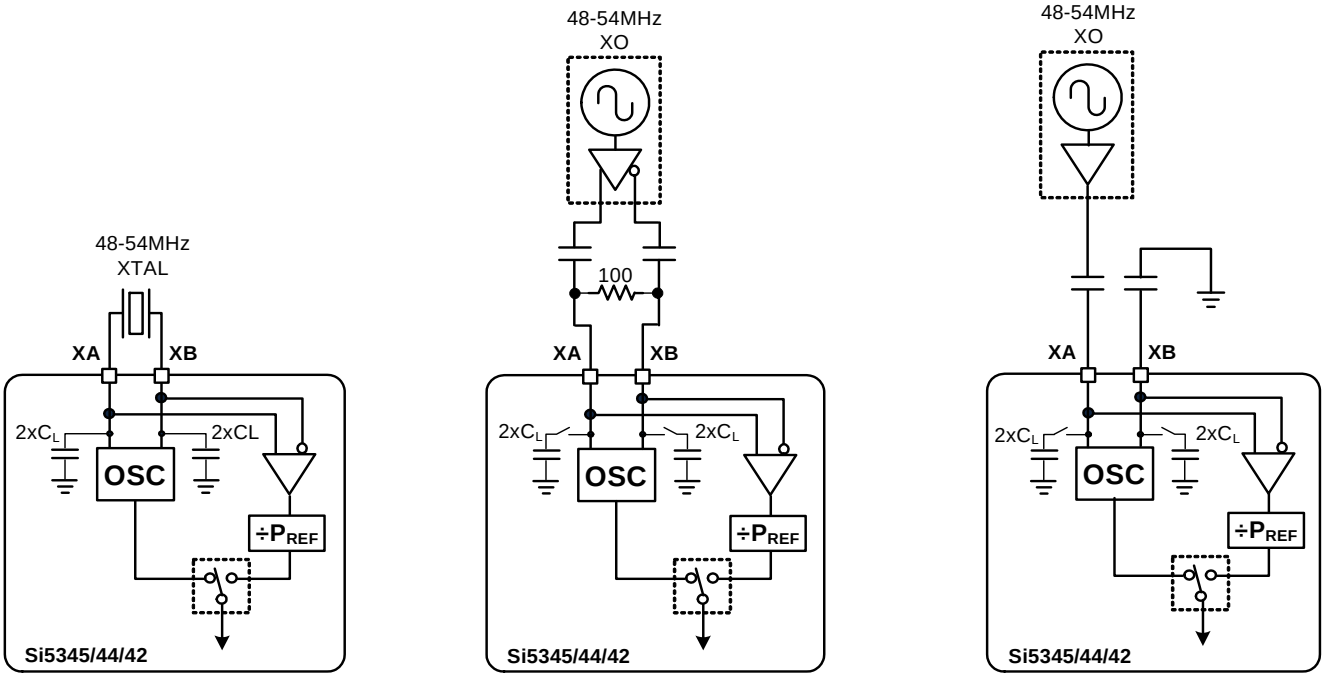
4.4. External Reference (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in Figure 9. The device includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to Table 11 for crystal specifications. A crystal in the range of 48 MHz to 54 MHz is recommended for best jitter performance. Frequency offsets due to C_L mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±200 ppm. The Si5345/44/42 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

The device can also accommodate an external reference clock (REFCLK) instead of a crystal. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (C_L) are disabled in this mode. Refer to Table 3 for REFCLK requirements when using this mode. A P_{REF} divider is available to accommodate external clock frequencies higher than 54 MHz. Frequencies in the range of 48 MHz to 54 MHz will achieve the best output jitter performance.

4.5. Digitally Controlled Oscillator (DCO) Mode

The output MultiSynths support a DCO mode where their output frequencies are adjustable in pre-defined steps defined by frequency step words (FSW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. Any number of MultiSynths can be can be updated at once or independently controlled. The DCO mode is available when the DPLL is operating in either free-run or locked mode.



Crystal Resonator Connection

Differential XO Connection

Single-ended XO Connection

Figure 9. Crystal Resonator and External Reference Clock Connection Options

4.6. Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize the DSPLL. The inputs accept both differential and single-ended clocks. Input selection can be manual (pin or register controlled) or automatic with user definable priorities.

4.6.1. Manual Input Switching (IN0, IN1, IN2, IN3)

Input clock selection can be made manually using the IN_SEL[1:0] pins or through a register. A register bit determines input selection as pin selectable or register selectable. The IN_SEL pins are selected by default. If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode. When the zero delay mode is enabled, IN3 becomes the feedback input (FB_IN) and is not available for selection as a clock input.

Table 14. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input	
		Zero Delay Mode Disabled	Zero Delay Mode Enabled
0	0	IN0	IN0
0	1	IN1	IN1
1	0	IN2	IN2
1	1	IN3	Reserved

4.6.2. Automatic Input Selection (IN0, IN1, IN2, IN3)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on input clock qualification, input priority, and the revertive option. Only input clocks that are valid can be selected by the automatic clock selection state machine. If there are no valid input clocks available the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority will be initiated.

4.6.3. Hitless Input Switching

Hitless switching is a feature that prevents a phase transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or at a fractional frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during a input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz.

4.6.4. Glitchless Input Switching

The DSPLL has the ability of switching between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output during the transition.

4.6.5. Input Configuration and Terminations

Each of the inputs can be configured as differential or single-ended LVCMOS. The recommended input termination schemes are shown in Figure 10. Differential signals must be AC coupled, while single-ended LVCMOS signals can be ac or dc coupled. Unused inputs can be disabled and left unconnected when not in use.

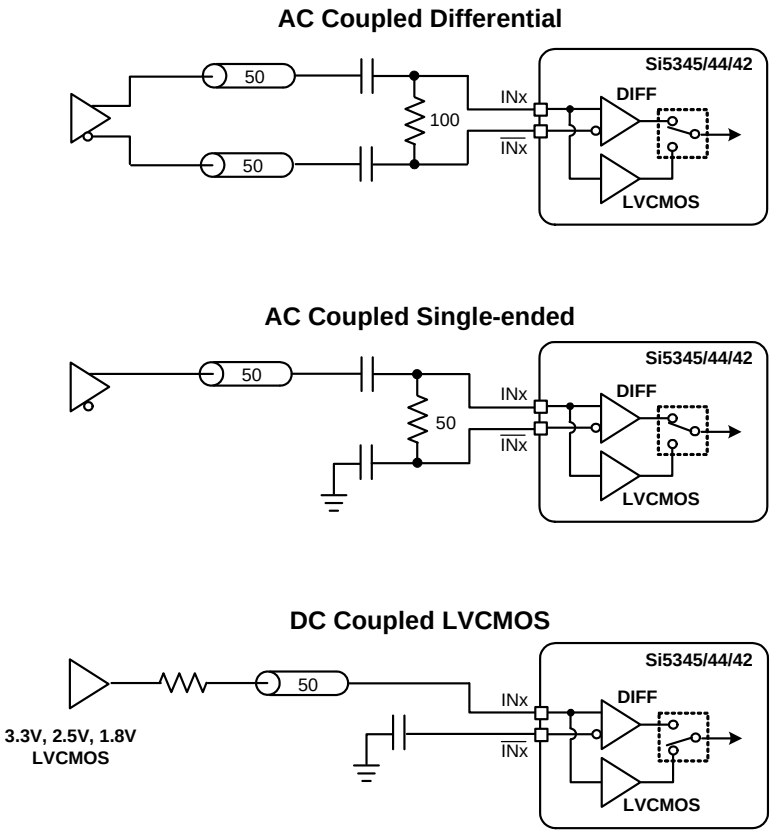


Figure 10. Termination of Differential and LVCMOS Input Signals

4.6.6. Synchronizing to Gapped Input Clocks

The DSPLL support locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in Figure 11. For more information on gapped clocks, see “AN561: Introduction to Gapped Clocks and PLLs”.

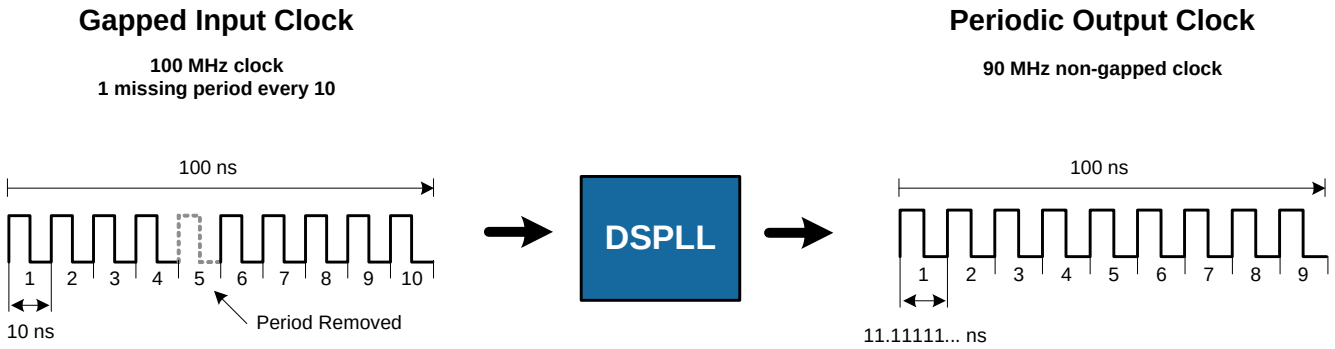


Figure 11. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every 8. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 8 when the switch occurs during a gap in either input clocks.

4.7. Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3/FB_IN) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in Figure 12. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLL. There is also a Loss Of Lock (LOL) indicator which is asserted when the DSPLL loses synchronization.

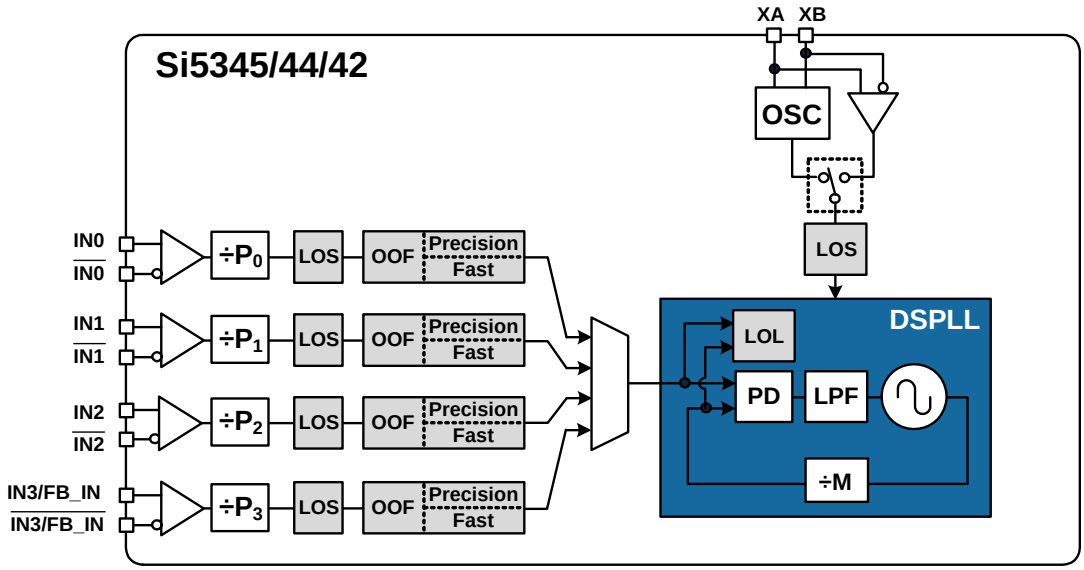


Figure 12. Si5345/44/42 Fault Monitors

4.7.1. Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility.

The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

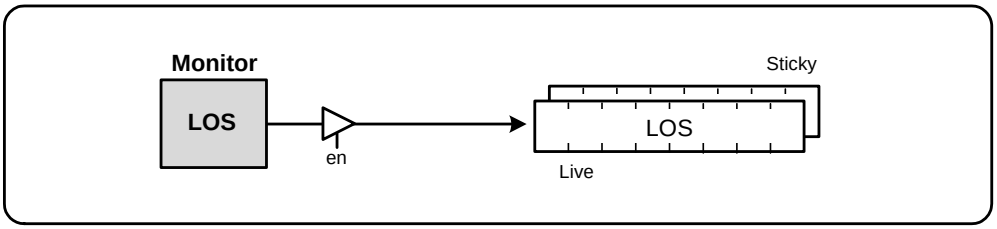


Figure 13. LOS Status Indicators

4.7.2. XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

4.7.3. OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0_ppm” reference.

This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in Figure 14. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

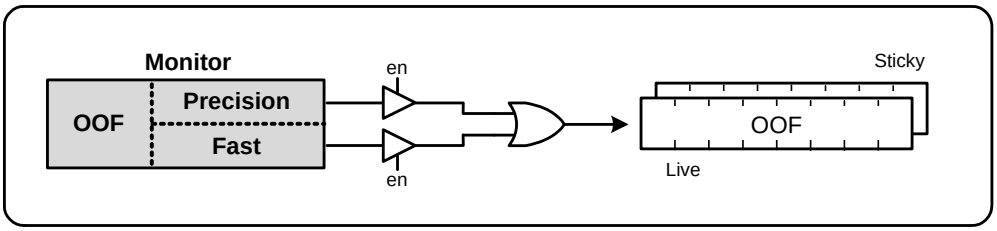


Figure 14. OOF Status Indicator

4.7.3.1. Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable from ±2 ppm to ±500 ppm in steps of 2 ppm.

A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in Figure 15. In this case the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 - IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register configurable.

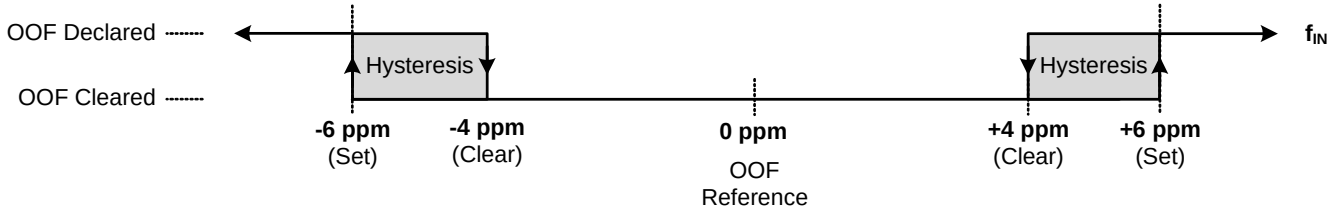


Figure 15. Example of Precise OOF Monitor Assertion and De-assertion Triggers

4.7.3.2. Fast OOF Monitor

Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

4.7.4. LOL Detection

The Loss Of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock.

There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in Figure 16. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The $\overline{\text{LOL}}$ pin reflects the current state of the LOL monitor.

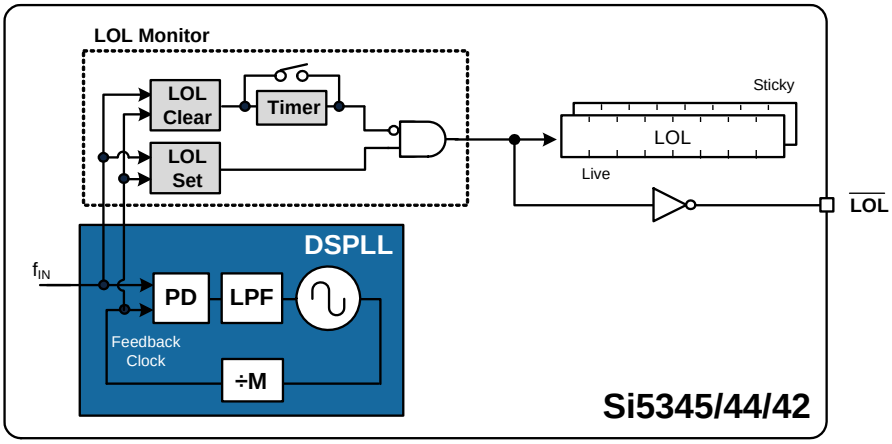


Figure 16. LOL Status Indicators

The LOL frequency monitors has an adjustable sensitivity which is register configurable from 0.2 ppm to 20000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status.

An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 2 ppm frequency difference is shown in Figure 17.

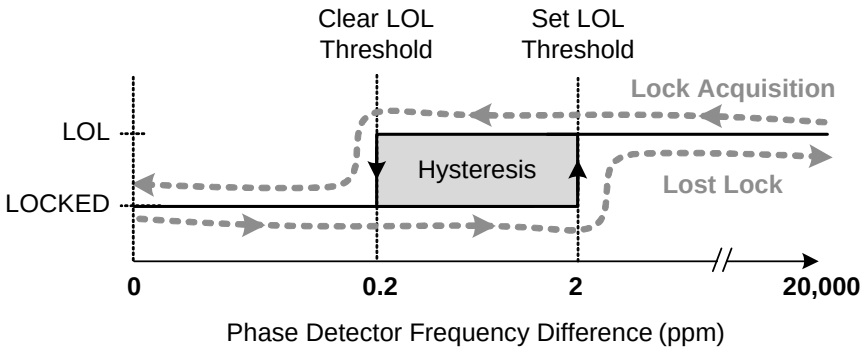


Figure 17. LOL Set and Clear Thresholds

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

4.7.5. Interrupt pin (INTR)

An interrupt pin (INTR) indicates a change in state of the status indicators (LOS, OOF, LOL, HOLD). Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the status register that caused the interrupt.

4.8. Outputs

Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

4.8.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the MultiSynths as shown in Figure 18. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

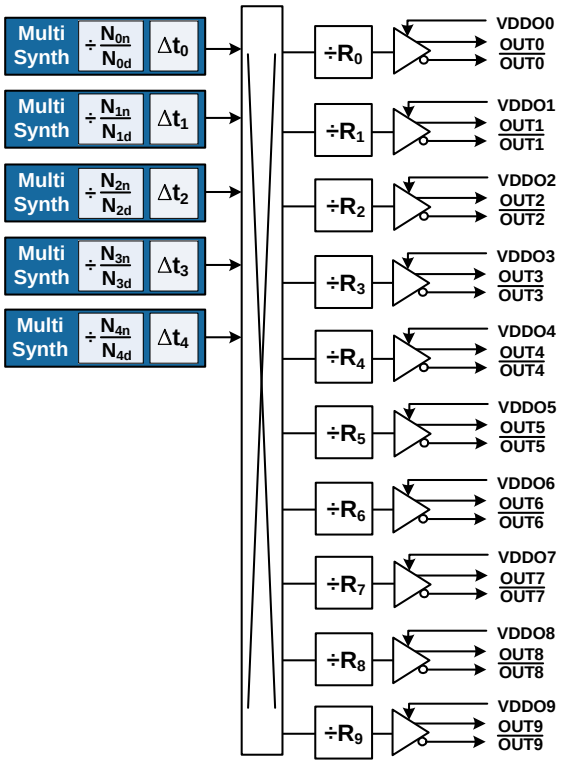


Figure 18. MultiSynth to Output Driver Crosspoint

4.8.2. Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

4.8.3. Differential Output Terminations

The differential output drivers support both AC coupled and DC coupled terminations as shown in Figure 19.

4.8.4. Differential Output Swing Modes

There are two selectable differential output swing modes: Normal and low power. Each output can support a unique mode.

- **Differential Normal Swing Mode:** When an output driver is configured in normal swing mode, its output swing is selectable as one of 7 settings ranging from 200 mVpp_se to 800 mVpp_se in increments of 100 mV. The output impedance in the Normal Swing Mode is 100 Ω differential. Any of the terminations shown in Figure 19 are supported in this mode.

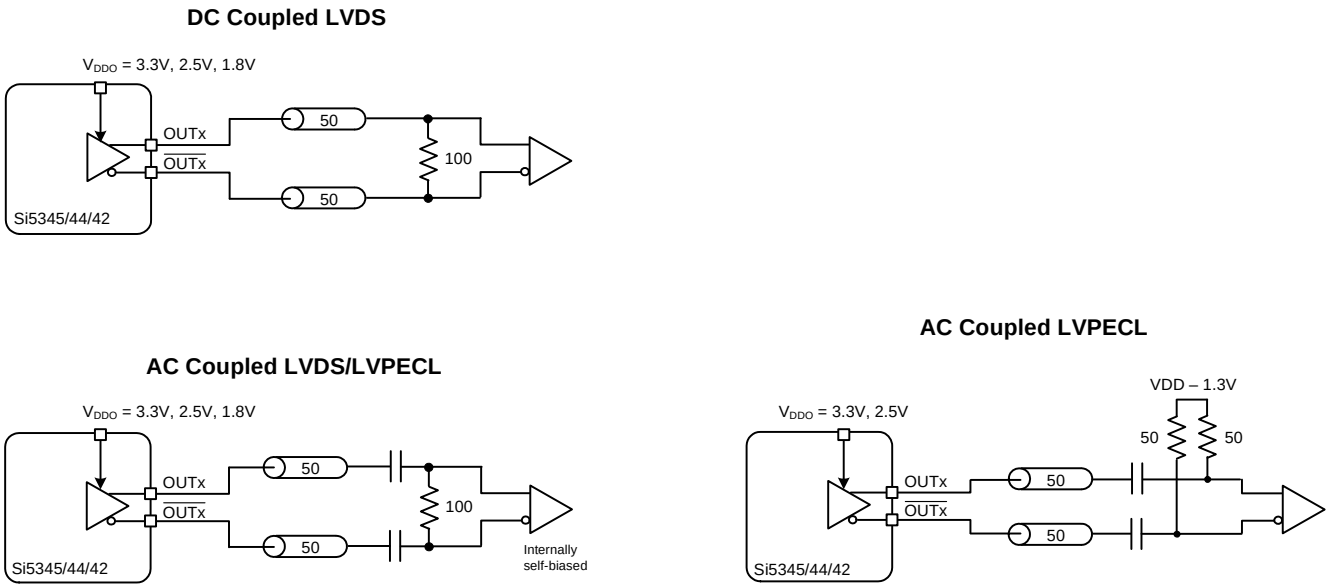


Figure 19. Supported Differential Output Terminations

- **Differential High Swing Mode:** When an output driver is configured in high swing mode, its output swing is configurable as one of 7 settings ranging from 400 mVpp_se to 1600 mVpp_se in increments of 200 mV. The output driver is in high impedance mode and supports standard 50 Ω. PCB traces. Any of the terminations shown in Figure 19 are supported in this mode.

4.8.5. Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential Normal and High Swing modes is programmable in 100 mV increments from 0.7 V to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when DC coupling the output drivers.

4.8.6. LVCMOS Output Terminations

LVCMOS outputs are DC coupled as shown in Figure 20.

DC Coupled LVCMOS

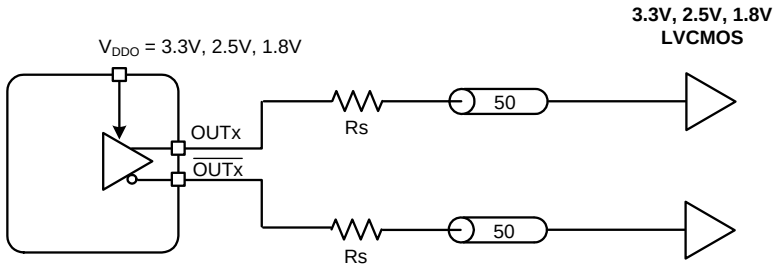


Figure 20. LVCMOS Output Terminations

4.8.7. LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances. A source termination resistor is recommended to help match the selected output impedance to the trace impedance, where Rs = Transmission line impedance – Z_O. There are three programmable output impedance selections (CMOS1, CMOS2, CMOS3) for each VDDO options as shown in Table 15. Note that selecting a lower the source impedance will result in higher output power consumption.

Table 15. Typical Output Impedance (Z_S)

	CMOS_DRIVE_Selection		
VDDO	**CMOS1**	**CMOS2**	**CMOS3**
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

4.8.8. LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

4.8.9. LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and $\overline{\text{OUTx}}$). By default the clock on the $\overline{\text{OUTx}}$ pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

4.8.10. Output Enable/Disable

The $\overline{\text{OE}}$ pin provides a convenient method of disabling or enabling the output drivers. When the $\overline{\text{OE}}$ pin is held high all outputs will be disabled. When held low, the outputs will be enabled. Outputs in the enabled state can be individually disabled through register control.

4.8.11. Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable low, disable high, or disable high-impedance.

4.8.12. Synchronous Output Disable Feature

The output drivers provide a selectable synchronous disable feature. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

4.8.13. Output Skew Control ($\Delta t_0 - \Delta t_4$)

The Si5345 uses independent MultiSynth dividers (N_0 - N_4) to generate up to 5 unique frequencies to its 10 outputs through a crosspoint switch. By default all clocks are phase aligned. A delay path (Δt_0 - Δt_4) associated with each of these dividers is available for applications that need a specific output skew configuration. This is useful for PCB trace length mismatch compensation. The resolution of the phase adjustment is approximately 0.28 ps per step definable in a range of ±9.14 ns. Phase adjustments are register configurable. An example of generating two frequencies with unique configurable path delays is shown in Figure 21.

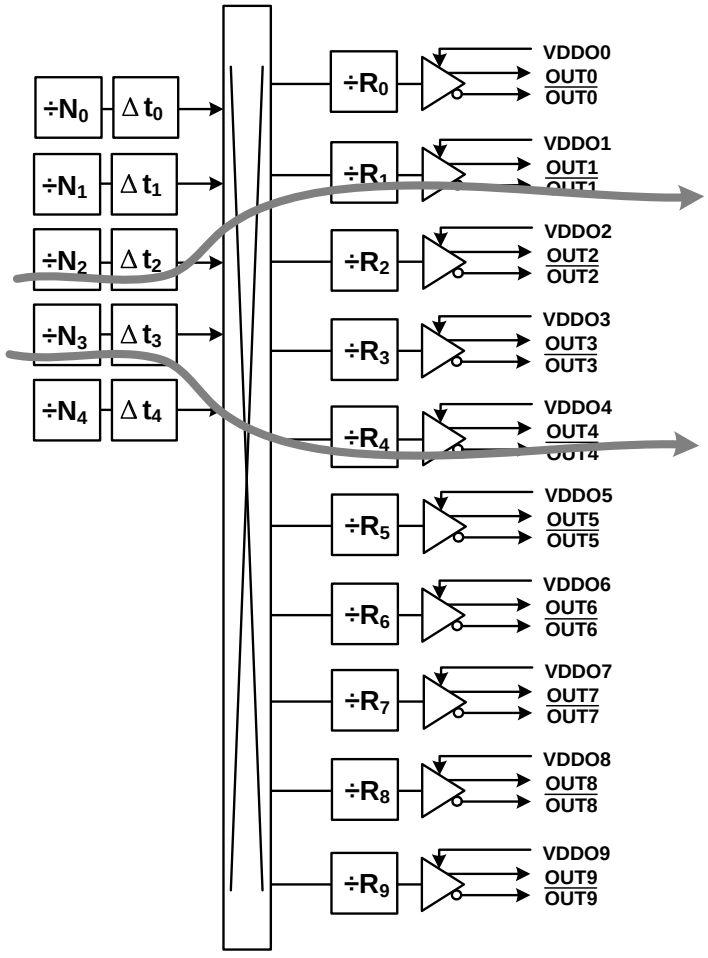


Figure 21. Example of Independently Configurable Path Delays

All phase delay values are restored to their default values after power-up, hard reset, or a reset using the $\overline{\text{RST}}$ pin. Phase delay default values can be written to NVM allowing a custom phase offset configuration at power-up or after power-on reset, or after a hardware reset using the $\overline{\text{RST}}$ pin.

4.8.14. Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in Figure 22.

This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9 and FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. Note that automatic input clock switching and hitless switching features are not available when zero delay mode is enabled.

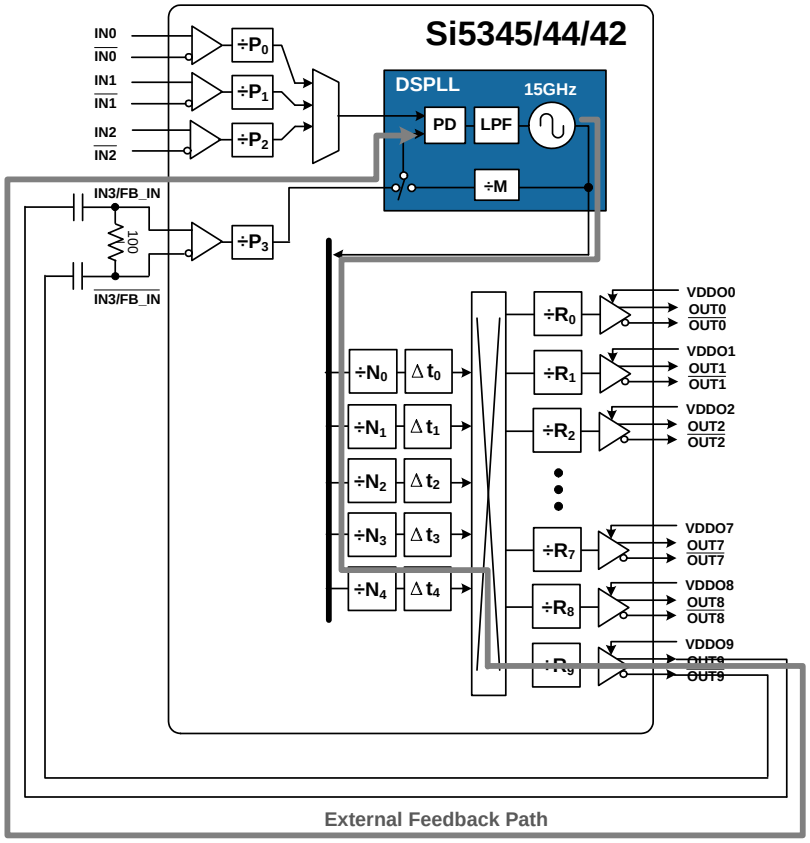


Figure 22. Si5345 Zero Delay Mode Setup

4.8.15. Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the $\overline{\text{RST}}$ pin or asserting the hard reset bit will have the same result. Asserting the sync register bit provides another method of re-aligning the R dividers without resetting the device.

4.9. Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Si5345/44/42 Family Reference Manual and ClockBuilder Pro configuration utility for details.

4.10. In-Circuit Programming

The Si5345/44/42 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5345/44/42 Family Reference Manual for a detailed procedure for writing registers to NVM.

4.11. Serial Interface

Configuration and operation of the Si5345/44/42 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3V and 1.8V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Si5345/44/42 Family Reference Manual for details.

4.12. Custom Factory-Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship to you within two weeks.

5. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible register such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in “5.2. High-Level Register Map” . Refer to the Si5345/44/42 Family Reference Manual for a complete list of register descriptions and settings. Silicon Labs strongly recommends using ClockBuilderPro to create and manage register settings.

5.1. Addressing Scheme

The device registers are accessible using a 16-bit address which consists of an 8-bit page address + 8-bit register address. By default the page address is set to 0x00. Changing to another page is accomplished by writing to the ‘Set Page Address’ byte located at address 0x01 of each page.

5.2. High-Level Register Map

Table 16. High-Level Register Map

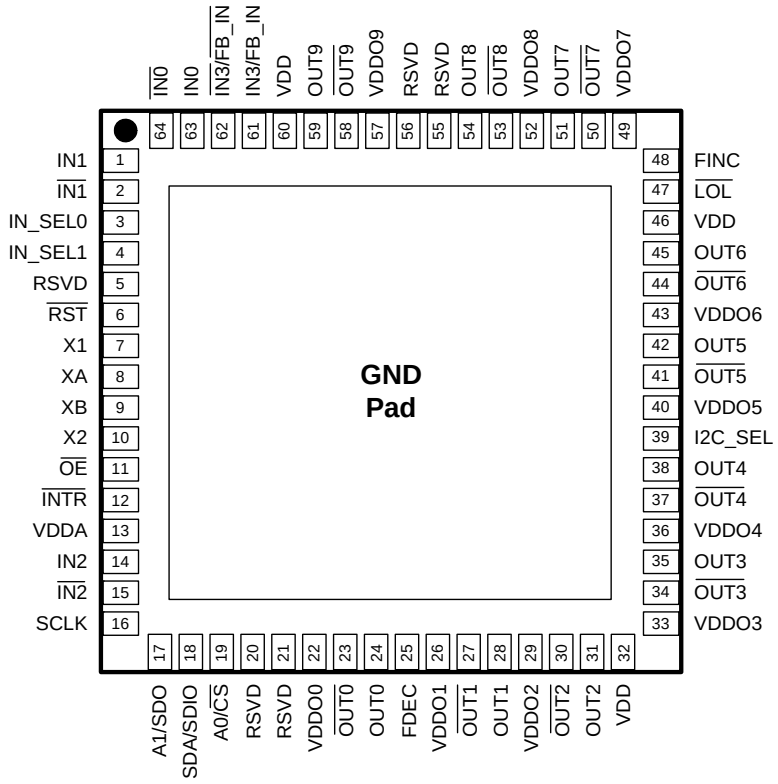
16-Bit Address		Content
8-bit Page Address	**8-bit Register Address Range**	
00	00	Revision IDs
	01	Set Page Address
	02–0A	Device IDs
	0B–15	Alarm Status
	17–1B	INTR Masks
	1C	Reset controls
	1D	FINC, FDEC Control Bits
	2B	SPI (3-Wire vs 4-Wire)
	2C–E1	Alarm Configuration
	E2–E4	NVM Controls
	FE	Device Ready Status
01	01	Set Page Address
	08–3A	Output Driver Controls
	41–42	Output Driver Disable Masks
	FE	Device Ready Status
02	01	Set Page Address
	02–05	XTAL Frequency Adjust
	08–2F	Input Divider (P) Settings
	30	Input Divider (P) Update Bits
	47–6A	Output Divider (R) Settings
	6B–72	User Scratch Pad Memory
	FE	Device Ready Status

Table 16. High-Level Register Map (Continued)

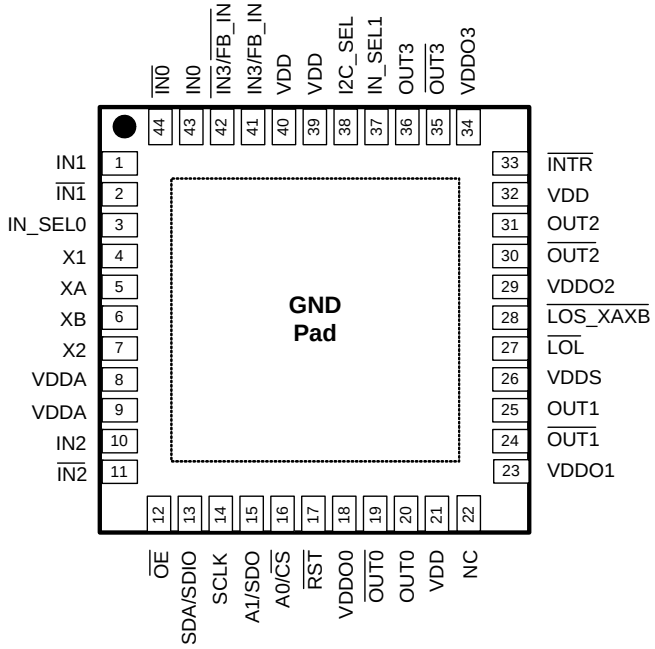
16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
03	01	Set Page Address
	02–37	MultiSynth Divider (N0–N4) Settings
	0C	MultiSynth Divider (N0) Update Bit
	17	MultiSynth Divider (N1) Update Bit
	22	MultiSynth Divider (N2) Update Bit
	2D	MultiSynth Divider (N3) Update Bit
	38	MultiSynth Divider (N4) Update Bit
	39–58	FINC/FDEC Settings N0 - N4
	59–62	Output Delay (Δt) Settings
	FE	Device Ready Status
04	87	Zero Delay Mode Set Up
05	0E - 14	Fast Lock Loop Bandwidth
	15–1F	Feedback Divider (M) Settings
	2A	Input Select Control
	2B	Fast Lock Control
	2C–35	Holdover Settings
	36	Input Clock Switching Mode Select
	38–39	Input Priority Settings
	3F	Holdover History Valid Data
06–08	00–FF	Reserved
09	01	Set Page Address
	1C	Zero Delay Mode Settings
	43	Control I/O Voltage Select
	49	Input Settings
10–FF	00–FF	Reserved

6. Pin Descriptions

Si5345
Top View



Si5344 44QFN
Top View



Si5342 44QFN
Top View

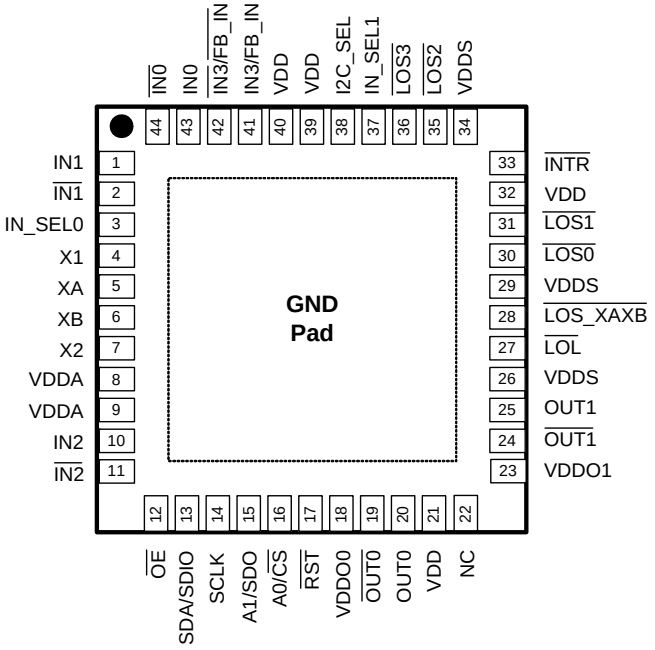


Table 17. Si5345/44/42 Pin Descriptions

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
Inputs					
XA	8	5	5	I	**Crystal Input** Input pins for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode.
XB	9	6	6	I	
X1	7	4	4	I	**XTAL Shield** Connect these pins directly to the XTAL ground pins. X1, X2 and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5345/44/42 Family Reference Manual for layout guidelines. These pins should be left disconnected when connecting XA/XB pins to an external reference clock (REFCLK).
X2	10	7	7	I	
IN0	63	43	43	I	**Clock Inputs** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to "4.6.5. Input Configuration and Terminations" on page 27 for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock.
$\overline{\text{IN0}}$	64	44	44	I	
IN1	1	1	1	I	
$\overline{\text{IN1}}$	2	2	2	I	
IN2	14	10	10	I	
$\overline{\text{IN2}}$	15	11	11	I	
IN3/FB_IN	61	41	41	I	**Clock Input 3/External Feedback Input** By default these pins are used as the fourth clock input (IN3/$\overline{\text{IN3}}$). They can also be used as the external feedback input (FB_IN/$\overline{\text{FB\_IN}}$) for the optional zero delay mode. See section "4.8.14. Zero Delay Mode" on page 35 for details on the optional zero delay mode.
$\overline{\text{IN3}}$/$\overline{\text{FB\_IN}}$	62	42	42	I	

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5345/44/42 Pin Descriptions (Continued)

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
Outputs					
OUT0	24	20	20	O	**Output Clocks** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in “4.8.3. Differential Output Terminations” and section "4.8.6. LVCMOS Output Terminations" on page 33. Unused outputs should be left unconnected.
$\overline{\text{OUT0}}$	23	19	19	O	
OUT1	28	25	25	O	
$\overline{\text{OUT1}}$	27	24	24	O	
OUT2	31	31	—	O	
$\overline{\text{OUT2}}$	30	30	—	O	
OUT3	35	36	—	O	
$\overline{\text{OUT3}}$	34	35	—	O	
OUT4	38	—	—	O	
$\overline{\text{OUT4}}$	37	—	—	O	
OUT5	42	—	—	O	
$\overline{\text{OUT5}}$	41	—	—	O	
OUT6	45	—	—	O	
$\overline{\text{OUT6}}$	44	—	—	O	
OUT7	51	—	—	O	
$\overline{\text{OUT7}}$	50	—	—	O	
OUT8	54	—	—	O	
$\overline{\text{OUT8}}$	53	—	—	O	
OUT9	59	—	—	O	
$\overline{\text{OUT9}}$	58	—	—	O	

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5345/44/42 Pin Descriptions (Continued)

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
Serial Interface					
I2C_SEL	39	38	38	I	I^2C Select This pin selects the serial interface mode as I^2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high. Leave disconnected when unused. See Note [2].
SDA/SDIO	18	13	13	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when is SPI mode. Tie low when unused. See Note [2].
A1/SDO	17	15	15	I/O	**Address Select 1/Serial Data Output** In I^2C mode this pin functions as the A1 address input pin. In 4-wire SPI mode this is the serial data output (SDO) pin. Leave disconnected when unused. See Note [2].
SCLK	16	14	14	I	**Serial Clock Input** This pin functions as the serial clock input for both I^2C and SPI modes. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. Tie high or low when unused. See Note [2].
A0/$\overline{CS}$	19	16	16	I	**Address Select 0/Chip Select** This pin functions as the hardware controlled address A0 in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left unconnected when not in use. See Note [2].

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5345/44/42 Pin Descriptions (Continued)

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
Control/Status					
$\overline{\text{INTR}}$	12	33	33	O	**Interrupt** This pin is asserted low when a change in device status has occurred. This pin must be pulled-up using an external resistor of at least 1 kΩ. It should be left unconnected when not in use. See Note [2].
$\overline{\text{RST}}$	6	17	17	I	**Device Reset** Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up and can be left unconnected when not in use. See Note [2].
$\overline{\text{OE}}$	11	12	12	I	**Output Enable** This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. See Note [2].
$\overline{\text{LOL}}$	47	—	—	O	**Loss Of Lock (Si5345)** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use. See Note [2].
	—	27	27	O	**Loss Of Lock (Si5344/42)** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use. See Note [3].
$\overline{\text{LOS0}}$	—	—	30	O	**Loss Of Signal for IN0** This pin indicate a loss of clock at the IN0 pin when low. See Note [3].
$\overline{\text{LOS1}}$	—	—	31	O	**Loss Of Signal for IN1** This pin indicate a loss of clock at the IN1 pin when low. See Note [3].
$\overline{\text{LOS2}}$	—	—	35	O	**Loss Of Signal for IN2** This pin indicate a loss of clock at the IN2 pin when low. See Note [3].
$\overline{\text{LOS3}}$	—	—	36	O	**Loss Of Signal for IN3** This pin indicate a loss of clock at the IN3 pin when low. See Note [3].

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5345/44/42 Pin Descriptions (Continued)

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
$\overline{\text{LOS\_XAXB}}$	—	28	28	O	**Loss Of Signal on XA/XB Pins** This pin indicates a loss of signal at the XA/XB pins when low. See Note [3].
FINC	48	—	—	I	**Frequency Increment Pin** This pin is used to step-up the output frequency of a selected output. The affected output and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use. See Note [2].
FDEC	25	—	—	I	**Frequency Decrement Pin** This pin is used to step-down the output frequency of a selected output. The affected output driver and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use. See Note [2].
IN_SEL0	3	3	3	I	**Input Reference Select** The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in Table 14 on page 26. These pins are internally pulled low. See Note [2].
IN_SEL1	4	37	37	I	
RSVD	5	—	—	—	**Reserved** These pins are connected to the die. Leave disconnected.
	20	—	—	—	
	21	—	—	—	
	55	—	—	—	
	56	—	—	—	
NC	—	22	22		**No Connect** These pins are not connected to the die. Leave disconnected.

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

Table 17. Si5345/44/42 Pin Descriptions (Continued)

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
Power					
VDD	32	21	21	P	**Core Supply Voltage** The device operates from a 1.8 V supply. A 0.1 µF bypass capacitor should be placed very close to this pin.
	46	32	32	P	
	60	39	39	P	
	—	40	40	P	
VDDA	13	8	8	P	**Core Supply Voltage 3.3 V** This core supply pin requires a 3.3 V power source. A 1 µF bypass capacitor should be placed very close to this pin.
	—	9	9	P	
VDDS	—	26	26	P	**Status Output Voltage** The voltage on these pins determines the V_{OL}/V_{OH} on some of the LOL and LOS status output pins. Connect to 3.3 V or 1.8 V. A 0.1 uF bypass capacitor should be placed very close to this pin.
	—	—	29	P	
	—	—	34	P	
VDDO0	22	18	18	P	**Output Clock Supply Voltage** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, $\overline{\text{OUTn}}$ outputs. For unused outputs, leave VDDO pins unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	26	23	23	P	
VDDO2	29	29	—	P	
VDDO3	33	34	—	P	
VDDO4	36	—	—	P	
VDDO5	40	—	—	P	
VDDO6	43	—	—	P	
VDDO7	49	—	—	P	
VDDO8	52	—	—	P	
VDDO9	57	—	—	P	
GND PAD	—	—	—	P	**Ground Pad** This pad provides connection to ground and must be connected for proper operation.

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

7. Ordering Guide

Ordering Part Number (OPN)	Number of Input/Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes (Typical Jitter)	Package	Temperature Range
Si5345					
Si5345A-A-GM[1,2]	4/10	0.001 to 800 MHz	Integer (100 fs) Fractional (150 fs)	64-Lead 9x9 QFN	–40 to 85 °C
Si5345B-A-GM[1,2]		0.001 to 350 MHz			
Si5345C-A-GM[1,2]		0.001 to 800 MHz	Integer Only (100 fs)		
Si5345D-A-GM[1,2]		0.001 to 350 MHz			
Si5344					
Si5344A-A-GM[1,2]	4/4	0.001 to 800 MHz	Integer (100 fs) Fractional (150 fs)	44-Lead 7x7 QFN	–40 to 85 °C
Si5344B-A-GM[1,2]		0.001 to 350 MHz			
Si5344C-A-GM[1,2]		0.001 to 800 MHz	Integer Only (100 fs)		
Si5344D-A-GM[1,2]		0.001 to 350 MHz			
Si5342					
Si5342A-A-GM[1,2]	4/2	0.001 to 800 MHz	Integer (100 fs) Fractional (150 fs)	44-Lead 7x7 QFN	–40 to 85 °C
Si5342B-A-GM[1,2]		0.001 to 350 MHz			
Si5342C-A-GM[1,2]		0.001 to 800 MHz	Integer Only (100 fs)		
Si5342D-A-GM[1,2]		0.001 to 350 MHz			
Si5345/44/42-EVB					
Si5345-EVB	—	—	—	Evaluation Board	—
Si5344-EVB					
Si5342-EVB					

Notes:
1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by Silicon Labs and the ClockBuilder Pro software utility.
3. Custom part number format is: e.g. Si5345A-Axxxxx-GM where “xxxxx” is a unique numerical sequence representing the pre-programmed configuration.

8. Package Outlines

8.1. Si5345 9x9 mm 64-QFN Package Diagram

Figure 23 illustrates the package details for the Si5347. Table 18 lists the values for the dimensions shown in the illustration.

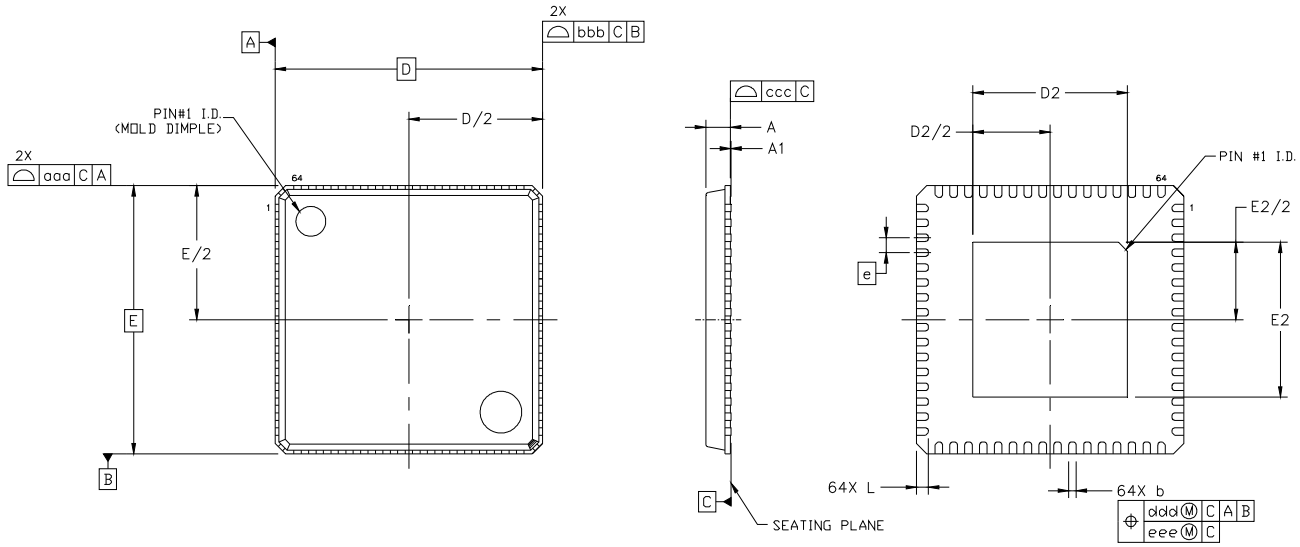


Figure 23. 64-Pin Quad Flat No-Lead (QFN)

Table 18. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2. Si5344 and Si5342 7x7 mm 44-QFN Package Diagram

Figure 24 illustrates the package details for the Si5344 and Si5342. Table 19 lists the values for the dimensions shown in the illustration.

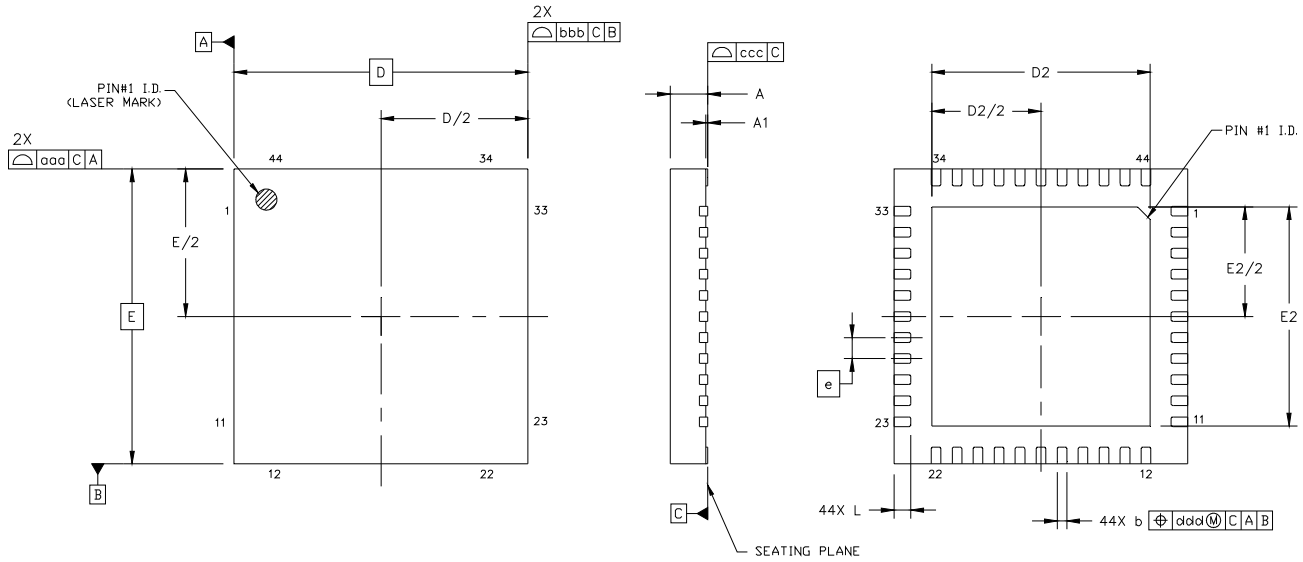


Figure 24. 44-Pin Quad Flat No-Lead (QFN)

Table 19. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		7.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

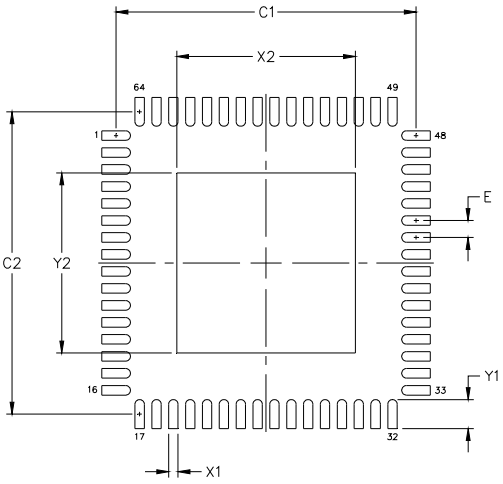
Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. PCB Land Pattern

Figure 25 illustrates the PCB land pattern details for the devices. Table 20 lists the values for the dimensions shown in the illustration.

Si5345



Si5344 and Si5342

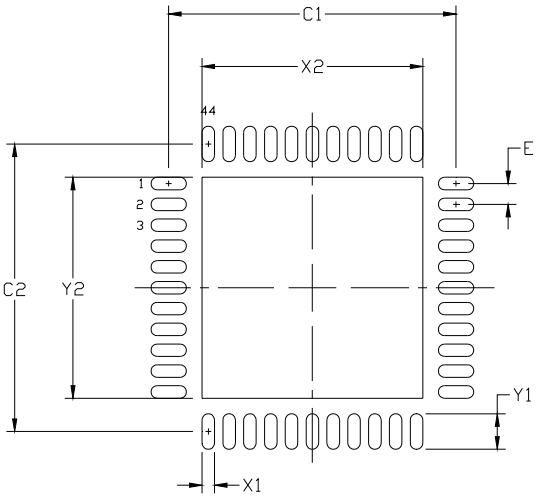


Figure 25. PCB Land Pattern

Table 20. PCB Land Pattern Dimensions

Dimension	Si5347 (Max)	Si5346 (Max)
C1	8.90	6.90
C2	8.90	6.90
E	0.50	0.50
X1	0.30	0.30
Y1	0.85	0.85
X2	5.30	5.30
Y2	5.30	5.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

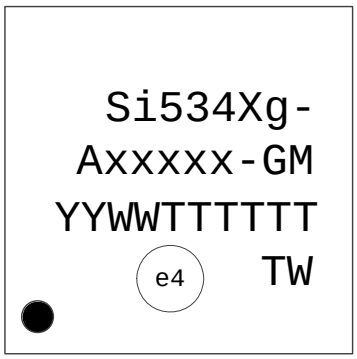
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 3x3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Top Marking

64-QFN



44-QFN

Line	Characters	Description
1	Si534Xg-	Base part number and Device Grade for Any-frequency, Any-output, Jitter Cleaning Clock (single PLL): X = 5: 10-output Si5345: 64-QFN X = 4: 4-output Si5344: 44-QFN X = 2: 2-output Si5342: 44-QFN g = Device Grade (A, B, C, D). See Ordering Guide for more information. – = Dash character.
2	Axxxxx-GM	A = Product revision. (Refers to die revision A1). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See Ordering Guide for more information. –GM = Package (QFN) and temperature range (-40 to +85C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) or 1.4 mm (44-QFN) diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

11. Device Errata

Please log in or register at www.silabs.com to access the device errata document.

APPENDIX—ADVANCE PRODUCT INFORMATION REVISION HISTORY

Table 21 lists the advance product information revision history.

Table 21. Advance Product Information Revision History

Revision	Change Description	Date
0.10	First Draft	Feb 2012
0.11	■ Major updates to all sections	May 2012
0.20	■ Major revisions to all sections. ■ New block diagrams showing 5 unique frequencies instead of 10. ■ Combined the Si5345, Si5344, Si5342 datasheets ■ Added application diagrams ■ Newly revised AC/DC Specification tables ■ Added register map information ■ Finalized Pinouts	Oct 2013
0.21	■ Updated Section 9 - Ordering Guide ■ Updated typical jitter performance to 150 fs ■ Added P_{REF} divider to figures 2, 3, 4, 7. ■ Minor edits	Oct 2013
0.22	■ Corrected Si5342 pin numbering errors: • VDDO0 changed from 23 to 18 • VDDO1 changed from 29 to 23 ■ Renamed pin 22 on the Si5344 and Si5342 from RSVD to NC	Nov 2013
0.23	■ Corrected typo in the dimension table title.	Dec 2013
0.24	■ Updated register names to match with the register map in the Si5345/44/42 Family Reference Manual.	Jan 2014
0.25	■ Minor register name updates	Jan 2014
0.30	■ Moved the register descriptions to the Si5345/44/42 Reference Manual. ■ Moved the majority of the contents of the Serial Interface section to the Si5345/44/42 Reference Manual. ■ Changed the output delay specification from “1 ps steps with a range of ±8.32 ns” to “0.28 ps steps with a range of ±9.14 ns”. Added this to the specification table. ■ Updated LVCMOS output impedance values in Table 15. ■ Added Control Input and Status Output table specifications. ■ Changed pin names XGND to X1 and X2. Functionality remains the same.	Apr 2014
0.31	■ Added serial interface timing diagrams and specifications ■ Renamed XGND pins to X1, X2.	Jun 2014

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